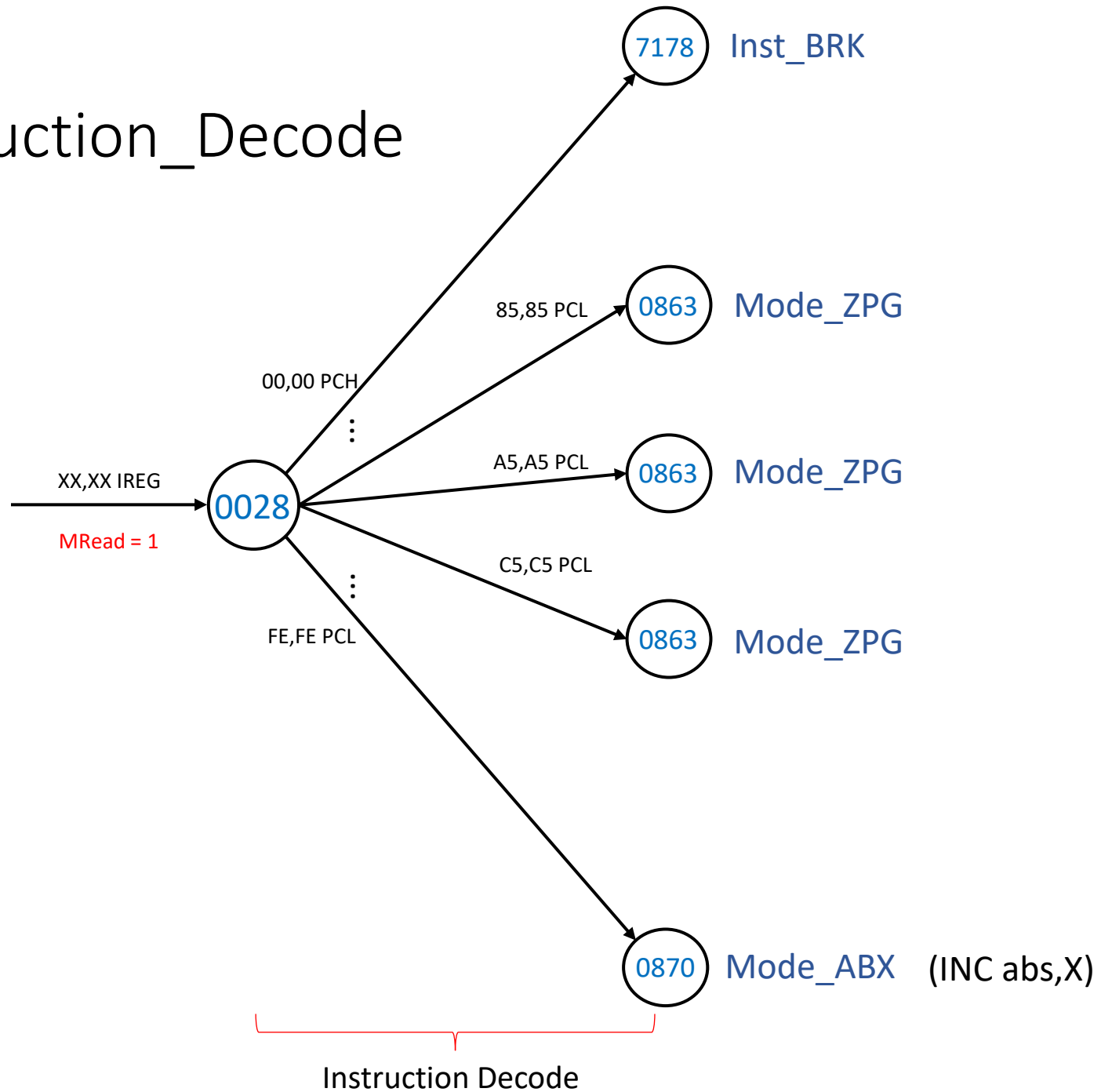
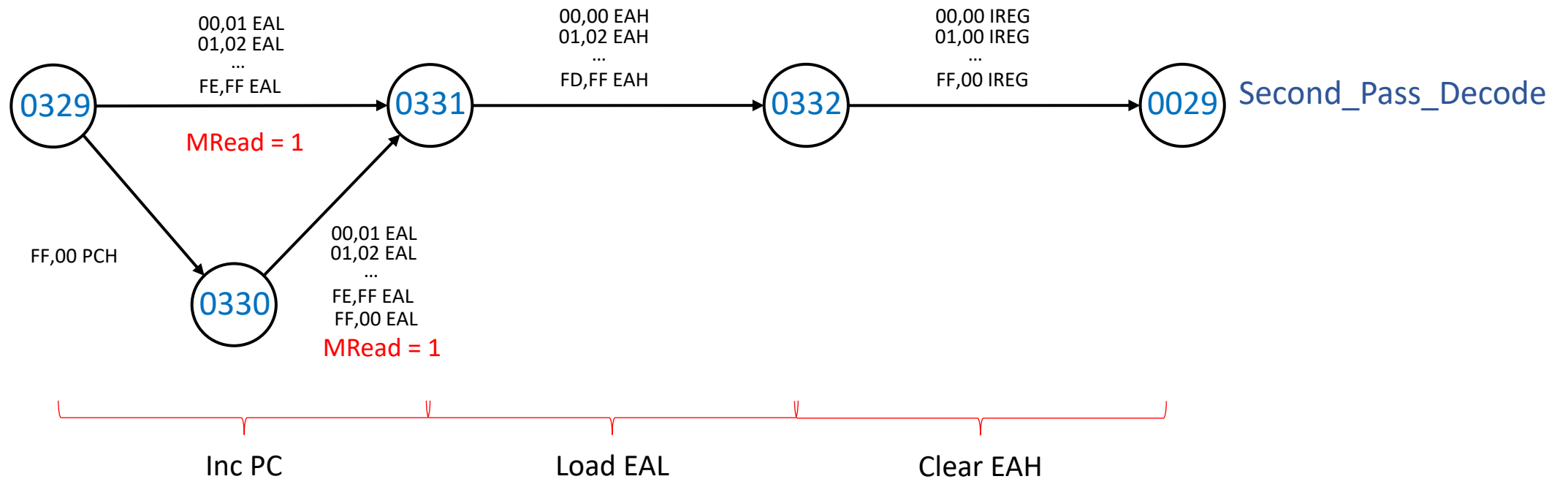


# Instruction\_Decode



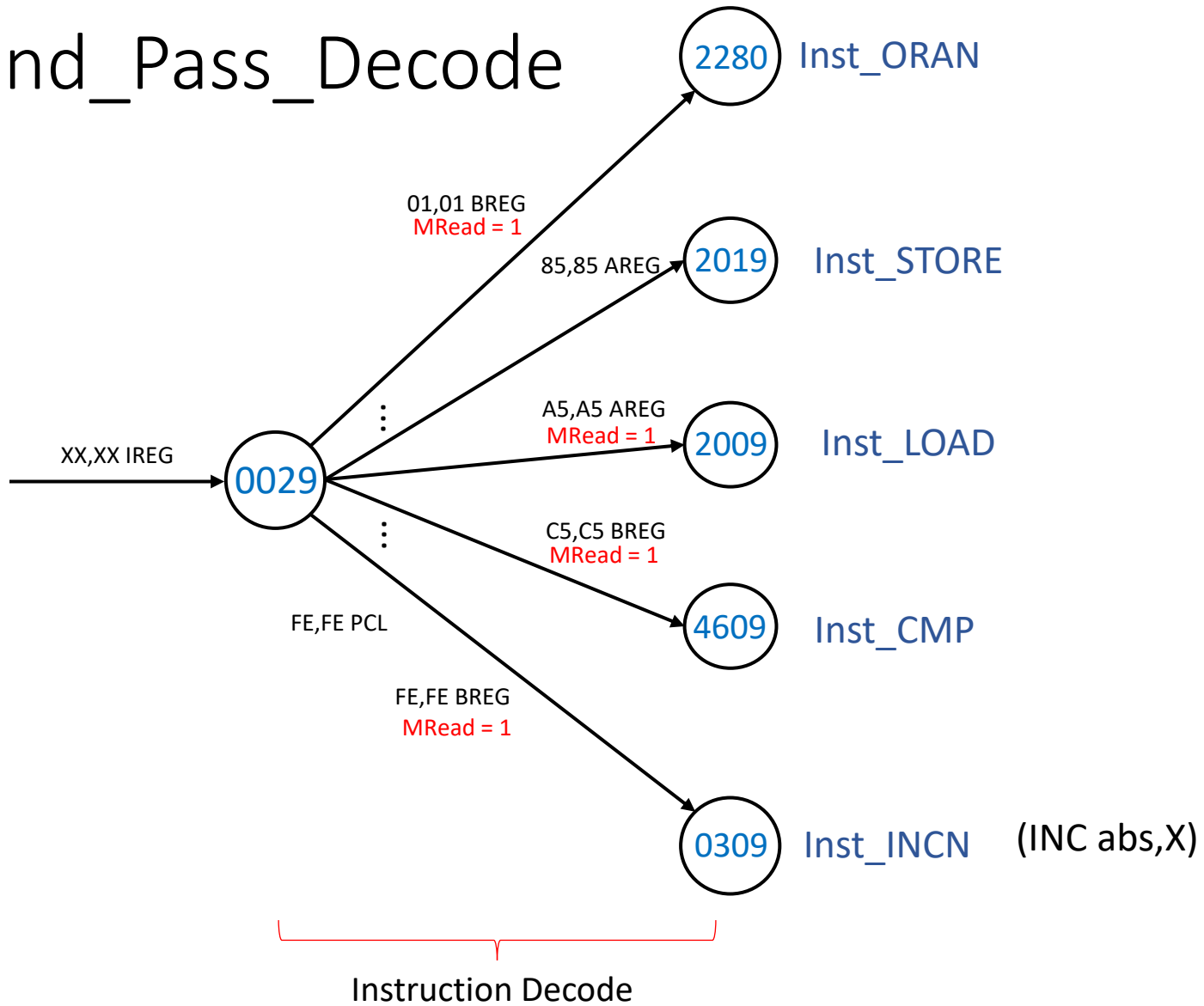
## Turing 6502 State Diagrams

# Mode\_ZPG



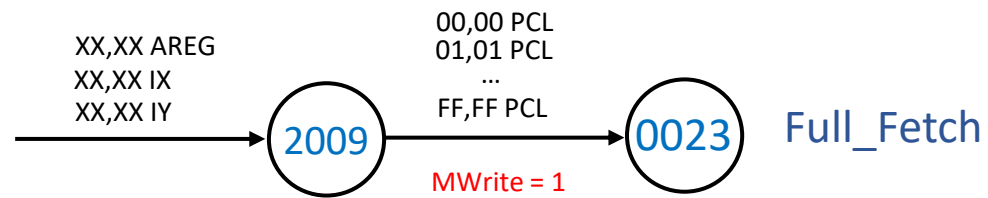
## Turing 6502 State Diagrams

# Second\_Pass\_Decode



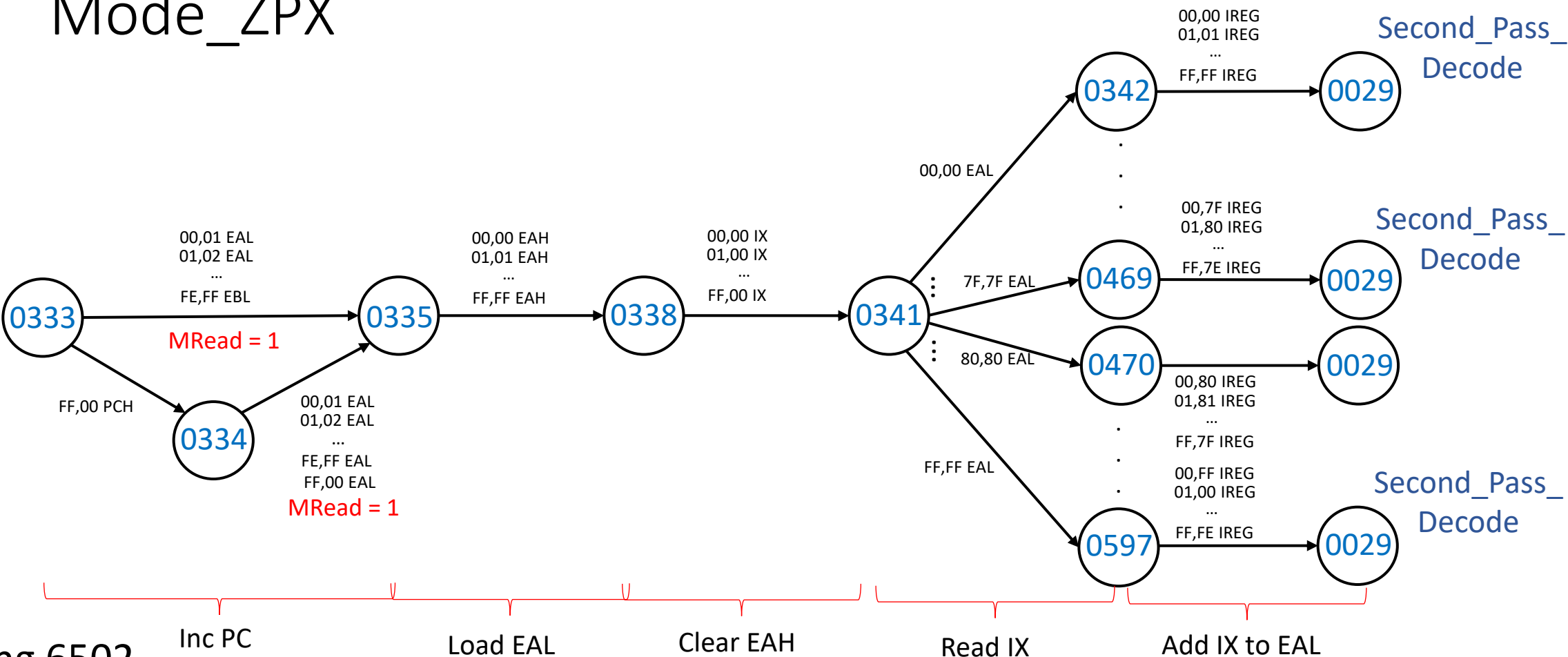
## Turing 6502 State Diagrams

# Inst\_STORE

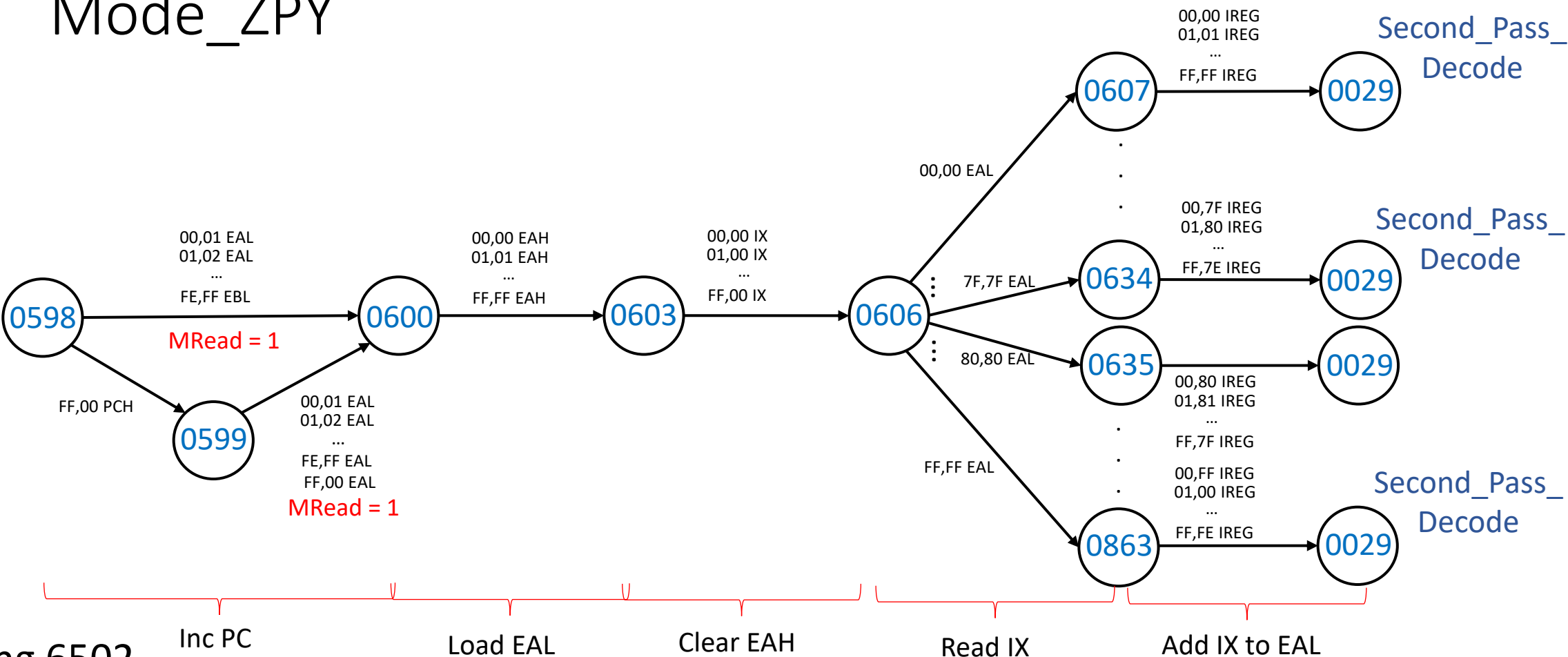


Store AREG  
(IX/IY)

# Mode\_ZPX

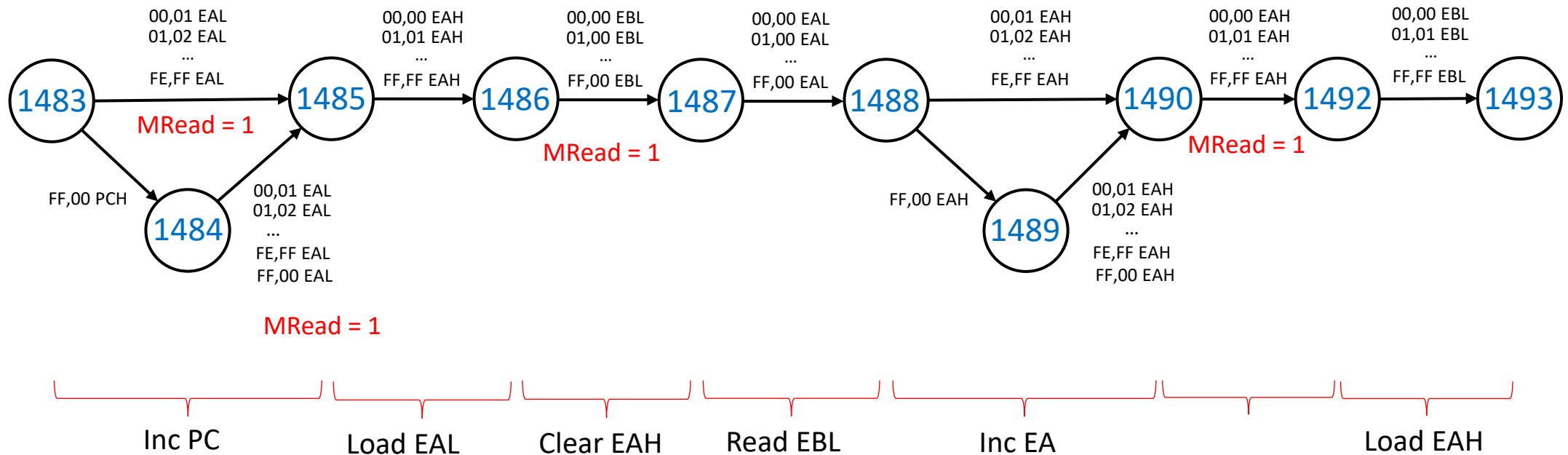


# Mode\_ZPY



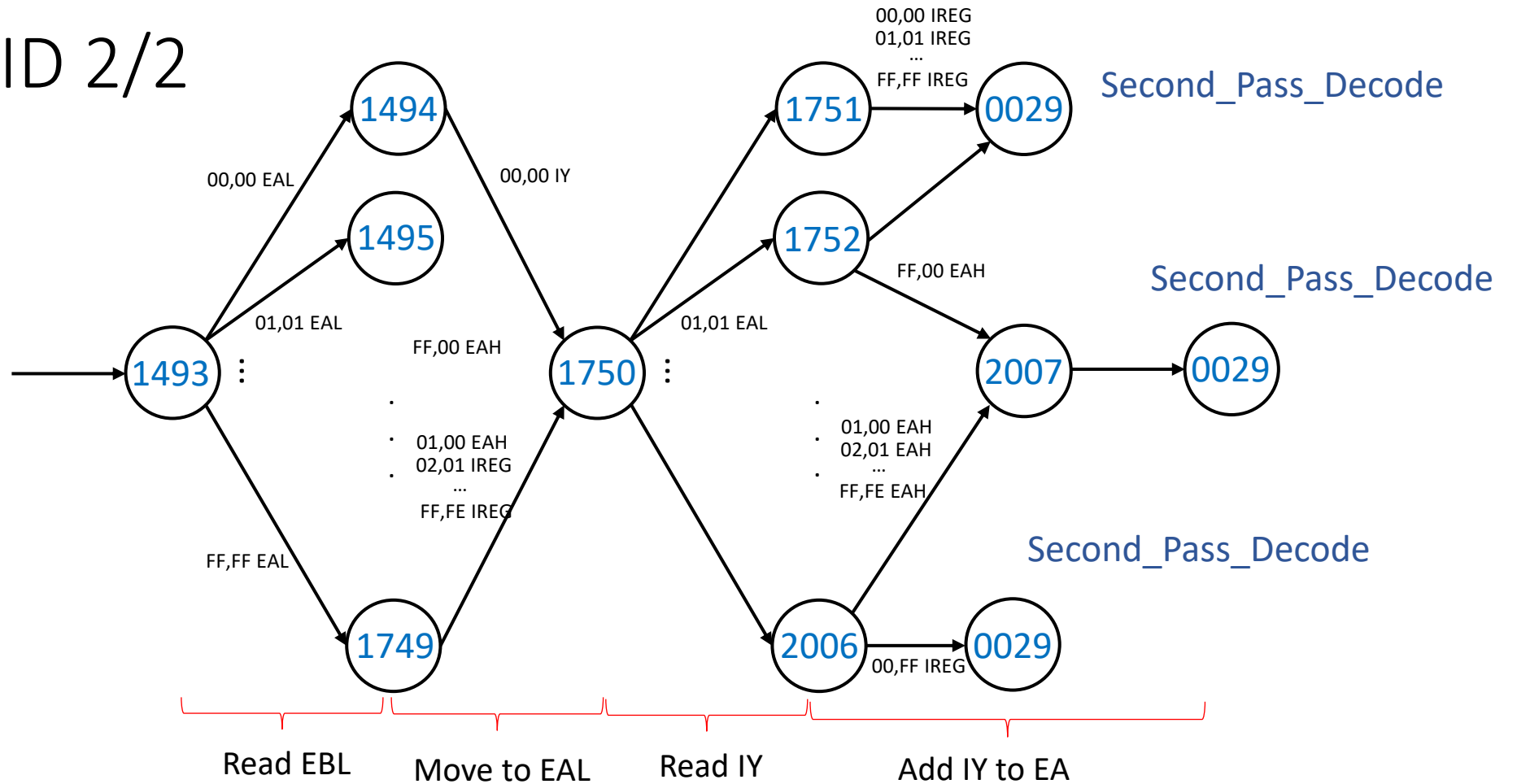
Turing 6502  
State Diagrams

# Mode\_YID 1/2



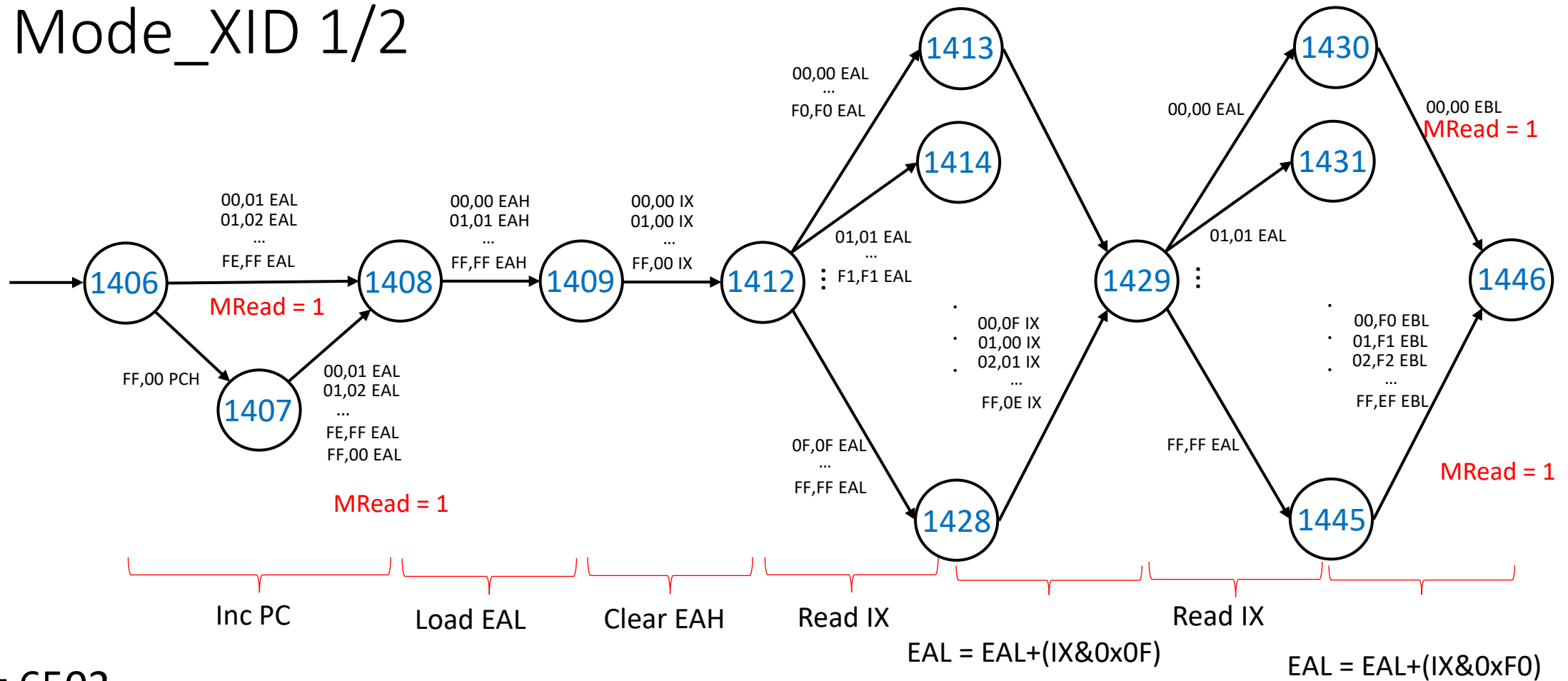
## Turing 6502 State Diagrams

## Mode\_YID 2/2



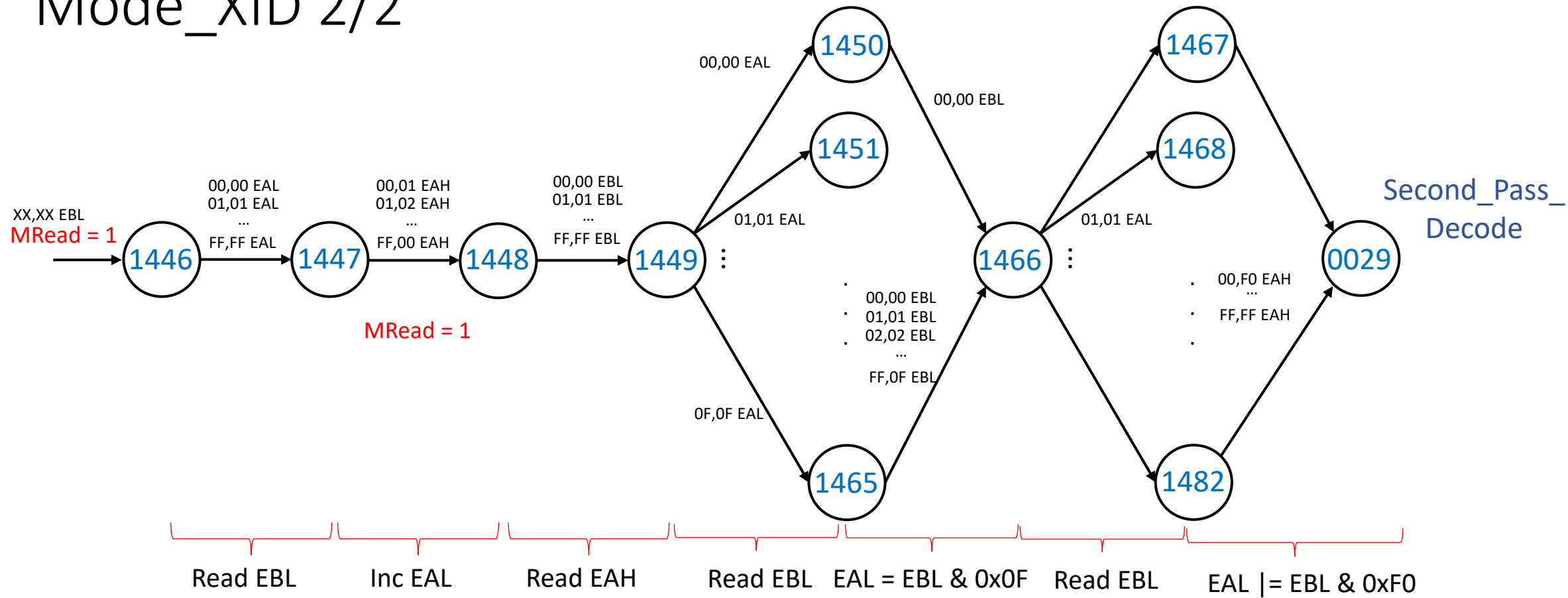


# Mode\_XID 1/2



## Turing 6502 State Diagrams

## Mode\_XID 2/2



## Turing 6502 State Diagrams