Notes:

- y_Q: present state
- y_D: present state

State transitions are specified by two separate always blocks.

The first block describes the required combinational circuit. It uses a case statement to give the value of the next state for each value of the present state. Each case alternative corresponds to a present state of the machine, and the associated if-else statement specifies the next state to be reached according to the value of input.

The second always block introduces flip-flops into the circuit. Its sensitivity list comprises the reset and clock signals.

Part 1 State Table

Table 1: State Table

State	**w = 0**	**w = 1**	**z**
A	A	B	0
B	A	C	0
C	E	D	0
D	E	F	0
E	A	G	0
F	E	F	1
G	A	C	1

Part 1 Output Logic

z is only 1 when the states are F and G. Therefore, the output is:

```
assign z = ((y_Q == F) | (y_Q == G));
```