Notes:

- y_Q: present state
- y_D: present state

State transitions are specified by two separate always blocks.

The first block describes the required combinational circuit. It uses a case statement to give the value of the next state for each value of the present state. Each case alternative corresponds to a present state of the machine, and the associated if-else statement specifies the next state to be reached according to the value of input.

The second always block introduces flip-flops into the circuit. Its sensitivity list comprises the reset and clock signals.

Part 1 State Table

Table 1: State Table

State	**w = 0**	**w = 1**	**z**
A	A	B	0
B	A	C	0
C	E	D	0
D	E	F	0
E	A	G	0
F	E	F	1
G	A	C	1

Part 1 Output Logic

z is only 1 when the states are F and G. Therefore, the output is:

```
assign z = ((y_Q == F) | (y_Q == G));
```

Part 2 Terminology

Datapath: refers to the component that performs data processing and manipulation. It includes registers, arithmetic and logic units, and other elements used for data operations. The datapath is responsible for executing the operations specified by the control unit.

Control Path: responsible for determining the sequence of operations to be performed by the datapath. It controls the flow of data and instructions within the FSM, guiding the execution of specific tasks based on the current state and inputs.

FSM: Control Path, ALU: Datapath