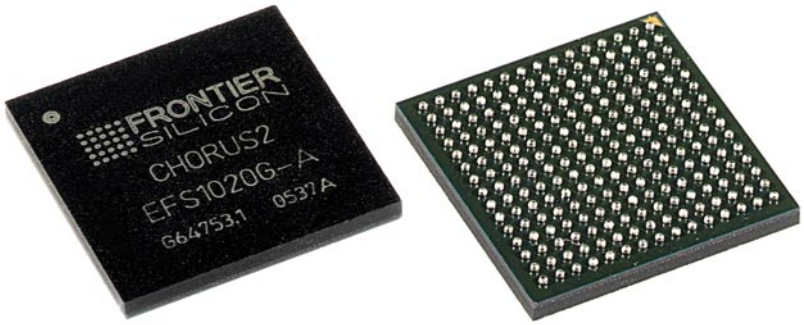
Chorus 2 FS1020

Highly-integrated DAB/DAB+/streaming audio system-on-chip



Chorus 2 chip - 13.0 x 13.0 x 1.7 mm

APPLICATIONS

- Portable digital radio
- Portable music player
- Car radio and audio system
- Home audio and multimedia system
- Internet radio
- Multimedia-enhanced PDA
- Advanced digital radio (on-demand and data services)
- Digital music server/jukebox

OVERVIEW

The Chorus 2 FS1020 is an advanced DAB/DAB+/T-DMB/streaming audio programmable baseband receiver, enabling audio, video, and data services for portable digital radios and other handheld devices, with industry-leading performance, cost and size. It supercedes the best-selling Chorus 1 processor, which powers most DAB radios currently in use.

Chorus 2 is an extremely flexible baseband receiver covering a number of physical layer standards, particularly those utilising COFDM modulation. The baseband signal processing is achieved using a blend of hardware and software to optimise trade-offs between power, cost and flexibility.

At the front end, an integrated high-performance 10-bit ADC provides a differential IF input suitable for a broad range of IF input frequencies. The core is a META122 CPU with extensive DSP capabilities. This executes multiple DSP tasks without cross-task interference.

The chip integrates sufficient memory to provide full DAB ensemble decoding on-chip. Chorus 2 can also decode DAB+ transmissions with the addition of external memory. Powerful DSP architecture allows implementation of other embedded applications such as software FM, further audio codecs, and rights management.

Chorus 2 has an extensive software suite, including code for use at the heart of a new generation of streaming Internet radio and music file-based audio systems.

The chip also includes a rich set of peripheral interfaces to enable communication with other system devices and to provide value-adding interface ports.

ADVANCED POWER MANAGEMENT

Chorus 2 uses dynamic and static power management techniques including fully-static design, clock-gating and inactive period state minimisation for low power usage without compromising performance. The processor clock is generated by a PLL which can be reprogrammed dynamically, enabling power consumption to be minimised for specific applications.

FEATURES

- ETSI EN 300 401 (EUREKA-147) compliant receiver
- Ultra low-power DAB/DAB+ baseband reception
- Flexible hardware-assisted DSP architecture to support various applications such as FM-RDS, MP3, WMA and AAC+
- Decodes multiple audio, video, and data services up to the maximum 1.8 Mbps with no external RAM
- Temperature range:
  operation: -40 to +85°C
  storage: -40 to +125°C
- USB 2.0 full-speed interface
- Highly integrated SoC with low external component count through integrated mixed-signal components:
  - DCXO
  - Power-on reset
  - ADC
  - PLL
- Multiple memory options:
  - Expansion Memory Interface - SRAM, Cellular SRAM, mobile SDRAM
  - Non-volatile memory Interface - NOR Flash, serial Flash

TOOL AND SOFTWARE SUPPORT

- Comprehensive toolkit support including compiler, assembler and debugger.
- A range of evaluation and development systems
- Powerful PC GUI Software for system evaluation.

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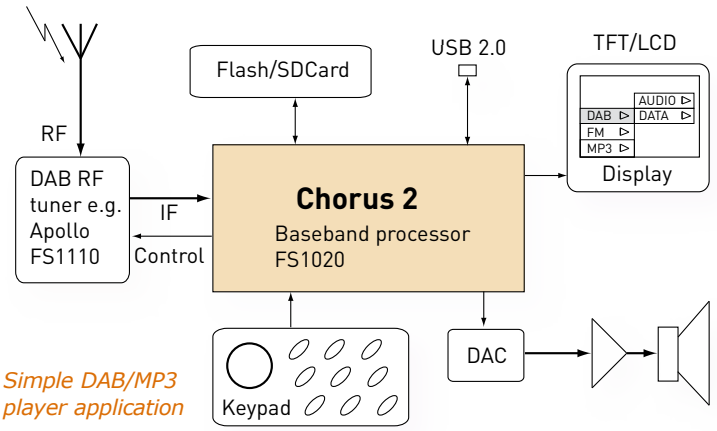
ARCHITECTURE

The META multithreaded core is a high-performance low-power modular device enabling extensive customisation. It is designed for use in applications such as audio signal processing and next-generation digital wireless.

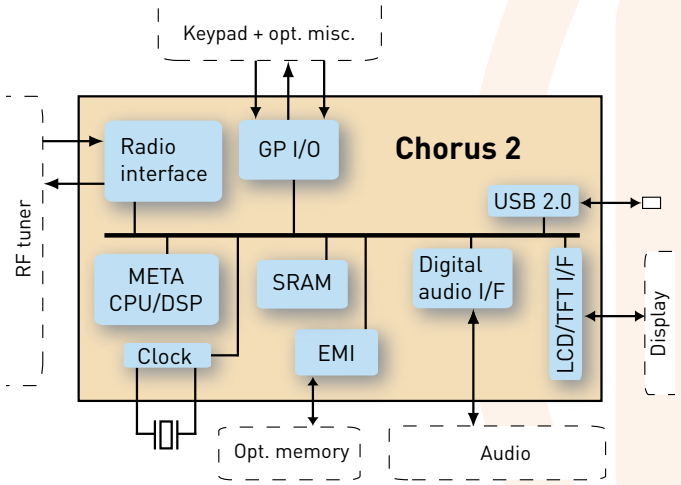
Processor architecture	Multithreaded 3-operand register based
Data types and registers	16/32-bit integer ALU with multiple 32-bit register files
System architecture	Independent 64-bit instruction and data interfaces
Exceptions and interrupts	Memory, instruction, and interrupt handling on each thread
Instruction set	RISC 32-bit with DaOpPaMe template extensions to 64-bit
Pipeline	3-stage



Simple DAB/MP3 player application

Actual size

225 LFBGA, 0.8 mm pitch



Chorus 2 block diagram

EXTENSIVE PERIPHERALS

- **USB 2.0** interface with support for full-speed operation (12 Mbps)
- Integrated support for **TFT** and **LCD** displays
- **SD** interface for optional mass storage applications
- Extensive and flexible **GPIO**
- **S/PDIF** audio input and output
- Up to 8-channel I2S output of decoded audio data (both master and slave modes)
- Support for 3 **SPI slave** devices (including DMB TS data output, SD card profile and optional local SPI Flash)
- SPI slave port available for autonomous TS data, boot and control to/from host
- 2 **SCP** (I2C-compatible) ports for control of RF devices and optional control from host
- Up to 4 PDM DAC outputs for interface to dual RF tuners such as Frontier Silicon Apollo FSFS1110 and third-party (e.g. wideband AGC, IF AGC)
- Two 16550-compliant **UARTs**, with optional flow control
- **JTAG** interface for test and emulator support
- Support for expansion RAM (SRAM, Cellular SRAM, SDRAM or mobile SDRAM) for the most demanding applications.
- Full RoHS compliance

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