

Andy Wanna

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Personal Statement: I am looking to further develop my experience with hardware engineering, especially surrounding the use of FPGAs as extremely fast and efficient processors.

Education

Imperial College London

Oct 2020 – Present

- Electronic and Information Engineering
 - Year 1 – 1st Class Honours (Digital Arithmetic & Computer Architecture, Programming)
 - Year 2 – 1st Class Honours (Instruction Architectures & Compilers, Information Processing, Software Systems)
 - Year 3 – 1st Class Honours (Advanced Computer Architecture, Digital System Design, Digital Signal Processing)

Dharan High School

Sept 2018 – Jun 2020

- IB diploma programme
- SAT and SAT subject tests

Technical Experiences and Projects

- Research in Hardware Synthesis Optimization using E-Graphs Oct 2022 – Present
 - Created Rust software to compile common hardware expressions into an optimised representation
- Digital Design Industrial Placement at Quantum Motion Apr 2023 – Oct 2023
 - Direct Digital Synthesis Modulator for High-Speed Qubit Feedback on an FPGA in HDL, using Vivado
 - Program Raspberry Pi Pico to communicate using TCP/IP over ethernet connections in C using lwIP
- Cosine Accelerator on FPGA in Verilog Feb 2023 – Mar 2023
 - Notably reduced output latency by implementing Cosine on an FPGA using CORDIC in SystemVerilog
 - Designed customised hardware Floating-Point arithmetic blocks for further speed-ups
- GymBro Embedded Raspberry PI Device Jan 2023 – Mar 2023
 - Built a Network hosting an AWS server, a Raspberry Pi Client, and MySQL Database
 - Expanded functionality for multiple users, using Node.js and MySQL, ensuring scalability and security
- Digital Synthesiser in Embedded C Jan 2023 – Mar 2023
 - Programmed an STM32 using Multi-Threading in Embedded C
 - Developed advanced functionality while maintaining thread safety, without affecting latency
- Maximised Energy Efficiency of a SuperScalar CPU by varying MicroArchitectural Parameters Nov 2022
 - Explored effect of Branch Predictors, Memory Hierarchy, and Instruction Parallelism
- Analogue and Digital IC Validation Intern at Quantum Motion Jul 2022 – Oct 2022
 - Automated Data analysis using Python scripting
 - Validated operation of Ring Oscillator hardware on silicon chips
 - Characterised properties of silicon across a range of chips, at room and cryogenic Temperatures (2K)
- Webapp for Mars Rover May 2022 – Jul 2022
 - Backend using AWS and Node.js for communication between the web app, rover and MySQL database
- C to MIPS Assembly compiler in C++ Feb 2022 – Mar 2022
- Automatic Scheduler in C++ Jul 2022 – Oct 2022
 - Created software to allocate projects within a set schedule to improve time management
- Video game with FPGA hand-held controller Feb 2022 – Mar 2022
 - Instantiated NIOS 2 softcore CPU onto FPGA using Quartus
 - Programmed FPGA accelerometer functionality and low-level local processing and networking in C
 - Client side-communication and further data processing using Python
- MIPS 32-bit CPU in Verilog Nov 2021 – Dec 2021
 - MIPS 32-bit CPU written in Icarus Verilog to process standard instructions
 - Wrote testbenches to systematically test edge cases for each instruction

Leadership and Team Experiences

- Vice-President of Electrical Engineering Society Oct 2022 – Present
- Year 2 Academic Representative Oct 2021 – Jun 2022
- Fundraising Officer at Habitat for Humanity Aug 2019 – Jun 2020
- President of Robotics Club Aug 2018 – Jun 2019
- Founder of BISAK Tutoring Club Sept 2016 – Jul 2018

Skills, Strengths, and Achievements

- Proficient in (written and spoken) English, French, and Arabic
- Completed Math and Further pure maths iGCSE, 2 years early
- Achieved Best delegate at 4 international MUN conferences, chairing 4 further ones