Andy Wanna

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Education

Imperial College London — Oct 2020 – Present

- Electronic and Information Engineering
  - Year 1 – 1st Class Honours
    - Digital Arithmetic & Computer Architecture, Programming
  - Year 2 – 1st Class Honours
    - Instruction Architectures & Compilers, Information Processing, Software Systems, Discrete Maths,
  - Year 3 – 1st Class Honours
    - Advanced Computer Architecture, Operations Research, Embedded Systems, Machine-Learning, Computer-Vision, Digital Systems Design
  - Year 4
    - Math for Machine Learning, Large Dimensional Data Processing, Probability and Stochastic Processes, Deep-Learning, Advanced Deep-Learning Systems
  - Awards – Dean's List Year 3 (Top 10% of year)

Dharan High School — Sept 2018 – Jun 2020

- IB diploma programme
- SAT and SAT subject tests

Technical Experiences

- **FPGA Engineering Placement at Quantum Motion** — Apr 2023 – Oct 2023
  - Designed and integrated bespoke signal generator into QICK stack for High-Speed Qubit Feedback on an **FPGA** in **System Verilog**, using **Vivado.**
  - Built a high-level, user-friendly software library to interface with and take advantage of optimised **FPGA** hardware with **PYNQ** and QICK **Python** libraries.
  - Programmed an RP2040 to communicate using TCP/IP over ethernet connections in **C** using the light-weight IP library.
  - Ported functions into **C** to be used on the RP2040, building an extensive codebase.
- **Analogue and Digital IC Validation Intern at Quantum Motion** — Jul 2022 – Oct 2022
  - Automated custom data pre-processing and analysis in **Python.**
  - Analysed properties of silicon across a range of chips, at room and cryogenic Temperatures (2K), to create model predicting transistor threshold-voltage.
  - Designed a low noise, wide-range (1na-10ma), wideband (100MHz) current sensor schematic and PCB.
  - Validated operation of Ring Oscillator hardware on silicon chips.

Publications & Research Experience

- **OptiMult - Multiplier Optimization via E-Graph Rewriting – Primary Author**
  - Created tool in **Rust** to compile common hardware arithmetic expressions into an optimized representation for both area and latency.
  - Demonstrated up to a **46% latency reduction** in squarer circuits and **9% latency reduction** in general **multiplication** against industry standard logic synthesis tools.
  - This paper has been presented at ASILOMAR 2023 to be published soon
- **Accelerating Interpretable Deep Neural Networks for medical Imaging using FPGAs – Final Year Project**

Technical Projects

- **Cosine Accelerator on FPGA in SystemVerilog** — Jan 2023 – Mar 2023
  - **Reduced the output latency of vector function by 77%** by implementing custom cosine block on an **FPGA** using CORDIC in **SystemVerilog** with **Quartus.**
  - Designed customized hardware Floating-Point Arithmetic blocks for further speed-ups.
  - Optimised function further via low-level programming in **C.**
- **MRI Diagnosis Model using Computer Vision in PyTorch** — Feb 2023 – Mar 2023
  - Implemented a **U-Net CNN** architecture to perform image classification and segmentation on brain scans.

- Digital Synthesiser in Embedded C — Jan 2023 – Mar 2023
  - Programmed an STM32 microcontroller using **Multi-Threading in Embedded C.**
  - Developed advanced functionality while maintaining thread safety, without affecting latency of sound output.
  - Enabled automatic detection and integration of additional devices to expand the synthesiser's functionality.
- GymBro Embedded Raspberry PI Device — Jan 2023 – Mar 2023
  - Built a network hosting an **AWS** server, a **Raspberry Pi** Client, and **MySQL Database.**
  - Expanded functionality for multiple concurrent users, using **Express.js**, **Node.js** and **MySQL.**
  - Ensured security by adding user authentication.
- House Price Regression Model in PyTorch — Nov 2022 – Dec 2022
  - Designed a **regression model** using a **neural network**.
  - Preformed data pre-processing, **K-fold hyperparameter validation**, early stopping, **batched gradient descent** and various other ML optimisation techniques.
  - Implemented a custom NN training and inference mini library with batched gradient descent, arbitrary layers and custom activation functions.
- Maximised Energy Efficiency of a SuperScalar CPU — Nov 2022
  - Varied microarchitectural parameters such as **Branch Predictors**, **Memory Hierarchy**, and **Instruction Parallelism**, investigating their impact on energy usage.
- Webapp for Mars Rover — May 2022 – Jul 2022
  - Developed backend for webserver using **AWS, Node.js** and **Express.js** for communication between the webapp and embedded system on Mars Rover.
  - Designed front-end with **HTML/CSS/JavaScript.**
  - Utilised **MySQL** on an **AWS** instance as a database for the WebApp, to maintain live rover position and data.
- C to MIPS Assembly compiler in C++ — Feb 2022 – Mar 2022
  - Built Object Oriented Compiler from base including Lexer and Parser in **C++.**
  - Compiles complex expressions in C such as **pointer arithmetic**, **arrays** and **advanced function calls**.

  Automatic Scheduler in C++ — Jul 2022 – Oct 2022
  - Created software to allocate projects within a set schedule to improve time management in **C++**.
- Video game with FPGA hand-held controller — Feb 2022 – Mar 2022
  - Instantiated NIOS-II soft-core CPU onto **FPGA** using **Quartus.**
  - Programmed **FPGA** accelerometer functionality and low-level local processing and networking in **C** using **Quartus** and **Eclipse**.
  - Developed client-side communication with server and user along with advanced signal processing for motion detection in **Python.**
- MIPS 32-bit CPU in Verilog — Nov 2021 – Dec 2021
  - MIPS 32-bit CPU written in **Icarus Verilog** to process standard assembly instructions.
  - Wrote **testbenches** to systematically test edge cases for each instruction.
- Boolean Algebra Solver in C++ — May 2021
  - Programmed tool that could reduce and solve Boolean algebra expressions using **trees** in **C++**.

Leadership and Team Experiences

- Vice-President of Electrical Engineering Society — Oct 2022 – Jun 2023
- Year 2 Academic Representative — Oct 2021 – Jun 2022
- Fundraising Officer at Habitat for Humanity — Aug 2019 – Jun 2020
- President of Robotics Club — Aug 2018 – Jun 2019
- Founder of School Tutoring Club — Sept 2016 – Jul 2018

Skills Strengths and Achievments

- Programming Languages: C/C++, Python, Rust, JavaScript (NodeJS), SQL, SystemVerilog
- Technologies: AWS, Git, FPGAs, Microcontrollers, TCP/IP, PyTorch, Vivado, Quartus, Eclipse, LTSpice, QICK
- Proficient in (written and spoken) English, French, and Arabic
- Completed Math and Further pure maths iGCSE, 2 years early