Introduction to CAD tools

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Introduction

The purpose of this lab is to learn about the basic CAD tools and how to use Quartus II software to create and simulate block diagram schematics and VHDL based designs. The use of CAD tools can significantly decrease cost as not all circuits have to be built out to test their functionality. Using Quartus II, we can observe the outputs of the circuits created which can help further the learning process about logic gates and using VHDL.

Results

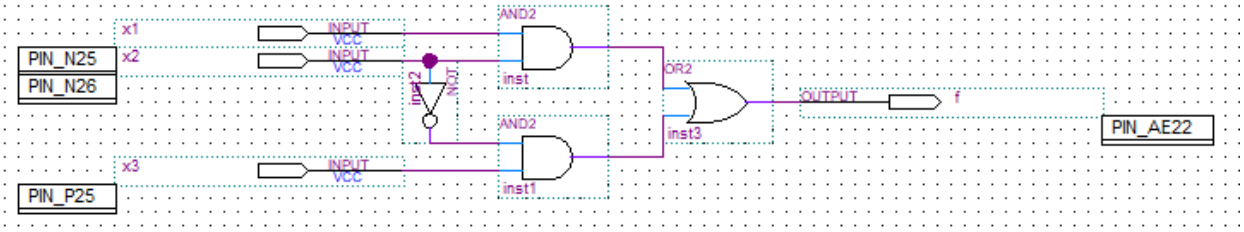

Figure 1: Block diagram schematic of Part 1

x_1	x_2	x_3	f
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

Figure 1.1: Desired output of Figure 1

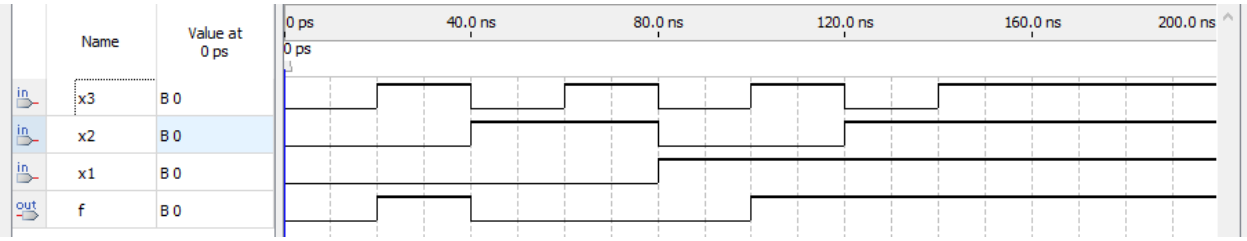

Figure 2: Waveform with output waveform of the block diagram schematic in Figure 1

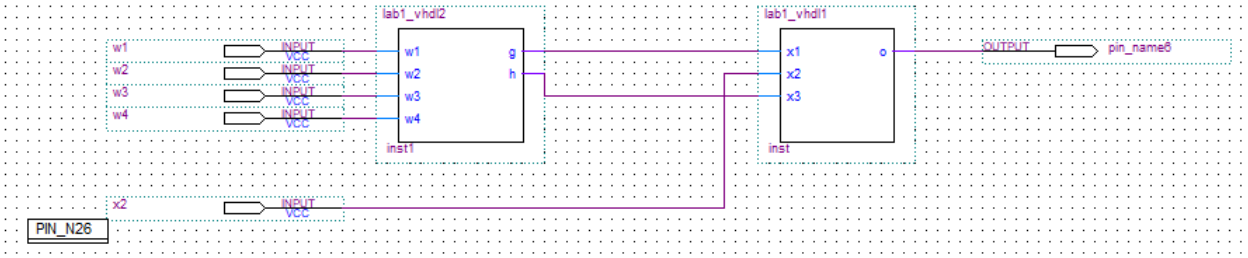

Figure 3: Block diagram schematic of Part 2 using the symbols created with VHDL

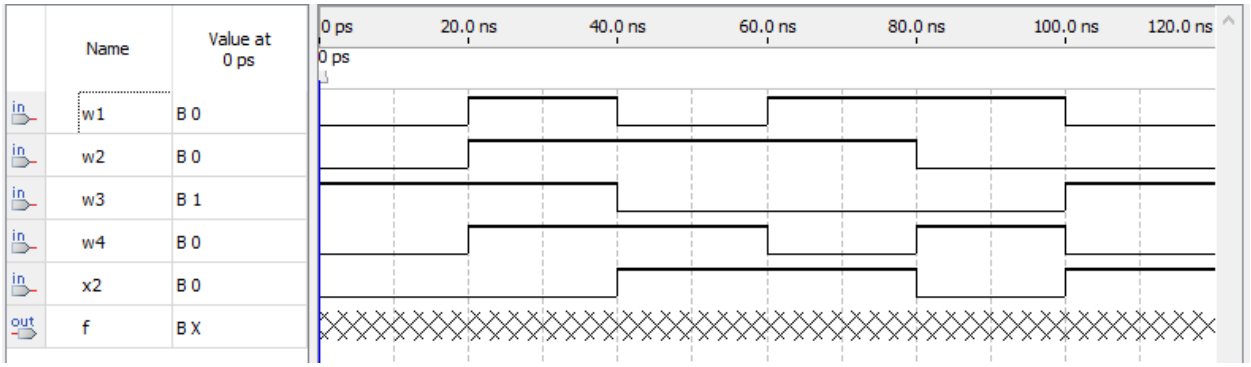

Figure 4: Incomplete waveform program with no output given inputs

Analysis

In Figure 1, the block diagram schematic is built with 2 AND gates, 1 OR gate and 1 NOT gate. This would produce the desired output for this lab which is show in the waveform in Figure 2. The desired output is shown in Figure 1.1 which corresponds to the resultant output in Figure 2 produced by the circuit. The first part of the lab was to demonstrate the general equation $f = x_1x_2 + \overline{x_2}x_3$. Since this equation is in its minimal form, the circuit presented in Figure 1 is a direct visualization and implementation of the equation using CAD tools.

Figure 3 shows the 2 symbols that were created from the VHDL. VHDL1 models the equation $f = x_1x_2 + \overline{x_2}x_3$ where VHDL2 models 2 different equations $g = w_1w_2 + w_3w_4$ and $h = w_1w_3 + w_2w_4$.Unfortunately, the waveform did not compile as expected and the problem was left to the inability to figure out how pin assignments worked for pins that were not in the top level file. Theis would mean that even if the pins were given signal values, it could not pass those signal values to specific pins which meant that the pins in the schematic did not receive any signals. This would ultimately not result in an output from the block diagram, leaving this part of the lab incomplete as seen in Figure 4.