Function Implementation and Minimization

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Introduction

The purpose of this lab is to learn about Karnaugh maps and how they are implemented to aid in minimization of circuits. Minimizing circuits can help reduce costs significantly, especially if the circuit is going to be mass produced or used repeatedly in a circuit or circuits.

Results

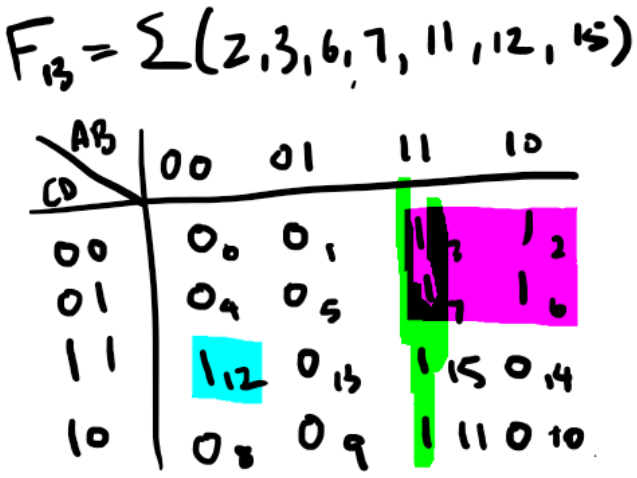

Figure 1: Karnaugh map of the given Sum of Products

$$F = A\bar{C} + AB + \bar{A}\bar{B}CD$$
$$= (\bar{C} + B)A + \bar{A}\bar{B}CD$$

Figure 2: Simplified Boolean equation of the Sum of Products

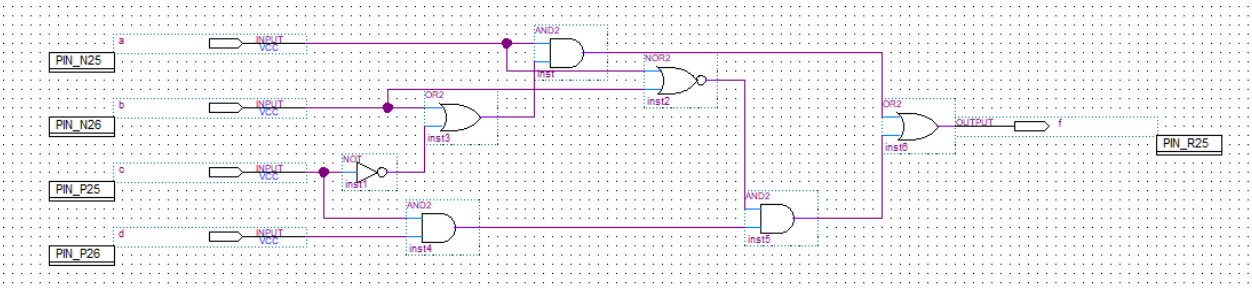

Figure 3: Block Schematic diagram of given Sum of products

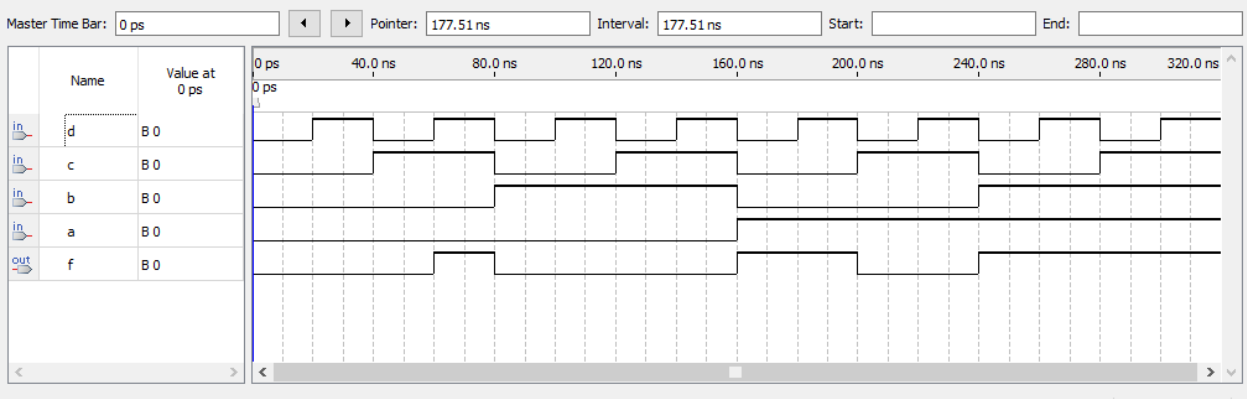

Figure 4: Waveform of given block schematic diagram

Analysis

In Figure 1, the Karnaugh map shows the given Sum of products where the 1s were grouped up and highlighted in their specific colors. The AB column had an where AB!C!D and AB!CD were shared between 2 groups. To properly group 1s on a K-map, the largest of groups were formed. These groups could only be in the shape of squares or rectangles that contained only specific number of 1s; 1, 2, 4, 8, or 16. Properly reading the K-map will result in a Sum of Products that is shown in Figure 2. The first Boolean equation is the direct translation of the K-map while the second line is the minimized version of the first line. The minimization was through the application of a known law called the distributive law. Figure 3 shows the block schematic diagram realization Figure 2. It uses AND, OR, NOT and NOR logic gates to produce the waveform shown in Figure 4. The VHDL code in produces the same results as for waveforms shown in Figure 4.