

ZCU111 MIG Design Creation

December 2018



XTP514

Revision History

Date	Version	Description
12/10/18	2.0	Updated to 2018.3. Some screenshots not updated.
07/09/18	1.0	Initial version.

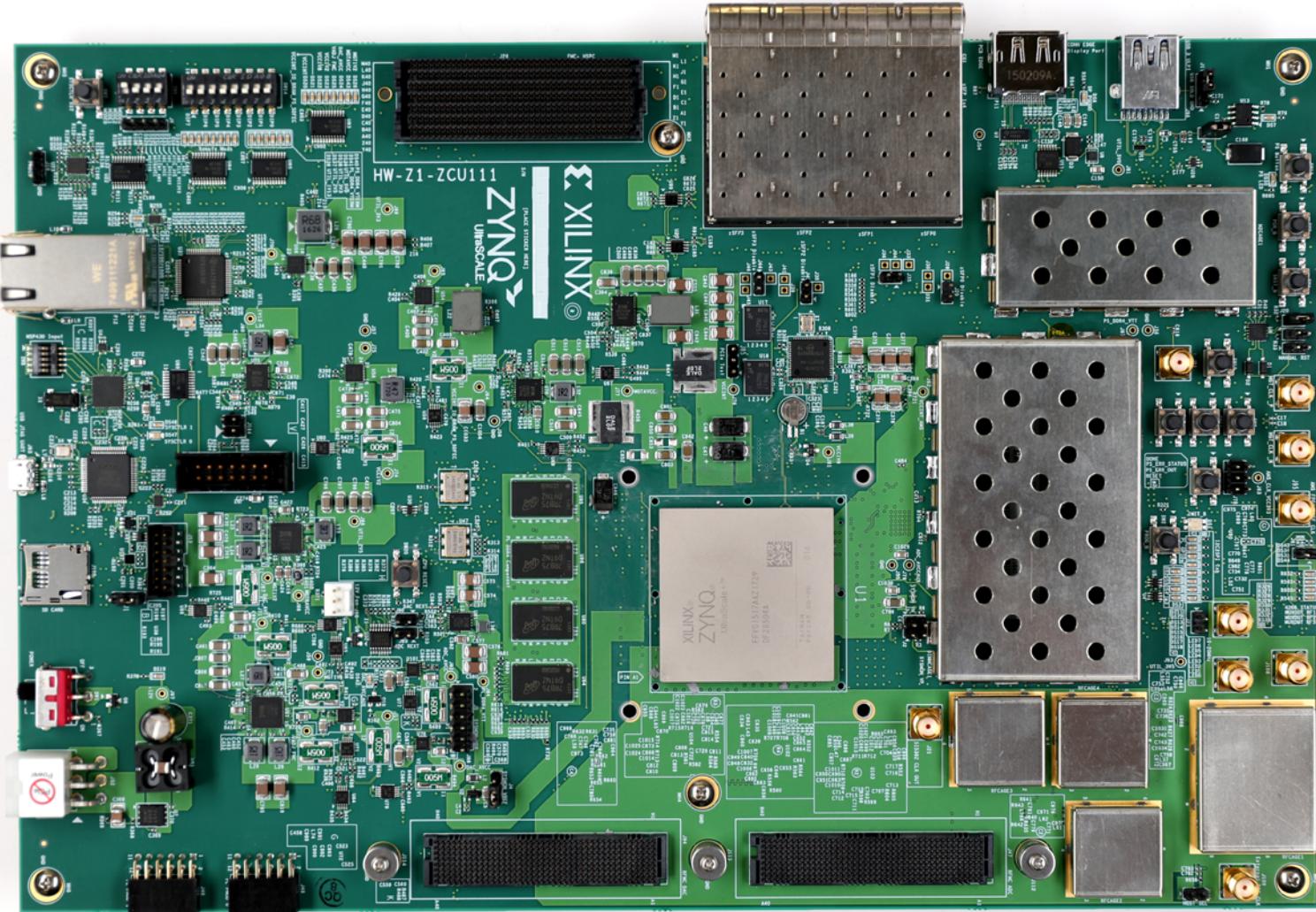
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Overview

- > **Xilinx ZCU111 Board**
- > **ZCU111 Software Install and Board Setup**
- > **Generate MIG Example Design**
- > **Compile Example Design**
 - » Modifications to Example Design
- > **Run MIG Example Design**
- > **References**

Xilinx ZCU111 Board



Note: Presentation applies to the ZCU111

ZCU111 Software Install and Board Setup

- > Refer to XTP518 – ZCU111 Software Install and Board Setup for details on:
 - » Software Requirements
 - » ZCU111 Board Setup

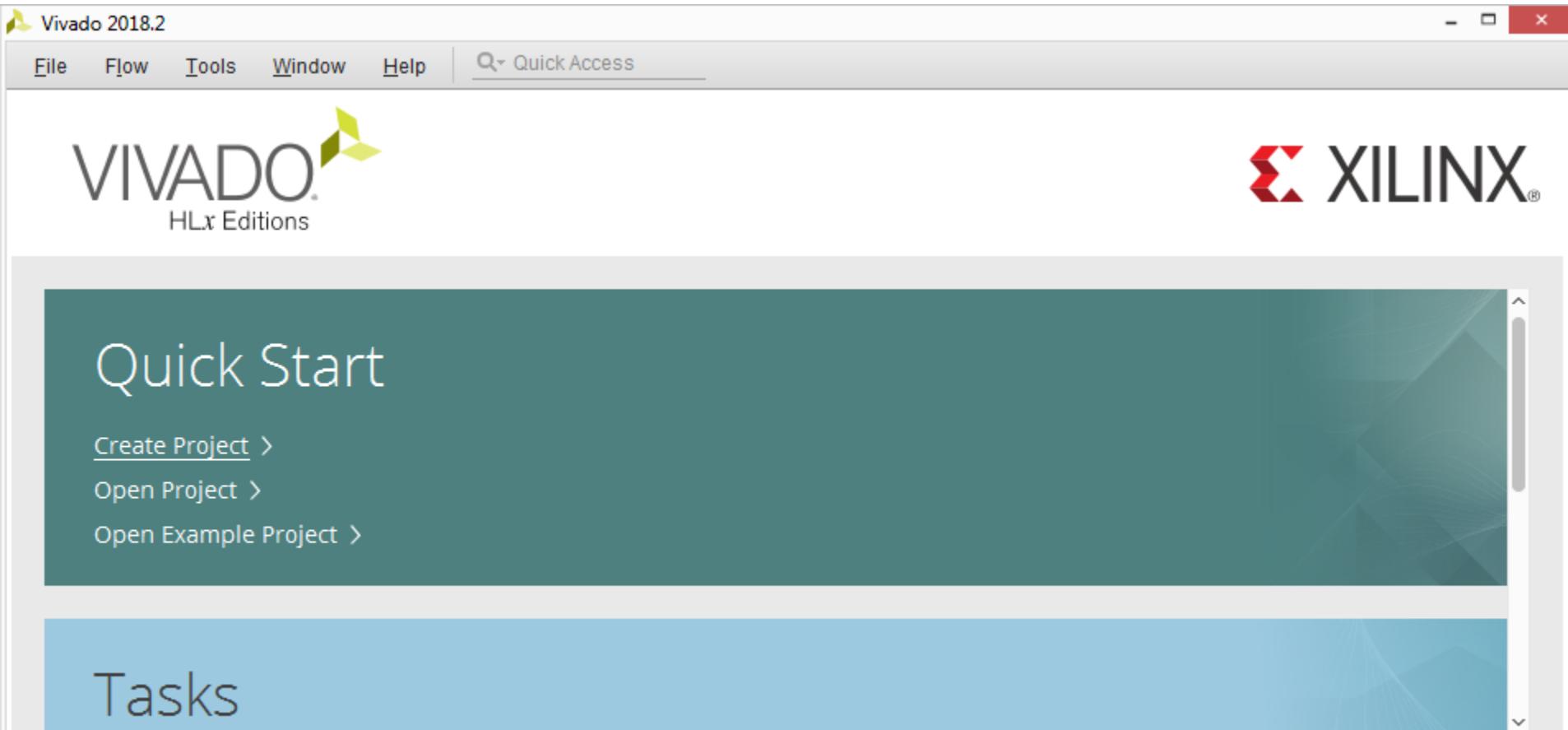


Generate MIG Example Design

> Open Vivado

Start → All Programs → Xilinx Design Tools → Vivado 2018.3 → Vivado

> Select Create Project



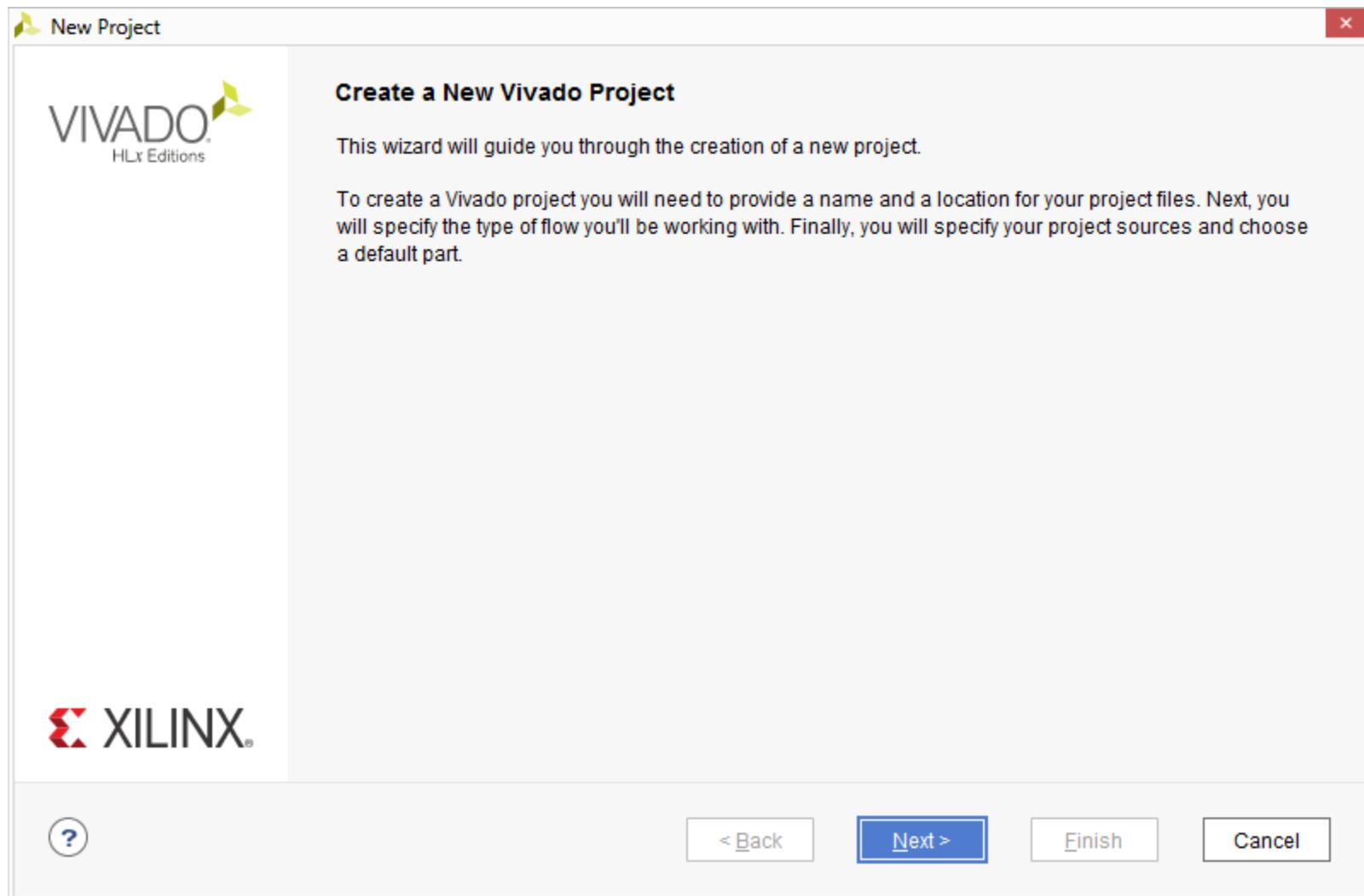
New Project Wizard will guide you through the process of selecting design sources and a target device for a new project.

Note: Presentation applies to the ZCU111

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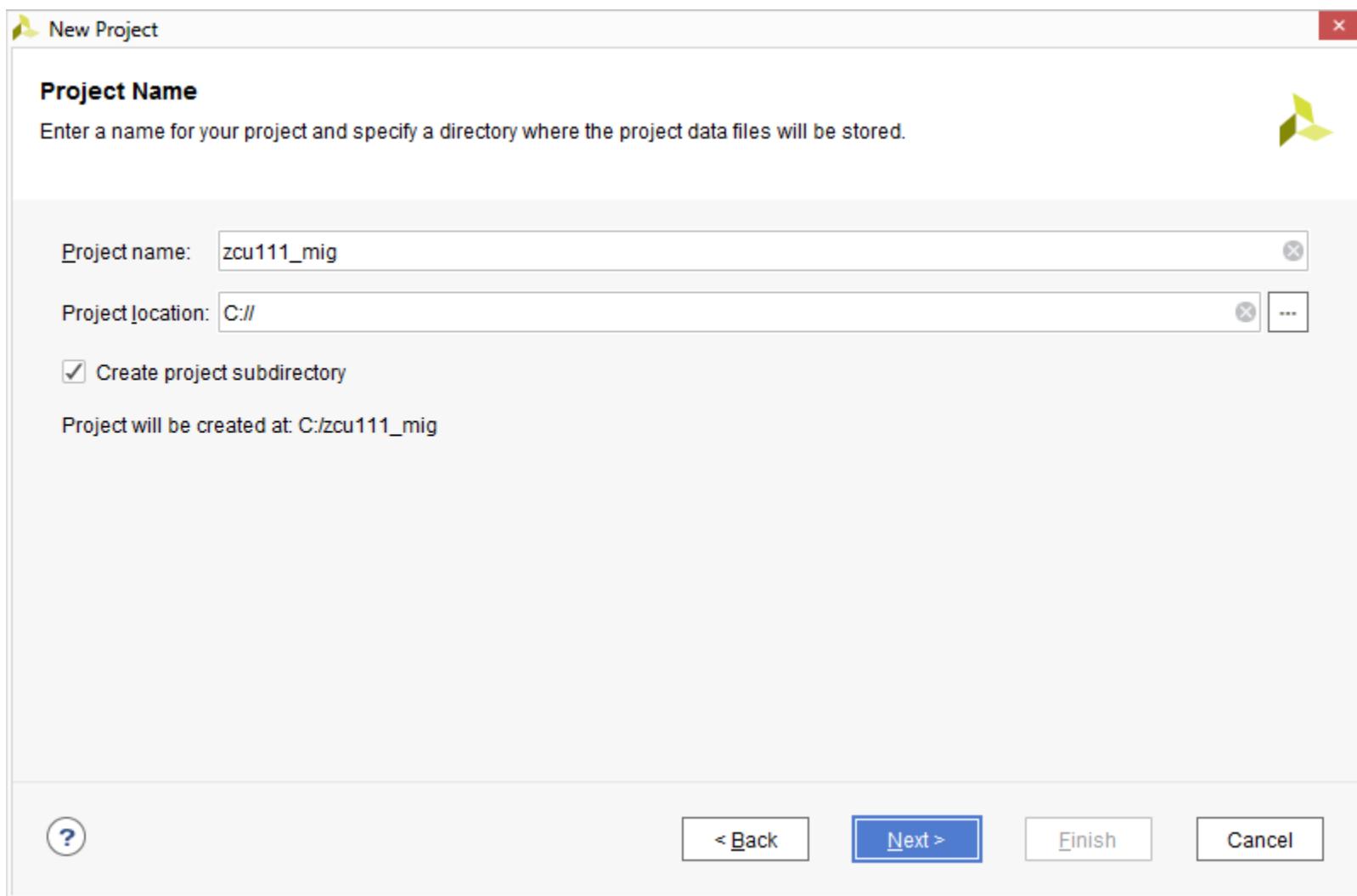
Generate MIG Example Design

> Click Next



Generate MIG Example Design

- > Set the Project name and location to zcu111_mig and C:/
 - » Check Create project subdirectory

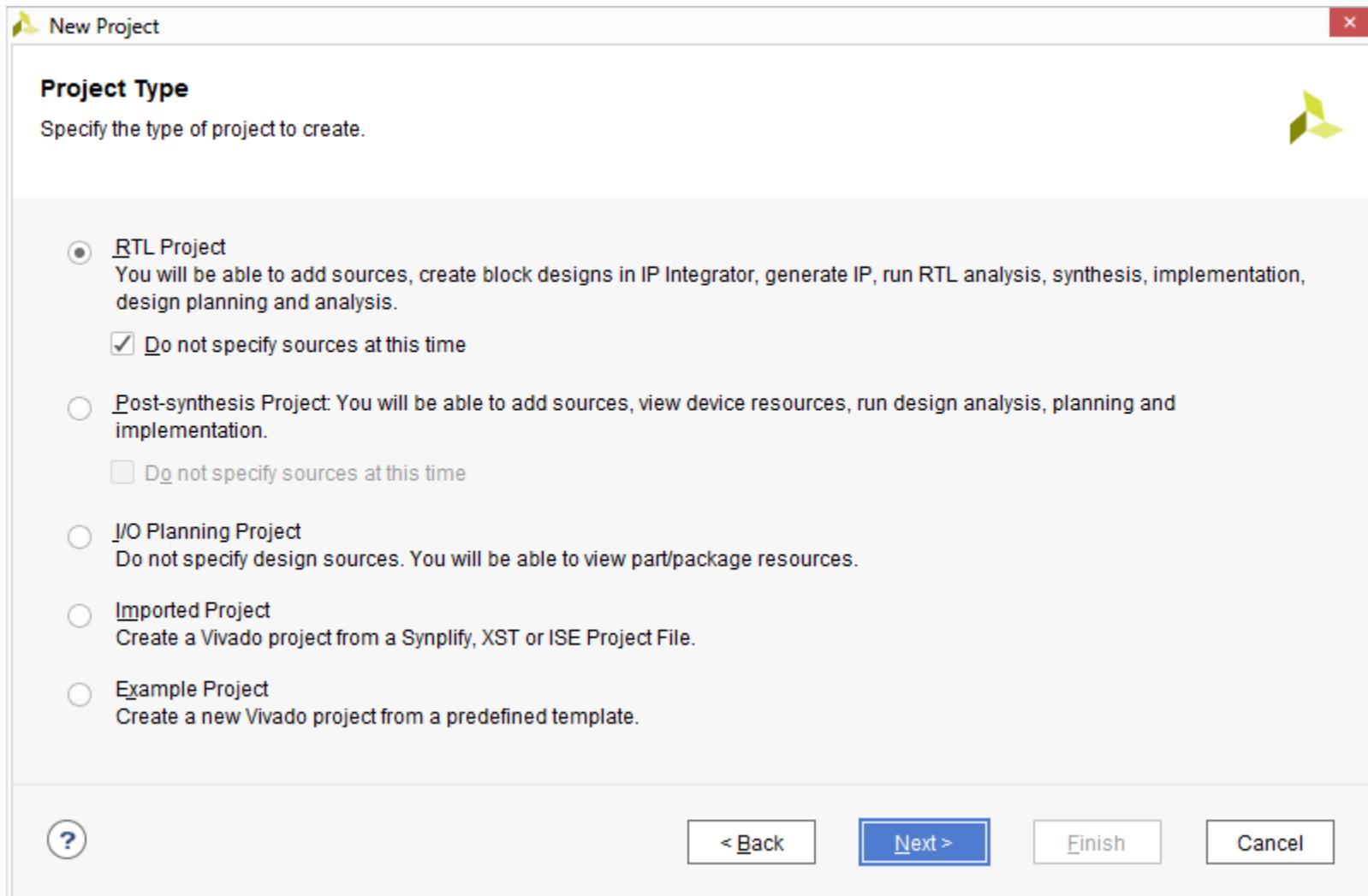


Note: Vivado generally requires forward slashes in paths

Generate MIG Example Design

> Select RTL Project

» Select Do not specify sources at this time



Generate MIG Example Design

- > Under Boards, select the ZCU111 Evaluation Platform

New Project

Default Part
Choose a default Xilinx part or board for your project. This can be changed later.

Parts | Boards

Reset All Filters

Vendor: All Name: All

Search:

Display Name	Preview	Vendor	File V
Zynq UltraScale+ ZCU111 Evaluation Platform		xilinx.com	1.1
Zynq UltraScale+ ZCU111-ES1 Evaluation Platform		xilinx.com	1.0

< >

?

< Back

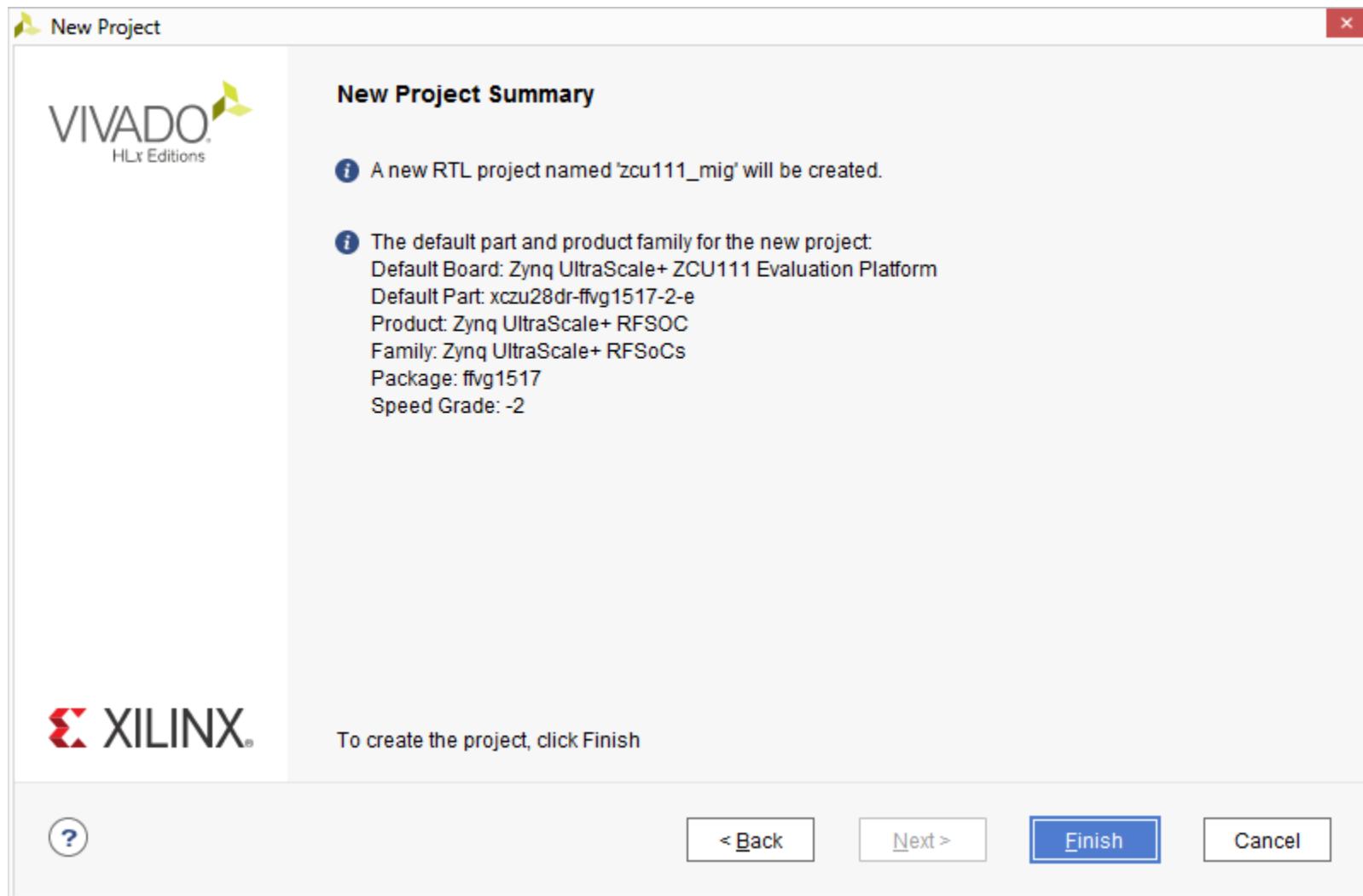
Next >

Finish

Cancel

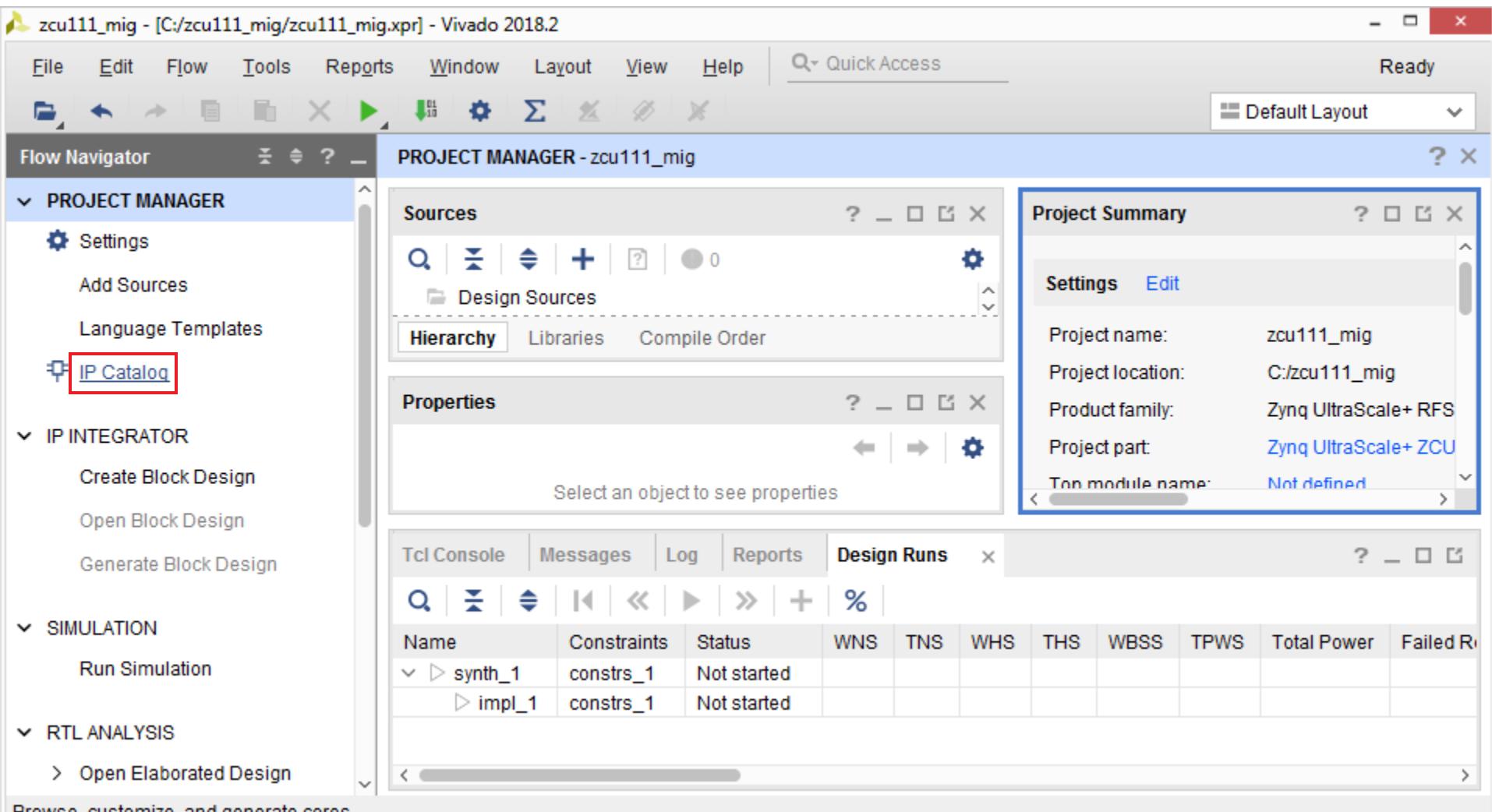
Generate MIG Example Design

> Click Finish



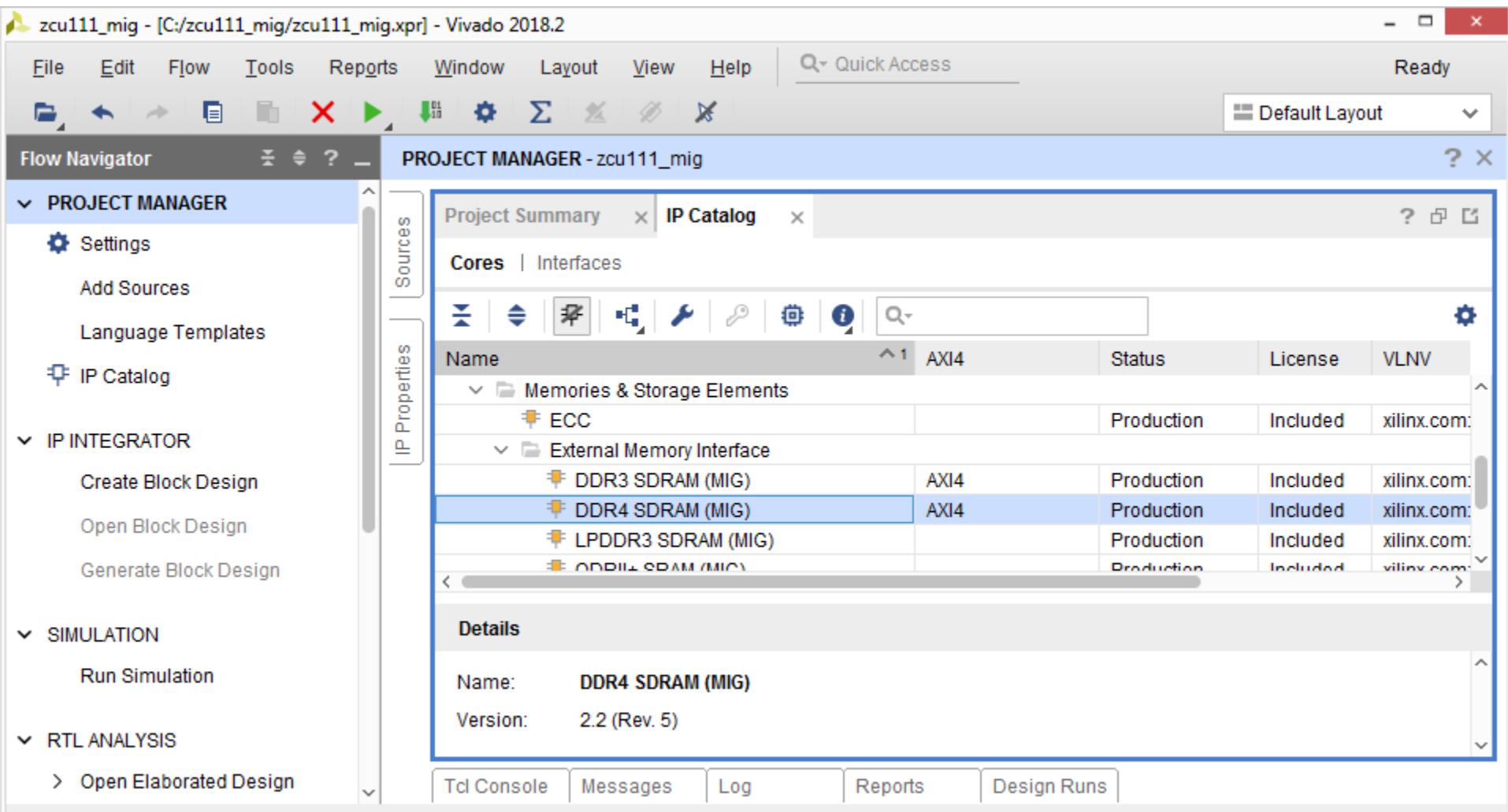
Generate MIG Example Design

- > Click on IP Catalog



Generate MIG Example Design

- > Select DDR4 SDRAM (MIG), v2.2



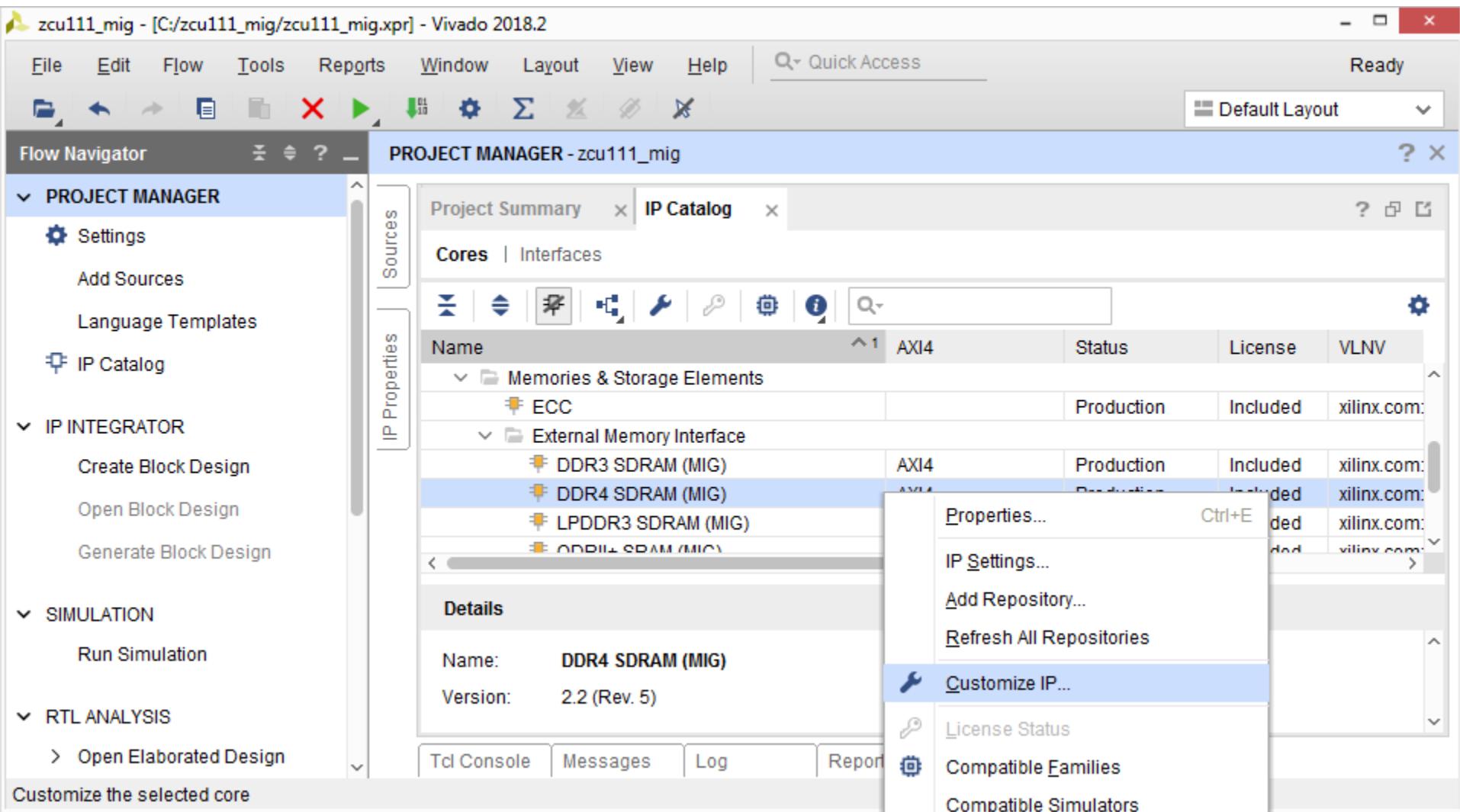
Note: Presentation applies to the ZCU111

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Generate MIG Example Design

- > Right click on DDR4 SDRAM (MIG)

- » Select Customize IP

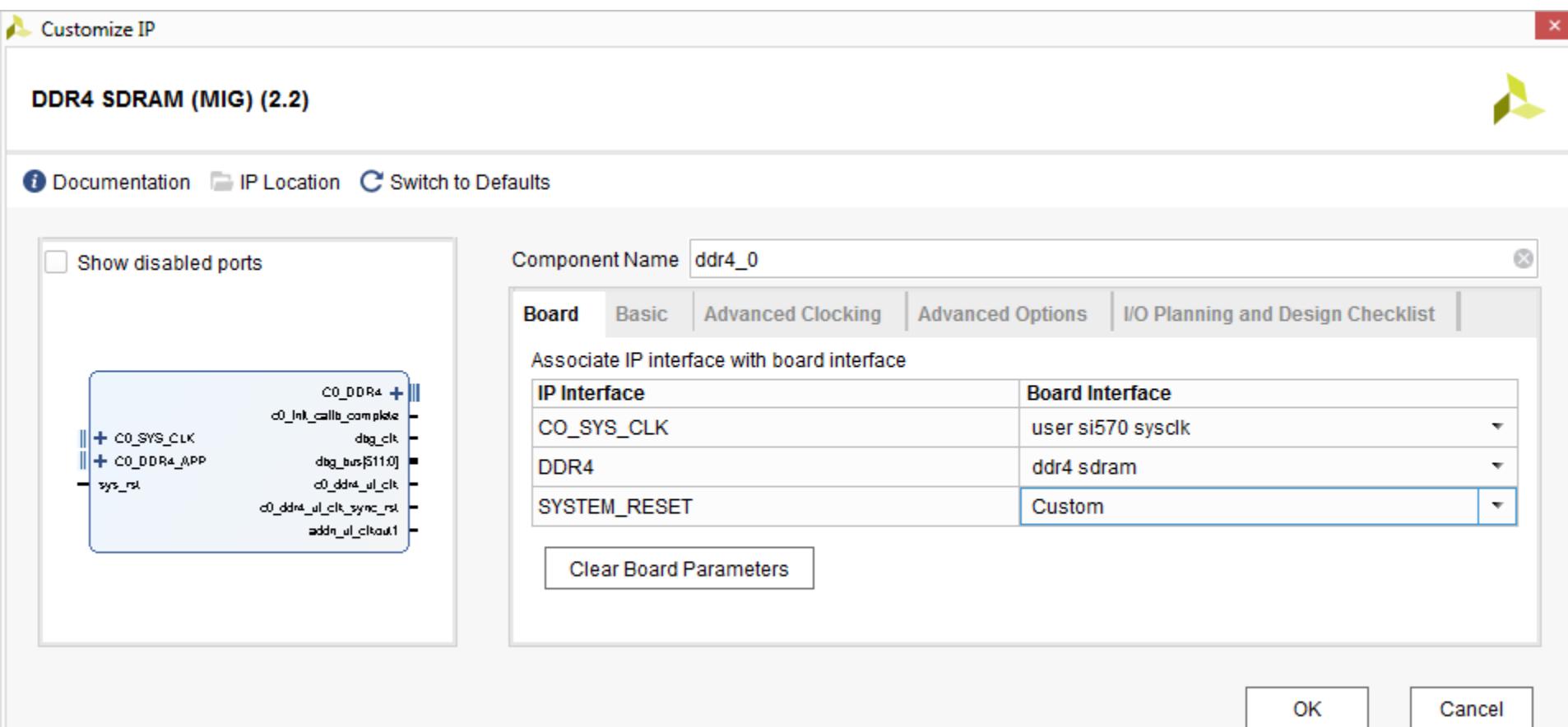


Note: Presentation applies to the ZCU111

Generate MIG Example Design

> Under the Board tab, set the Board Interfaces

- » Set C0_SYS_CLK to user si570 sysclk
- » Set C0_DDR4 to ddr4 sram
- » Set SYSTEM_RESET to Custom

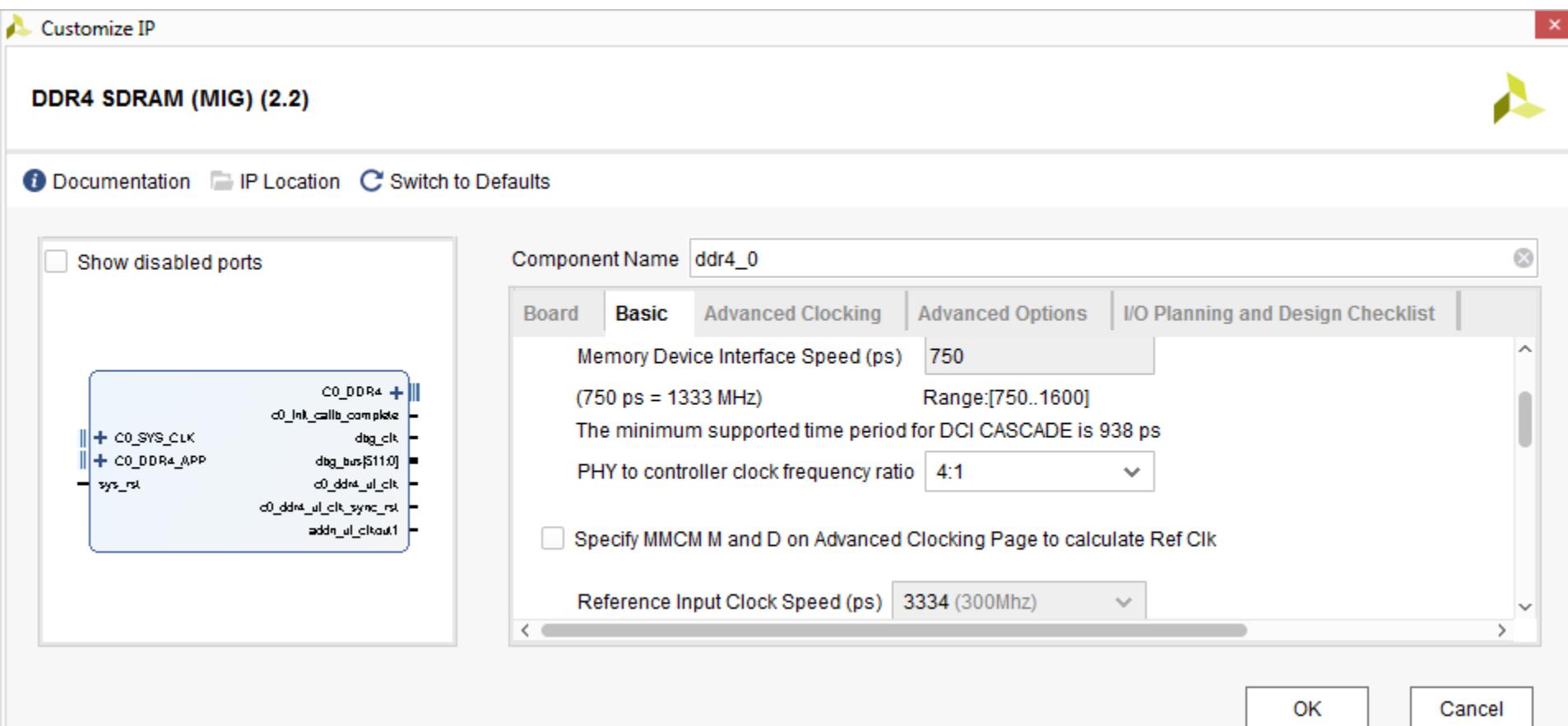


Generate MIG Example Design

> Under the Basic tab

- » The Memory Device Interface Speed is preset to 750 ps
- » The Reference Input Clock Speed is preset to 3334 ps

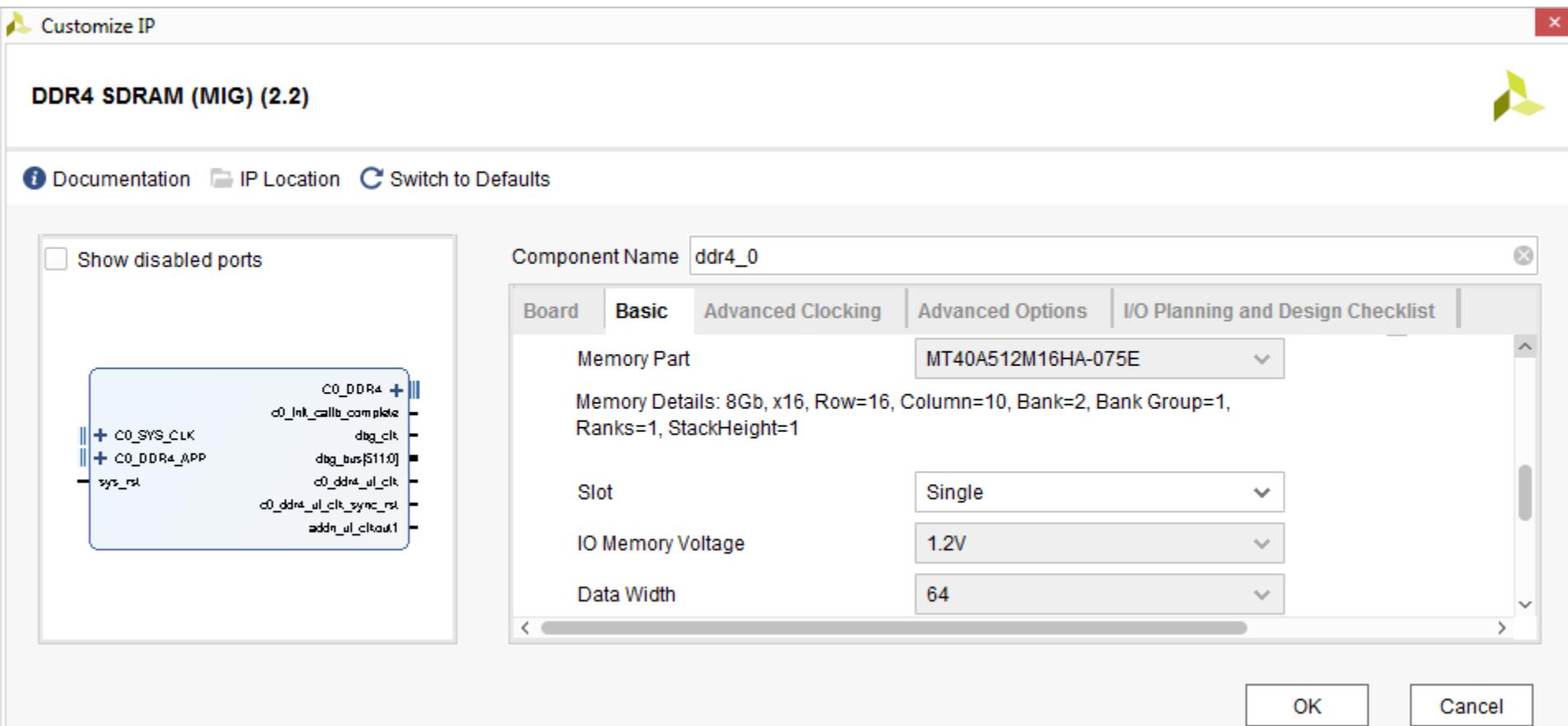
> Scroll down



Generate MIG Example Design

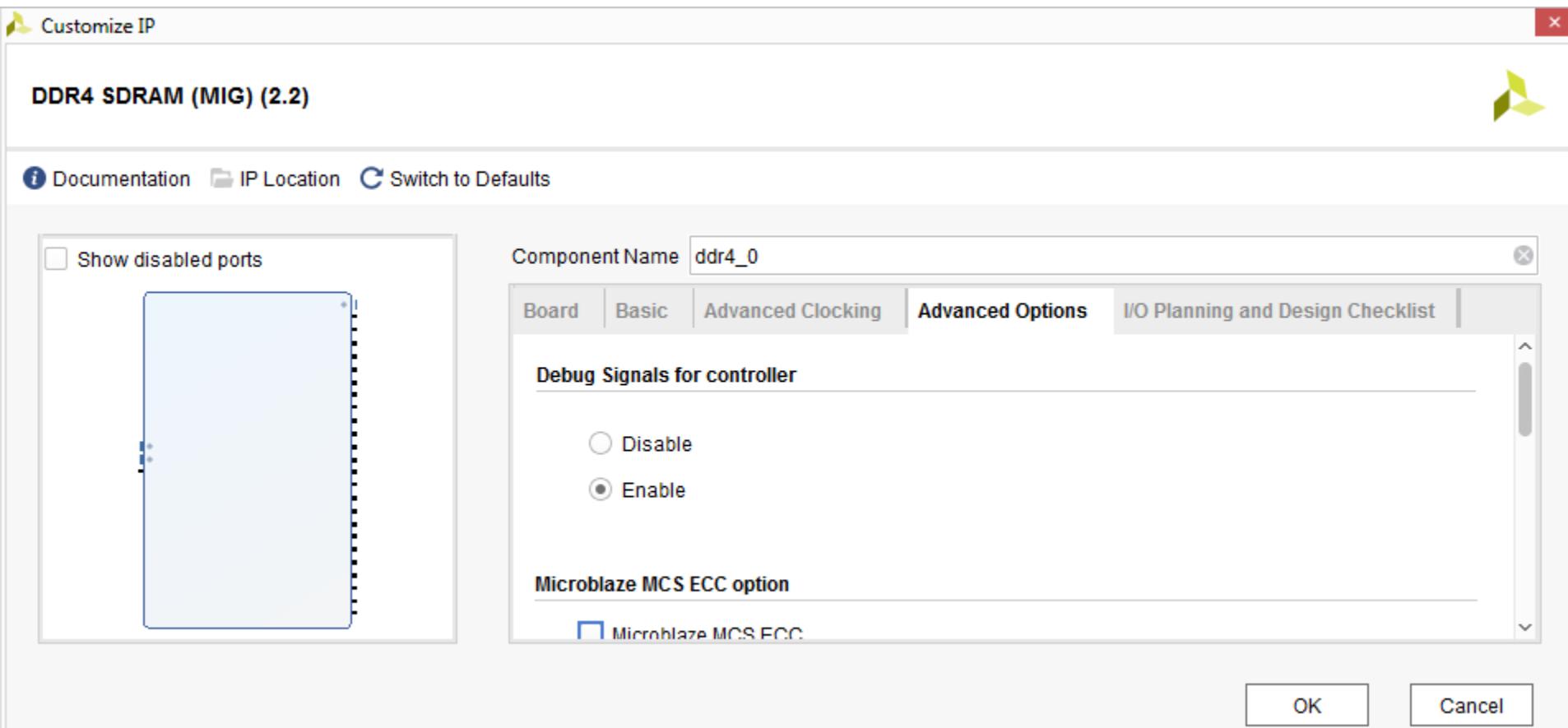
> Under the Basic tab

- » The Memory Part is preset to MT40A512M16HA-075E
- » The Data Width is preset to 64



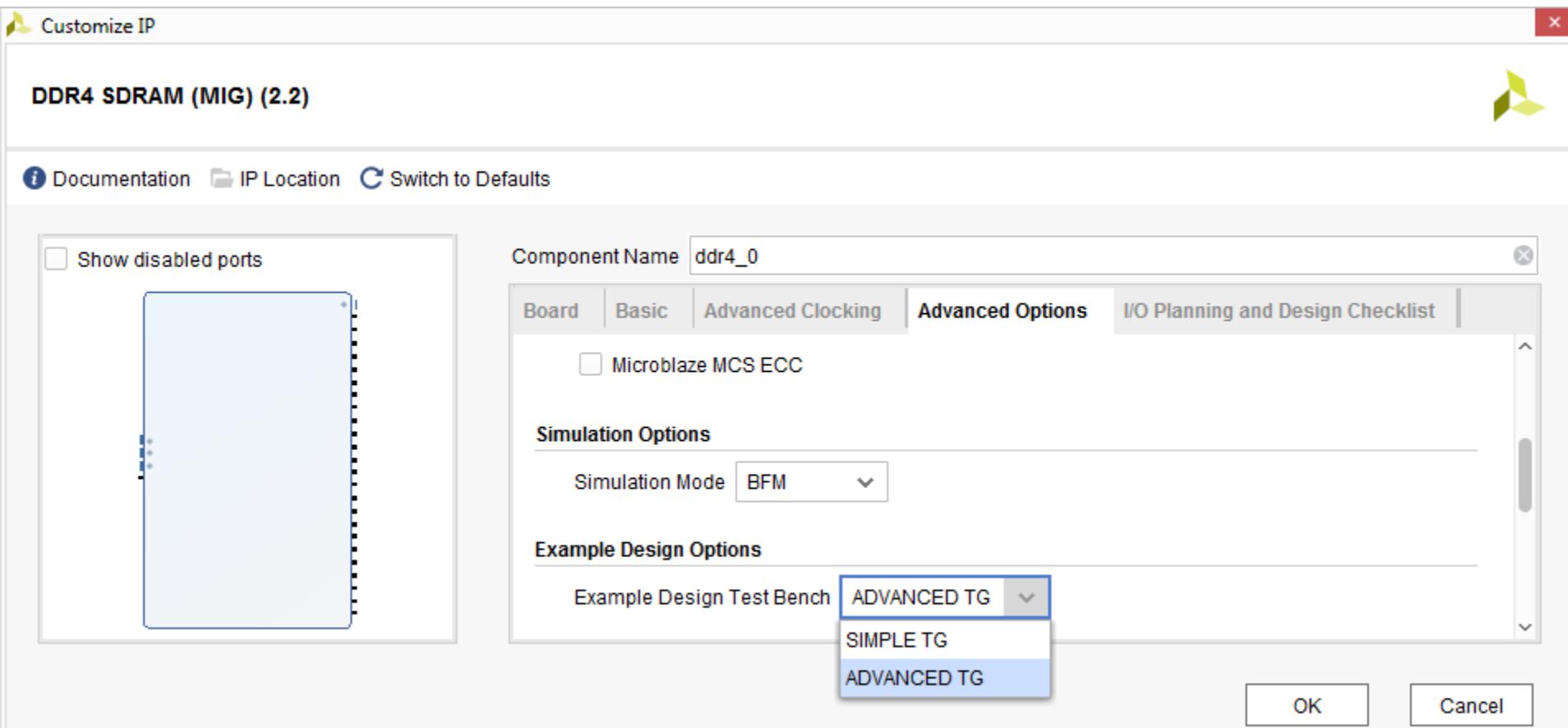
Generate MIG Example Design

- > Under the Advanced Options tab
 - » Set the Debug Signals to Enable
- > Scroll down



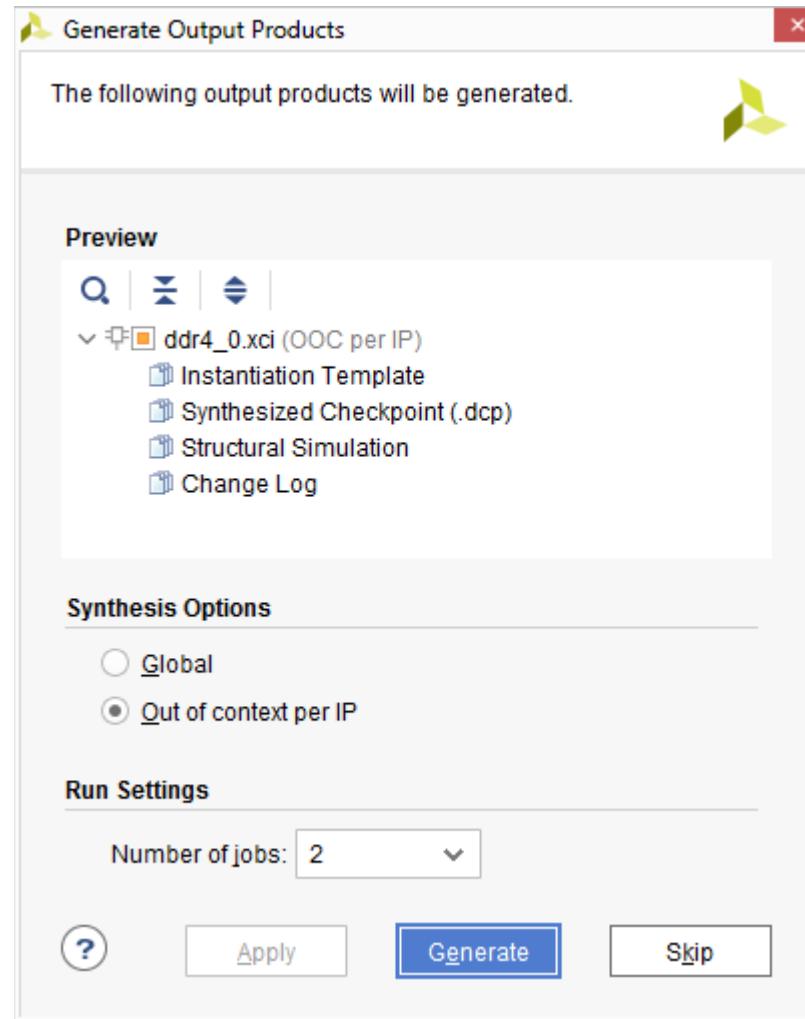
Generate MIG Example Design

- > Under the Advanced Options tab
 - » Set the Debug Signals to Enable
- > Click OK



Generate MIG Example Design

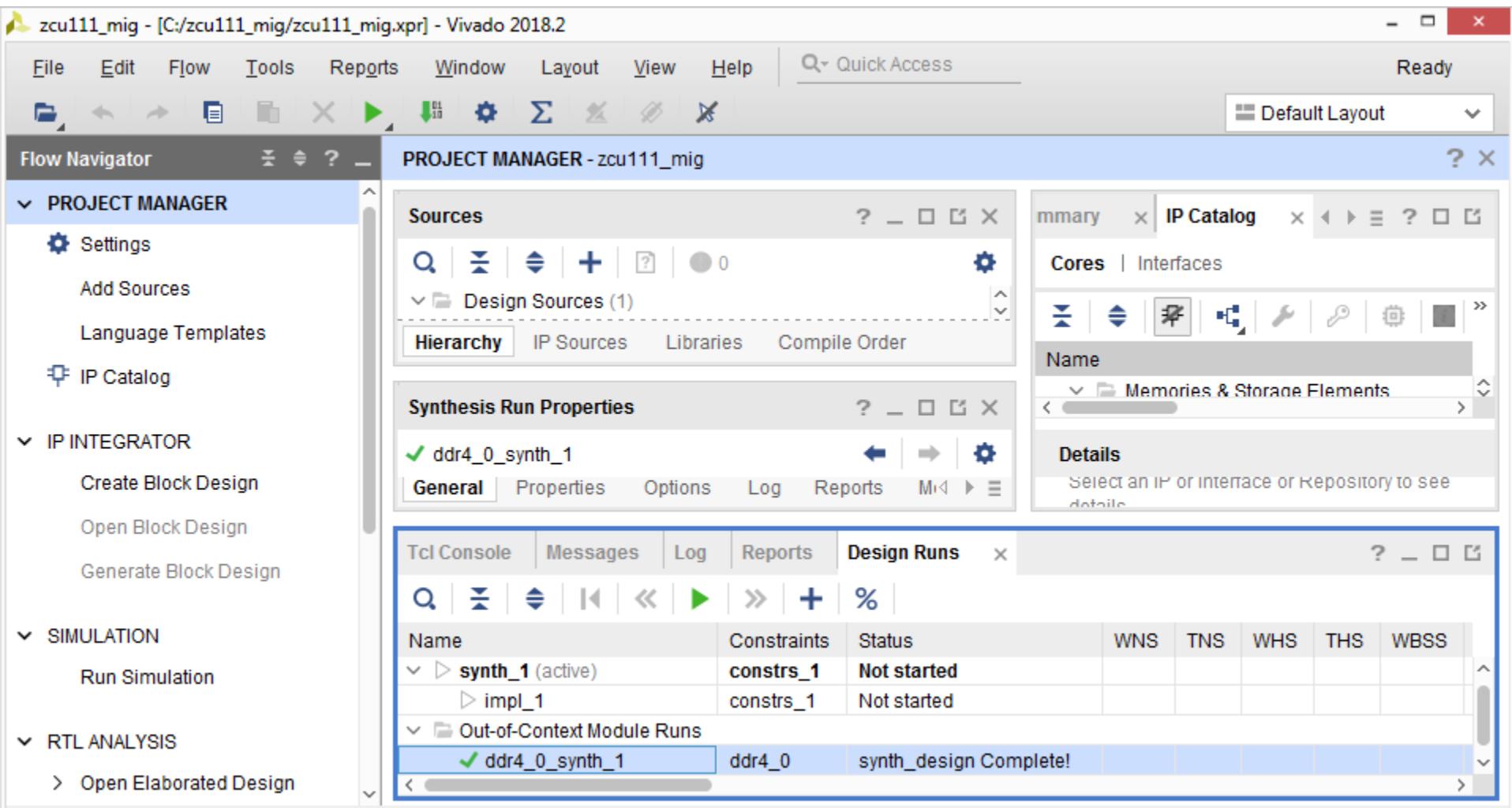
> Click Generate



Note: This step will take about 8 minutes

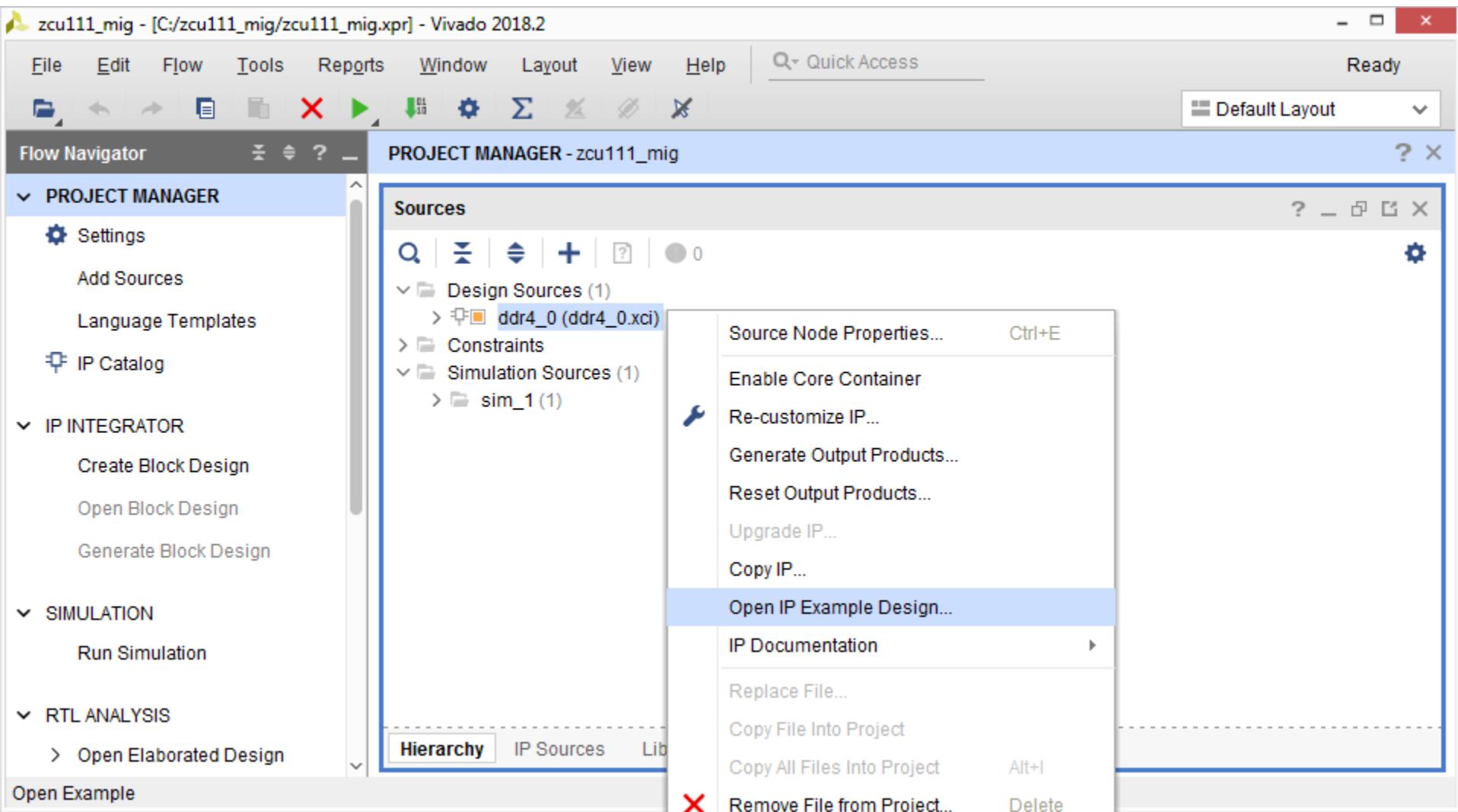
Generate MIG Example Design

- > Wait until checkmark appears on ddr4_0_synth_1



Compile Example Design

- > Right click on ddr4_0 and select Open IP Example Design...

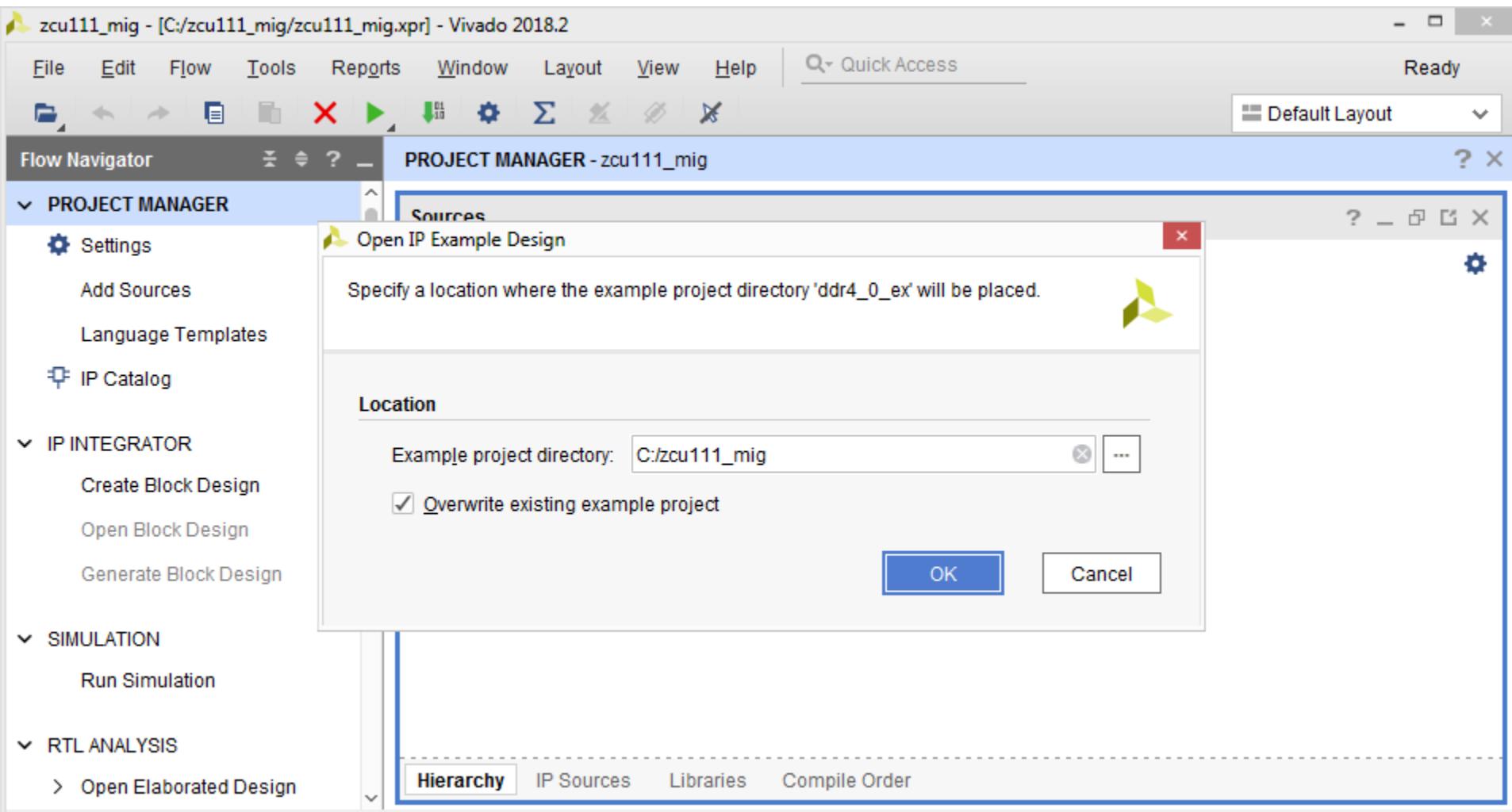


Note: Presentation applies to the ZCU111

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Compile Example Design

- > Set the location to C:/zcu111_mig and click OK



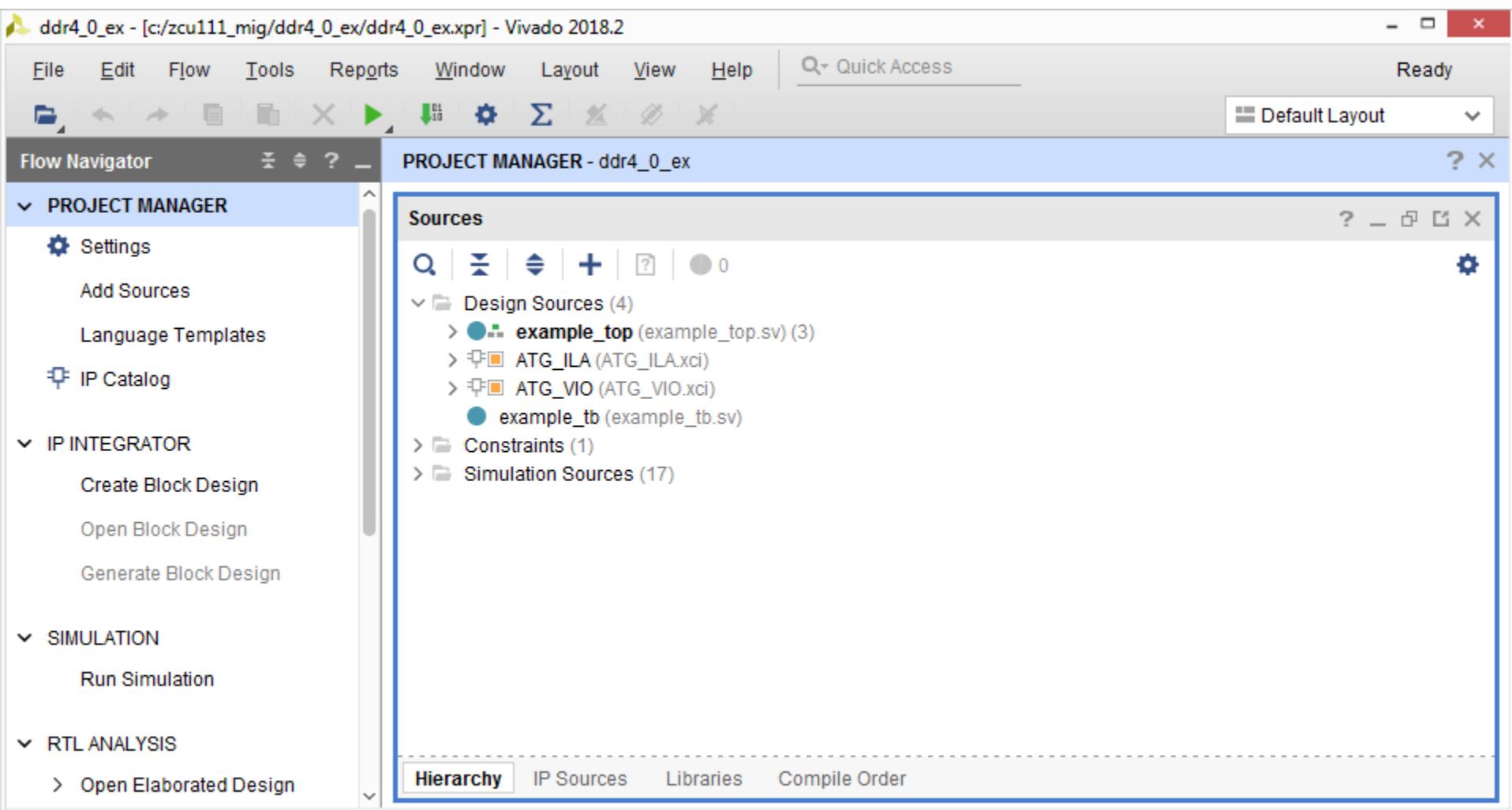
Open Example

Note: Presentation applies to the ZCU111

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Compile Example Design

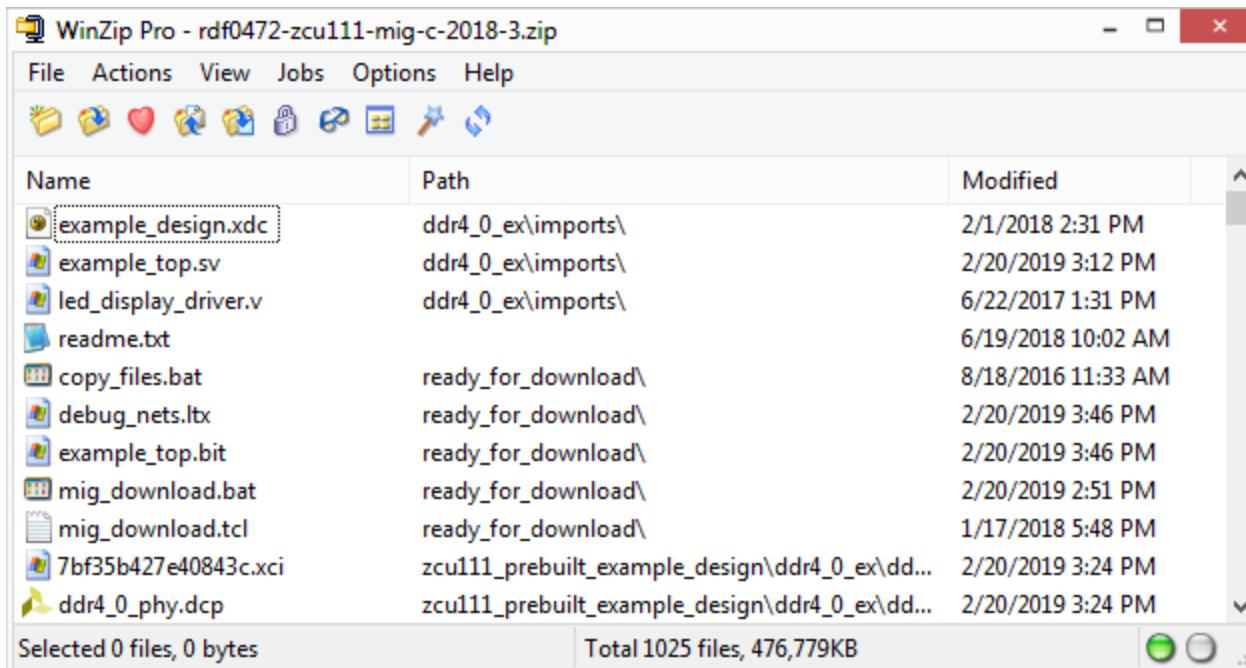
- > A new project is created under <design path>/



Note: The original project window can be closed

Modifications to Example Design

- > Unzip the **RDF0472 – ZCU111 MIG Design Files (2018.3 C) ZIP file** to your **C:\zcu111_mig** directory
 - » Contains several changes needed to support Zynq UltraScale+ devices
 - » Do this after creating the Example Design; changes only affect the Example Design



Modifications to Example Design

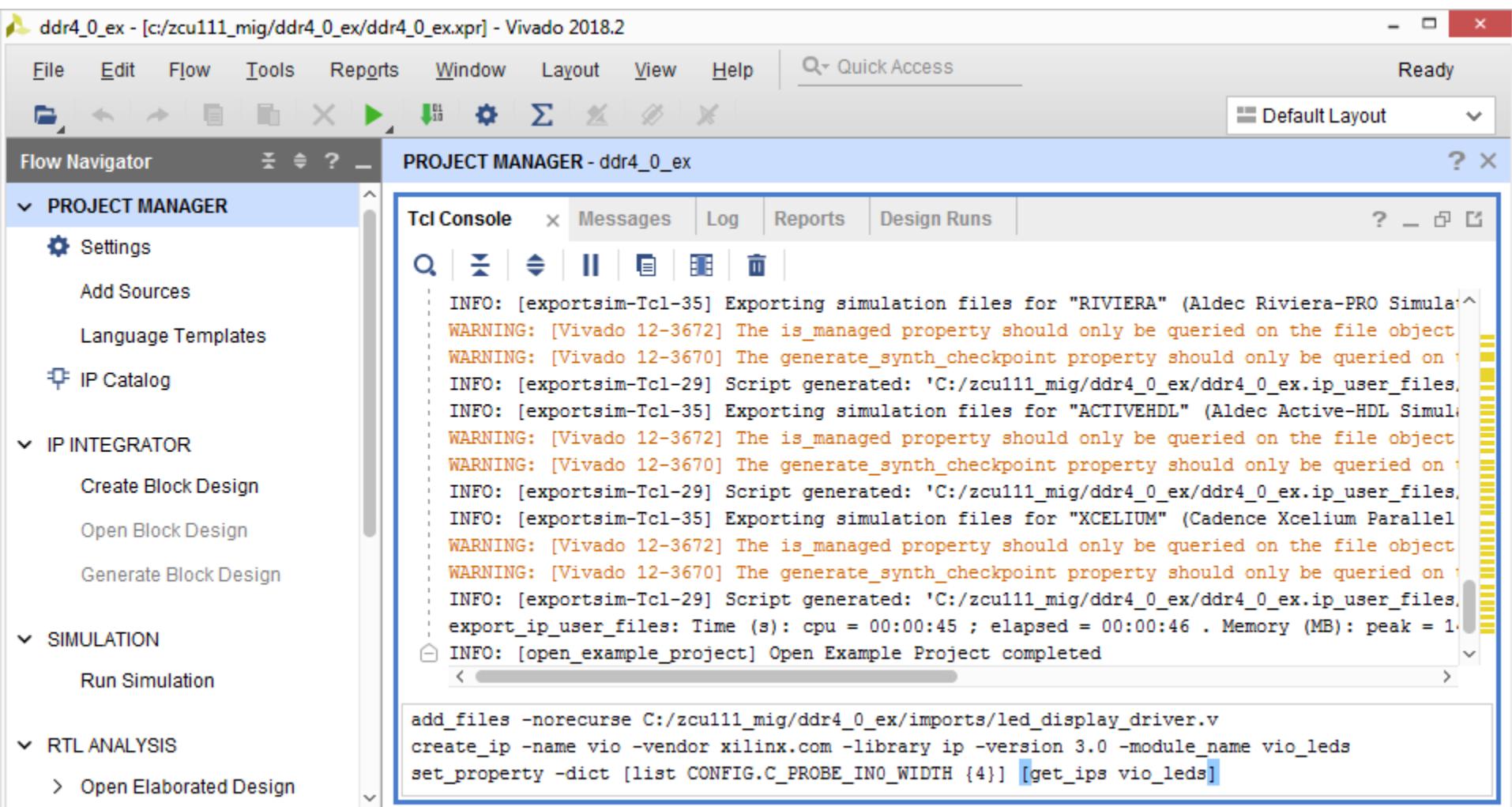
> Modifications to the example design

- » Added RTL and XDC modifications to drive LEDs
- » The following commands will add the led_display_driver.v and create the required VIO IP
- » From the Tcl Console, run these commands:

```
add_files -norecurse C:/zcu111_mig/ddr4_0_ex/imports/led_display_driver.v
create_ip -name vio -vendor xilinx.com -library ip -version 3.0 -module_name
vio_leds
set_property -dict [list CONFIG.C_PROBE_IN0_WIDTH {4}] [get_ips vio_leds]
```

Modifications to Example Design

- > Press enter after entering Tcl commands



Modifications to Example Design

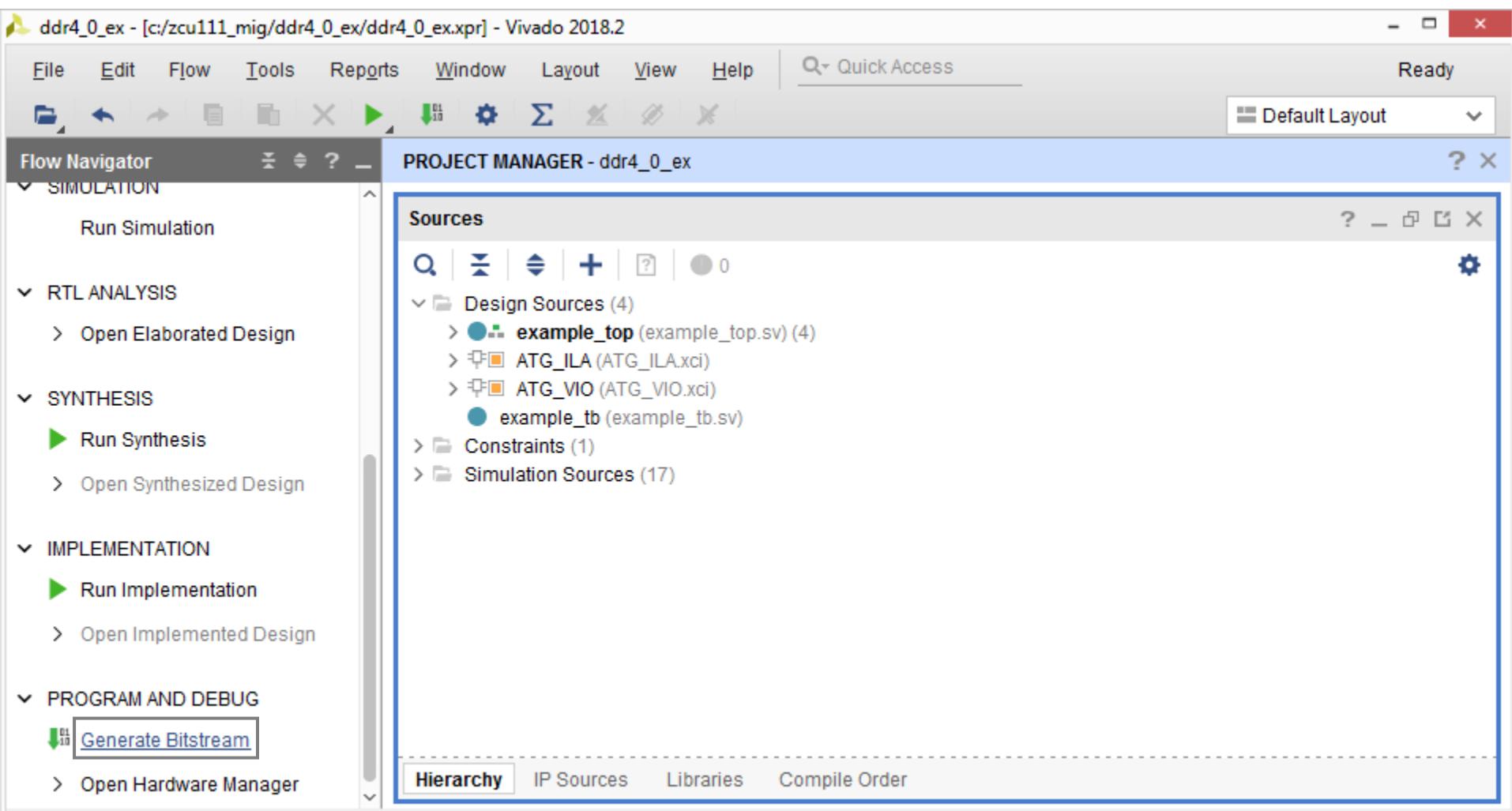
- > Tcl commands completed successfully

The screenshot shows the Vivado 2018.2 interface with the project "ddr4_0_ex" open. The left sidebar contains the Project Manager, IP Integrator, Simulation, and RTL Analysis sections. The main area is the PROJECT MANAGER - ddr4_0_ex window, which includes tabs for Tcl Console, Messages, Log, Reports, and Design Runs. The Tcl Console tab is active, displaying the following output:

```
INFO: [exportsim-Tcl-29] Script generated: 'C:/zcu111_mig/ddr4_0_ex/ddr4_0_ex.ip_user_files'
INFO: [exportsim-Tcl-35] Exporting simulation files for "XCELIUM" (Cadence Xcelium Parallel)
WARNING: [Vivado 12-3672] The is_managed property should only be queried on the file object
WARNING: [Vivado 12-3670] The generate_synth_checkpoint property should only be queried on t
INFO: [exportsim-Tcl-29] Script generated: 'C:/zcu111_mig/ddr4_0_ex/ddr4_0_ex.ip_user_files
export_ip_user_files: Time (s): cpu = 00:00:45 ; elapsed = 00:00:46 . Memory (MB): peak = 1
INFO: [open_example_project] Open Example Project completed
update_compile_order -fileset sources_1
add_files -norecurse C:/zcu111_mig/ddr4_0_ex/imports/led_display_driver.v
C:/zcu111_mig/ddr4_0_ex/imports/led_display_driver.v
create_ip -name vio -vendor xilinx.com -library ip -version 3.0 -module_name vio_leds
c:/zcu111_mig/ddr4_0_ex/ddr4_0_ex.srcs/sources_1/ip/vio_leds/vio_leds.xci
set_property -dict [list CONFIG.C_PROBE_IN0_WIDTH {4}] [get_ips vio_leds]
0
update_compile_order -fileset sources_1
```

Compile Example Design

- > Click on Generate Bitstream



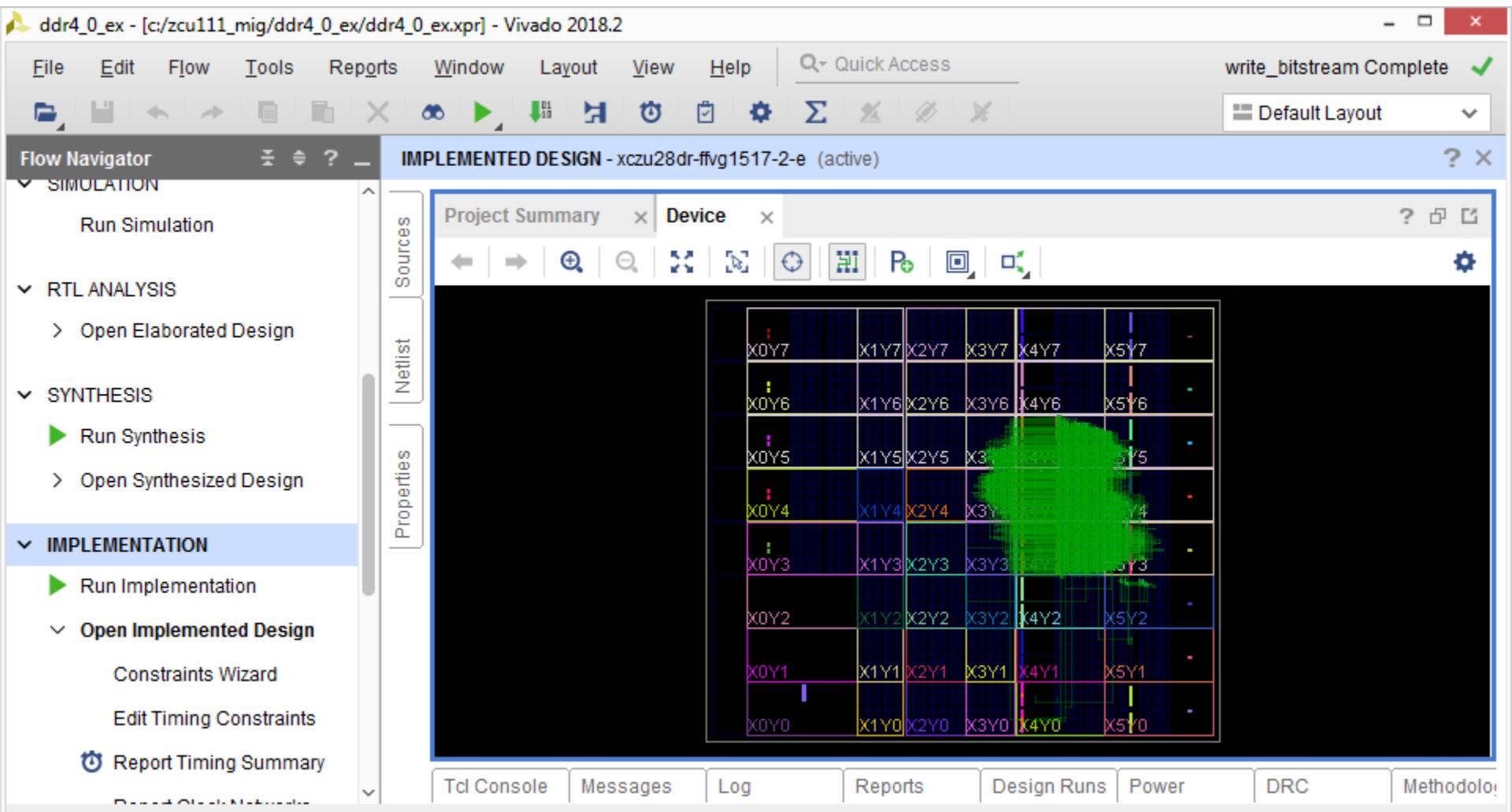
Generate a programming file after implementation

Note: Presentation applies to the ZCU111

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Compile Example Design

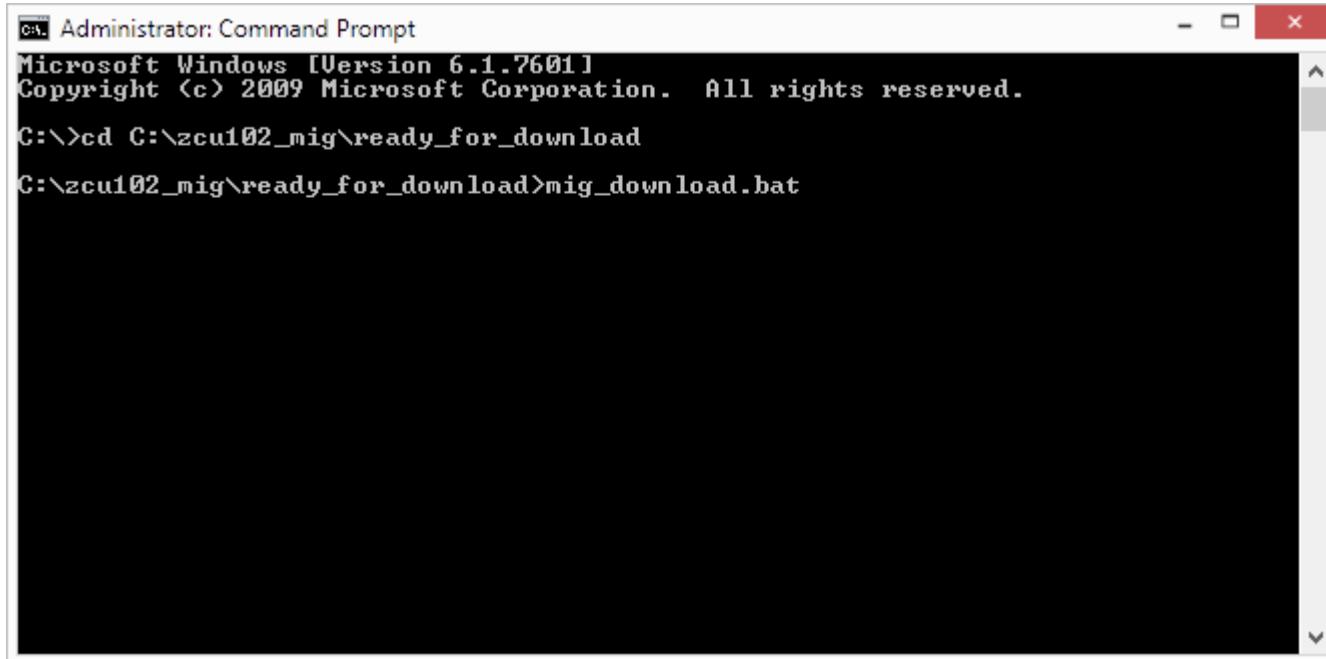
- > Open and view the Implemented Design



Run MIG Example Design

- > From a Command Prompt, type:

```
cd C:\zcu111_mig\ready_for_download  
mig_download.bat
```

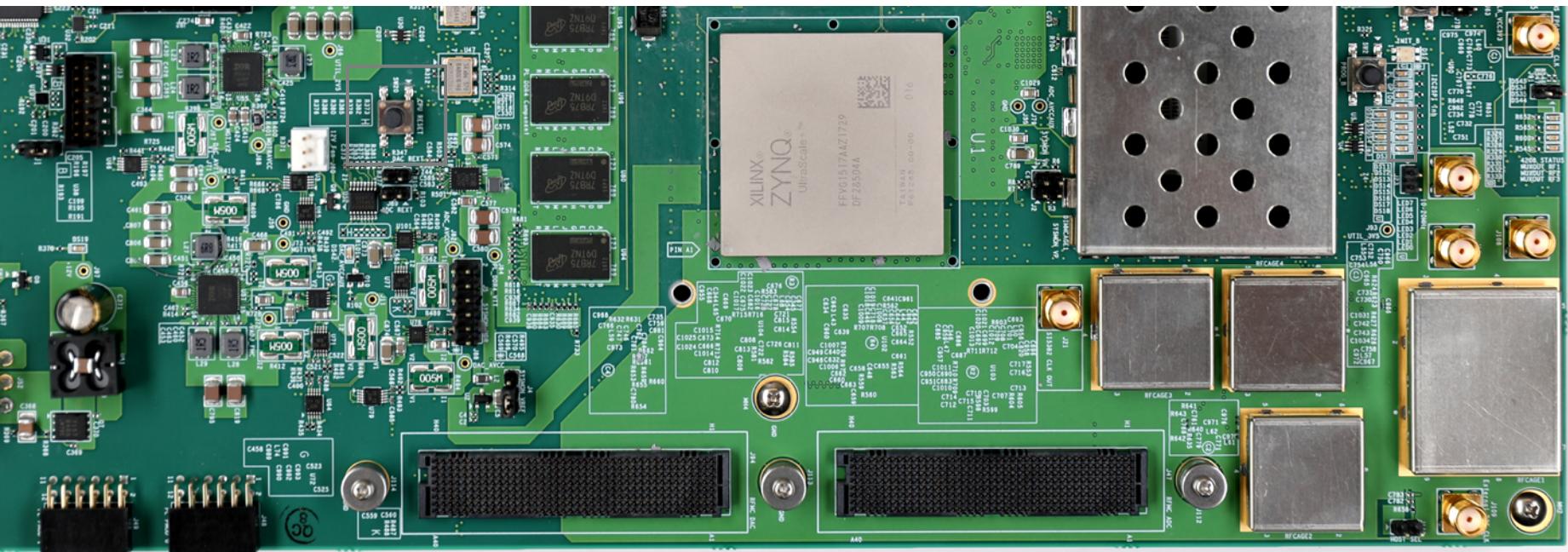


The screenshot shows a Windows Command Prompt window titled "Administrator: Command Prompt". The window is running on Microsoft Windows [Version 6.1.7601]. The command history shows the user navigating to the directory C:\zcu102_mig\ready_for_download and executing the batch file mig_download.bat. The output of the command is a large black rectangular area, likely indicating a progress bar or a redacted log.

```
C:\>cd C:\zcu102_mig\ready_for_download  
C:\zcu102_mig\ready_for_download>mig_download.bat
```

Run MIG Example Design

- > After bitstream loads, LED 0 (bottom most LED) will be lit, and LED1 will be blinking
- > LED 3 will light and stay on
 - » This indicates Calibration has completed
 - » Calibration may take a few seconds
- > If an error occurs, LED 0 will go out and LED 2 will light
 - » The “CPU_RESET” button, SW20, is the reset



References



References

> Zynq UltraScale Memory

- » UltraScale FPGA Memory Interface Solutions Product Guide – PG150
 - https://www.xilinx.com/support/documentation/ip_documentation/ultrascale_memory_ip/v1_4/pg150-ultrascale-memory-ip.pdf
- » Memory IP UltraScale Design Checklist – XTP359
 - http://www.xilinx.com/support/documentation/ip_documentation/ultrascale_memory_ip/xtp359-memory-ip-ultrascale-design-checklist.zip

> Vivado Programming and Debugging

- » Vivado Design Suite Programming and Debugging User Guide – UG908
 - http://www.xilinx.com/support/documentation/sw_manuals/xilinx2018_3/ug908-vivado-programming-debugging.pdf

Documentation



Documentation

> Zynq UltraScale+

- » Zynq UltraScale+ RFSoC
 - <https://www.xilinx.com/products/silicon-devices/soc/rfsooc.html>

> ZCU111 Documentation

- » Xilinx Zynq UltraScale+ RFSoC ZCU111 Evaluation Kit
 - <https://www.xilinx.com/products/boards-and-kits/zcu111.html>
- » ZCU111 Board User Guide – UG1271
 - https://www.xilinx.com/support/documentation/boards_and_kits/zcu111/ug1271-zcu111-eval-bd.pdf
- » ZCU111 Evaluation Kit Quick Start Guide User Guide – XTP490
 - https://www.xilinx.com/support/documentation/boards_and_kits/zcu111/xtp490-zcu111-quickstart.pdf
- » ZCU111 - Known Issues Master Answer Record
 - <https://www.xilinx.com/support/answers/70958.html>