COL215P Assignment 1: 4-Digit 7-Segment Display

Abhinav Shripad(2022CS11596)
Aneeket Yadav(2022CS11116)

August 2023

1 Task

Design and implement a circuit that takes a 4-digit decimal/hexadecimal number (so each number is 4-bit) from switches in the Basys3 board and displays it on the 4-seven segment displays on the board. Use the on-board clock and create a timing circuit to drive all the displays

2 Overview

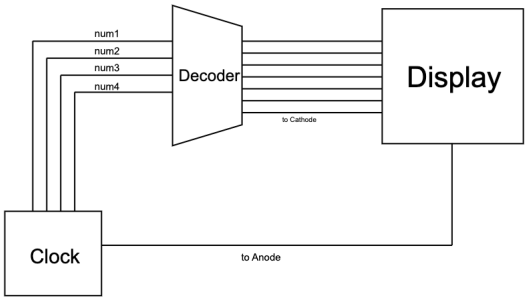

Figure 1: Block Diagram of Stopwatch

3 Implementation

3.1 Digits

Since we are implementing hexadecimal system, we need 16 digits to represent the output. We use the following symbols.

Figure 2: Hexadecimal Digits

3.2 Boolean Table

Digit	A	B	C	D	E	F	G
0	1	1	1	1	1	1	0
1	0	1	1	0	0	0	0
2	1	1	0	1	1	0	1
3	1	1	1	1	0	0	1
4	0	1	1	0	0	1	1
5	1	0	1	1	0	1	1
6	1	0	1	1	1	1	1
7	1	1	1	0	0	0	0
8	1	1	1	1	1	1	1
9	1	1	1	1	0	1	1
A	1	1	1	0	1	1	1
b	0	0	1	1	1	1	1
C	1	0	0	1	1	1	0
d	0	1	1	1	1	0	1
E	1	0	0	1	1	1	1
F	1	0	0	0	1	1	1

3.3 Minimum Combinational Logic

We use the notation that A,B,C,D,E,F and G denote the state of corresponding segment on the display. We will use the K-Map to solve and get the minimum combinational logic between the variables.

Writing the corresponding minterms for each K-Map(wherever 1 is present) we get the minimized boolean logic for all.

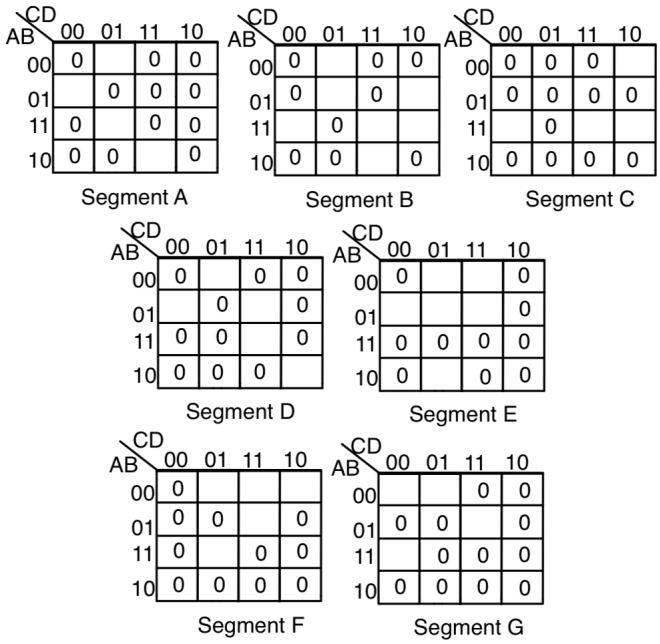

Figure 3: K-Maps for 7 Segments

Solving the above K-Maps will result in the following Boolean relations:-

$$A = a'b'c'd + a'bc'd' + abc'd + ab'cd$$

$$B = a'bc'd + abc'd' + bcd' + acd$$

$$C = a'b'cd' + abc'd' + abc$$

$$D = a'b'cd' + a'bc'd' + bcd + ab'cd'$$

$$E = a'd + a'bc' + b'c'd$$

$$F = a'b'c + a'b'd + a'cd + abc'd$$

$$G = a'b'c' + a'bcd + abc'd'$$

$$DP = 0$$

4 Modules

4.1 Decoder

The decoder is a combinational module which takes in 4 bit input and generates signal for the cathode pins of the display. We created a minimum SOP expressions for each of the 7 cathode pins using Karnaugh maps.

4.2 Timing Circuit

The timing circuit essentially contained the logic on which the clock operates. Based on its input the value a,b,c and d changes their value periodically.

5 Submission Details and References

The submission consists of files- basys3.xdc (which contains the signal mapping for the board), SegmentDisplay.vhf,testbench.vhd and the generated SegmentDisplay.bit file along with LUTs screenshots with project related images of the working project. The LUTs has been attached below:-

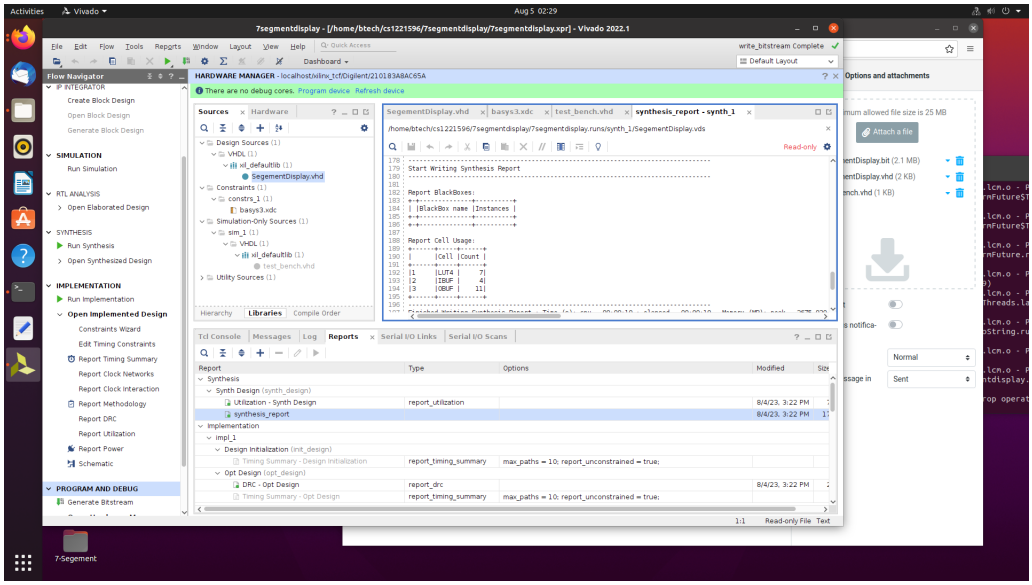

Figure 4: LUTs