THE POINT SEVEN

Department of Electronics & Communications Engineering

A PROJECT REPORT

on

Design And Implementation of 6T SRAM Cells

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Abstract

Static Random Access Memory is one of the important memory devices which stores data on a chip.SRAM has played a major role as a key component in VLSI chips because of its high storage density and quick access time. Due to the necessity of low power consumption and low voltage memory, SRAM has been prioritised. It is a cache memory which can be directly interfaced with the CPU.This report focuses on design and implementation of 6T SRAM cell with read and write operations in standard CMOS process technology at 90nm technology. The schematic,DC Analysis and the layout are also included in this work.Cadence Virtuoso software has been used to simulate.The Static Noise Margin curves were analysed to understand the performance of SRAM cell.

Introduction

There are different types of memory types as shown in the fig 1.

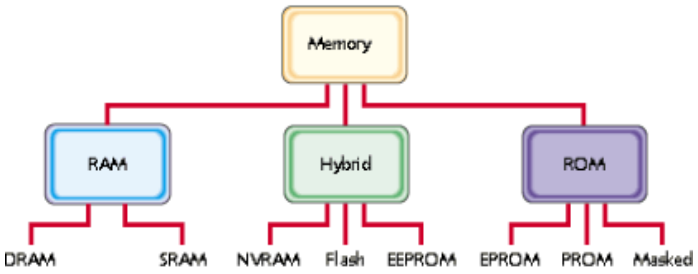


fig.1:Hirearchy of memory

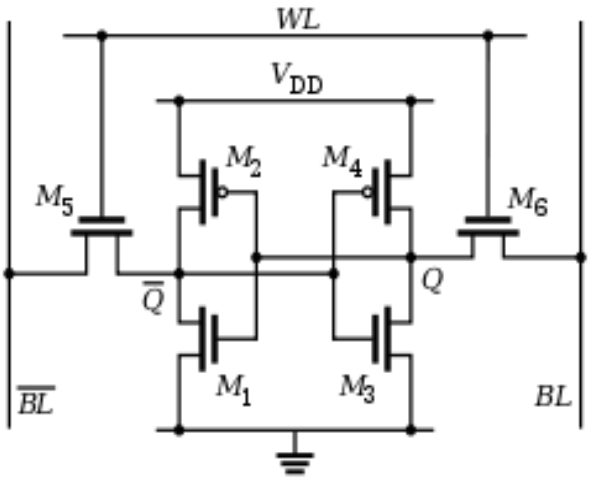
SRAM is a semiconductor memory cell used in a variety of electronic devices.It is mostly operated in battery operated devices which requires less area and has low power consumption.The processors which require less read and write delay constitute SRAM.It uses latching circuitry to store each bit. SRAM being a volatile memory,the data will be lost when the power is switched off.Unlike DRAM,SRAM does not require any refresh circuit.The two main objectives while designing a SRAM are low operating voltage and low power consumption for battery operated devices.It is widely used in personal computers and peripheral equipment.It is also used in Digital Signal Processing circuits.

The different types of SRAM includes

1. Non-volatile SRAM
2. Pseudostatic RAM
3. By transistor type RAM
4. By feature
5. By function

There are many other different types of SRAM based on the function and the features .Typical SRAM cell is made up of six MOSFETs,familiar as 6T SRAM cell.Four Transistors form the cross coupled inverters in which each bit is stored.The other two transistors are the access transistors.With the advantages of SRAM these cells are used in many portable devices.

Working :



The 6T SRAM cell contains a pair of weakly cross coupled inverters holding the state (inv1-M1&M2, inv2-M3&M4), It also contains a pair of access transistors (M5 & M6) to read and write the states. The write operation is done by driving the desired value and its compliment into the bit lines named as BL and $\underline{BL}$, then raising the word line named as WL.

The Overpowering of the data is done using the cross coupled inverters. The pre charging of the two bit lines is first set to high and then let to float. When word is raised the $\underline{BL}$ is pulled down, indicating the value of the data. The main challenge of the SRAM is to ensure that the

circuit holding the state is weak enough to ensure the write operation by overpowering the previously stored value and strong enough so that it can be retained during the read operation. Both of them should be ensured to for proper READ and WRITE operations respectively.

Access transistors M5 and M6 are connected to BL and $\underline{BL}$, so that we can read from the memory or write into the memory. If WL is equal to 1, we can access the access transistors and hence read and write operations can be performed. If WL is equal to 0, the access to the transistors will be off and memory will be in hold state. In hold mode (i.e. WL=0) the access transistors M5 and M6 are turned off. So as long as SRAM in this mode, the data will remain unchanged. To write into the memory BL and $\underline{BL}$ acts as input, to read from the memory BL and $\underline{BL}$ acts as output lines.

Read/Write operation:

READ operation:

In SRAM, for any operation to be performed, the word line(WL) should be high. To perform read operation, initially memory should have some value. Therefore let us consider memory has Q=1 and $\underline{Q}$=0. Raise the word line(WL=0) to high, to perform the read operation BL and $\underline{BL}$ acts as output lines, and these bit lines are initially pre-charged i.e. there will be a node voltage Vdd at bit and bit_b . As Q and BL are high, there will be no discharge in the circuit . As $\underline{Q}$ is 0, there will be a voltage difference between the $\underline{Q}$ and the node voltage at $\underline{BL}$, hence $\underline{BL}$ voltage decreases. Therefore there will be discharge in the circuit and current flows. BL and $\underline{BL}$ are connected to the sense amplifier , this sense amplifier acts as a comparator, so When $\underline{BL}$ is low and BL is high the output will be 1. Hence input Q=1 and we got the output as 1, read operation verified . In the same way consider Q=0 and $\underline{Q}$=1 in the memory. There will be a discharge in the circuit at Q and BL, since there is voltage difference. As BL voltage decreases the output will be 0 when input Q=0, the output we get is 0. Therefore in both the cases read operation is verified.

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WRITE operation :

Consider the memory bits consists of Q=0 and $\underline{Q}$ =1. Initially word line (WL=1) is high and hence write operation can be performed. In the write operation BL and $\underline{BL}$ are input lines. As we have control on the bit lines, initially make the $\underline{BL}$ connected to ground so that we can have the voltage difference between $\underline{Q}$ and $\underline{BL}$. As there is potential difference between $\underline{Q}$ and $\underline{BL}$, current starts to flow from $\underline{Q}$ to $\underline{BL}$, this results in potential drop at $\underline{Q}$ and this in turn decreases Vg of M1 . At a certain drop , when Vg is less than the threshold voltage of M1 then M1 turns off and M2 is turned on . Now the voltage Vdd flows through M2 and charges Q to 1 , which initially was 0. And $\underline{Q}$ which initially was 1 is now 0. Hence the data is written successfully into the memory .

And when the memory bits are Q=0 and $\underline{Q}$ =1 if the input lines BL and $\underline{BL}$ is given as 0 and 1 ,then there will be no potential difference across input and output nodes and there will no voltage drops and the data stays the same i.e. the data written as Q=0 and $\underline{Q}$ =1 . This is the way how write operation is performed.

Static Noise Margin Estimation :

The stability of a Sram depends upon the Static noise margin this is also known as the 'Butterfly Curve' of the Sram, Greater the SNM correlates to proper read and write operation of the Sram. A basic SNM of a sram is obtained by plotting the voltage transfer characteristics(VTC) of one of the inverter outputs to that of inverse VTC of another inverter.

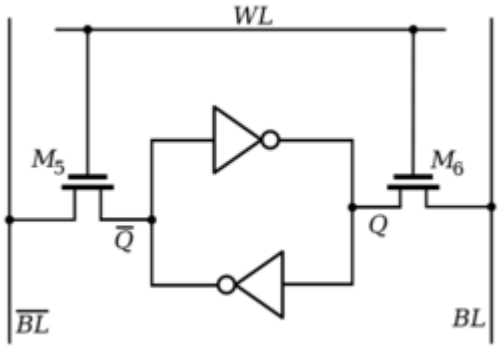


Fig 1: represents standard convention of sram

To get the SNM curve we need to sweep the value of one of the inputs of the inverter (let say input of bottom inverter) from 0 to Vdd and plot its output (Qbar) transition with respect of the varying input , therefore the standard sram convention reduces down to a simple inverter.

As the output of the inverter is feedback to the input of the other upper inverter (input of Q) , the output will be opposite to that of Qbar as both of the inverters are symmetrical .(i.e) as the Qbar falls from Vdd to 0 ,Q rises from 0 to vdd in similar fashion as Qbar .

Now by plotting the inverse VTC of Q with that of the Qbar , we can estimate the noise margin provided by the sram , SNM is obtained as maximum difference between Q and Qbar or also the maximum square which is able to fit inside the two lobe shaped waves of the butterfly curve.

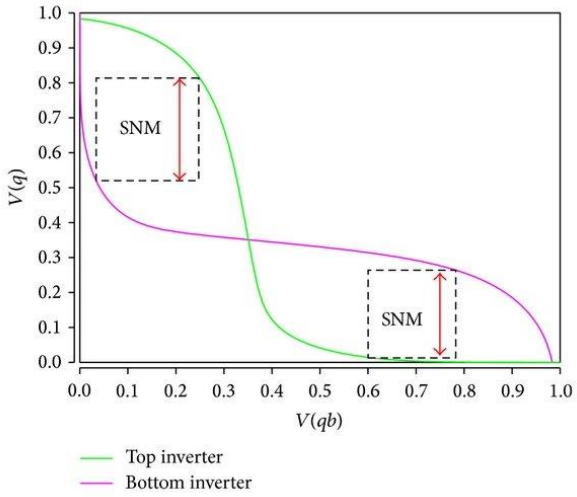


Fig 2: Standard butterfly curve of the Sram

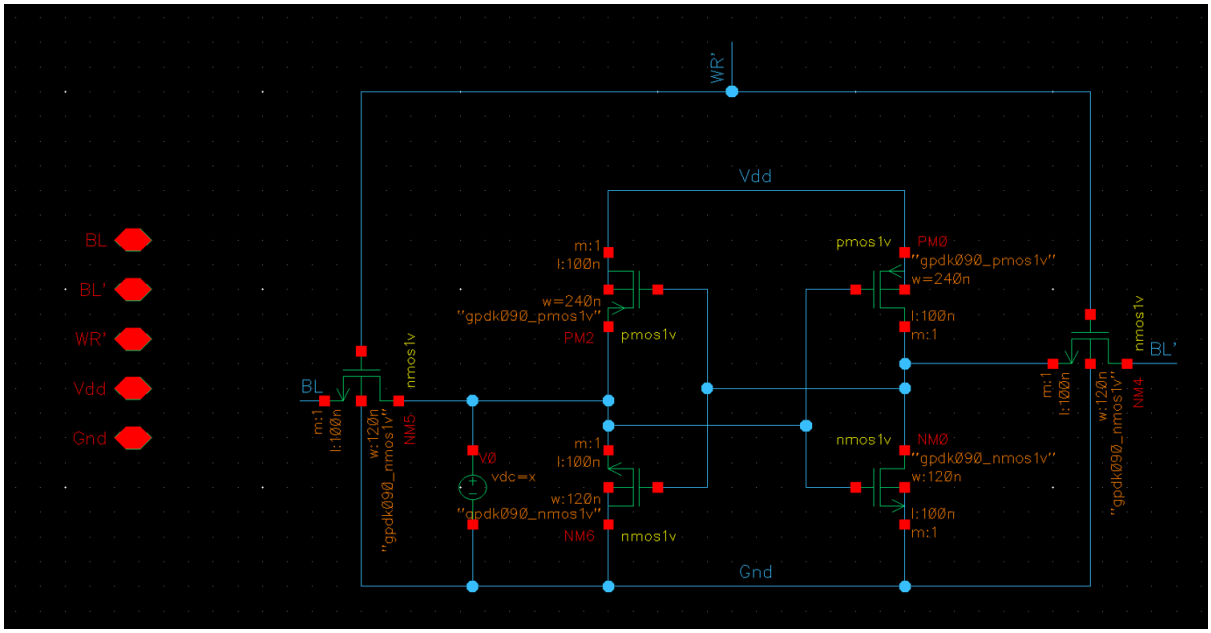
Consider the case when the value of the noise sources with value Vn are introduced at each of the internal nodes in the bit cell. When the value of Vn increases from 0, this causes the VTC-1 of the bottom inverter in Figure 2 to move downward and the VTC for the second inverter to move to the right. Once both move by the SNM value, If the difference of the curve is not high then this results in improper reading of the bit cell .

SNM is becoming an important factor to check the stability during read operation. the SNM takes its lowest value and the cell is in its weakest state .Therefore SRAM cell immunity to static noise is measured in terms of SNM that quantifies the maximum amount of voltage noise that can be tolerated at the cross-inverters output nodes without flipping the cell . so it is needed

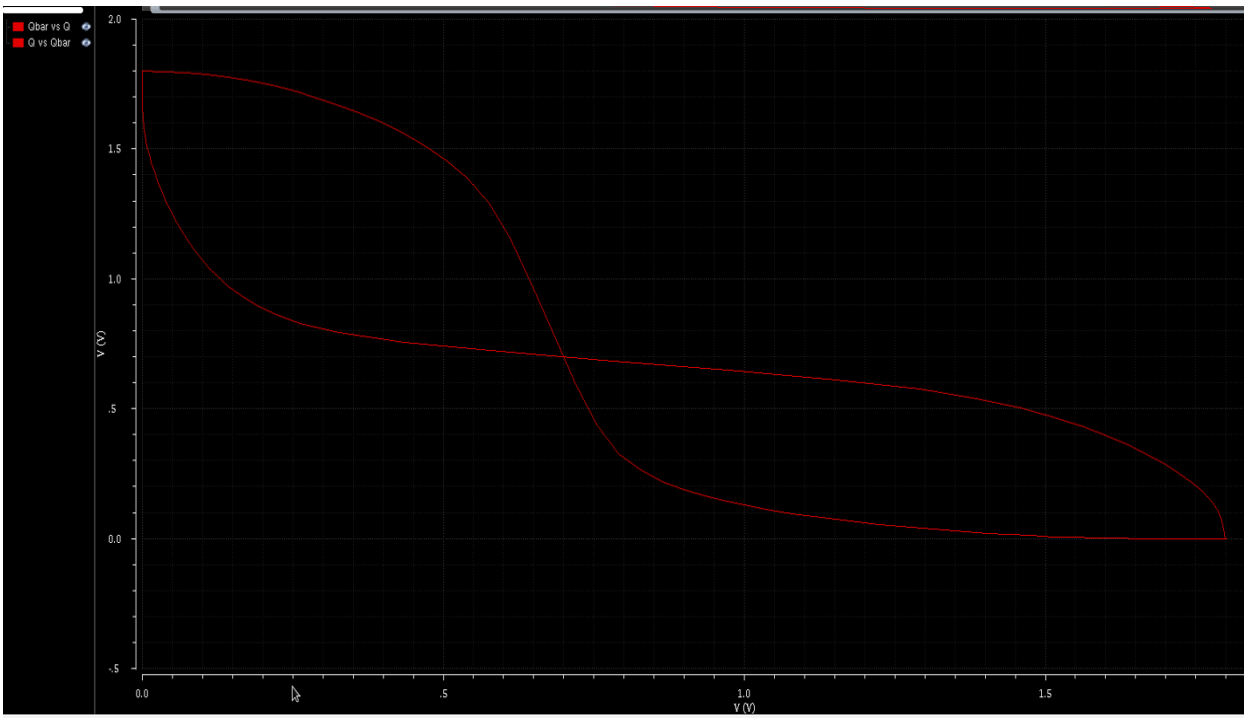
for a sram to have a greater SNM value such that temperature and noise does not affect the values of the Sram

Simulation results

Schematics

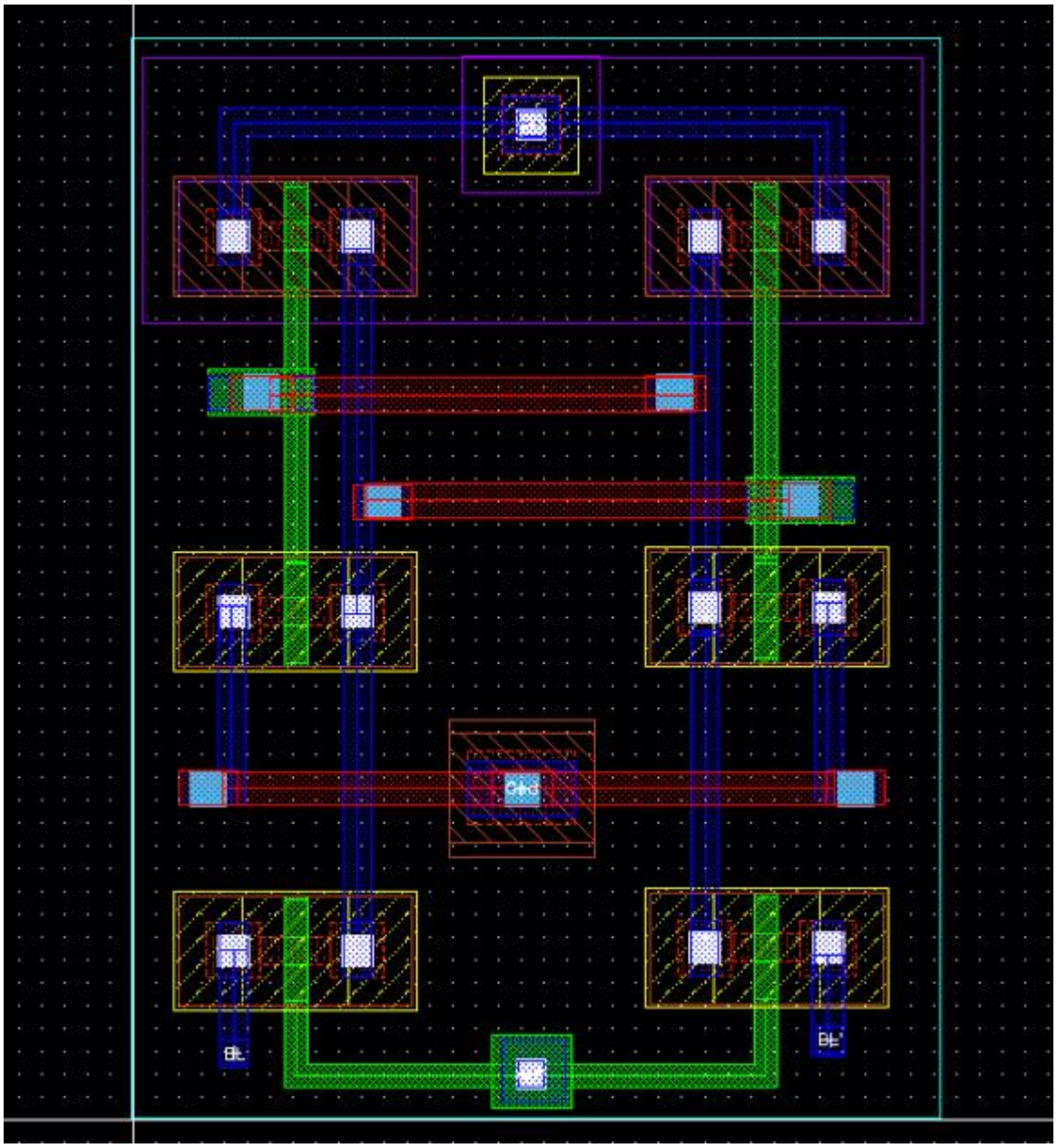


Butterfly curve /SNM curve



SRAM Layout :

SRAM LAYOUT



Conclusion :

The analysis of 6T Static Random-Access Memory is done .

Another major factor that is the Static Noise Margin has been done and the noise responses obtained are shown for both read and write operations.

All the simulations were carried out utilizing Cadence Virtuoso Tools in 90nm CMOS technology.

In the future, we can upgrade the Static Random Access Memory cell and make it dependable and robust to the noise present in the environment.

Future Works :

In the coming future there is a lot of work that can be done in the field of SRAM in terms of designing SRAM cells with reduced number of transistors with ultralow power dissipation.

The feasibility of 2T and single transistor SRAM cells can also be evaluated as it can highly improve the density of SRAM array which is a major problem in present day.

Also, one can work on making fast sense amplifiers which contribute to less delay and speed up the performance of the SRAM system.