VISVESVARAYA TECHNOLOGICAL UNIVERSITY
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Belagavi-590018, Karnataka

Innovation/Entrepreneurship/Societal Internship Report

DESIGN AND VERIFICATION OF APB MEMORY

Submitted in Partial fulfillment for the award of Degree of

Bachelor of Engineering
in
ELECTRONICS AND COMMUNICATION ENGINEERING
21INT68
Submitted by

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1DS21EC029

Internship carried out

at

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2023-24

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(Accredited by National Assessment & Accreditation Council (NAAC) with 'A' grade)

CERTIFICATE

Certified that the internship work (21INT68) entitled, "DESIGN AND VERIFICATION OF APB MEMORY" was carried out by the Aneesh Vinod Savalgi (1DS21EC029), a bonafide student of ECE Department, Dayananda Sagar College of Engineering, Bengaluru, Karnataka, India in partial fulfillment for the award of Bachelor of Engineering in Electronics & Communication Engineering, Visvesvaraya Technological University, Belagavi, Karnataka, during the academic year 2023-24. It is certified that all corrections / suggestions indicated for internship work have been incorporated in the internship report deposited in the department library. The internship report has been approved as it satisfies the academic requirement in respect of internship work prescribed for the said undergraduate degree.

Internship Guide	Evaluator	Head of the Department,
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Dr. B G Prasad,
Principal

CIE examiners (Viva-Voce):

Name of the internship examiners

1: Signature & date: _____

2: Signature & date: _____

EXCEL VLSI
APPLYING SKILL

CERTIFICATE

THIS CERTIFICATE IS AWARDED TO

Mr.ANEESH V.S

FOR SUCEESSFULLY COMPLETING INTERNSHIP PROGRAM ON
"IP DESIGN AND VERIFICATION"
FACILITATED BY VLSI EXPERTS AT EXCEL VLSI TECHNOLOGIES PVT. LTD
*FROM **01-NOV-2023 TO 30-NOV-2023**.*

PROGRAM DIRECTOR	01-JAN-2024 DATE

Declaration

I hereby declare that the internship work (21INT68) entitled, “DESIGN AND VERIFICATION OF APB MEMORY” has been carried out under the guidance of Prof Bindu H.M., Department of Electronics and Communication Engineering, Dayananda Sagar of Engineering, Bengaluru. This report has not been submitted in part or full for the award of any degree of this or any other University.

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Date : / /

Place : Bengaluru -78

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I extend my sincere thanks to the management of DSCE, for providing me with excellent infrastructure and facilities.

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My accomplishments would be incomplete without my beloved parents, for without their support and encouragement I would not have reached up to this level. I owe my achievements to them and also to the *Almighty*.

Aneesh Vinod Savalgi

ABSTRACT

An Intellectual Property (IP) core in Semiconductors is a reusable unit of logic or functionality or a cell or a layout design that is normally developed with the idea of licencing to multiple vendor for using as building blocks in different chip designs.
In today's era of IC designs more and more system functionality are getting integrated into single chips (System on Chip /SOC designs).
In these SOC designs, these pre-designed IP cores/blocks are becoming more and more important. This is because most of the SOC designs have a standard microprocessor and lot of system functionality which are standardized and hence if designed once can be re-used across several designs.
IP cores are generally licensed as either Soft IP cores or Hard IP cores.
Soft IP cores are IP blocks generally offered as synthesizable RTL models. These are developed in one of the Hardware description language like SystemVerilog or VHDL.
Hard IP cores on the other hand are offered as layout designs in a layout format like GDS which is mapped to a process technology and can be directly dropped by a consumer to the final layout of the chip. These cores cannot be customized for different process technologies.
Generally digital logic cores are developed and licensed as Soft IP cores. eg: a DRAM controller IP, Ethernet MAC IP, AMBA bus procotol IPs etc.
Analog and Mixed signal logic designs for serdes, PLLs, ADC or DAC, Phy layer logic for DDR, PCIE etc are generally developed and licensed as Hard IP cores.
With increased trend of IP based designs, there also came the need for Verification Intellectual Properties(VIPs). Similar to design IPs, Verification IPs are pre-defined functional blocks that can be inserted into the testbenches used for verifying a design.
Verification of a large SOC designs typically takes more than 50% of the overall project life cycle and is done at multiple stages – Verifying smaller logical blocks, Verifying a group of logic components at a sub-system level and then verification of the entire SOC chip.

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Chapter 1 : About the Company

Fig 1: Company Logo

About Excel VLSI

Excel VLSI is established to build solutions in VLSI and provide design services to Semiconductor Industry.

Company Mission and Vision

- Excel VLSI **vision** is to be the best company that offers quality engineering solutions and services to the semiconductor industry.
- **Mission** is to encourage the innovative minds and leverage their expertise to design and develop cutting edge products and solutions.
- The **core values** of Excel VLSI are **Learn, Serve, Respect and Celebrate.**

Company Profile

Industry :- Semiconductor Manufacturing

Company Size :- 51-200 employees

Headquarters :- Bengaluru , Karnataka

Type :- Privately Held

Founded :- 2017

Specialities :- VLSI,RTL,Verification,Physical Design,UVM,SOC Verification,GLS,Synthesis,STA,System Verilog,Verilog,PCI Express,AMBA AXI,AHB,APB,Semiconductor Industry,USB,internships, projects and services

Overview of the Internship

This internship covered 7 modules namely :- Need of HDL fundamentals,VLSI Design-FPGA and ASIC Flows,Verilog for Combinational Circuits,Key Construct and Code example for Combinational Logic,Verilog for Sequential Digital Circuits,Verilog for Finite State Machine and Memory Design,Design Verification Process and Projects

Chapter 2: Background Theory

In the beginning, designs involved just a few gates. Thus it was possible to verify these circuits on paper or with breadboards. As designs grew larger and more complex, designers began using gate-level models described in a Hardware Description Language(HDL) to help with verification before fabrication. When designers began working on 100,000 gate designs, these gate-level models were too low level for the initial functional specification and early high level design exploration. Designers again turned to HDLs for help, wherein, abstract behavioural models written in an HDL as per the specification.

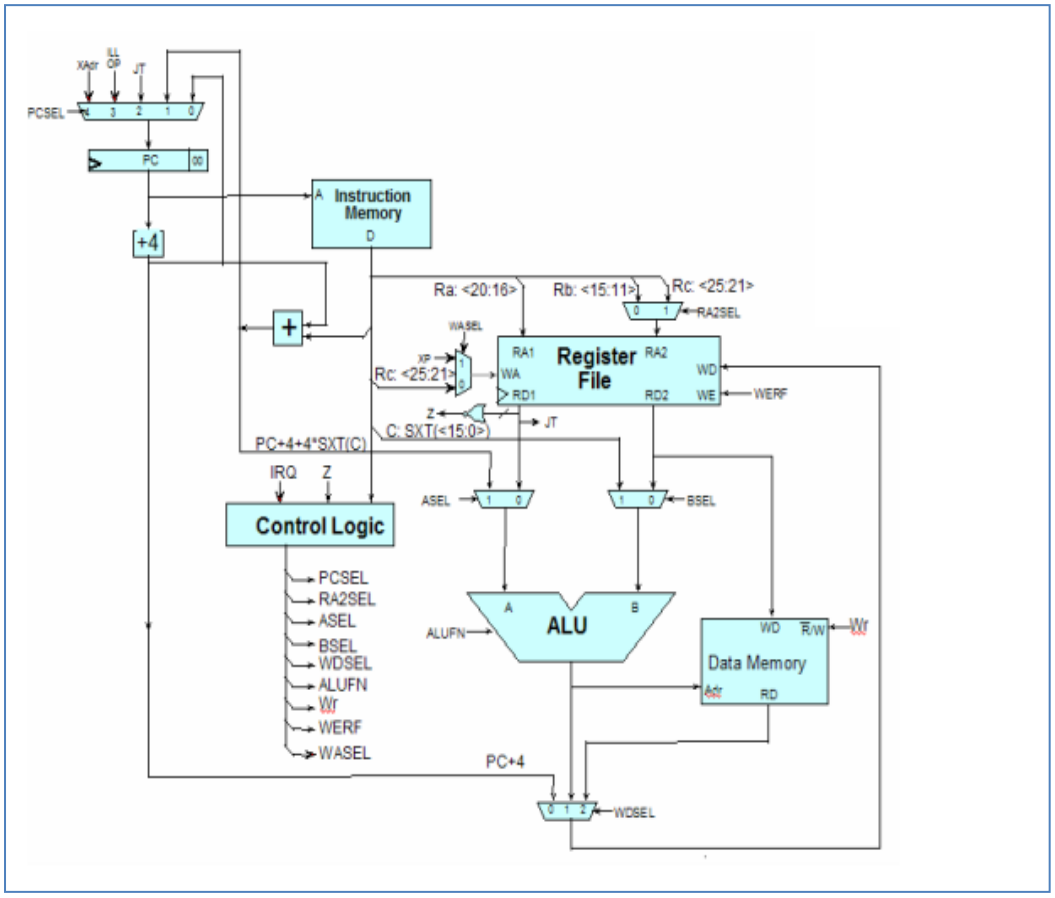


Fig 2: A behavioural model of a simple processor

HDL allows designers to talk about what the hardware does without actually designing the hardware. In other words, HDLs helps to separate **behaviour** from **implementation** of functionality. In other words, HDLs helps to separate **behaviour** from **implementation** of functionality. Virtually every ASIC is designed using either Verilog or VHDL (HDLs)

HDLs are used for :

- Describing the concurrent behavior of hardware,
- Structural Modeling for cell libraries.
- Behavior modeling for procedural and sequential description of hardware
- Developing stimulus generator and checkers and, at large for verification.
- Representing synthesized netlists (generated from RTL using synthesis tools)

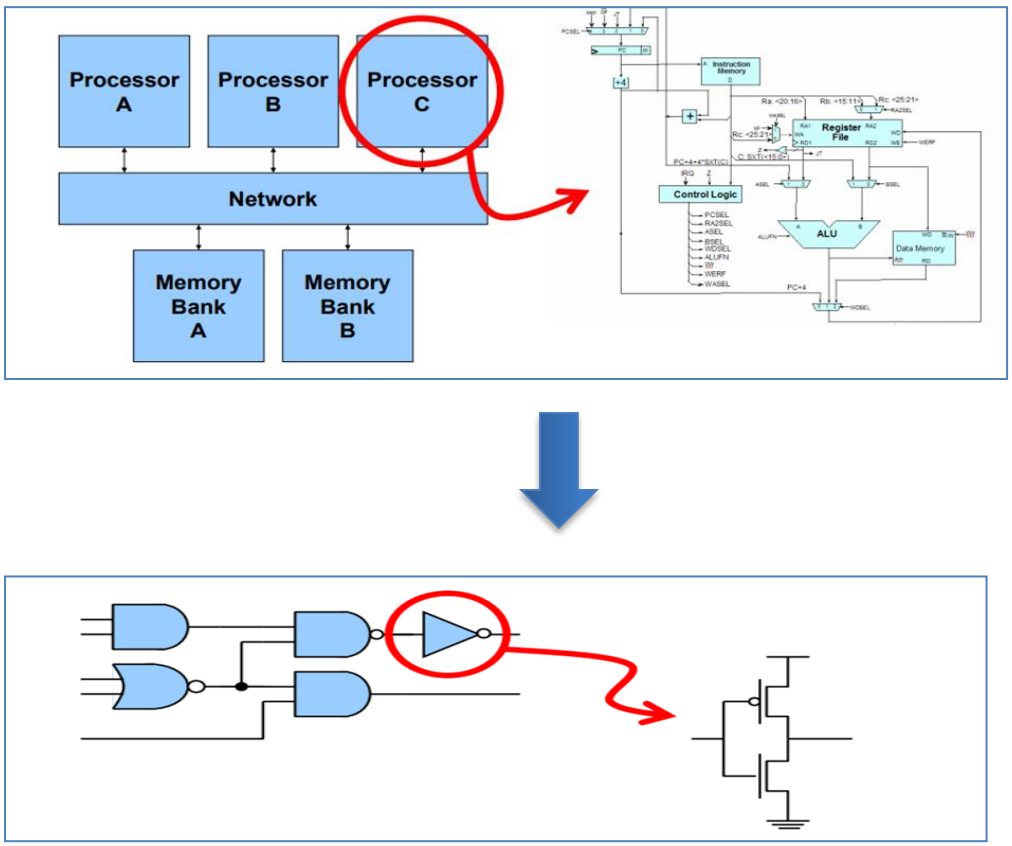


Fig 3: Representation of modeling of gates

Chapter 3: Introduction

Motivation

To understand the VLSI design flow and specifically get an insight into the RTL Coding and Functional Verification aspects of it.

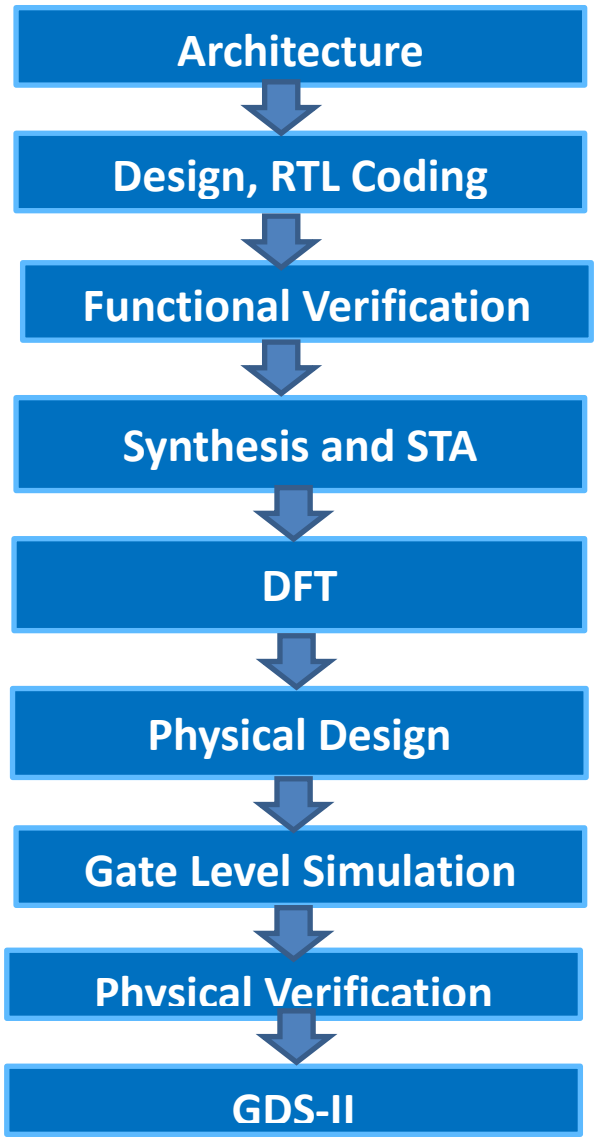
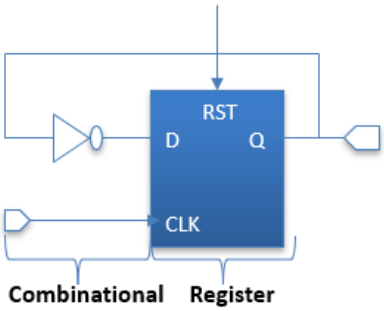


Fig 4 : VLSI Design Flow

RTL Coding

Design is about modeling a synchronous digital circuit is using Register Transfer Logic (RTL). Represents Flow of digital signals between hardware registers with certain logical operation. Consists of two kind of elements: registers (sequential) and gates (combinational).




```
// Verilog code
module VERILOG_HDL (CLK, RST, Q);
 input CLK, RST;
 output reg Q;
wire D;
assign D = ~Q;
always @(posedge CLK or RST)
  begin
   if (RST == 1)
    Q <= 0;
   else
    Q <= D;
  end
endmodule
```

Fig 5: Netlist to RTL Code

Verification

Goal is to check the Design for the Correct Functionality.

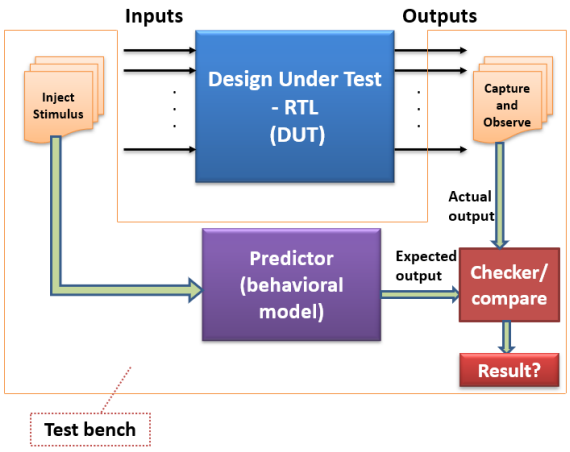


Fig 6: Model of a Testbench

Problem Statement

To design an APB memory with a capacity of 1kB

Objectives

- To understand the need for APB protocol
- To implement a simple IP for visualising APB
- To verify the design and get a clear picture of the working of the APB protocol with its state diagram by applying suitable stimuli through testbench

Expected Outcomes

Successful implementation of APB protocol after understanding the pre-requisites like Finite State Machine and analysis of the read and write operations from the output waveforms.

Chapter 4: Design and Development Details

Block Diagram

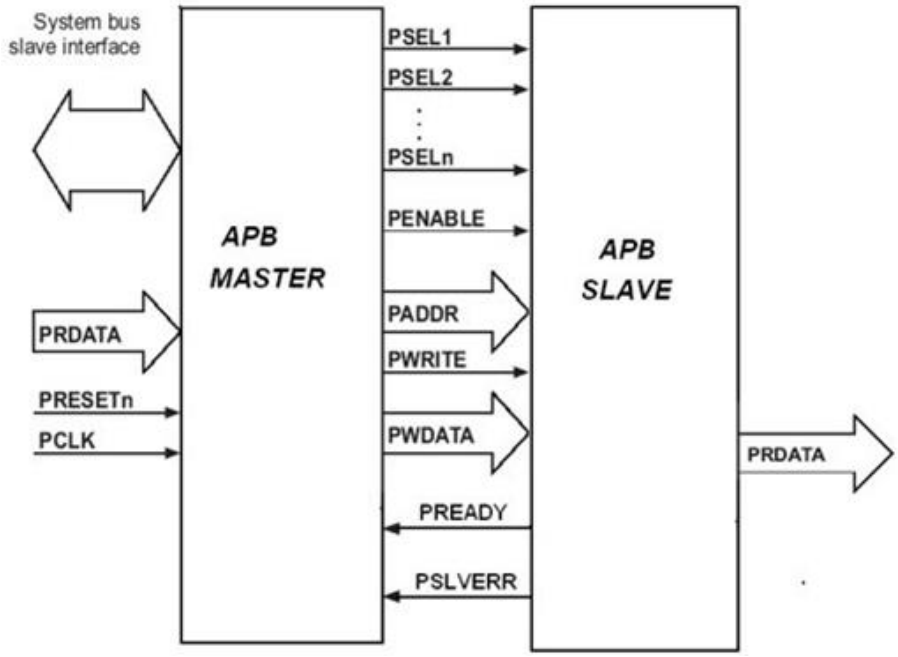


Fig 7: APB Block Diagram

Methodology

Signal Specification of APB

PCLK Clock: The rising edge of PCLK times all transfers on the APB.

PRESET: System bus equivalent Reset. The APB reset signal is active LOW.

PADDR: 32 bit address bus PSEL The slave device is selected and that a data transfer is required.

PENABLE Enable: This signal indicates the second and subsequent cycles of an APB transfer.

PWRITE: Access when HIGH.

PWDATA: 32 bits Write data PWRITE is HIGH.

PREADY: Ready To extend an APB transfer.

PRDATA: 32 bits Read data and PWRITE is LOW.

PSLAVERR Slave error: This signal indicates a transfer failure.

Write Operation

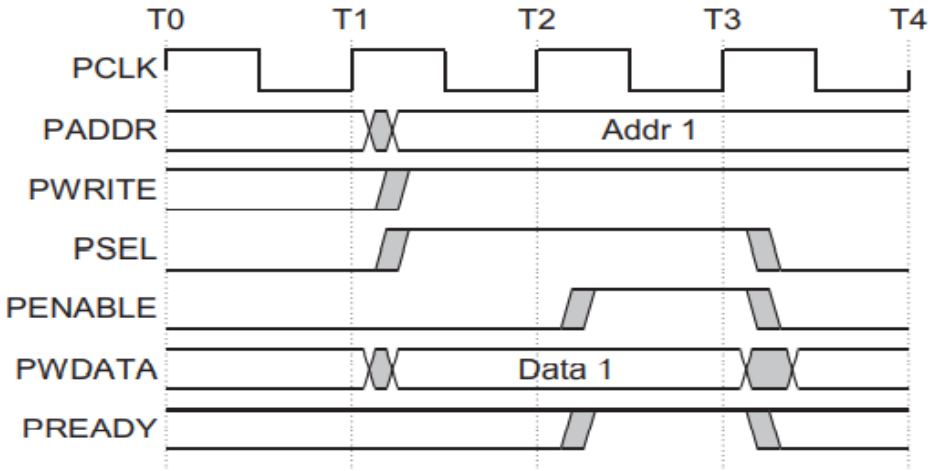


Fig 8: APB Write Operation

- At T1, a write transfer starts with PADDR, PWDATA, PWRITE, and PSEL, being registered at the rising edge of PCLK. It is called the SETUP cycle.

- At the next rising edge of the clock T2 it is called ACCESS cycle, PENABLE, and PREADY, are registered. When asserted, PENABLE indicates starting of Access phase of the transfer. When asserted, PREADY indicates that the slave can complete the transfer at the next rising edge of PCLK.

- The PADDR, PWDATA, and control signals all remain valid until the transfer completes at T3, the end of the Access phase.

- The PENABLE, is disabled at the end of the transfer. The select signal PSEL is also disabled unless the transfer is to be followed immediately by another transfer to the same peripheral.

Read Operation

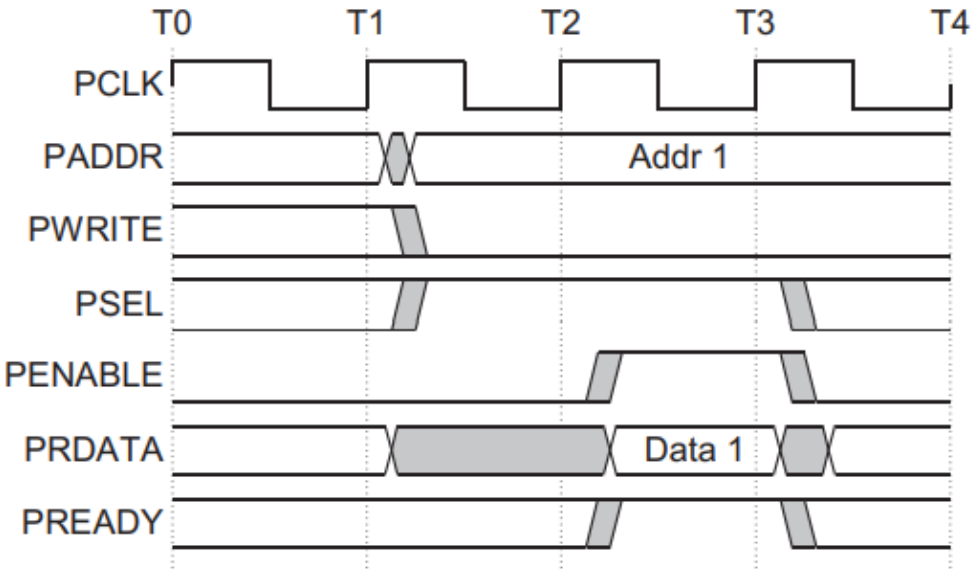


Fig 9: APB Read Operation

- During read operation the PENABLE, PSEL, PADDR PWRITE, signals are asserted at the clock edge T1 (**SETUP cycle**).

- At the clock edge T2, (**ACCESS cycle**), the PENABLE, PREADY are asserted and PRDATA is also read during this phase. The slave must provide the data before the end of the read transfer.

Tool

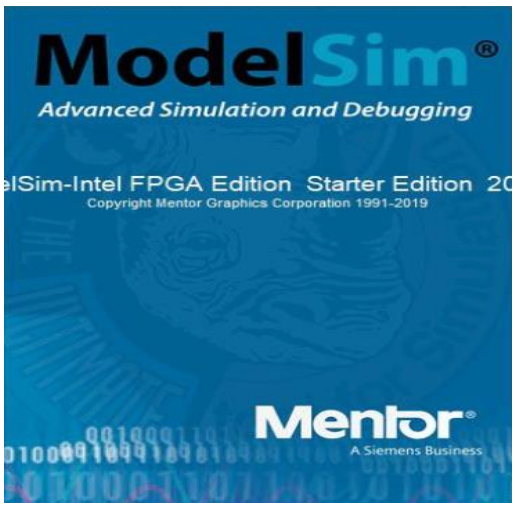


Fig 10:Modelsim startup view

ModelSim is a multi-language environment by Siemens (previously developed by Mentor Graphics) for simulation of hardware description languages such as VHDL, Verilog and SystemC, and includes a built-in C debugger. ModelSim can be used independently, or in conjunction with Intel Quartus Prime, PSIM,Xilinx ISE or Xilinx Vivado. Simulation is performed using the graphical user interface (GUI), or automatically using scripts.

Challenges

Implementation of this APB(Advanced Peripheral Bus) protocol required a basic understanding of the basic AMBA architecture to appreciate its function.

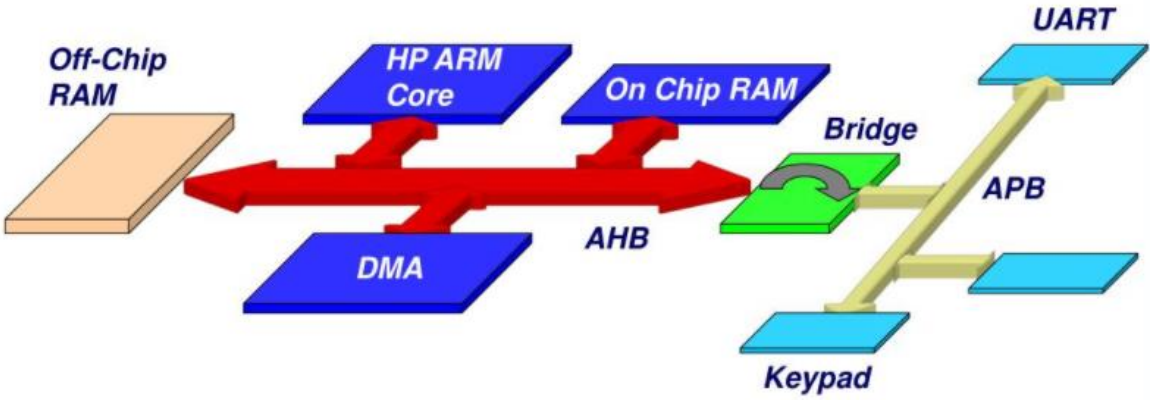


Fig 11: AMBA Architecture

Outcomes

The APB acts as a means to interface to any peripherals which are low bandwidth and do not require the high performance of a pipelined bus interface. AMBA APB provides the basic peripheral macro cell communications infrastructure as a secondary bus from the higher bandwidth pipelined main system bus. It consist of interfaces which are memory-mapped registers.

Chapter 5: Implementation Details

State Diagram

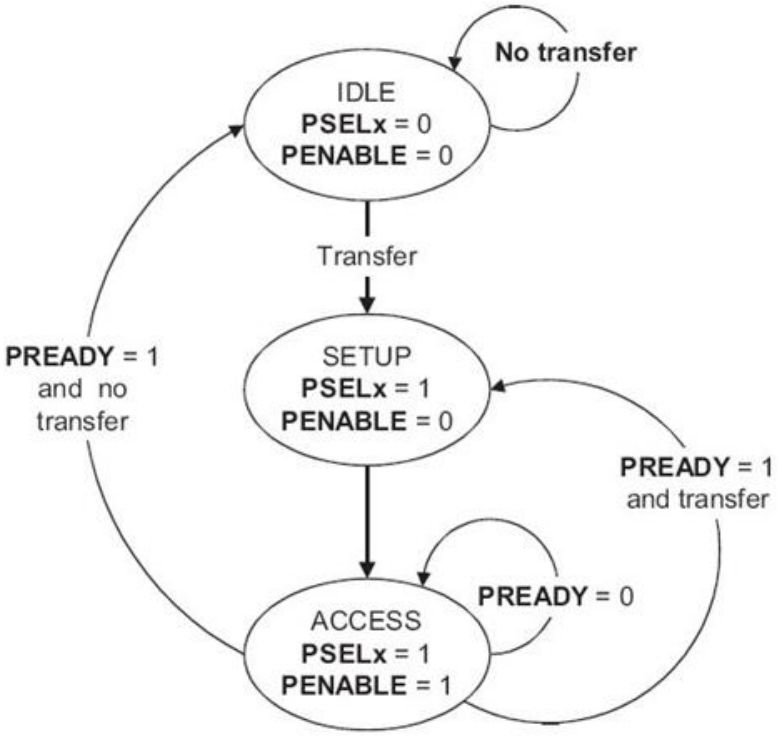


Fig 12: APB State Diagram

Design and operating states of APB

IDLE : This is the default state of the APB.

SETUP: When a transfer is required the bus moves into the SETUP state, where the appropriate select signal, PSELx, is asserted. The bus only remains in the SETUP state for one clock cycle and always moves to the ACCESS state on the next rising edge of the clock.

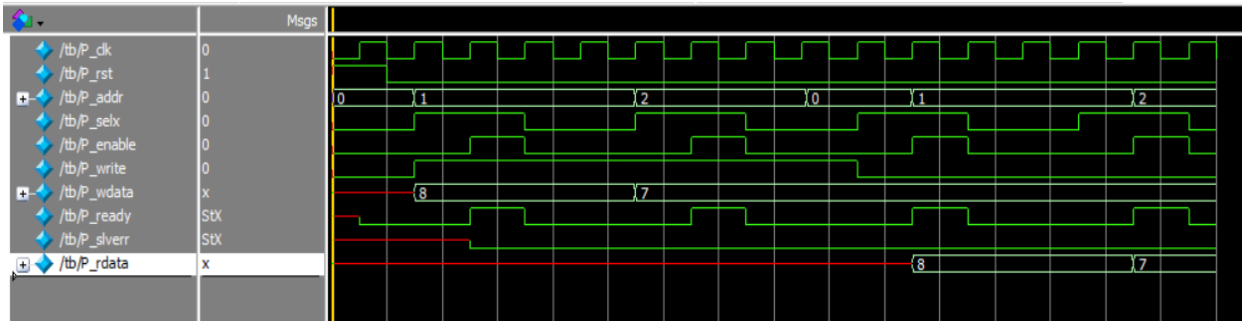
ACCESS: The enable signal, PENABLE, is asserted in the ACCESS state. The address, write, select, and write data signals must remain stable during the transition from the

SETUP to ACCESS state. Exit from the ACCESS state is controlled by the PREADY signal from the slave:

- If PREADY is held LOW by the slave then the peripheral bus remains in the ACCESS state.

- If PREADY is driven HIGH by the slave then the ACCESS state is exited and the bus returns to the IDLE state if no more transfers are required. Alternatively, the bus moves directly to the SETUP state if another transfer follows.

Chapter 6: Results and Discussions



Here the width of the memory is 32 and the depth is also 32, therefore the total capacity is 1kB. The memory is operational only when the reset P_rst is low. First the memory is in idle state with all the control signals low . When P_selx is high the memory is setup state, for write operation P_write is made high and the data to be written is loaded into P_wdata. The data is then written into the memory when the P_enable is high and the memory is in access state.For the read operation the same cycle is followed with P_write being low and the data is read from the address P_addr and stored in P_rdata. Here first write operation performed on the addresses 1 and 2 in P_addr and was verified to be written without any error by performing the read operation on the same addresses. Therefore the working of the APB memory is successfully verified.

Chapter 7: Conclusions and Future Scope

The simulation results show that the data read from a particular memory location is same as the data written to the given memory location. The results obtained after the simulation were compared with the expected results and were found to be satisfactory.

This report shows the implementation of APB protocol,along similar lines even the AHB protocol can be implemented and also a bridge can be designed to interface the high speed AHB and the low power APB.

References

[1] *ARM, "AMBA Specification Overview"*

[2] *http://www.differencebetween.net/technology/difference-between-ahb-and-apb*

[3] *Samir Palnitkar, "Verilog HDL: A guide to Digital Design and Synthesis (2nd Edition), Pearson, 2008*