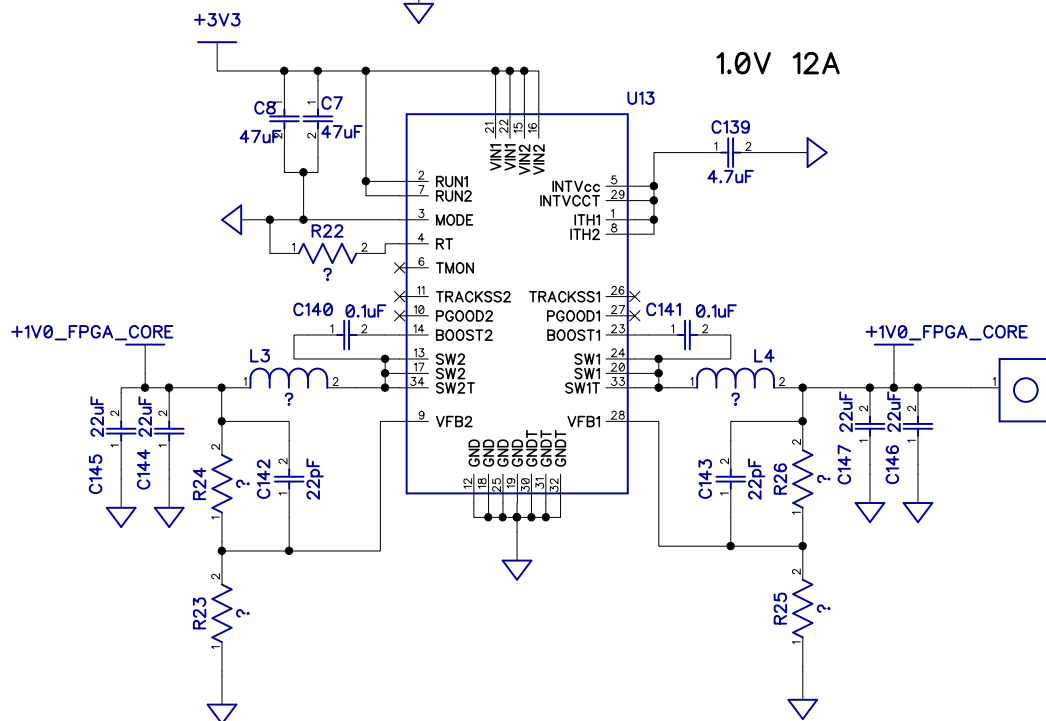
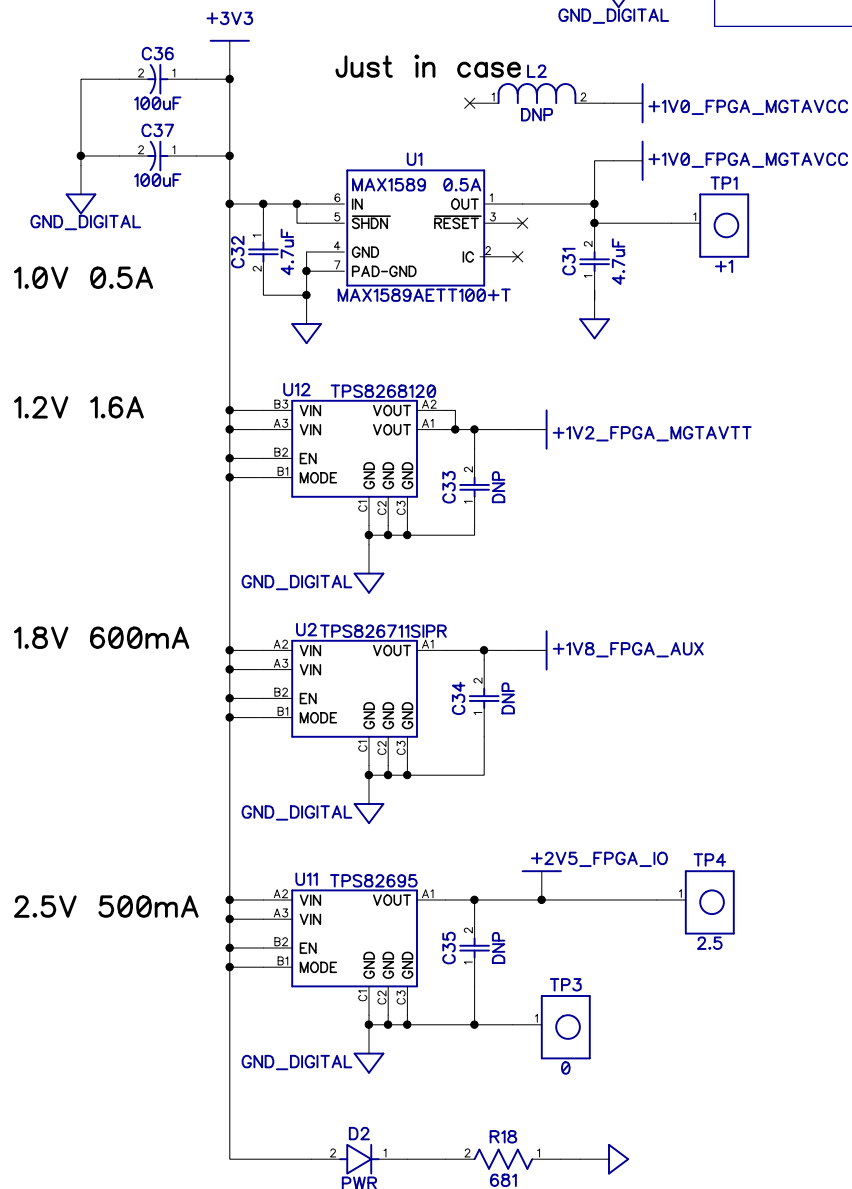
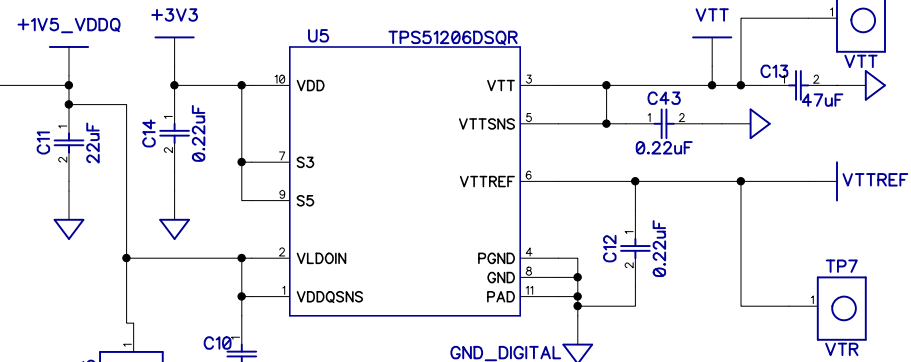
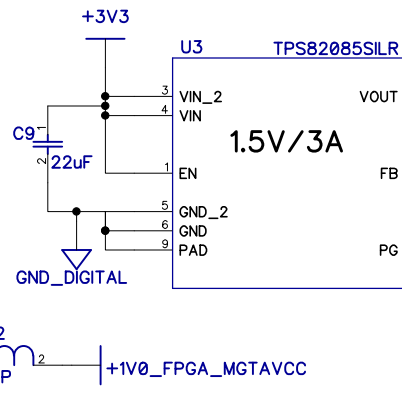


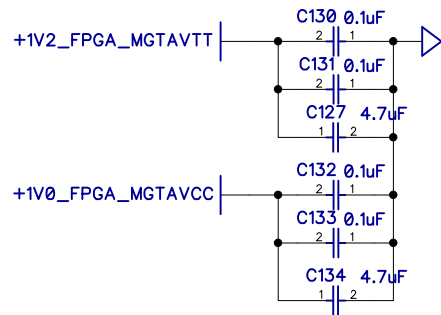
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Title	
Block Diagram	
Size	Number
Rev	
Date	Drawn by
Filename	Sheet

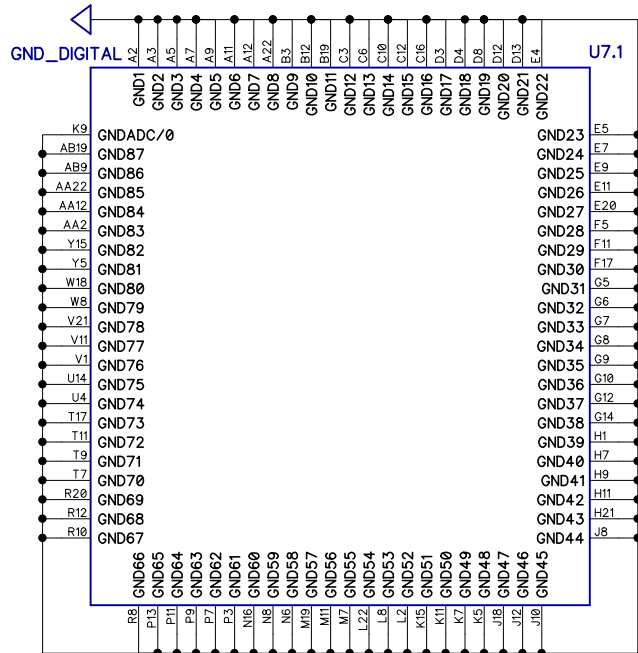
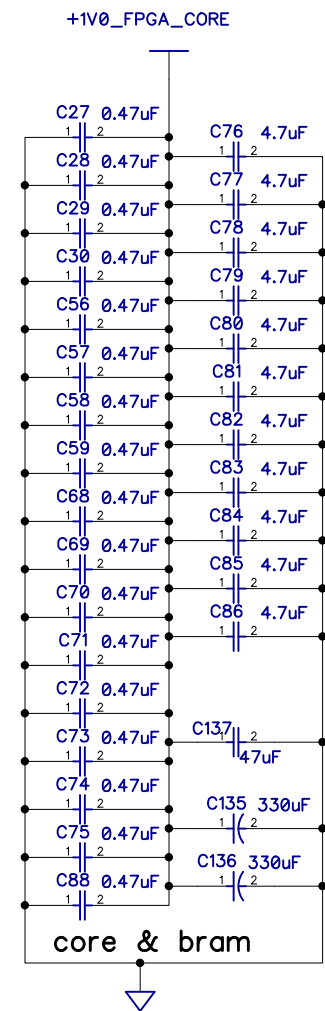
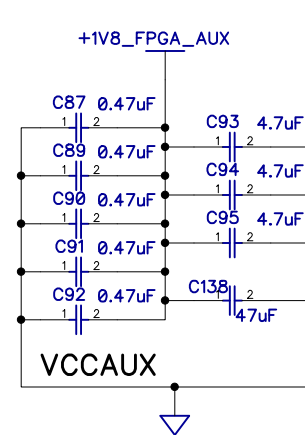
Voltage	Current	Purpose
+1.5	3A	DDR3 VDD
+0.75	1.5A	DDR VTT
+0.75	100mA	DDR VTT ref
+1.0	12A	FPGA core
+1.0	0.5A	MGT supply
+1.2	1A	MGT supply
+1.8	0.6A	FPGA Aux
+2.5	2.5V	LVDS I/O



Title		
Power		
Size	Number	Rev
Date		Drawn by
Filename		Sheet

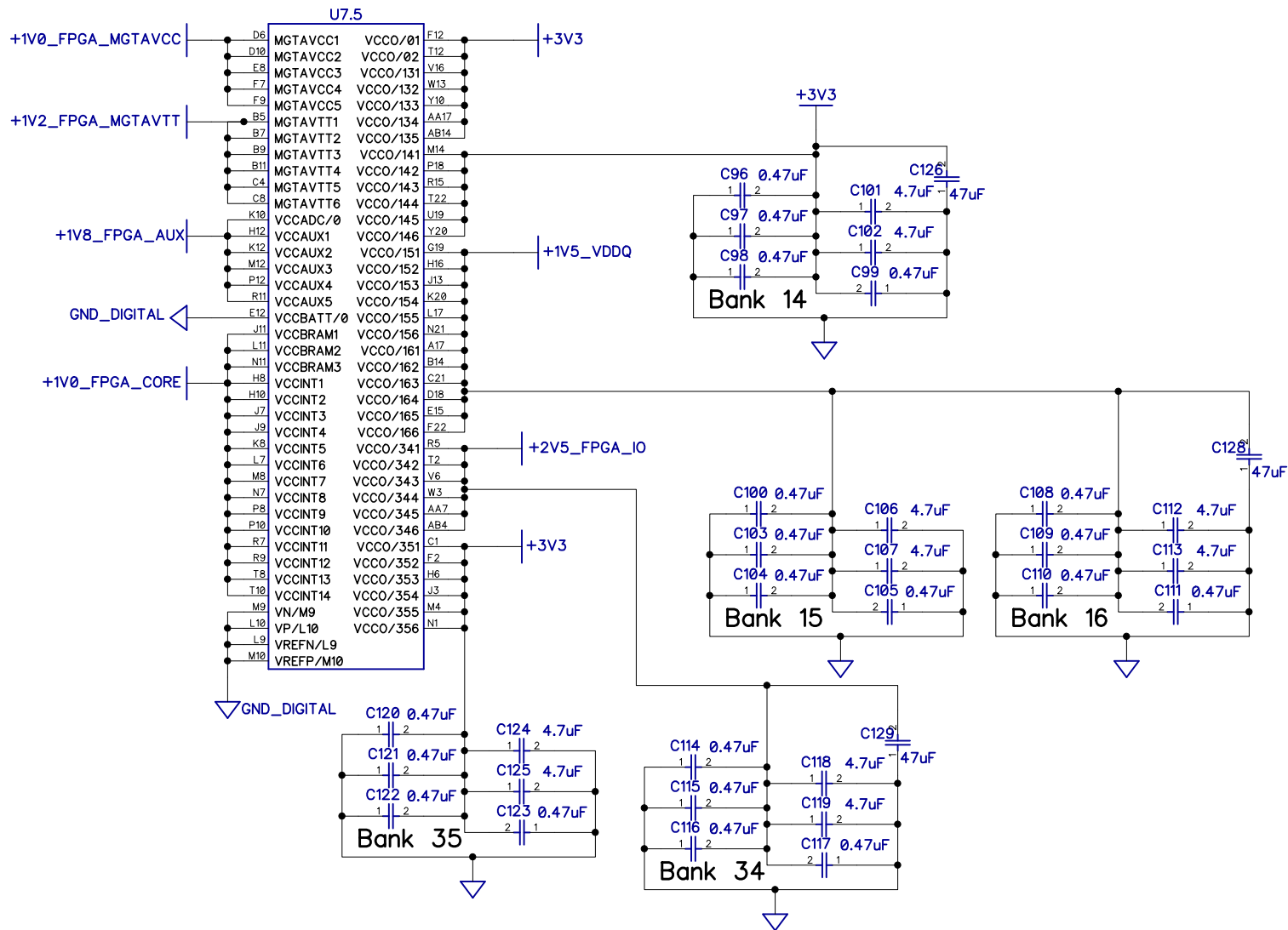


MGT Decouplers



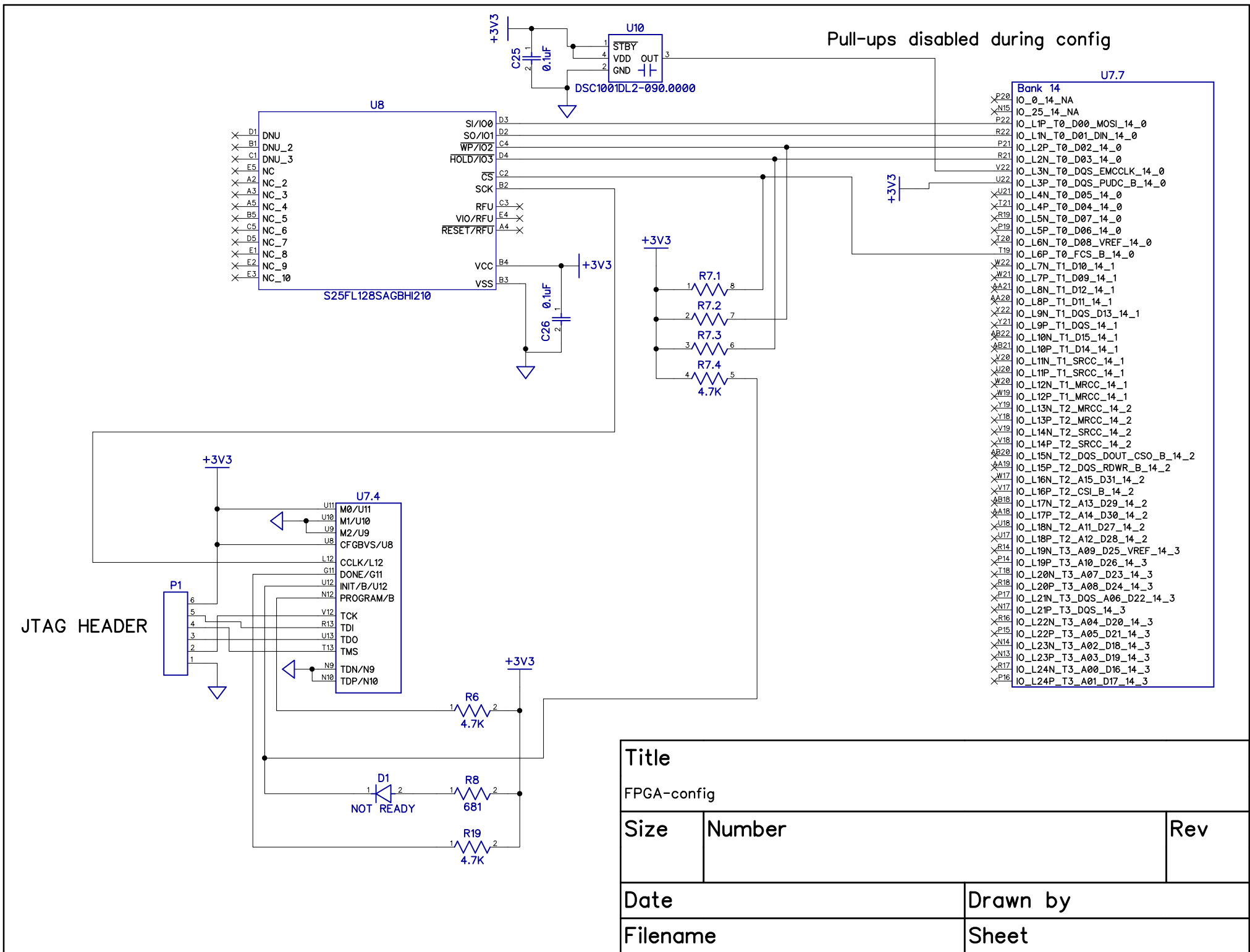
Bars	Value
0	
1 (A)	0.1uF
2 (B)	4.7uF
3 (C)	0.47uF

Title		
FPGA power and decoupling		
Size	Number	Rev
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Filename		Sheet



Bank	Voltage	Purpose
0	3.3	SPI, JTAG
13	3.3	Unused (NA on A50)
14	3.3	Config & 3.3V IO
15	1.5	DDR Addr/CTL
16	1.5	DDR data
34	2.5	LVDS I/O
35	3.3	3.3V I/O

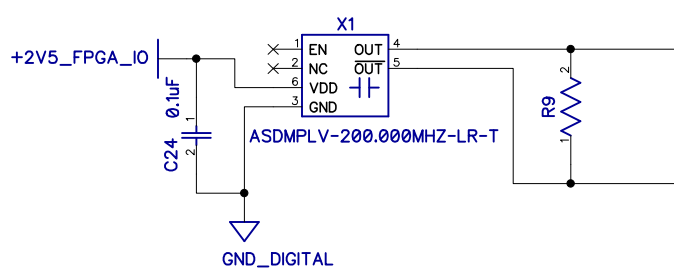
Title		
FPGA I/O decoupling		
Size	Number	Rev
Date		Drawn by
Filename		Sheet



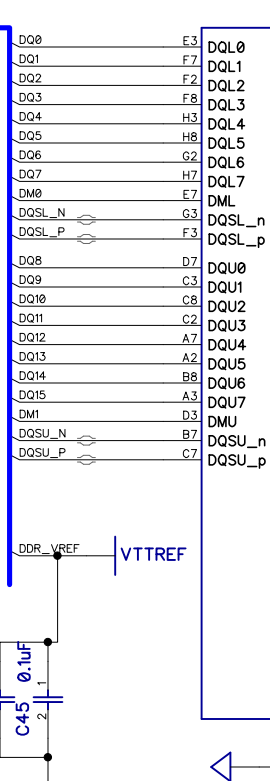
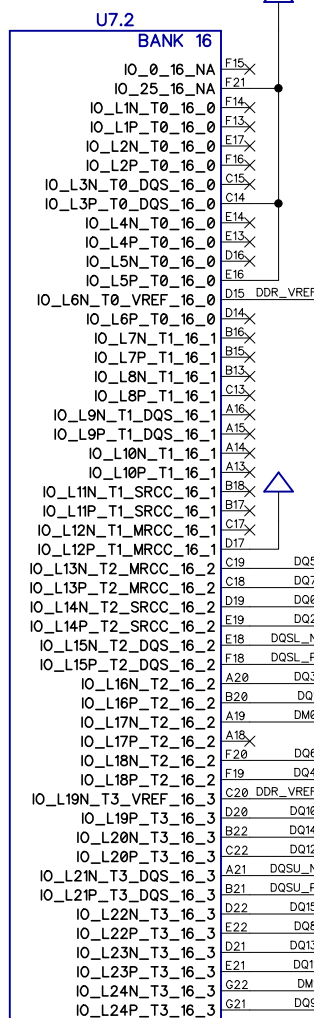
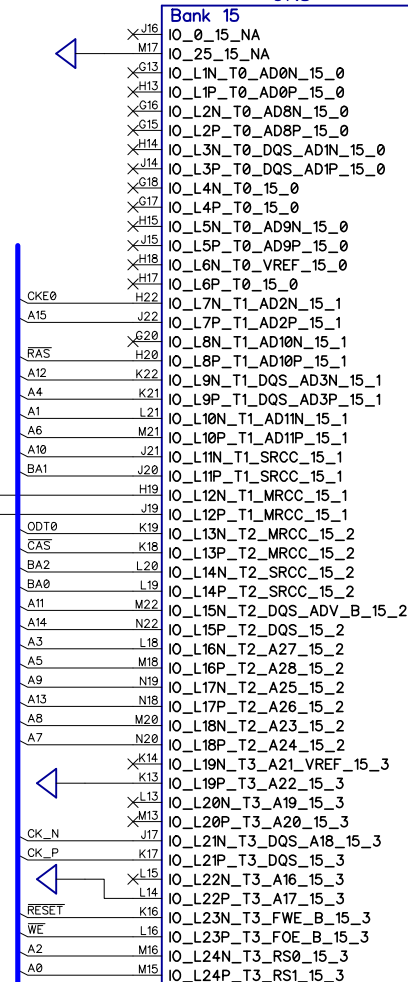
DDR Termination



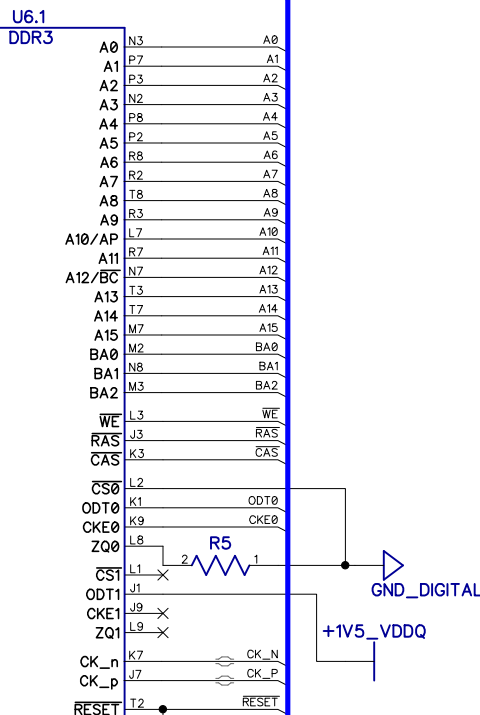
200MHz DDR clock



U7.8



FPGA VTTRef decouplers



DDR

Size

Number

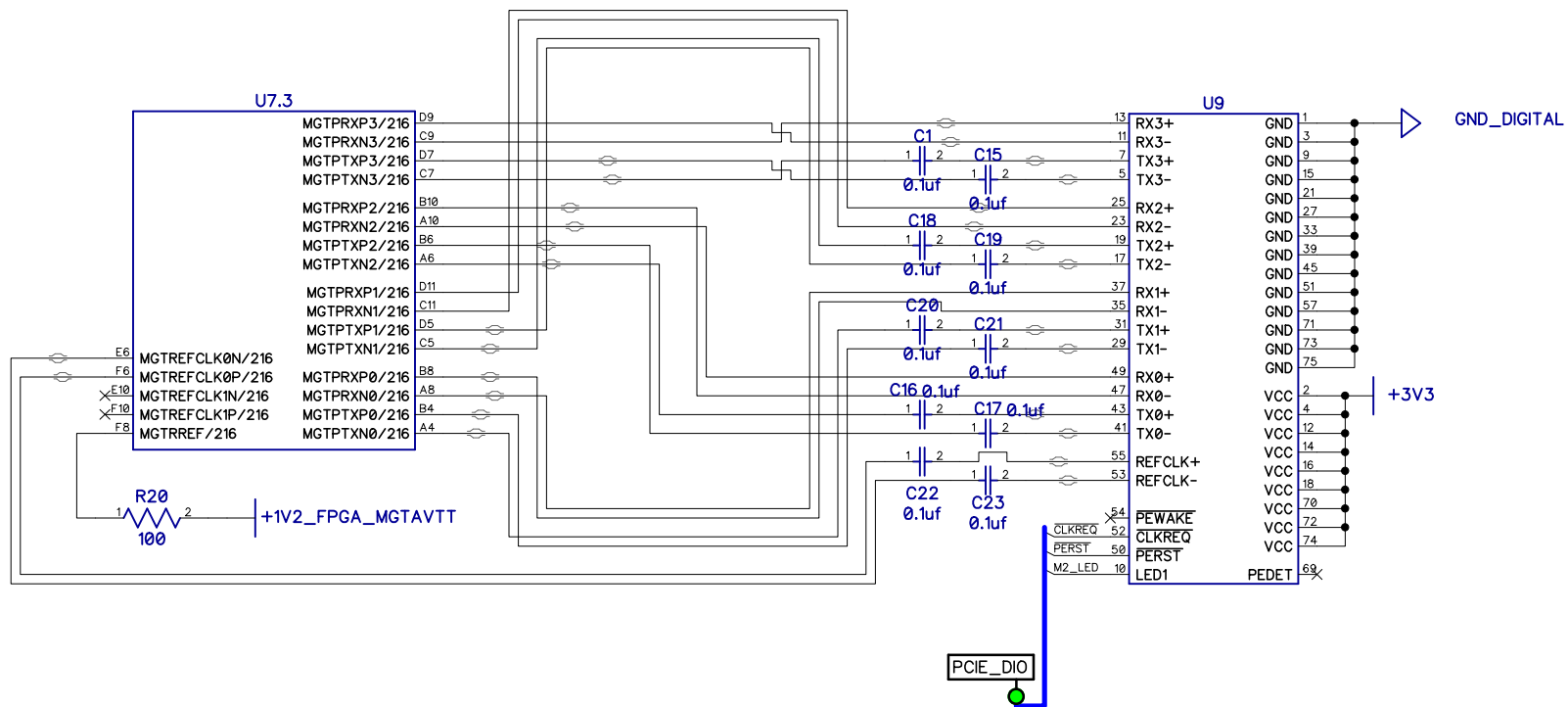
Rev

Date

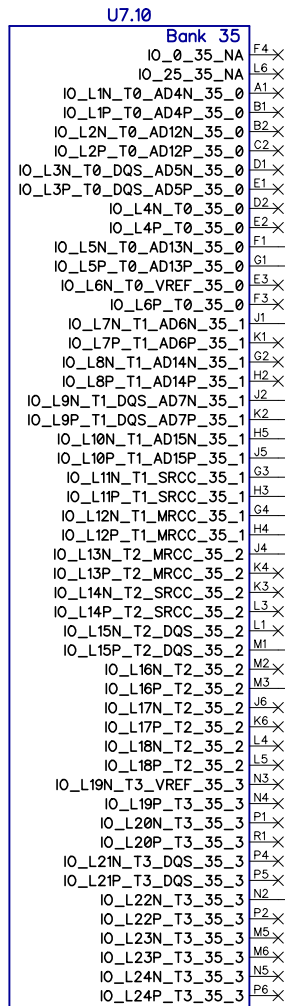
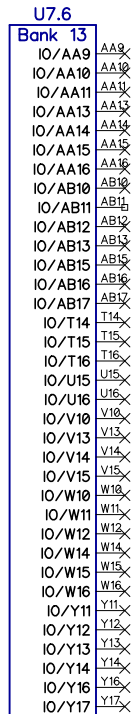
Drawn by

Filename

Sheet



Title		
FPGA-MGT		
Size	Number	Rev
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Filename		Sheet



PCIE_DIO

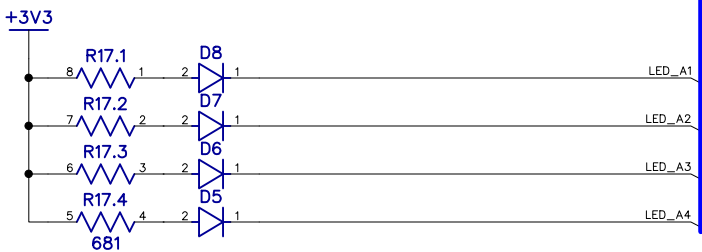
CLKREQ

PERST

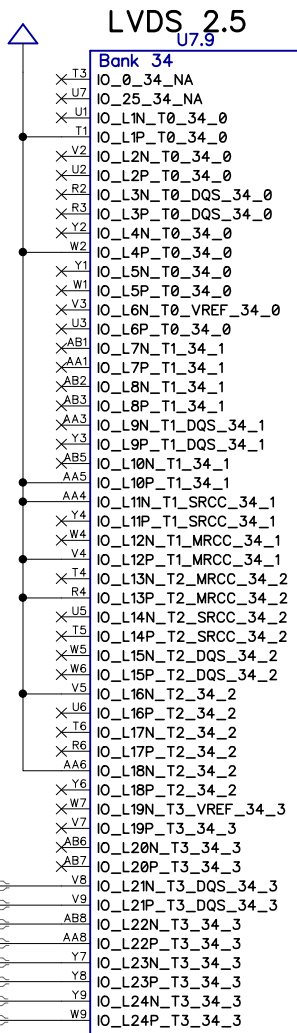
M2_LED

2.5V LVDS pairs
+ 3.3V Multi purpose

Multi-purpose duplicated

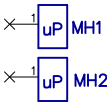


User LEDs

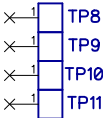


Title		
FPGA-IO		
Size	Number	Rev
Date		Drawn by
Filename		Sheet

Heatsink mounting holes/standoffs



Stencil Alignment Pads



Title		
Mechanical		
Size	Number	Rev
Date		Drawn by
Filename		Sheet

REV	Date	DESC
R2	5/21/2018	Added ODT signal Added LED signal to M.2 edge Swapped PCIe TX/RX
R1		Replaced core supply w/12A supply. Fixed pinout of U1. Fixed FPGA T6/R1 pins.

Title		
Revision history		
Size	Number	Rev
		R2
2018-05-11		DPR
uEVB		Sheet