

Realization of 2-Way RF Resistive Power Dividers Using NMOS

Introduction

Power dividers are passive networks that equally divide an input signal over a number of lines. A two way power divider is a three port lossy network which is matched at all three ports and as the name suggests it divides the input signals over two output ports. Half of input power is dissipated across resistors and the power transfer from the input to each of the output port is around -6db.

Abstract

This project analyses the implementation of a two way resistive power divider by using NMOS technology instead of resistors fabricated on chip. Traditional resistors face problems like nonlinearity and poor tolerance and hence the motivation for this project.

Circuit Implementation

A two way resistive power divider can be implemented using a star network or a delta network. Each port is terminated in with load impedance equal to its characteristic impedance (50ohm). This project implements the delta configuration as per the following circuit diagram.

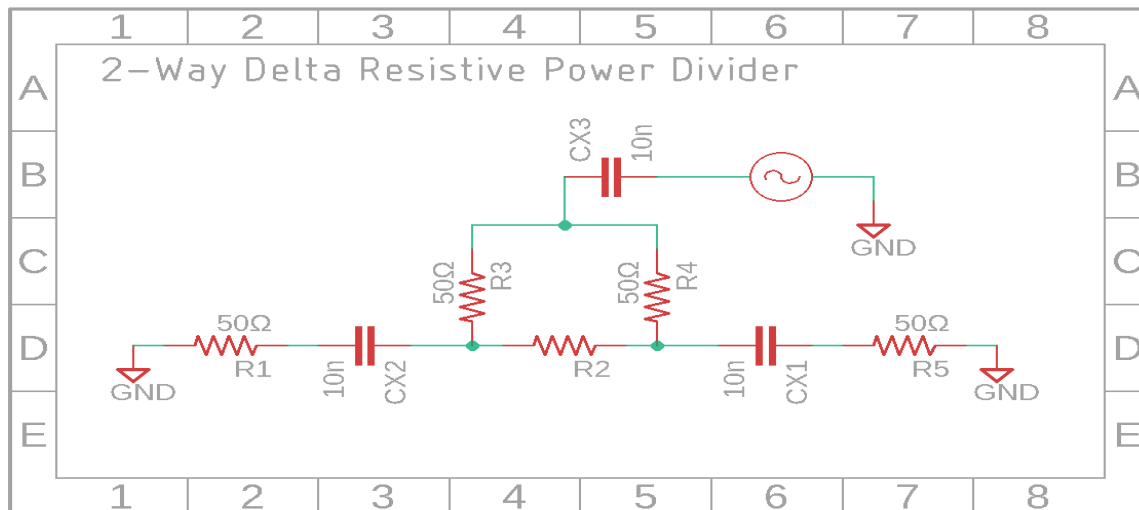


Fig1: 2-Way Resistive Power Divider

In the above circuit we replace the resistors with NMOS biased using single ended sources as shown below.

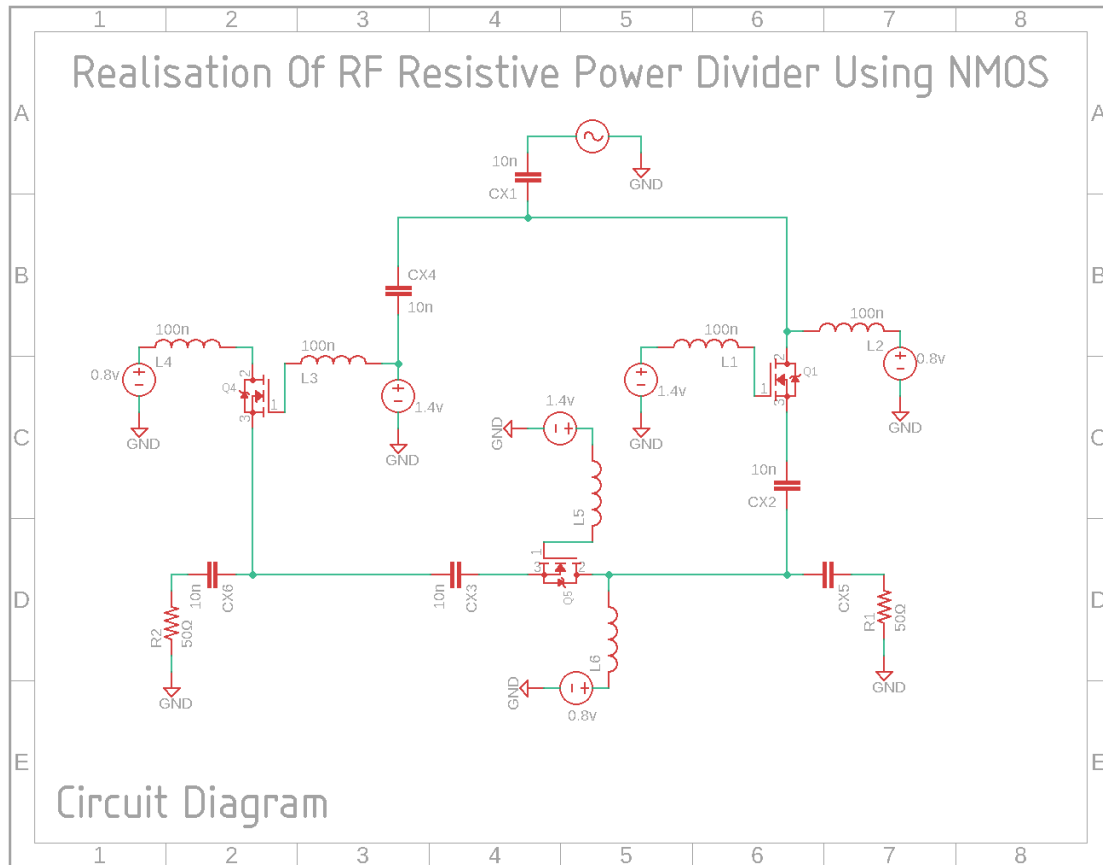


Fig2:- Circuit diagram of NMOS implementation of Power Divider

- Prior to the AC analysis of the circuit, the bias condition for each MOSFET was set to $V_{gs}=1.4\text{v}$ and $V_{ds}=0.8\text{v}$. The width of the MOSFET was set to $80\mu\text{m}$ and 12 devices were placed in parallel. The above circuit yielded a drain source resistance of about 50Ω .
- For the AC analysis, the gate was biased at 1.4 through a series inductor of 100nH . The drain terminal was biased at 0.8v through a series inductor of 100nH .

- Spice simulation requires each node of the circuit to have at least one dc path to ground. To ensure the same, a high value ($1.0e12$) shunt resistor (not shown here) to ground was connected at each node.
- DC blocking capacitors and Series inductors of relatively small values like 10nF and 100nH respectively were used.
- AC analysis was performed over the range of frequencies from 100 MHz to 100 GHz to verify the analysis.

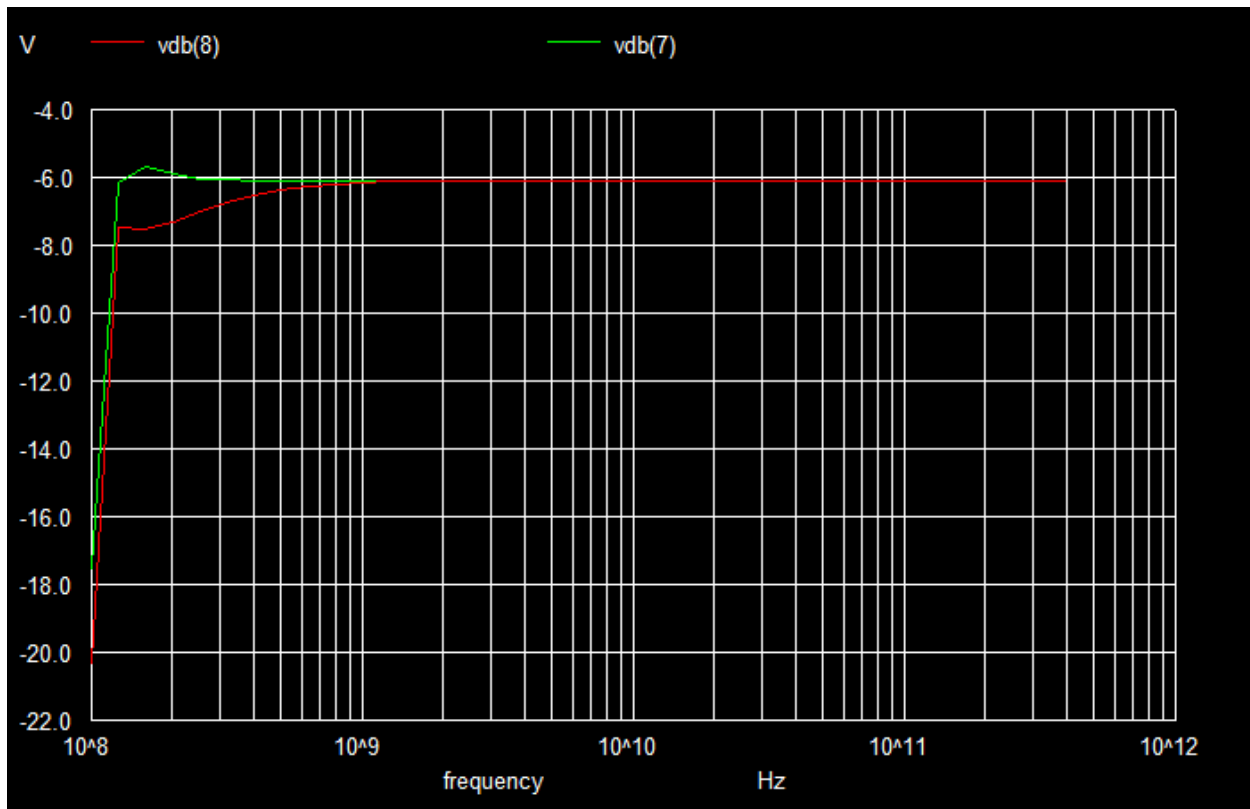


Fig3:- AC analysis plot of output voltages expressed in db.

Challenges

1. Occurrences of Singular matrix errors, non-convergence of iterations while obtaining node voltages and branch current, failed source stepping were among the notable errors encountered during the simulation.
2. Absence of a dc path at each node of the circuit, connections of voltage sources/inductors in a loop were the major reasons for the above errors.
3. Use of the command *.option rshunt = 1.0e12* ensured each node is pulled down to ground through a high value resistor providing a dc path. Further a series inductor was used with each voltage source.

Submitted by -

Angad Pattanaik

Under the Guidance of

Dr. Debapratim Ghosh

(IIT Bhubaneswar)