Realization of 2-Way RF Resistive Power Dividers Using NMOS

Introduction

Power dividers are passive networks that equally divide an input signal over a number of lines. A two way power divider is a three port lossy network which is matched at all three ports and as the name suggests it divides the input signals over two output ports. Half of input power is dissipated across resistors and the power transfer from the input to each of the output port is around -6db.

Abstract

This project analyses the implementation of a two way resistive power divider by using **180 nm NMOS technology** instead of resistors fabricated on chip. Traditional resistors face problems like nonlinearity and poor tolerance and hence the motivation for this project.

Circuit Implementation

- A two way resistive power divider can be implemented using a star network or a delta network. Each port is terminated in with load impedance equal to its characteristic impedance (50ohm). This project implements the **delta configuration** as per the following circuit diagram.

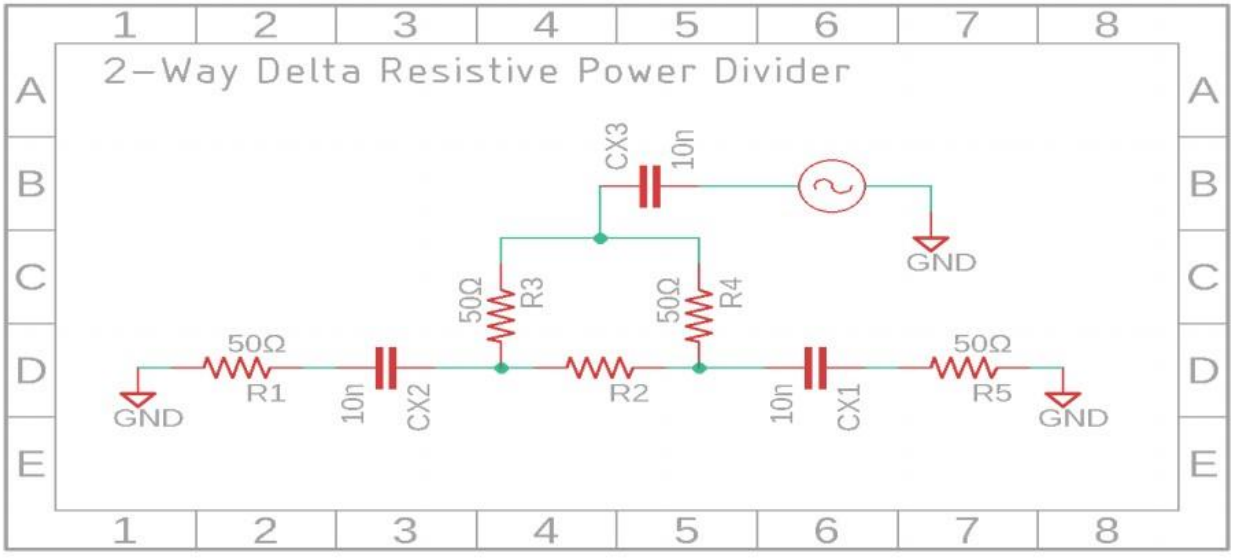

Fig1: 2-Way DELTA Resistive Power Divider

- In the above circuit we replace the resistors with NMOS transistors biased using single ended sources as shown below.

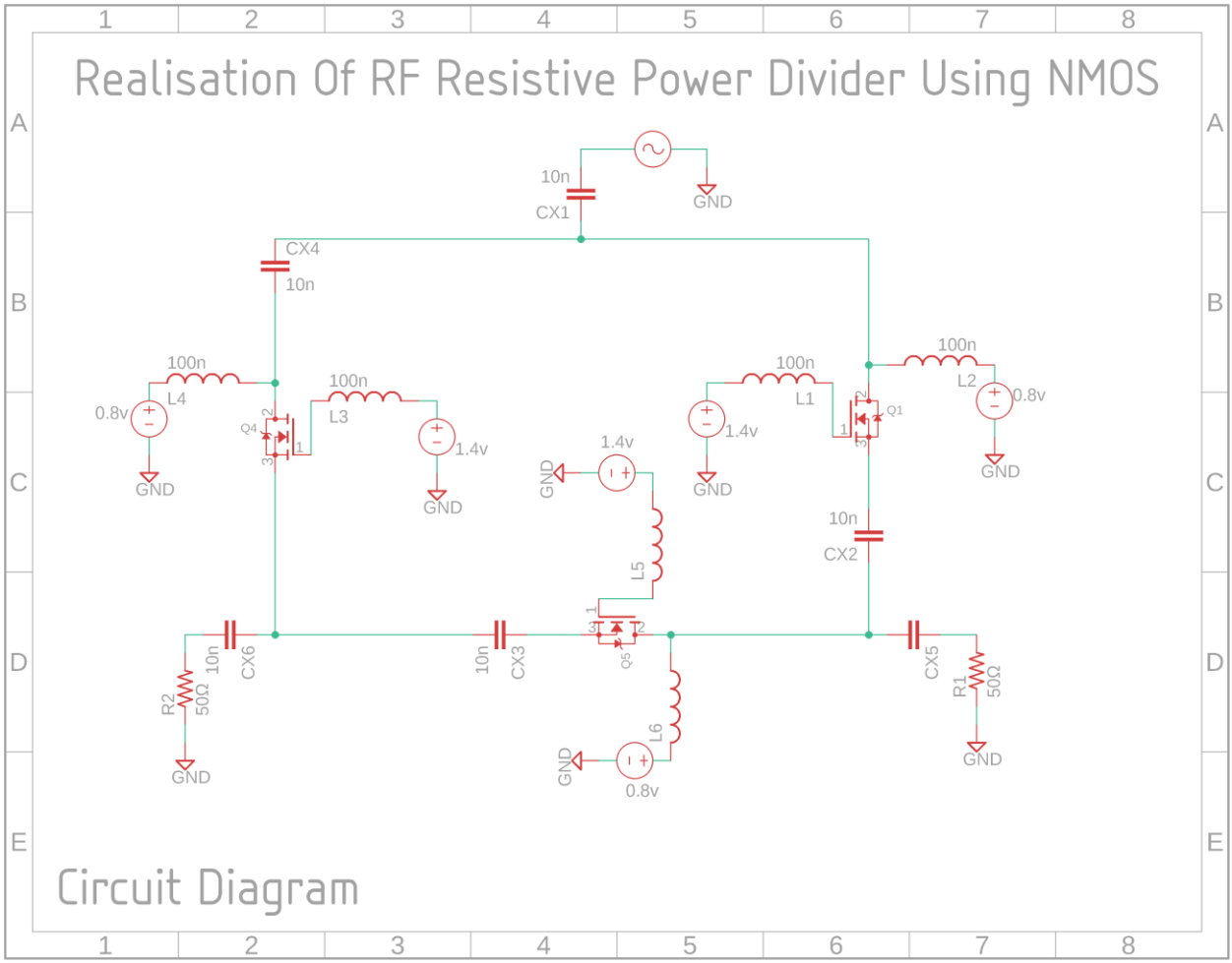

Fig2:- Circuit diagram of NMOS implementation of Power Divider

Calculation of DC Operating Point

- Prior to the AC analysis of the circuit, the bias condition for each MOSFET was set to yield **a drain to source resistance of 50 ohms**.

- **Vgs** was set to a nominal value of **1.4v** and **a DC sweep** was performed using Vds, keeping in mind that the MOS was in triode region.

- From the DC Sweep it was inferred that a **Vds of 0.8v** would correspond to the required drain-source resistance of 50ohms

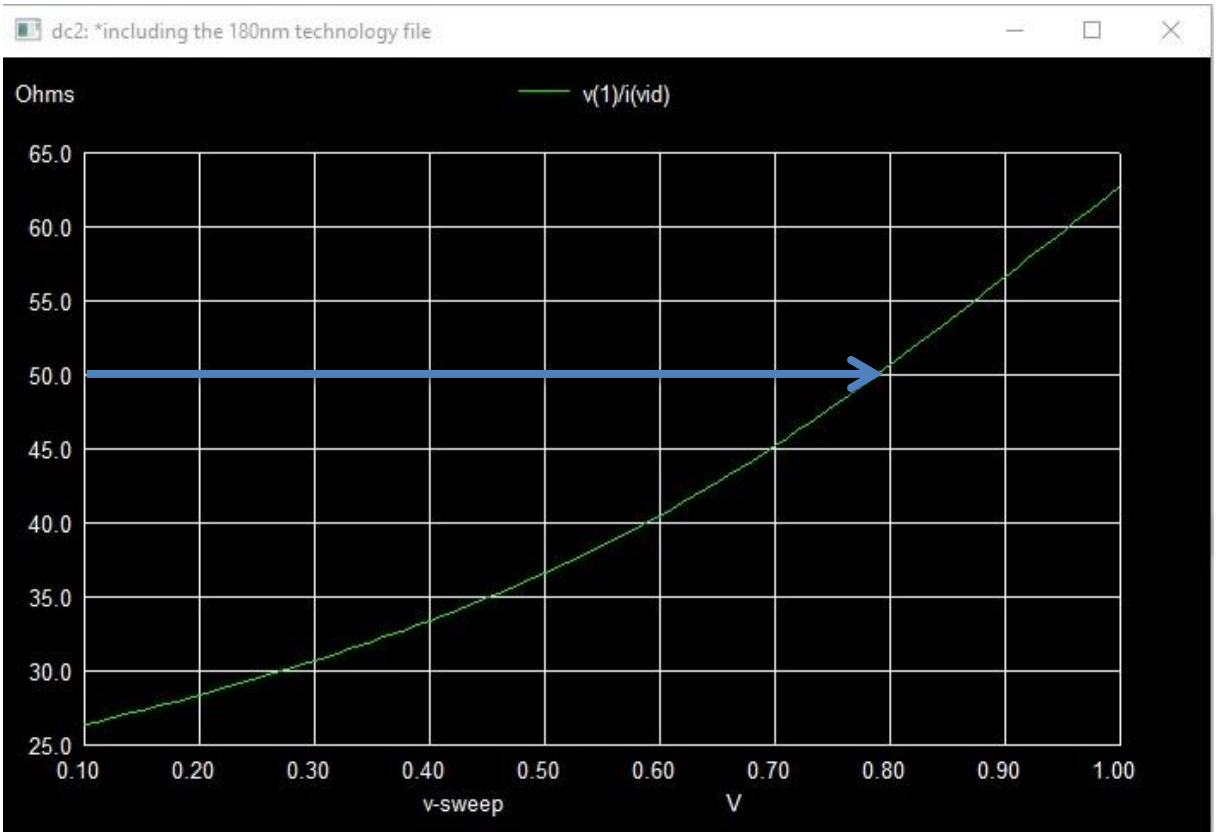

Fig 3:- DC Sweep for operating point.

(X-axis- Vds (Vdd) (in volts) Y-axis- Rds(in ohms))

- For the AC analysis, the gate was biased at 1.4v through a **series inductor of 100nH**. The drain terminal was biased at 0.8v through a series **inductor of 100nH**.

- Spice simulation requires **each node of the circuit to have at least one dc path to ground**. To ensure the same, a high value (1.0e12) shunt resistor (not shown here) to ground was connected at each node.

- DC blocking capacitors and Series inductors of relatively small values like 10nF and 100nH respectively were used.

- AC analysis showed that the circuit performed as per theoretical results over a range of frequencies from 100 MHz to 100 GHz .

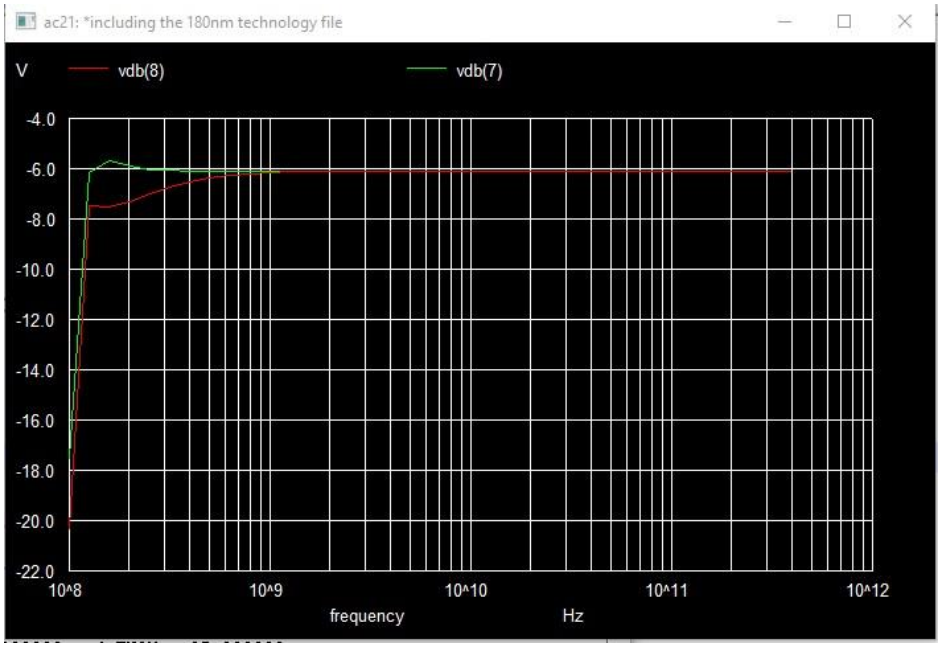

Fig 3:- AC analysis of MOS based power divider

X-axis- frequency of input (in Hz) Y-axis- Output Voltages at two ports (in dB)

Transient Analysis

- The following were the results of inspecting the **output node** under transient analysis using the below-mentioned criteria.
- In all plots ***V(9) represents input sine wave and V(8) is the output node voltage. Y-axis is voltage in mV and X axis shows time in ns.***

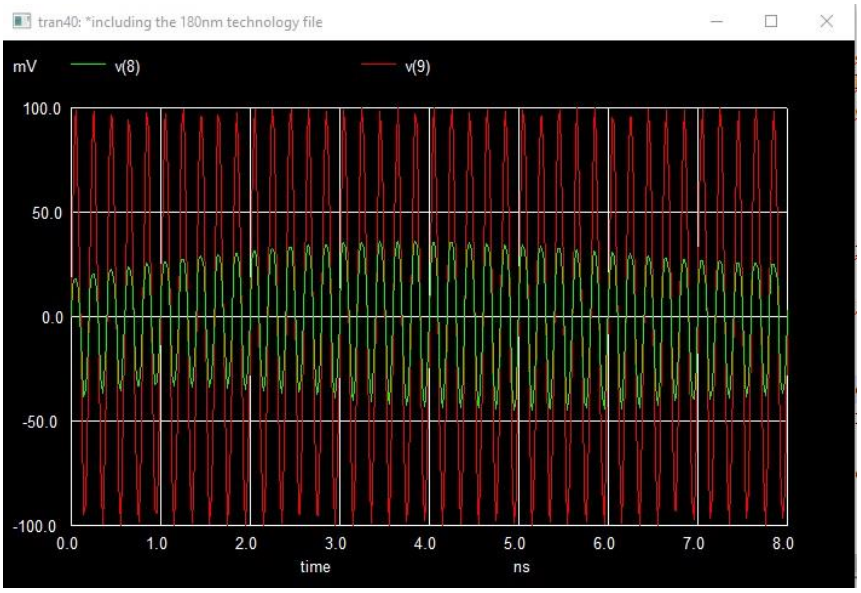

*Fig- Transient Analysis with **100mV** peak sine wave (5GHz) at input.*

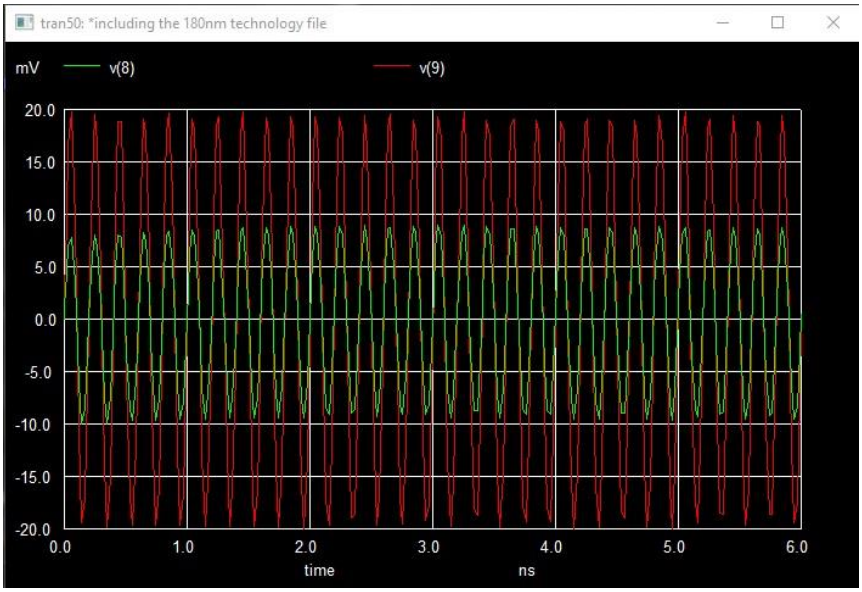

*Fig- Transient Analysis with **20mV** peak sine wave (5GHz) at input.*

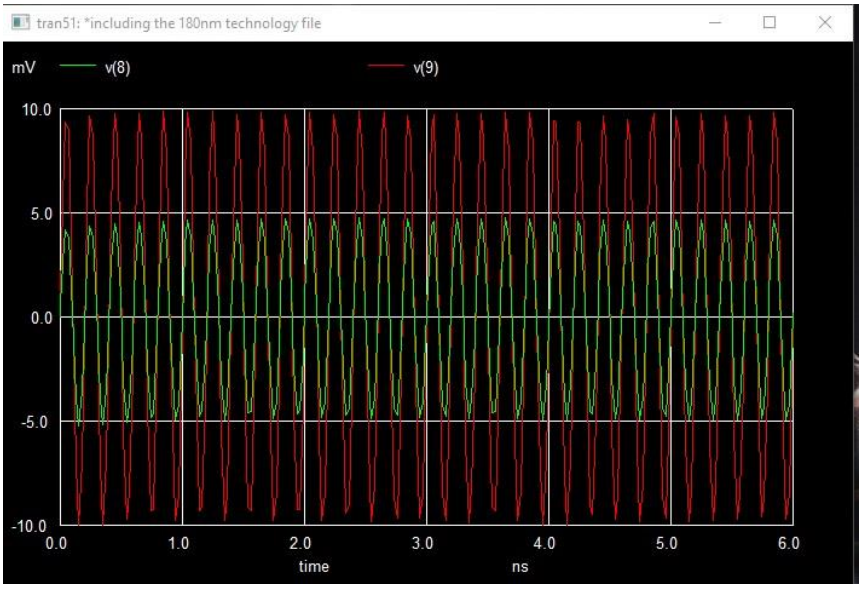

*Fig- Transient Analysis with **10mV** peak sine wave (5GHz) at input.*

Challenges

- Occurrences of Singular matrix errors, non-convergence of iterations while obtaining node voltages and branch current, failed source stepping were among the notable errors encountered during the simulation.
- Absence of a dc path at each node of the circuit, connections of voltage sources/inductors in a loop were the major reasons for the above errors.
- Use of the command .option rshunt = 1.0e12 ensured each node is pulled down to ground through a high value resistor providing a dc path. Further a series inductor was used with each voltage source.

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