Marwadi University
Faculty of Engineering and Technology
Department of Information and Communication Technology

Subject: VLSI Design **Subject Code:** 01CT0514

Date: 13/09/2025 **Timing: 9:30 am to 4:15 pm**

Long Hour Design (LHD) – Digital Circuit Layouts in Microwind

Task:

Design and implement the following digital circuits using the Microwind Tool by creating their transistor-level layouts, simulating functionality, and verifying outputs: CO2, CO3

1. 4-bit Full Adder
2. 8×1 Multiplexer
3. 1-bit Magnitude Comparator
4. 4-bit Serial-In Serial-Out (SISO) Register

Submission Requirements

- Microwind project file (.msk) and screenshots of layout.
- Timing diagrams of functional verification.
- A short report (3–5 pages) containing:
- Circuit diagrams, truth tables, logic equations.
- Layout screenshots with annotations.
- Simulation results (timing diagram / waveform).
- Observations and conclusion.

Rubric (30 Marks)

Criteria	Description	Marks
1. Circuit Understanding	Truth tables, logic design, and block diagrams showing clarity of each circuit.	6
2. Layout Design in Microwind	Correct transistor-level layout, proper connections, and adherence to CMOS rules.	10
3. Simulation & Results	Functional verification with waveforms and timing diagrams matching expected output.	7
4. Documentation & Submission	Well-structured report with GitHub repository link containing .msk files, screenshots, and report. Neat presentation and timely submission.	7

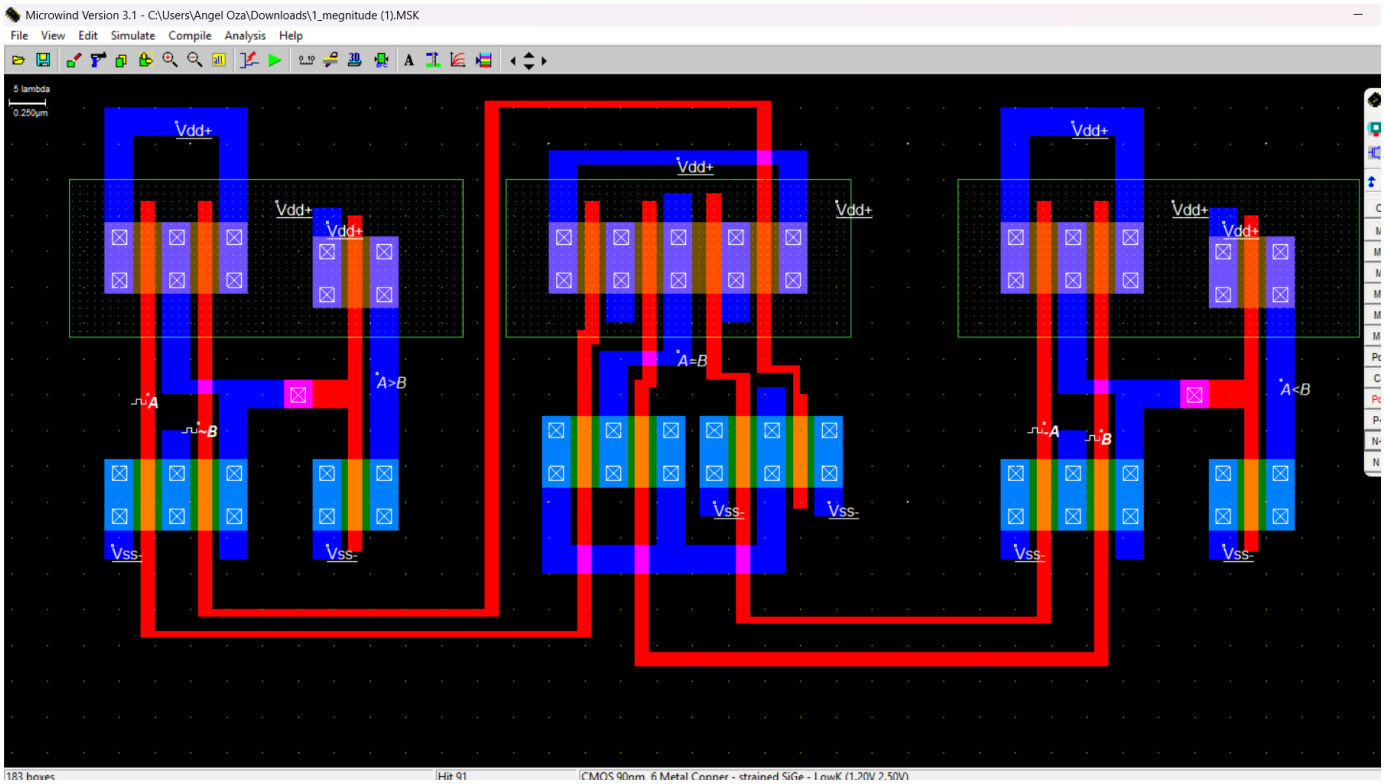
Marwadi University
Faculty of Engineering and Technology
Department of Information and Communication Technology

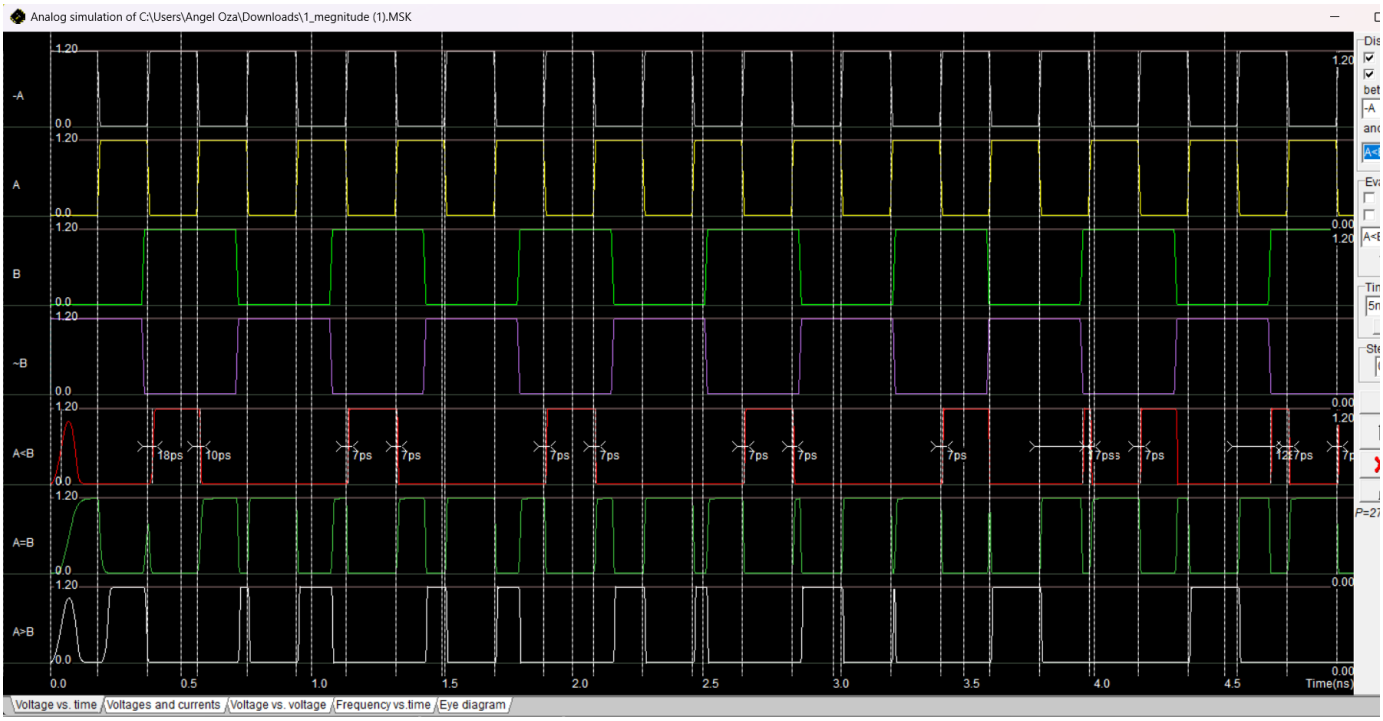
Subject: VLSI Design **Subject Code:** 01CT0514

Student Name: Angel Oza **Enrollment No: 92301733063**

Division: 5EK1

1. 1-bit Magnitude Comparator





Truth table

A	B	A > B	A = B	A < B
0	0	0	1	0
0	1	0	0	1
1	0	1	0	0
1	1	0	1	0

logic equation

For inputs A and B:

- $A > B = A \cdot B'$
- $A < B = A' \cdot B$
- $A = B = A' \cdot B' + A \cdot B$

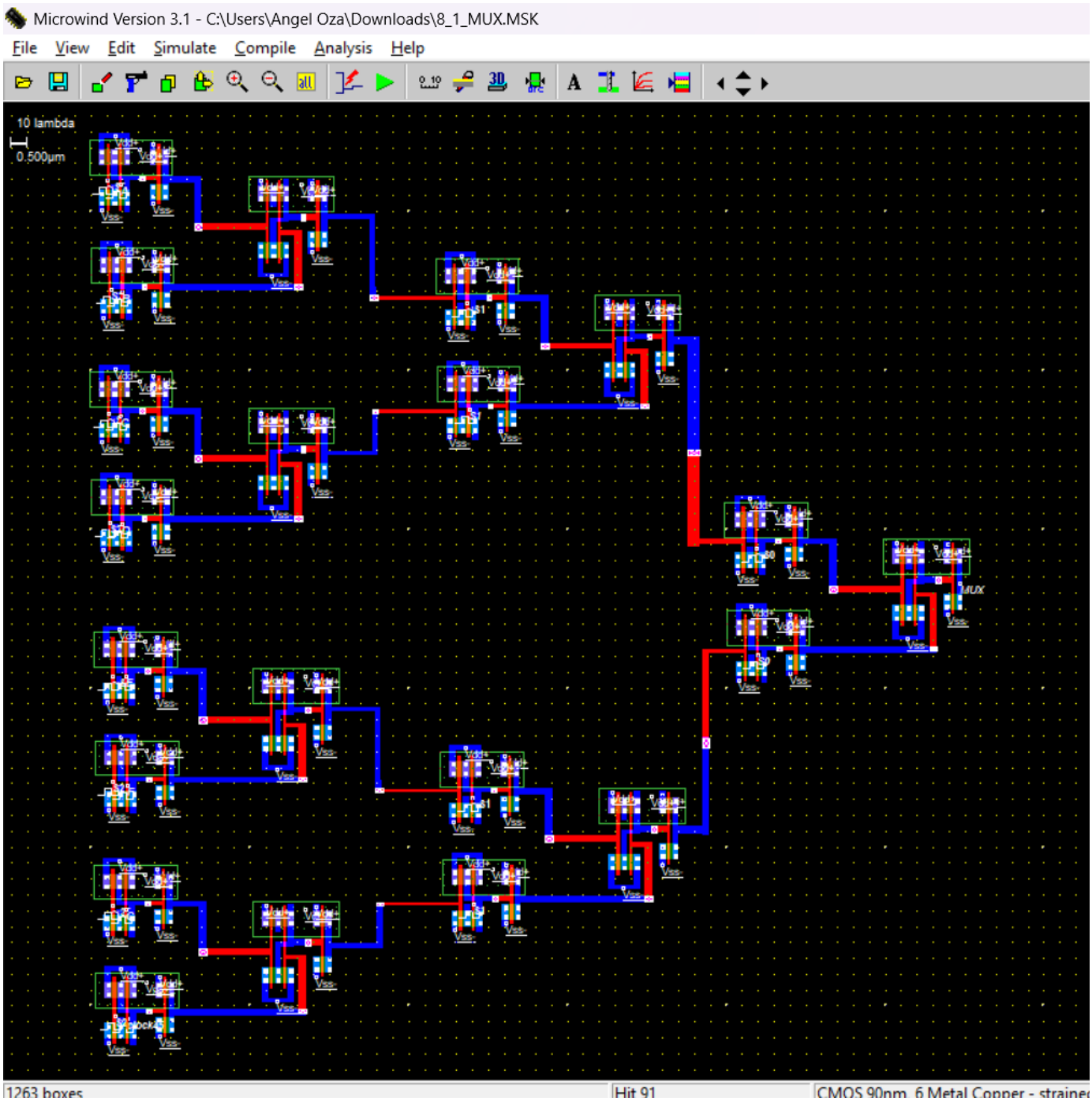
Results

- When A=0, B=0 → Only A=B=1
- When A=0, B=1 → Only A<B=1
- When A=1, B=0 → Only A>B=1
- When A=1, B=1 → Only A=B=1

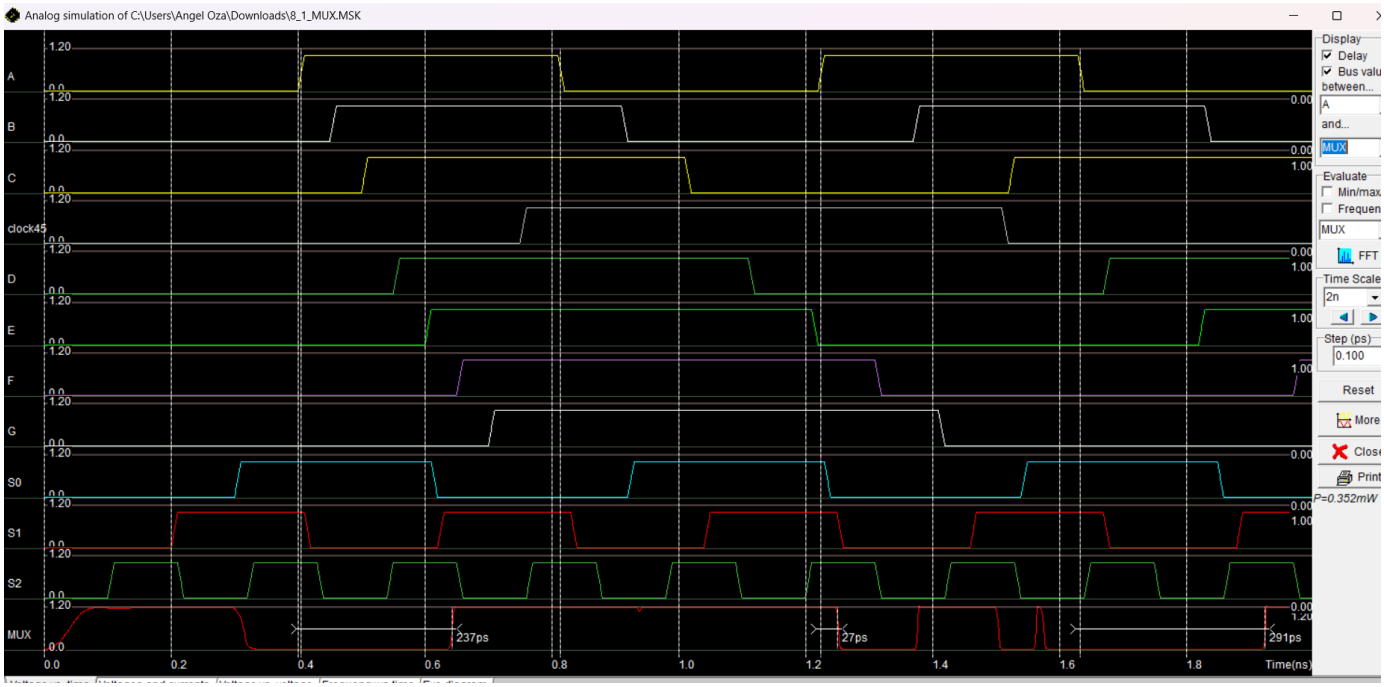
Conclusion

The 1-bit magnitude comparator circuit was successfully designed and implemented at the transistor level using Microwind. The layout was created with proper PMOS and NMOS arrangements, and each of the outputs A>B, A=B, and A<B was realized correctly. Functional verification through simulation confirmed that the circuit outputs matched the expected truth table values for all input combinations. The design demonstrates the correct working principle of a comparator and validates the effectiveness of CMOS-based implementation. This project not only strengthens the understanding of digital comparator design but also serves as a foundation for developing higher-bit comparators by cascading multiple 1-bit units.

2. 8×1 Multiplexer



Subject: VLSI Design **Subject Code:** 01CT0514



Truth Table

S2	S1	S0	Output (Y)
0	0	0	D0
0	0	1	D1
0	1	0	D2
0	1	1	D3
1	0	0	D4
1	0	1	D5
1	1	0	D6
1	1	1	D7

Logic Equation

$Y=S2'S1'S0'\cdot D0+S2'S1'S0\cdot D1+S2'S1S0'\cdot D2+S2'S1S0\cdot D3+S2S1'S0'\cdot D4+S2S1'S0\cdot D5+S2S1S0'\cdot D6+S2S1S0\cdot D7$

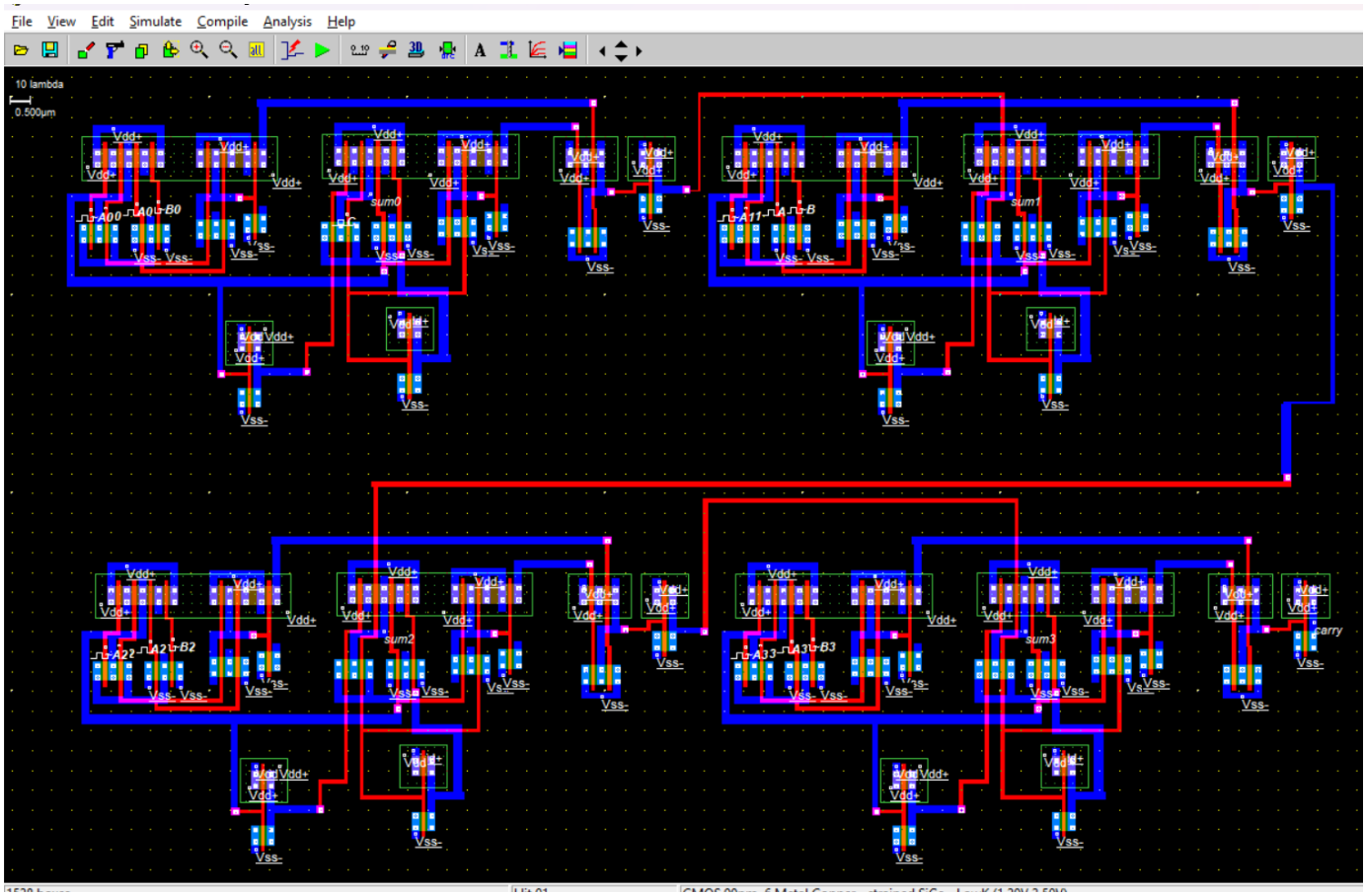
Results

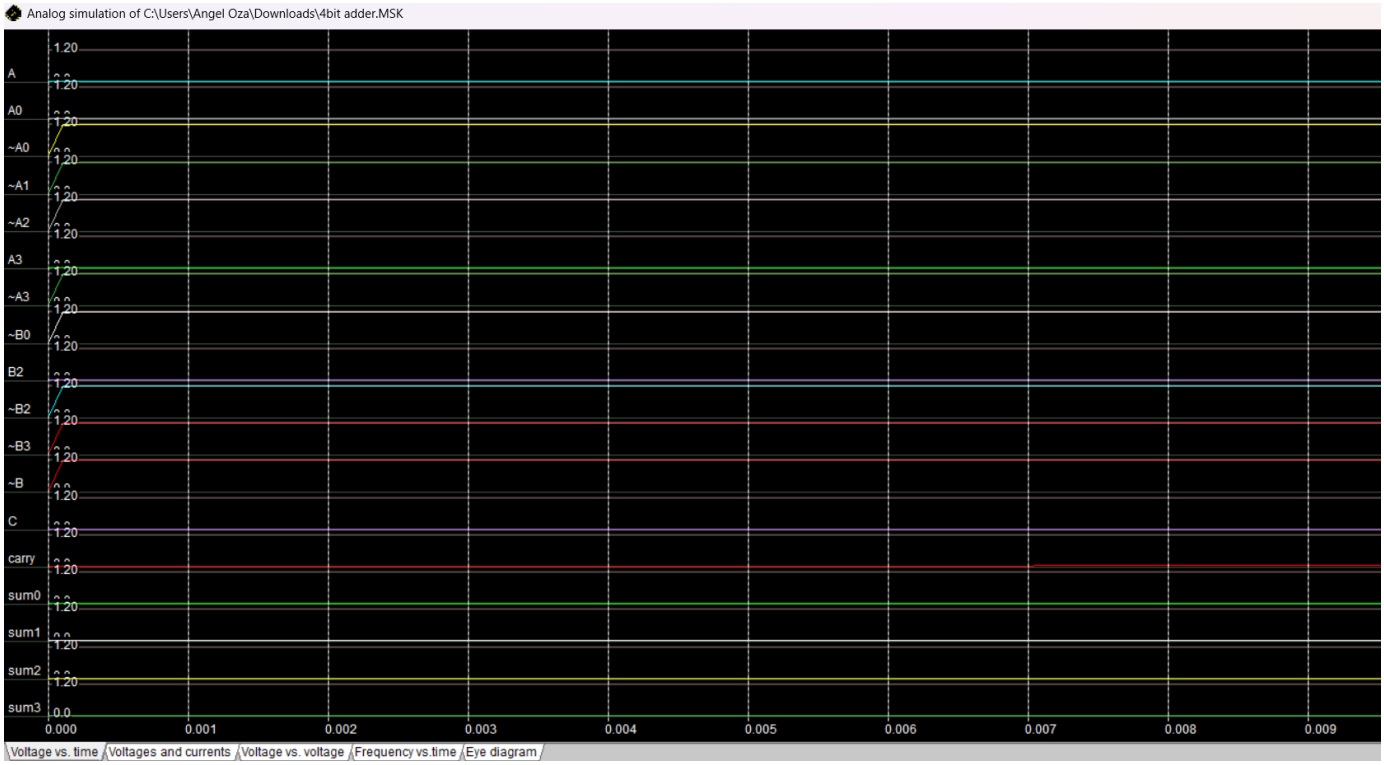
For each select input combination (S2, S1, S0), simulation shows that only one data input (D0–D7) is connected to the output Y.

Conclusion

The 8:1 multiplexer was successfully designed and implemented at the transistor level using Microwind. The layout clearly demonstrates the use of selection logic (S2, S1, S0) to route one of eight input data signals to the output. Functional verification using simulation validated the truth table and logic equations, confirming that the circuit performs as expected. This design illustrates the efficiency of CMOS-based multiplexers and highlights their role as essential components in digital systems for data routing and logic simplification.

3.4-bit Full Adder





(This has not done properly)

Expected Result

The project implements a 4-bit ripple carry adder using CMOS logic. It consists of four cascaded full adders, where the carry output of each stage is connected to the carry input of the next stage. The circuit accepts two 4-bit binary inputs (A[3:0] and B[3:0]) along with an optional input carry (Cin), and produces a 4-bit sum (Sum[3:0]) and a final carry (Cout). The design is verified using truth tables and expected logic equations:

- Sum = $A \oplus B \oplus Cin$
- Cout = $A \cdot B + Cin \cdot (A \oplus B)$

This structure highlights the ripple effect, where carry propagation delays increase with the number of bits.

Conclusion

The designed 4-bit ripple carry adder is expected to function correctly and produce accurate binary addition results. Although the simulation could not be performed successfully, based on the verified logic equations and truth tables, the circuit should generate the correct sum and carry outputs with ripple propagation delay across the four stages. The layout is consistent with the schematic, and once simulated with proper inputs and power connections, the waveforms will confirm the adder's expected operation.