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RNS Institute of Technology
Department of CSE
III Semester - II Test – November 2020
Computer Organization (18CS34)

Duration: 90 mins. **Max Marks: 50** **Time: 8:30-10:00 am** **Date: 01/12/2020**

NOTE: Answer *FIVE* full questions.
Don't write anything on question paper other than USN.

Q.No.		Questions	Marks	BCL	CO
1	a)	List the advantages of interrupt controlled I/O over program controlled I/O.	4	L1	CO3
	b)	When is the usefulness of DMA transfer evident? What is the role of processor during DMA transfer?	2+4	L1	CO3
		OR			
2	a)	What is the role of following registers in display interface? i) DIRQ ii) DEN	2	L1	CO3
	b)	Discuss the two methods to handle simultaneous requests?	4+4	L2	
3	a)	Discuss how vectored interrupts reduce the polling time of the processor?	4	L2	CO3
	b)	Which registers are helpful during DMA transfer? Mention their uses.	6		
		OR			
4	a)	Define i) Bus arbitration. ii) Cycle stealing iii) Burst mode data transfer	6	L1	CO3
	b)	Explain centralized bus arbitration along with suitable diagram to become bus master.	4	L2	CO3
5	a)	How distributed bus arbitration is different from centralized bus arbitration. Justify your answer with suitable example and block diagram.	2+4	L2	CO3
	b)	Discuss how write buffers and prefetching techniques are helpful in cache performance enhancement.	4	L2	CO4
		OR			
6	a)	List any 3 difference between SRAM (Static RAM) and DRAM (Dynamic RAM).	3	L1	CO4
	b)	Briefly explain the structure of a ROM cell and discuss about i) EPROM ii) EEPROM	3+4	L2	CO4
7	a)	Illustrate the burst read of length 4 in SDRAM (Synchronous DRAM) with suitable timing diagram.	6	L3	CO4
	b)	Consider main memory with 8M blocks with 32 words in each block. Find the number of bits in memory address. If it takes 5 clock cycles	2+2	L3	CO4

		to transfer the first word and clock rate of the processor is 100MHz, what is the memory latency?			
		OR			
8	a)	Summarize direct and set associative mapping techniques along with suitable diagram and divisions in main memory address.	8	L2	CO4
	b)	Calculate the total access time if 20 out of 100 instructions are available in the cache , miss penalty is 0.020ms and cache access time is 5 μsec.	2	L3	CO4
9	a)	Consider main memory having 64K words, cache having 1K words. Block size is 128 words. Answer the following questions: i) How many bits are there in MM address? ii) How many bits are there in tag, block and word fields? iii) How bits are there in tag and word if associative mapping is used? iv) How many bits will be there in tag, set and word fields if set associative mapping is used if 2 block per set is used ? if 4 block per set is used?	8	L2	CO4
	b)	Identify the technique used to achieve fast page data transfer mode in DRAM.	2	L4	CO4
		OR			
10	a)	Discuss how 1K memory is organized as 32x 32 memory cell array? Explain why the address is divided in to row and column address?	6	L2	CO4
	b)	To organize 8M x 32 memory using 512K x 8, how many i) Address lines are needed? ii) Rows, columns and chips needed?	4	L3	CO4

Course Outcomes (CO):

CO3 Explore different ways of communicating with I/O devices and interfaces.

CO4 Design and evaluate the performance of memory systems.