Module 1

Basic Structure of Computers

1. What is performance measurement? explain the overall SPEC rating for the computer in a program suite
2. Mention four types of operations to be performed by instructions in a computer. Explain with basic types of instruction formats to carry out C = [A]+[B].
3. Define an addressing mode. Explain the following addressing modes with example: immediate, indirect, index, relative and auto increment
4. What is a stack frame? Explain a commonly used layout for information in a subroutine stack frame
5. Explain shift and rotate operations with example
6. Draw the connection between processor and memory and mention the functions of each component in the connection.
7. Write the difference between RISC and CISC processors.
8. A program contain 1000 instructions. Out of that 25% instructions require 4 clock cycles, 40% instructions require 5 cock cycles and remaining requires 3 clock cycles for execution. Find the total time required to execute the program running in a 1 GHz machine.
9. Explain different rotate instructions.
10. Write ALP program to copy N numbers from array A to array B using indirect addresses.
11. Explain with necessary block diagram the basic functional unit of a computer.
12. Big Endian and ittle Endian assignments, explain with necessary figure. Represent the number 64243848H in 32 bits big endian and little endian memory.
13. List the name, assembler syntax and addressing functions for the different addressing modes.
14. Draw the arrangement of a single bus structure and brief about memory mapped IO.
15. Explain I) Interrupt enabling, II) Interrupt disabling, III) Edge triggering with respect to interrupts.
16. Explain how to encode the instructions into 32 bit words.
17. With a neat diagram explain the different processor registers.
18. What are the factors that affect the performance? Explain any four.
19. With a neat block diagram, describe the IO operations.
20. Discuss briefly encoding of machine instructions.
21. Derive the basic performance equation. Discuss the measures to improve the performance.
22. What is subroutine linkage? Explain with an example subroutine linkage using linkage register.
23. Registers R1 and R2 of a computer contain the decimal values 1200 and 4600. What is EA of the memory opened in each of the following instructions?
24. I) Load 20(R1),R5 II) Move #3000,R5 III) Store R5, 30(R1,R2)
25. IV) Add +(R2), R5 V) Subtract (R1)+ , R5

Module-2

INPUT/OUTPUT ORGANIZATION

1. In a situation where multiple devices capable of initiating interrupts are connected to processor, explain the implementation of interrupt priority, using individual INTER and INTA and a common INTR line to all devices.
2. Define the terms 'cycle stealing' and 'block mode'.
3. What is bus arbitration ? Explain the different approaches to bus arbitration.
4. Briefly discuss the main phases involved in the operation of SCSI bus.
5. Explain the tree structure of USB with split bus operation.
6. Explain the following terms I) interrupt service routine II) interrupt latency III)interrupt disabling
7. With a diagram explain daisy chaining technique
8. With a block diagram explain how the printer is interfaced to processor
9. Define two types of SCSI controller.
10. Explain the use of PCI bus in a computer with necessary figure.
11. List the SCSI bus signals with their functions.
12. Define memory mapped IO and IO mapped IO with examples.
13. What are the different methods of DMA? Explain them in brief. Explain the registers in DMA.
14. Explain the serial port and serial interface.
15. What is an interrupt? with example illustrate the concept of interrupts. Explain polling and vectored interrupts.
16. Describe how a read operation is performed on a PCI bus.
17. List the sequence of events that takes place when a processor sends a commands to the SCSI controller.
18. Define exceptions. Explain two kinds of exceptions
19. Draw and explain the general 8 bit parallel processing.
20. Explain the following with respect to USB, I) USB architecture, II) USB addressing, III) USB protocols.
21. List out the functions of an IO interface.

Module-3

The Memory System

1. Explain the internal organization of a 16 megabit DRAM chip, configured as 2M x 8 cells. Also explain as at how can be made to work in fast page mode.
2. With a block diagram, explain the direct and set associative mapping between cache and main memory.
3. Describe the principles of magnetic disk.
4. What is virtual memory? With a diagram, explain how virtual memory address is translated.

5. Draw for 1K x 1 memory chip with neat figure.
6. Analyze with diagram the memory hierarchy with respect to speed, size and cost.
7. Briefly explain any four non - volatile memory concepts.
8. Discuss the internal organization of a 2M x 8 asynchronous DRAM chip.
9. Describe the different mapping functions in cache.
10. Define: i)memory latency ii) memory bandwidth iii) hit rate iv) miss penalty
11. Explain any one feature of memory design that leads to improved performance of computer.

Module -4
Arithmetic

1. Explain with figure the design and working of a 16 bit carry look ahead adder built from 4 bit adders.
2. Explain booth algorithm. Apply booth algorithm to multiply the signed numbers +13 x -6 and -13 x +9.
3. Write circuit arrangement for sequential binary multiplier, explain with example.
4. Differentiate between restoring and non - restoring division. Perform restoring division for the given binary numbers 1000/11, show all cycles.
5. Design 4 bit carry look ahead logic and explain how it is faster than 4 bit ripple adder.
6. Multiply 14 x -8 using booth's algorithm.
7. Explain normalization, excess exponent and special values with respect to IEEE floating point representation.
8. With figure explain circuit arrangements for binary division.
9. IEEE standard for floating point numbers, explain
10. Design a logic circuit to perform addition/ subtraction of two 'n' bit numbers X and Y. Explain the different arithmetic operation on floating point numbers

Module-5
Basic Processing Unit

1. With a diagram, explain typical single bus processor data path.
2. List out the actions needed to execute the instruction ADD (R3), R1. Write and explain sequence of control steps for the execution of the same.
3. Write the control sequence for an un – conditional branch instruction.
4. Write down the control sequence for the instruction ADD R4,R5,R6 for three bus organization.
5. Explain the process of fetching a word from memory along with a timing diagram.
6. With a neat block diagram, explain hardwired control unit. Show the generation Zin and END control signals.
7. With the neat diagram, the basic organization of a micro programmed control unit.
8. With an example, explain the field coded microinstructions.
9. Differentiate hardwired and micro programmed control unit.
10. Write a micro – routine for the instruction add –(Rsrc), Rdst.