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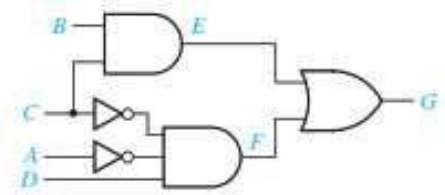
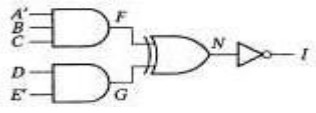
RNS Institute of Technology
Department of CSE
III Semester – II Test – December 2020
Analog & Digital Electronics (18CS33)

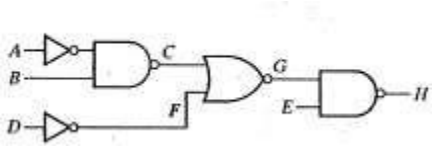
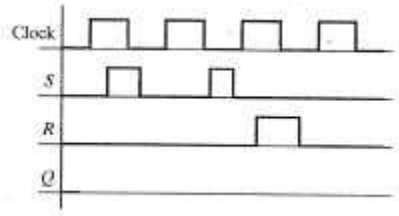
Duration: 90 mins. **Max. Marks: 50** **Time: 1:00-02:30 p.m.** **Date: 01/12/2020**

NOTE: Answer *FIVE* full questions.

Don't write anything on question paper other than USN.

VISION: Preparing better computer professionals for a real world

Qn.No		Questions	Marks	BCL	CO
1	a)	What is three-state buffer? Draw logic symbol and truth table for the 4 kinds of a three-state buffer.	5	L2	CO3
	b)	With neat diagram explain how three state buffers can be cascaded to get one 2-to-1 multiplexer.	5	L3	
		OR			
2	a)	Realize the given functions using 2 input NAND gates F1=∑m(0,2,3,4,5), F2=∑m(1,2,6,7)	3+3	L3	CO3
	b)	For the following circuit: Assume that the inverters have a delay of 1ns and the other gates have a delay of 2ns. Initially A= 0 and B=C=D=1, and C changes to 0 at time 2ns. Draw a timing diagram and identify the transient that occurs. 	4	L2	
3	a)	Analyze the occurrence of static-1 and static-0 hazards in logic circuits with an example for each and sketch the relevant waveforms to illustrate the same.	2*3	L3	CO3
	b)	Show how to overcome the static-1 and static-0 hazards with relevant examples.	2*2		
		OR			
4	a)	Realize the following functions using PLA f1(a,b,c,d)=∑m(1,2,4,5,6,8,10,12,14)	4	L4	CO3
	b)	Show how to implement the given circuits using a PAL i) Full adder ii) Full subtractor	3+3		
5	a)	Write VHDL code to implement 4:1 multiplexer using conditional assignment statements	5	L3	CO5
	b)	Write a VHDL statements that represent the following circuit i) Write statement for each gate ii) Write one statement for the whole circuit 	3+2	L3	
		OR			
6		Derive characteristic equations for the given flip flops i) SR flip flop ii) JK flip flop iii) D flip flop iv) T flip flop v) Gated D latch	5*2=10	L3	CO4

VISION: Preparing better computer professionals for a real world	7	a)	Write a VHDL code to implement 4-bit parallel adder using structural style	6	L3	CO5
		b)	Write a signal concurrent VHDL statements to represent the given circuit 	4	L3	
			OR			
	8	a)	Give an application of SR latch. Explain its working	5	L3	CO4
		b)	With a neat block diagram and wave form, explain how a D flip flop can be constructed using two gated D latches	5		
	9		With the following block diagram, logic diagram, truth table, timing diagram, explain the working of JK flip flop.	10	L3	CO4
			OR			
	10	a)	Complete the given timing diagram of Negative edge triggered SR Flip Flop. Assume that Q begins at 0. 	4	L4	CO4
		b)	Write a note on flip flops with additional inputs. Show how clear and preset are given to a flip flop	6	L2	

Bloom's Cognitive Levels (BCL): L1: Remember, L2: Understand, L3: Apply, L4: Analyze, L5: Evaluate, L6: Create

Course Outcomes (CO):

CO3: Design and analyze various data processing circuits.

CO4: Explain Gates and flip flops and make us in designing different data processing circuits, registers and counters and compare the types

CO 5: Develop simple HDL programs