

DRAM

MOSFET array as the gate.

8421  
1110  
1110

2-10  
3-11  
4-12  
5-13

0 → 0X00EE0000

1 2 3 4

R <sub>1</sub>	0	(1,1) 0	(1,2) 1	(1,3) 2	(1,4) 3
R <sub>2</sub>	1	(2,1) 4	(2,2) 5	(2,3) 6	(2,4) 7
R <sub>3</sub>	1	(3,1) 8	(3,2) 9	(3,3) A	(3,4) B
R <sub>4</sub>	1	(4,1) C	(4,2) D	(4,3) E	(4,4) F
Rows		C <sub>1</sub>	C <sub>2</sub>	C <sub>3</sub>	C <sub>4</sub>

R C  
E E (1,1) - 1  
E D (1,2) - 2  
E B (1,3) - 3  
E 7 (1,4) - 4

8 4 2 1  
R<sub>4</sub> R<sub>3</sub> R<sub>2</sub> R<sub>1</sub>  
1 1 1 0 = R<sub>1</sub> = E  
1 1 0 1 = R<sub>2</sub> = D  
1 0 1 1 = R<sub>3</sub> = B  
0 1 1 1 = R<sub>4</sub> = 7

Columns  
8 4 2 1  
C<sub>4</sub> C<sub>3</sub> C<sub>2</sub> C<sub>1</sub>  
1 1 1 0 = C<sub>1</sub> = E  
1 1 0 1 = C<sub>2</sub> = D  
1 0 1 1 = C<sub>3</sub> = B  
0 1 1 1 = C<sub>4</sub> = 7

0 = (R<sub>1</sub>, C<sub>1</sub>) = (E, E)      6 = (R<sub>2</sub>, C<sub>3</sub>) = (D, B)  
1 = (R<sub>1</sub>, C<sub>2</sub>) = (E, D)      7 = (R<sub>2</sub>, C<sub>4</sub>) = (D, 7)  
2 = (R<sub>1</sub>, C<sub>3</sub>) = (E, B)      8 = (R<sub>3</sub>, C<sub>1</sub>) = (B, E)  
3 = (R<sub>1</sub>, C<sub>4</sub>) = (E, 7)      9 = (R<sub>3</sub>, C<sub>2</sub>) = (B, D)  
4 = (R<sub>2</sub>, C<sub>1</sub>) = (D, E)      10 = (R<sub>3</sub>, C<sub>4</sub>) = (B, B)  
5 = (R<sub>2</sub>, C<sub>2</sub>) = (D, D)      11 = (R<sub>4</sub>, C<sub>4</sub>) = (B, 7)