FM demodulator on FPGA

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Project goal:

The goal of this project is to integrate an FPGA IP core for FM demodulator on Pynq board. The IP core is based on the implementation of RF demodulator using RTLSDR, then with optimization and other effects, works in real time. After that, a visualization of the signal would be helpful for further analysis.

Deliverables:

From 11/22/2020 I have 3 weeks for the objective. The concrete weekly deliverables are a working mono FM demodulator that can returns playable audio and an FM demodulator IP core on FPGA. First of all, the mono FM demodulator takes RF signal and process it in a linear filter, downsampler and a discriminator sequentially. It returns an audio wave that can be handled and played by laptop. The IP core has the same function, but it works on the Pynq board with USB tuners and Pynq audio kits.

Timeline:

WEEK	WORK
11/22/2020 – 11/28/2020 (WEEK 1)	The first 2 weeks of this project would be focused on the implementation of mono FM demodulator. It would take one and a half weeks because it requires a clear understanding of the demodulator and new materials of the programming language used. The expectation of the first week would be a working linear filter function and a downsampler function in C. I will plot the process result of these 2 functions.
11/29/2020 – 12/05/2020 (WEEK 2)	By the end of week 2, a mono FM demodulator IP core is expected. It will pass the testbench and co-simulation on Vivado HLS.
12/06/2020 – 12/12/2020 (WEEK 3)	I will focus on demo, optimization, and visualization of data in week 3. The deliverable of week 3 includes the optimized IP core of the demodulator and the plots of visualized data (power spectrum or else).

Project requirements:

- ‘RTL2832’ USB tuners for RF signal input.
- The local FM radio channel. (94.1 in San Diego)