Core Definition and Generation for DDR3 and DDR2

ID	Description and Actions to Take	Links to Relevant Information	More Details	Status and Notes
1.1	**Xilinx Documentation and Training**			
1.1.1	**Read Users Guides and Datasheets**			
	7 Series FPGA Memory Interface User Guide - UG586	MIG 7 Series Documentation		
	7 Series FPGA Memory Interface Data Sheet - DS176	MIG 7 Series Documentation		
	7 Series FPGA AC and DC Switching Characteristics Datasheets. Includes memory interface performance specifications by device and package - See Maximum Physical Interface (PHY) Rate for Memory Interfaces.	7 Series Data Sheets > Select the appropriate DC and AC Switching Characteristics datasheet	Maximum data rate is based on the device, package, I/O column and target memory interface. The DC and AC Switching Characteristics datasheet and the MIG 7 Series tool include the correct limits.	
1.1.2	**Check the Xilinx MIG Solution Center**	Xilinx Answer 34243	Whether starting a new design with MIG or troubleshooting a problem, use the MIG Solution Center to guide you to the right information	
	Design Assistant	Xilinx Answer 51313	Helpful design and debug information for MIG 7 Series	
	Top Issues	Xilinx Answer 46227	Browse through common questions on MIG 7 Series	
1.1.3	**Read MIG 7 Series Release Notes**		Includes release information as well as known and resolved issues per release.	
	ISE MIG 7 Series Releases (Includes Vivado 2012.4 and earlier)	Xilinx Answer 45195		
	Vivado MIG 7 Series Releases (Starting with Vivado 2013.1)	Xilinx Answer 54025		
1.1.4	**Read Device and IP Notifications**			
	Have you subscribed to appropriate Design Advisories?	Xilinx Answer 18683		
	MIG Design Advisories - See issues that are important to designs currently in progress	Xilinx Answer 33566		
1.1.5	**See Video Demonstrations and White Papers**	http://www.xilinx.com/products/technology/memory-interfacing/index.htm		
1.2	**Understand Core Generation**			
1.2.1	**Using the MIG 7 Series Tool**	UG586 > DDR3/DDR2 > Getting Started		
	Create Design	UG586 > DDR3/DDR2 > Getting Started		
	Pin Compatible FPGAs - Use to create UCF/XDC files for compatible FPGAs	UG586 > DDR3/DDR2 > Getting Started		
	NOTE: Available max data rate may be reduced in pin compatible designs due to inabilty to meet the trace matching requirements	See 2.1 PCB Layout Requirements		
	Memory Selection - Select the target memory standard	UG586 > DDR3/DDR2 > Getting Started		
	Controller Option - Configure the memory interface	UG586 > DDR3/DDR2 > Getting Started	MIG supports up to 72-bit interfaces	
	Create Custom Part - Use when the desired memory part is not selectable in the MIG 7 Series tool.	UG586 > DDR3/DDR2 > Getting Started	Customize a base part to meet the target part's datasheet requirements.	
	Memory Options - Customize how the controller interfaces with the memory	UG586 > DDR3/DDR2 > Getting Started		
	FPGA Options	UG586 > DDR3/DDR2 > Getting Started		
	Define the clocking structure for the memory interface	1.3 Clocks		
	Set the Reset Polarity	1.4 Resets		
	Debug Signals - Enable to use the provided Chipscope debug cores for calibration failure and data error debug.	5.0 Hardware Debug		
	Internal Vref - Supported below 800Mbps	UG586 > DDR3/DDR2 Design Guidelines		
	IO Power Reduction - Enabled by default to reduce the average IO power	UG586 > DDR3/DDR2 > Getting Started	Disables the DQ/DQS IBUF and internal termination during writes and idle periods	
	XADC Instantiation	UG586 > DDR3/DDR2 > Getting Started		
	Extended FPGA Options	UG586 > DDR3/DDR2 > Getting Started		
	IO Planning Options	UG586 > DDR3/DDR2 > Getting Started		
	New Design - Use for new boards where pin locations are not yet defined.	UG586 > DDR3/DDR2 > Getting Started		
	Fixed Pin-Out - Use for boards where pin locations are defined. Manually entering pins or uploading a UCF/XDC are both supported.	UG586 > DDR3/DDR2 > Getting Started		
	DRC check ensures pin/bank rules are followed	UG586 > DDR3/DDR2 Design Guidelines		
	Bank Selection - Use to select the banks and byte groups for the memory interface signal groups	UG586 > DDR3/DDR2 > Getting Started		
	DRC check ensures pin/bank rules are followed	UG586 > DDR3/DDR2 Design Guidelines		
	System Signals Selection	UG586 > DDR3/DDR2 > Getting Started		
	System and Reference Clocks	2.2.3 Clock Pin Planning		
	Status Signals - May be connected internally or driven to an external IO	UG586 > DDR3/DDR2 > Getting Started		
	Verify Pin Changes and Update Design - Use to verify any pin changes and generate an updated design to match the new pin-out. Additionally, use to upgrade a MIG 7 Series IP to a newer release.	UG586 > DDR3/DDR2 > Getting Started UG586 > DDR3/DDR2 Design Guidelines		
1.3	**Understand Clocks**			
1.3.1	Check Clocking Requirements	Xilinx Answer 40603		
1.3.2	Clocking Architecture	UG586 > DDR3/DDR2 > Core Architecture > Clocking Architecture		
1.3.3	Clocking Parameters and RTL	UG586 > DDR3/DDR2 > Customizing the Core		
	All clock parameters are set based on the MIG 7 Series tool settings. Items such as the frequencies of the input and clocks, how the IDELYCTRL reference clock is generated, etc. Changes to the clocking should be done through the MIG 7 Series tool and not by making manual changes to these parameters.			
	Clock pin and placement planning	See 2.2.3 Clock Pin Planning and 2.2.4 Clock Resource Planning		
1.4	**Understand Resets**			
1.4.1	System Reset (sys_rst) - Used to reset the MIG 7 Series core and restart initialization and calibration		Asynchronous assertion. Synchronous deassertion	
	Can be internally or externally generated			
	Can be selected through the MIG 7 Series tool as either active high or active low. Drives top level rtl parameter RST_ACT_LOW (1=Active Low; 0=Active High)	UG586 > DDR3/DDR2 > Customizing the Core		

	Reset synchronization handled within MIG 7 Series rtl	Generated Design Directory = core_name/user_design/rtl/clocking/mig_7series_vx_x_infrastructure.v		
1.4.2	ui_clk_sync_rst - User Interface Active High Reset. Synchronous to ui_clk (User Interface Clock).	UG586 > DDR3/DDR2 > Core Architecture > User Interface		
1.4.3	RESET_N - DDR3 Reset	2.0 Pin and Board Planning		
1.5	**Understand XADC and Temperature Monitor**			
1.5.1	The XADC block is a required part of the temperature monitor system which keeps the read DQS centered in the read DQ window across temperature drift	UG586 > DDR3/DDR2 > Core Architecture > PHY		
	MIG 7 Series can instantiate the XADC or, if the user design already includes the XADC, receive the device temperature on a device_temp input to the MIG 7 Series core	Xilinx Answer 51867		
1.6	**Understand Top-Level RTL Parameters**			
1.6.1	The MIG 7 Series lower level rtl source files do not change. The options selected within the MIG 7 Series tool are used to set top-level rtl parameters to properly configure the lower level rtl source code. For information on these parameters, reference the relevant documenation.	UG586 > DDR3/DDR2 > Customizing the Core		
1.7	**Understand PHY Only Support**			
1.7.1	Usage of the MIG 7 Series PHY independently is supported.			
	The MIG 7 Series tool will always generate the full design with controller and user interface included. The PHY rtl is broken out for independent usage.	Generated Design Directory = core_name/user_design/rtl/phy		
	Full documentation on the PHY only solution is available.	UG586 > DDR3/DDR2 > Interfacing to the Core > Physical Layer Interface		

Pin and Board Planning for DDR3 and DDR2

ID	Description and Actions to Take	Links to Relevant Information	More Details	Status and Notes
2.1	**Check PCB Layout Requirements**			
2.1.1	**Termination**	UG586 > DDR3/DDR2 Design Guidelines		
	DQ/DQS/DM - DCI (HP Banks) or IN_TERM (HR Banks) are required at the FPGA. ODT is required at the memory			
	Addr/Cont/Cmd/CK - External termination is required. See relevant link for additional requirements at the memory.			
	RESET_N is not terminated but should be pulled low during memory initialization. See relavant link for requirements			
	CKE requirements vary between DDR3 and DDR2. DDR3 CKE should be terminated similar to addr/cont. DDR2 CKE should be pulled low during memory initialization. See relavant link for requirements.			
2.1.2	**IBIS Simulation is highly recommended for all interfaces**	UG586 > DDR3/DDR2 Design Guidelines		
	Ensure DQ/DQS lines and addr/cont lines are all simulated			
2.1.3	**Fly-By Topology is required for all DDR3 interfaces**	UG586 > DDR3/DDR2 Design Guidelines		
	MIG 7 Series performs write leveling for all DDR3 interfaces			
2.1.4	**40 Ohm Trace Impedance is required for interfaces above 1333Mbps. Below 1333Mbps can use 50 Ohm Trace Impedance.**	UG586 > DDR3/DDR2 Design Guidelines		
	NOTE: 40 Ohm traces required 80 Ohm VRN/VRP resistors			
2.1.5	**Internal Vref is supported below 800Mbps. Above 800Mbps requires external Vref.**	UG586 > DDR3/DDR2 Design Guidelines		
2.1.6	**VCCAUX_IO can be set to either 2.0V or 1.8V depending on device, I/O Column, and target memory data rate.**	7 Series Data Sheets		
2.1.7	**Power System and Plane Disontinuities**	UG483 7 Series FPGAs PCB Design and Pin Planning Guide		
2.1.8	**Optimal SelectIO Interface VREF Generation Circuits**	XAPP1087		
2.1.9	**Trace Length Matching is required and must include package delays. Trace length matching is required between the following groups. The relavant documentation should be referenced for specific delays.**	UG586 > DDR3/DDR2 Design Guidelines		
	DQ/DM and associated DQS/DQS#			
	Address and Control and the corresponding CK/CK#			
	CK/CK# and the DQS/DQS# signals			
	Package Delays can be found running PartGen or within the Vivado Pinout Table			
	Trace length matching can be derated when running below the maximum supported data rate for a given configuration. Review the Trace Derating tables for derating details.	UG586 > DDR3/DDR2 Design Guidelines		
	For Pin Compatible Designs, because package delays vary across parts, the max available data rate may be reduced due to the inability to meet the trace matching reqruiements. The worst case delays should be used to determine the available max data rate.	UG586 > DDR3/DDR2 Design Guidelines		
2.1.10	**Understand Simultaneous Switching Noise (SSN)**	Xilinx Answer 34569		
2.2	**Understand I/O and Clock Pin Planning**			
2.2.1	**I/O Pin Planning**			
	MIG 7 Series requires specific pin/bank placement. The MIG 7 Series tool must be used to generate or modify a pin-out. The generated design (UCF/XDC constraints and rtl parameters) are custom to the selected pin-out.	UG586 > DDR3/DDR2 Design Guidelines		
	New Design option in the MIG 7 Series tool creates a pin-out based on banks selected.	UG586 > DDR3/DDR2 > Getting Started		
	Fixed Pin-Out flow can be used to upload a desired pin-out and run a DRC check	UG586 > DDR3/DDR2 > Getting Started		
	Verify UCF and Update Design can be used to verify a modified pin-out, run a DRC check and create an updated design to match the modified pin-out.	UG586 > DDR3/DDR2 > Getting Started		
	Fitting a x16 in a single bank.	Xilinx Answer 41752		
	Sharing banks between multiple memory interfaces is not permitted	UG586 > DDR3/DDR2 Design Guidelines		
		Xilinx Answer 41706		
	Usage of unused VRN/VRP I/O (HP banks) when DCI Cascade is used or non-byte group I/O (HR banks) is permitted for Address/Control or Reset_N pins. See the referenced documentation for specific rules.	UG586 > DDR3/DDR2 Design Guidelines		
	Enabling Dynamic ODT special use case to remove ODT pin	Xilinx Answer 46082		
	Usage of the PUDC_B configuration pin	Xilinx Answer 50739		
	For Artix-7/Kintex-7, when CFGBVS is set to VCCO of Bank 0, then Banks 14 and 15 are limited to 3.3V or 2.5V for Configuration	Xilinx Answer 57045		
2.2.2	**RESET_N Pin Planning**			
	RESET_N can be connected to any available pin within the device, including the VRN/VRP pins if DCI cascade is used, as long as timing is met and an appropriate I/O voltage standard is used. The GUI restricts this pin to the banks used for the interface to help with timing, but this is not a requirement.	UG586 > DDR3 Design Guidelines		
	RESET_N Termination - Pull low with 4.7 kΩ resistor	UG586 > DDR3 Design Guidelines		
	Driving a 1.35V LVCMOS Reset to a DDR3L device	Xilinx Answer 47232		
2.2.3	**Clock Pin Planning**			

	MIG 7 Series has specific requirements for the system input clock (sys_clk). All supported clocking structures can be generated through the MIG 7 Series tool.	Xilinx Answer 40603		
	CCIO Input placement requirements	Xilinx Answer 40603		
	Sys_clk sharing requirements	Xilinx Answer 40603		
	Sys_clk jitter requirements	Xilinx Answer 40603		
	PLL multiply and divide requirements to reduce jitter	Xilinx Answer 40603		
	MIG 7 Series requires a 200MHz IDELAYCTRL reference clock (ref_clk). The general FPGA requirements of this clock must be followed.	7 Series Data Sheets > Select the appropriate DC and AC Switching Characteristics datasheet		
	If the input sys_clk and memory data rate allow generation of a 200MHz clock, the ref_clk can be generated by the MIG 7 Series clocking structure.	UG586 > DDR3/DDR2 > Getting Started		
2.2.4	**Clock Resource Planning**			
	MIG 7 Series requires a PLL and an MMCM for each interface within the bank selected for Address/Control	UG586 > DDR3 Design Guidelines		
	The generated MIG UCF/XDC file includes all appropriate placement constraints.	UG586 > DDR3 Design Guidelines		
2.3	**Understand Power Planning and Analysis**	Power Efficiency Website		
2.3.1	**Design**			
	Power System Design	UG483 7 Series FPGAs PCB Design and Pin Planning Guide		
2.3.2	**Analysis**			
	Power Analysis	ISE - UG440 Xilinx Power Estimator User Guide		
		Vivado - UG907 Power Analysis and Optimization		
	Download XPE	Power Efficiency Website		
2.4	**Understand XADC Board Setup**			
2.4.1	XADC is required with the continuous Temperature Monitor calibration	Xilinx Answer 51867		
		LogiCORE IP XADC Wizard Product Guide - PG091		
		UG586 > Core Architecture > PHY		

Simulation for DDR3 and DDR2

ID	Description and Actions to Take	Links to Relevant Information	More Details	Status and Notes
3.1	**Understand Supported Simulators**	7 Series FPGAs Memory Interface Solutions Datasheet - DS176		
3.1.1	**Additional Information**	Xilinx Answer 51671		
	Timing Simulation is not supported for MIG 7 Series IP			
3.2	**Check Simulation Parameters**	Xilinx Answer 51668		
3.2.1	**Speeding up simulation run time**	UG586 > Customizing the Core		
	Set SIM_BYPASS_INIT_CAL = "FAST";			
3.3	**Understand Simulation Analysis**			
	Using the provided Example Design with Traffic Generator	UG586 > DDR3/DDR2 > Getting Started > Quick Start Example Design		
		UG586 > DDR3/DDR2 > Getting Started > Modifying the Example Design		
	Calculating and Improving Efficiency	Xilinx Answer 36719		
	Simulation Debug	Xilinx Answer 51667		

Design Flows for DDR3 and DDR2				
ID	**Description and Actions to Take**	**Links to Relevant Information**	**More Details**	**Status and Notes**
4.1	**Understand Design Flow Options**			
4.1.1	**ISE Flow Options**			
	CORE Generator Flow	UG586 > DDR3/DDR2 > Getting Started		
	Generating a MIG 7 Series core from an existing ISE project	Xilinx Answer 37424		
	Creating an ISE project with a generated MIG 7 Series core	UG586 > Creating ISE Project Navigator Flow for MIG Example Design		
4.1.2	**Vivado Flow Options**	UG586 > Using MIG in Vivado Design Suite		
	Generate the MIG Example Design using the Open IP Example Design Vivado option	UG586 > Using MIG in Vivado Design Suite		
4.2	**Running Synthesis and Implementation**			
4.2.1	**ISE Synthesis and Implementation**			
	Execute the ise_flow.bat/.sh script file located in the example_design/par directory. The ise_flow.bat/.sh script file ensures the necessary synthesis and implementation options are enabled.	UG586 > DDR3/DDR2 > Getting Started		
	OR			
	Use the generated ISE project to implement the design	See 4.1.1 ISE Flow Options		
4.2.2	**Vivado Synthesis and Implementation**			
	Generate with either the user or example design Vivado project	See 4.1.2 Vivado Flow Options		
4.2.3	**Debugging the Synthesized/Implemented Design**			
	Does the design close timing post-synthesis or post-implementation? If not, was any portion of the generated design modified? The generated design will not fail timing.	See 4.4 Timing Closure		
	Were any rtl parameters or code modified? The generated design will not fail synthesis or implementation.	UG586 > DDR3/DDR2 > Customizing the Core		
	The top-level parameters and UCF/XDC constraints are generated based on the user input within the MIG 7 Series tool. Any required modifications must be made through the MIG 7 Series tool to generate a new set of rtl and constraints.	UG586 > DDR3/DDR2 > Getting Started		
4.3	**Understand IP Constraints**			
4.3.1	MIG 7 Series cores are generated with required UCF/XDC constraints.	See the example_design/par and user_design/constraints directories		
	Constraint Documentation	UG586 > DDR3/DDR2 Design Guidelines		
4.3.2	When DCI Cascade is implemented, users must manually enter the appropraite DCI Cascade constraint specifying the master and slave banks within the generated UCF/XDC.	Xilinx Constraints Guide		
4.3.3	Compatible UCF/XDC files will be generated if a device is selected on the Pin Compatible FPGAs screen within the MIG 7 Series tool	See the example_design/par/compatible_ucf and user_design/constraint/compatible_ucf directories		
4.4	**Understand Timing Closure**			
4.5.1	**Preliminary Timing Closure**			
	The MIG 7 Series IP should not fail timing out of the box. If there is a timing error in the default configuration, please open a webcase.	Webcase		
	Ensure all timing constraints provided in the MIG 7 Series generated UCF/XDC are being applied. MIG 7 Series provides all necessary constraints for the IP.	See 4.3 Constraints		
	Determine if the timing error is within the user logic or the MIG 7 Series design.			
4.5	**Understand Floorplanning**			
	Floorplanning is generally not needed to close timing with the MIG core.			
4.6	**Migrating to new Software Releases**			
4.6.1	**ISE**			
	Use the Verify UCF and Update Design MIG 7 Series feature	UG586 > DDR3/DDR2 > Getting Started		
4.6.2	**Vivado**			
	Upgrading ISE/CORE Generator MIG 7 Series cores in Vivado	UG586 > Upgrading the ISE/CORE Generator MIG Core in Vivado		
4.7	**Working with Third Party Tools**			
4.7.1	**Third Party Synthesis Tools**			
	MIG 7 Series can be synthesized with Synplify Pro	Search www.xilinx.com/support for answer records on Synplify Pro support		
	Other Third party synthesis tools have not been tested with MIG 7 Series IP			
4.7.2	**Third Party Simulation Tools**			
	MIG 7 Series can be simulated using Modelsim	7 Series FPGAs Memory Interface Solutions Datasheet - DS176		
	Other third party simulation tools as VCS from Synopsys or NC-Sim from Cadence Design Systems have not been tested with MIG 7 Series IP	Xilinx Answer 51671		

Hardware Debug for DDR3 and DDR2

ID	Description and Actions to Take	Links to Relevant Information	More Details	Status and Notes
5.1	**Initial Debug - REVIEW FIRST regardless of calibration failure or data error**			
5.1.1	**Verify all pin and board layout guidelines have been followed**	UG586 > DDR3/DDR2 Design Guidelines		
5.1.2	**Review the General Checks for hardware debug**	UG586 > DDR3/DDR2 > Debugging DDR3/DDR2 Designs > General Checks		
5.1.3	**Generate an identical MIG 7 Series core with Debug Signals Enabled**	UG586 > DDR3/DDR2 > Getting Started	When using a core with Debug Signals enabled, necessary core signals are pulled into Chipscope cores to ease the debug process and get to resolution quickly.	
5.1.4	**Try to reproduce failure using MIG 7 Series Example Design**	UG586 > DDR3/DDR2 > Getting Started > Quick Start Example Design	The MIG 7 Series Example Design is a known working solution that is a great starting point for hardware debug. It can be easily brought up in a system to rule out a user design issue and focus the debug.	
5.2	**Understand Calibration Failure Debug**			
5.2.1	**Determine the failing calibration stage**	UG586 > DDR3/DDR2 > Debugging DDR3/DDR2 Designs > Determining the Failing Calibration Stage		
5.2.2	**Determine the failing byte group and if possible failing bit**	UG586 > DDR3/DDR2 > Debugging DDR3/DDR2 Designs > Determining the Failing Calibration Stage		
5.2.3	**Determine how the calibration stage is failing (i.e., incorrect data pattern received, no edge detection, etc)**	UG586 > DDR3/DDR2 > Debugging DDR3/DDR2 Designs	Step through the section within the Deubbing DDR3/DDR2 Designs chapter specific to the calibration stage failing. These sections will provide specific details on Chipscope triggers to use, signals to analyze, board measurements to capture, etc.	
	When pattern detection fails, determine if the data error failure is due to the read or the write	UG586 > DDR3/DDR2 > Debugging DDR3/DDR2 Designs > Data Error Debug > Determining If a Data Error is Due to the Write or Read		
5.3	**Understand Data Error Debug**			
5.3.1	**Isolate the data error**	UG586 > DDR3/DDR2 > Debugging DDR3/DDR2 Designs > Data Error Debug > Isolate the Data Error		
	Bit or byte errors			
	Data shifted, swapped, garbage			
	Specific to certain addresses			
	Specific to certain data pattern(s)			
	Determine the frequency and reproducibility of the error			
	Determine if the error is recoverable			
5.3.2	**Determine if the data error is on the write or the read**	UG586 > DDR3/DDR2 > Debugging DDR3/DDR2 Designs > Data Error Debug > Determining If a Data Error is Due to the Write or Read		
	Issue a small initial number of writes, followed by continuous reads from those locations.			
5.3.3	**Analyze the read/write window size using the MIG 7 Series Example Design with Debug Signals Enabled**			
	Using the automatic window check	UG586 > DDR3/DDR2 > Debugging DDR3/DDR2 Designs > Data Error Debug > Automatic Window Check		
	Using the manual window check	UG586 > DDR3/DDR2 > Debugging DDR3/DDR2 Designs > Data Error Debug > Manual Window Check		