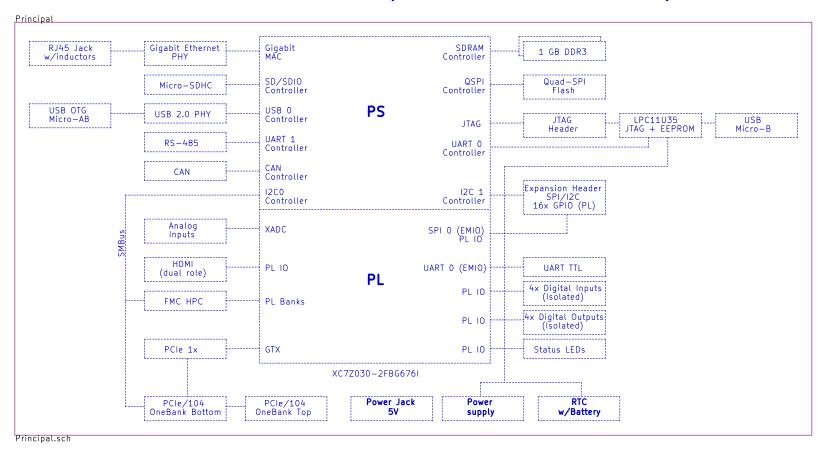
Computadora Industrial Abierta Argentina CIAA-ACC Xilinx XC7Z030 (2x Cortex A9 + Kintex-7 FPGA)









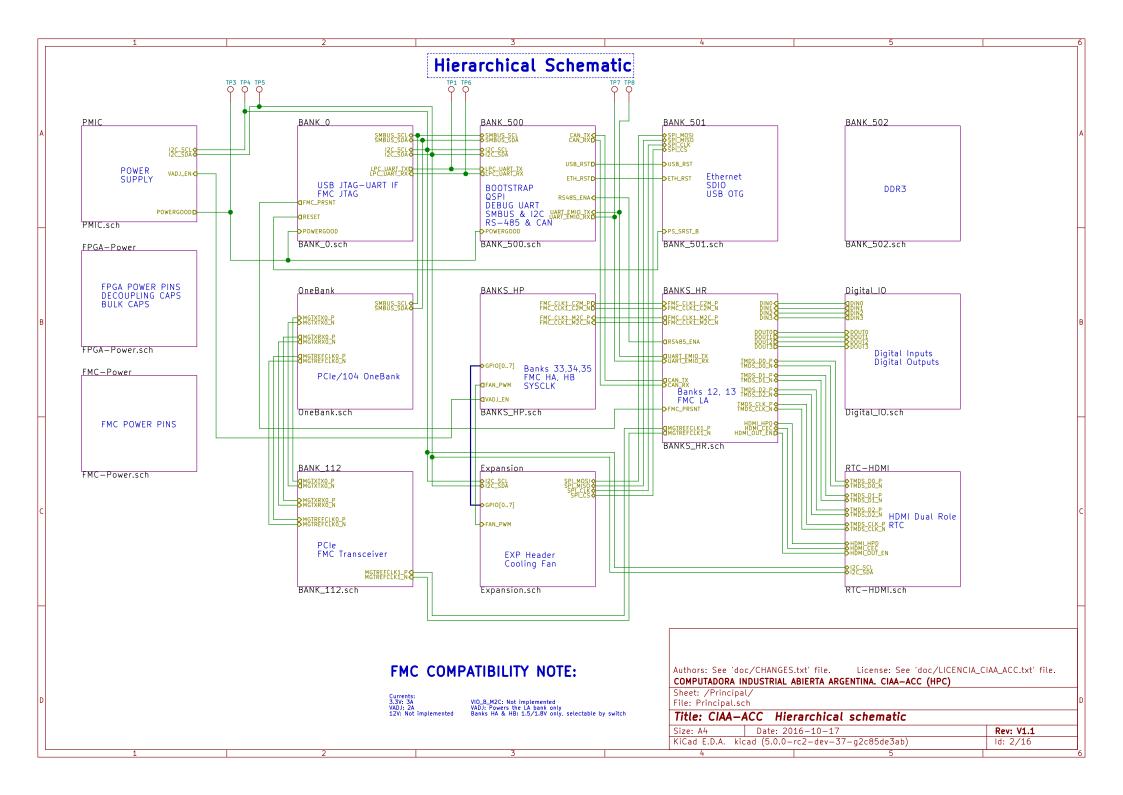
Authors: See 'doc/CHANGES.txt' file. License: See 'doc/LICENCIA_CIAA_ACC.txt' file. COMPUTADORA INDUSTRIAL ABIERTA ARGENTINA. CIAA—ACC (HPC)

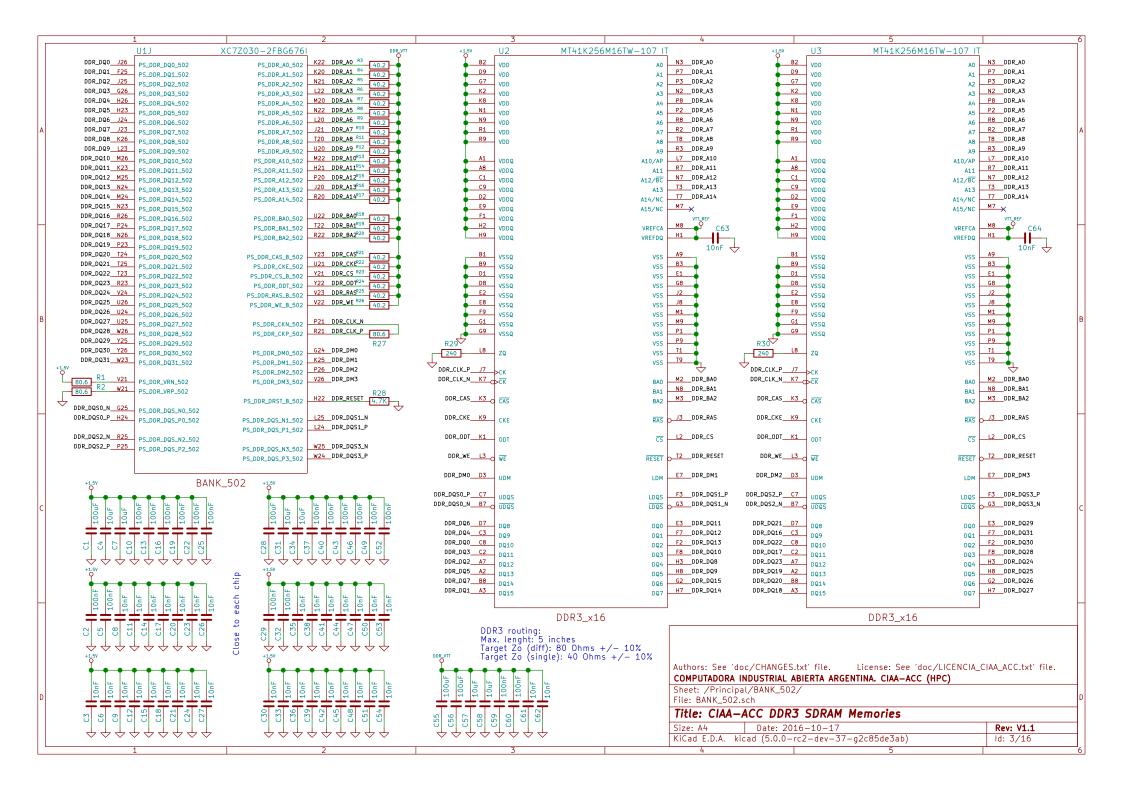
Sheet: / File: ciaa_acc.sch

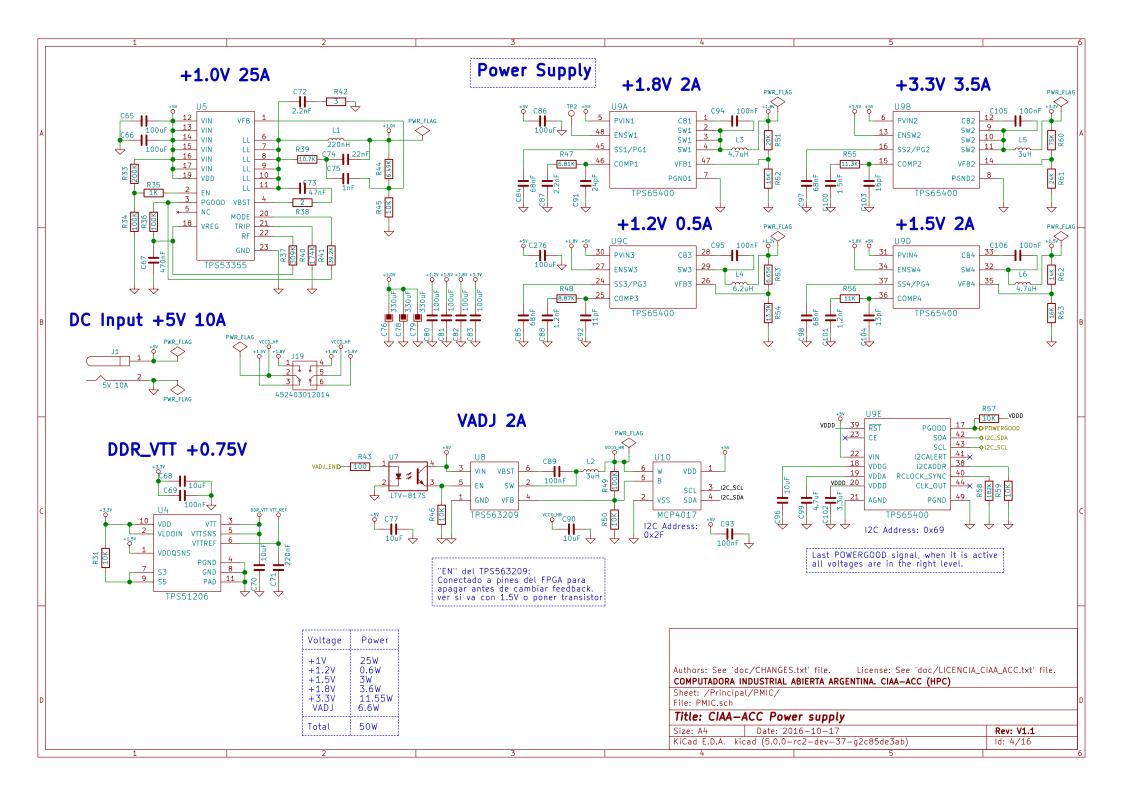
Title: CIAA-ACC Block Diagram

 Size: A4
 Date: 2016-10-17
 Rev: V1.1

 KiCad E.D.A. kicad (5.0.0-rc2-dev-37-g2c85de3ab)
 Id: 1/16



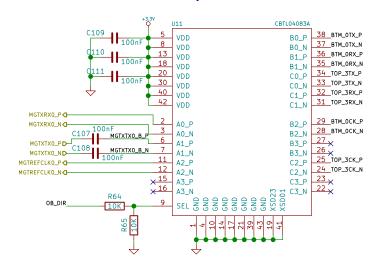


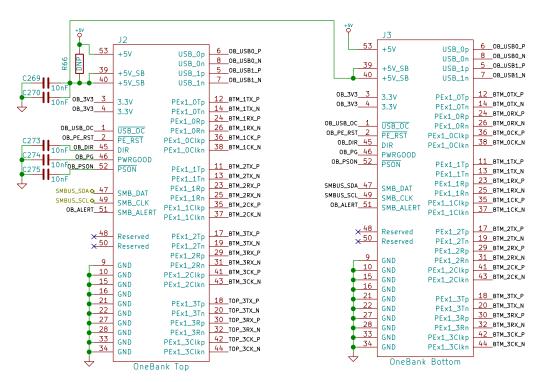


PCle/104 OneBank Connector

 $\begin{array}{ccc} & \text{H1} & \text{H3} \\ & \otimes & \otimes \\ & \text{H2} & \text{H4} \\ & \otimes & \otimes \\ & \text{Holes PCIe 104} \end{array}$

Mux/Demux Switch





PCIe OneBank device routing: Max. lenght: 4 inches Target Zo (diff): 85 Ohms +/- 15% Spacing between links: 20 mils Matching tolerance (intra-pair): 5 mils Matching tolerance (inter-pair): Not required

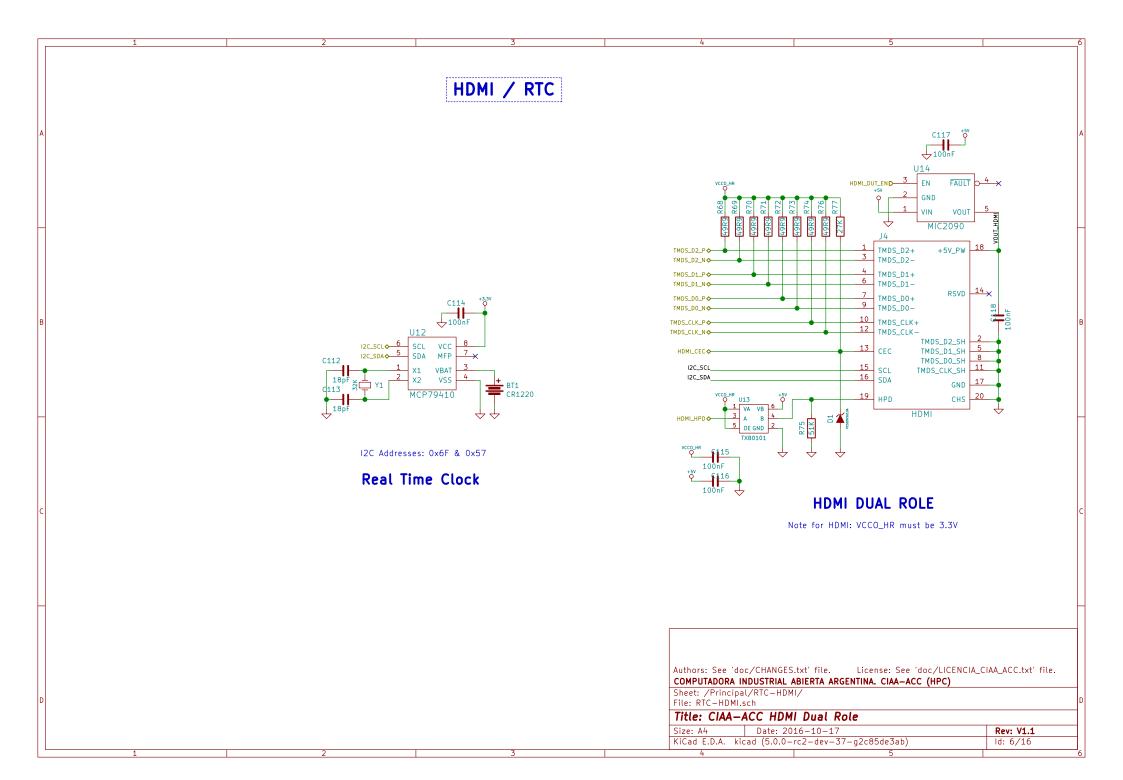
Authors: See 'doc/CHANGES.txt' file. License: See 'doc/LICENCIA_CIAA_ACC.txt' file.

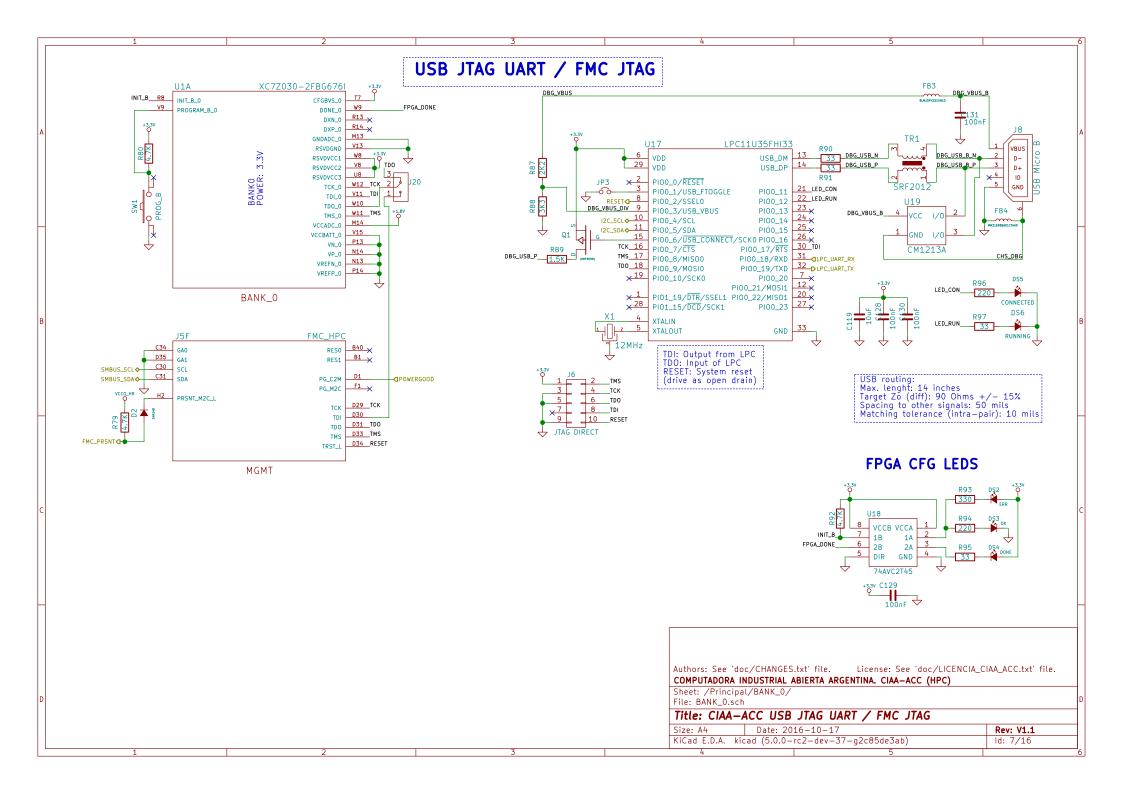
COMPUTADORA INDUSTRIAL ABIERTA ARGENTINA. CIAA-ACC (HPC)
Sheet: /Principal/OneBank/

File: OneBank.sch

Title: CIAA-ACC PCIe/104 OneBank Connector

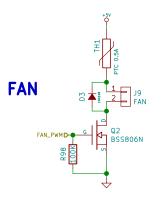
Size: A4	Date: 20	16-10-17	Rev: V1.1	7
KiCad E.D.A. kicad (5.0.0-rc2-dev-37-g2c85de3ab)		ld: 5/16	7	
4		5	•	-6

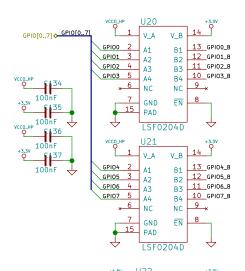


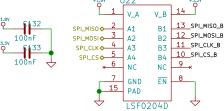


Expansion Header / FAN Connector

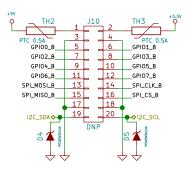
Voltage level translator







Expansion Header



GPIO Only available when VCCO_HP = 1.8V



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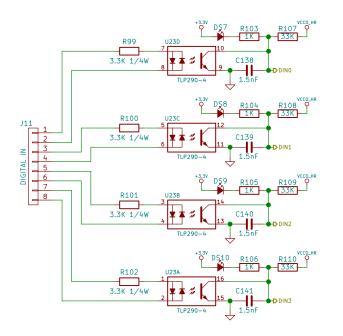
Sheet: /Principal/Expansion/

File: Expansion.sch

Title: CIAA-ACC Expansion Header (GPIO, SPI, I2C) / FAN Connector

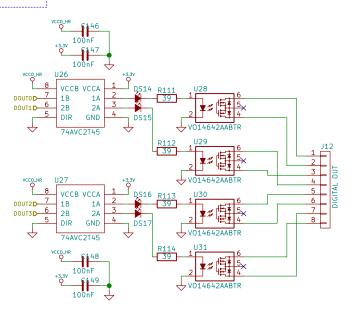
Size: A4	Date: 20	16-10-17	•	Rev: V1.1
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4		5		

Digital Inputs and Outputs



ISOLATED DIGITAL INPUTS

Range: 12 to 24 V



ISOLATED DIGITAL OUTPUTS

Range: up to 60 V

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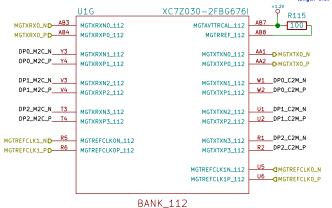
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Title: CIAA-A	ACC D	igital	Inputs	and	Outputs

Date: 2016-10-17 Rev: V1.1 KiCad E.D.A. kicad (5.0.0-rc2-dev-37-g2c85de3ab) ld: 9/16

PCIe / FMC Transceiver

MGTRREF must have matched length with MGTAVTTRCAL.





Coupling capacitor for transceivers must be in FMC mezzanine card.

PCIe routing: Target Zo (diff): 85 Ohms +/- 15% Spacing between links: 20 mils Matching tolerance (intra-pair): 5 mils Matching tolerance (inter-pair): Not required

TXRX

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Sheet: /Principal/BANK_112/ File: BANK_112.sch

Tite. BANK_IIZ.SCII

Title: CIAA-/	ACC FPG	A PCIe /	FMC transceiver

Size: A4	Date: 2016-10-17	Rev: V1.1
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· /ı	5	

