
VIVADO

# X-Tech

## Presented by Xilinx and Avnet

# OPTIMAL MEMORY INTERFACE DESIGN WITH XILINX 7 SERIES

XILINX
ALL PROGRAMMABLE

AVNET
electronics marketing

# MEMORY ARCHITECTURES & MAX DATA RATES

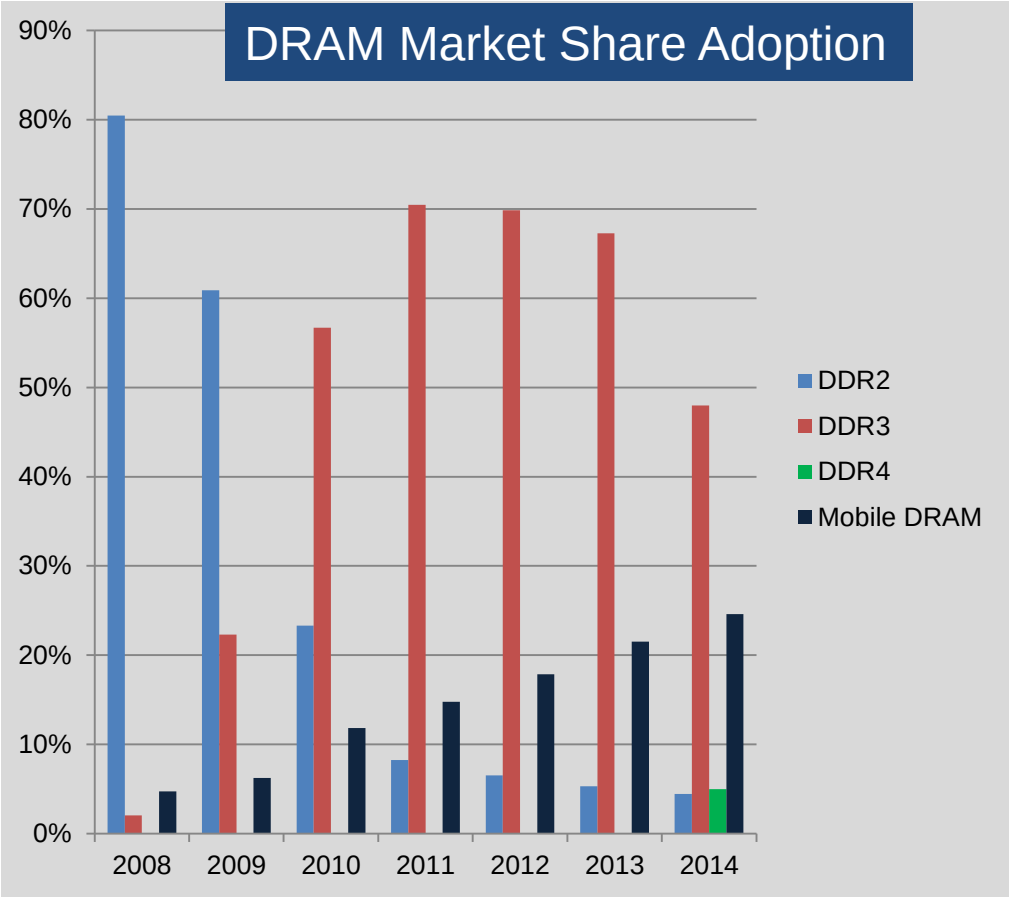
- 80% of FPGA designers use memory in their system
- 7 series supports a wide array of options
- Which one will you use?

| Memory Architectures | I/O Standard | Artix-7 (3.3V IO) | Kintex-7 (1.8V IO) | Virtex-7 (1.8V IO) |
|---|---|---|---|---|
| DDR2 | SSTL 1.8V | 400 MHz | 400 MHz | 400 MHz |
| DDR3<br>DDR3L | SSTL 1.5V<br>SSTL 1.35V | 533 MHz<br>400 MHz | 933 MHz<br>800 MHz | 933 MHz<br>800 MHz |
| RLDRAM2 | HSTL 1.5/1.8V | N/A | 533 MHz | 533 MHz |
| RLDRAM 3 | SSTL 1.2V | N/A | 800 MHz | 800 MHz |
| LPDDR2 | HSUL 1.2V | 333 MHz | 400 MHz | 400 MHz |
| DDR-II+ | HSTL 1.5/1.8V | N/A | 550 MHz | 550 MHz |
| QDR-II+ B2<br>QDR-II+ B4 | HSTL 1.5/1.8V | N/A | 333 MHz<br>550 MHz | 333 MHz<br>550 MHz |

Note: Memories may be able to perform faster than listed performance

# DRAM MARKET SEGMENTATION

- PC DRAM and Mobile Applications drive adoption
- DDR2 (1.8V)
  - Legacy designs with declining volumes
- DDR3 (1.5V)
  - High volume leader 2012-2014
- DDR4 introduction ~2014
- Mobile DRAM
  - Driven by the mobile phone market adoption of LPDDR2
  - DDR3L (1.35V) in some mobile apps.




Source: Industry Research

# COURSE OBJECTIVES

- Recognize trade-offs of different memory types
  - Cost
  - Density
  - Power
  - Bandwidth
  - Random transaction rate
  - Access latency
- Understand how to optimize the performance of your memory interface
- See design examples for DDR3, illustrating hardware development platforms and easy-to-use tools

# AGENDA

- DDR3 – Potential and Pitfalls
- Evaluating Memory Performance and Trade-offs
- Practical DDR3 design with 7 Series
- Next Steps

# AGENDA

- **DDR3 – Potential and Pitfalls**
- Evaluating Memory Performance and Trade-offs
- Practical DDR3 design with 7 Series
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# DDR3

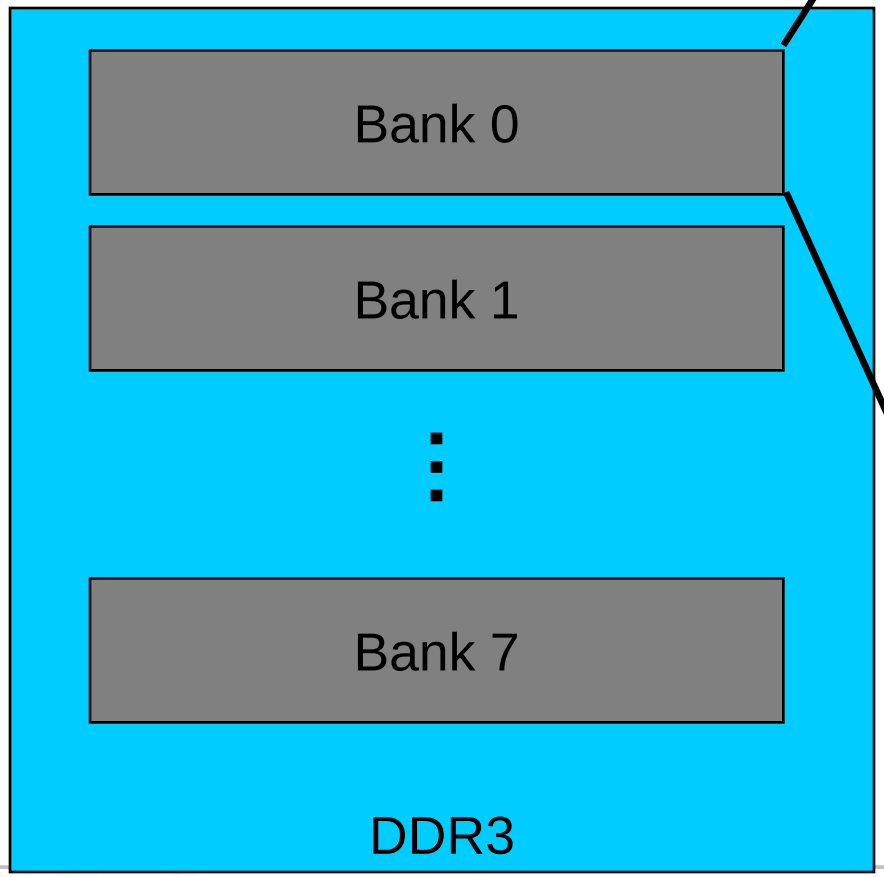
- DDR3 is commonly chosen because:
  - Lowest cost per memory bit
  - Largest density per chip
  - Fastest supported clock rates by Xilinx

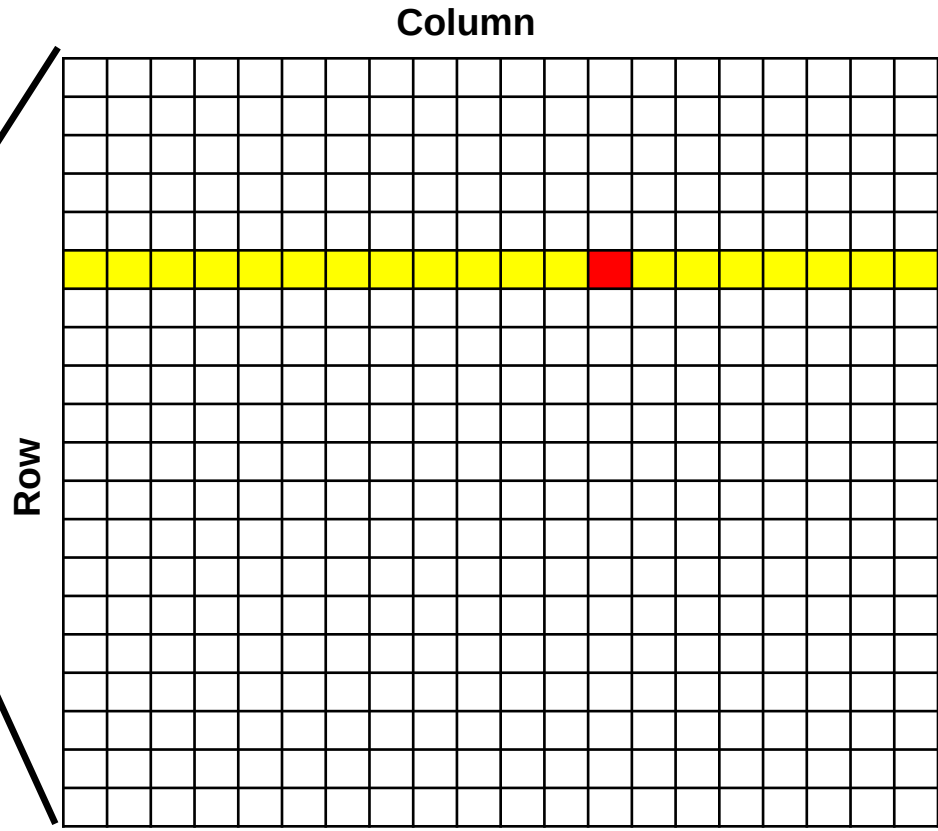

- Critical to understand
  - DDR3 operation and performance
  - DDR3 specs which limit performance
  - Options to improve performance
  - How to create the FPGA design

# DDR3 ARCHITECTURE

Organized as

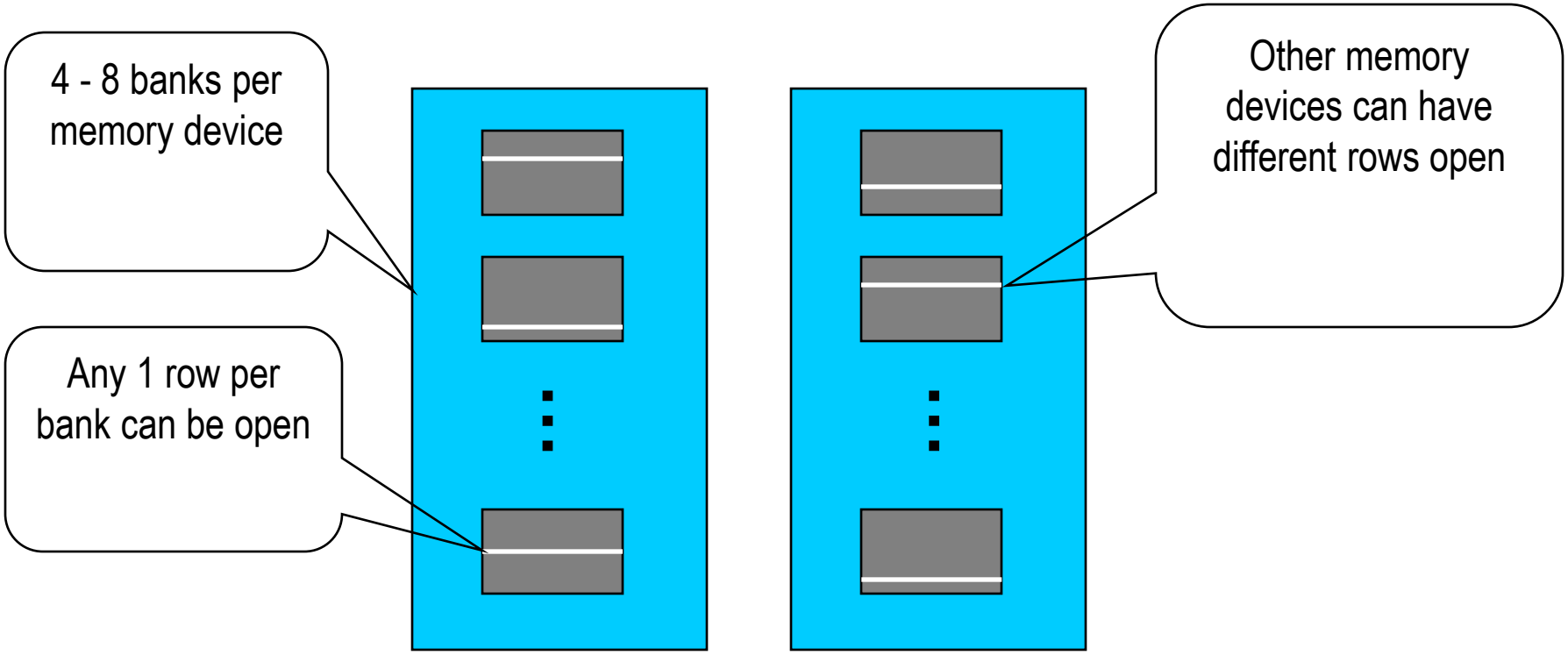
- **Banks**
- **Rows**
- **Columns**




- **Each needs addressing**
- **Addressing takes time**
- **Data must be refreshed**

# BANK MANAGEMENT




- Latency to open or close a row (tRC)
- Latency from one bank access to the next (tRRD)
- Latency after 4th bank before 5th can be opened (tFAW)
- Latency to move from read to write, and vice-versa

# DDR3 IDEAL BANDWIDTH

- Ideal Bandwidth = (Clock rate) * (DDR) * (data width)

- Example
  - Clock rate = 933 MHz (max supported by 7 series)
  - Runs double-data rate (x2)
    - 1866 Mbps *per bit data rate*
  - 16-bit wide data (x8 also supported)
  - Ideal Bandwidth = 1866 Mbps * 16 =

29.856 Gbps per DDR3!

- Real applications will not achieve this

# DDR3 BANDWIDTH REALITY CHECK

- Shared read and write interface
  - Read/Write or Write/Read transitions → penalty
- Row/column structure
  - New row access → penalty
- Cell architecture
  - Refresh → penalty

| x16, 933 MHz | % of Max | Bandwidth |
|---|---|---|
| Worst-Case | 1.1% | 330 Mbps |
| Best-Case | 90% | 26.5 Gbps |

*How fast will DDR3 run in your application?*

# AGENDA

- DDR3 – Potential and Pitfalls
- **Evaluating Memory Performance and Trade-offs**
- Practical DDR3 design with 7 Series
- Next Steps

# RANDOM TRANSACTION RATE (RTR)

- How often can you randomly address the memory to perform a transaction?
- Assumptions
  - Completely random address accesses
  - Could be either a read or a write
- Measured in Millions of Transactions per Second (MT/s)
- Does not account for data width
- Guaranteed random memory access bandwidth is

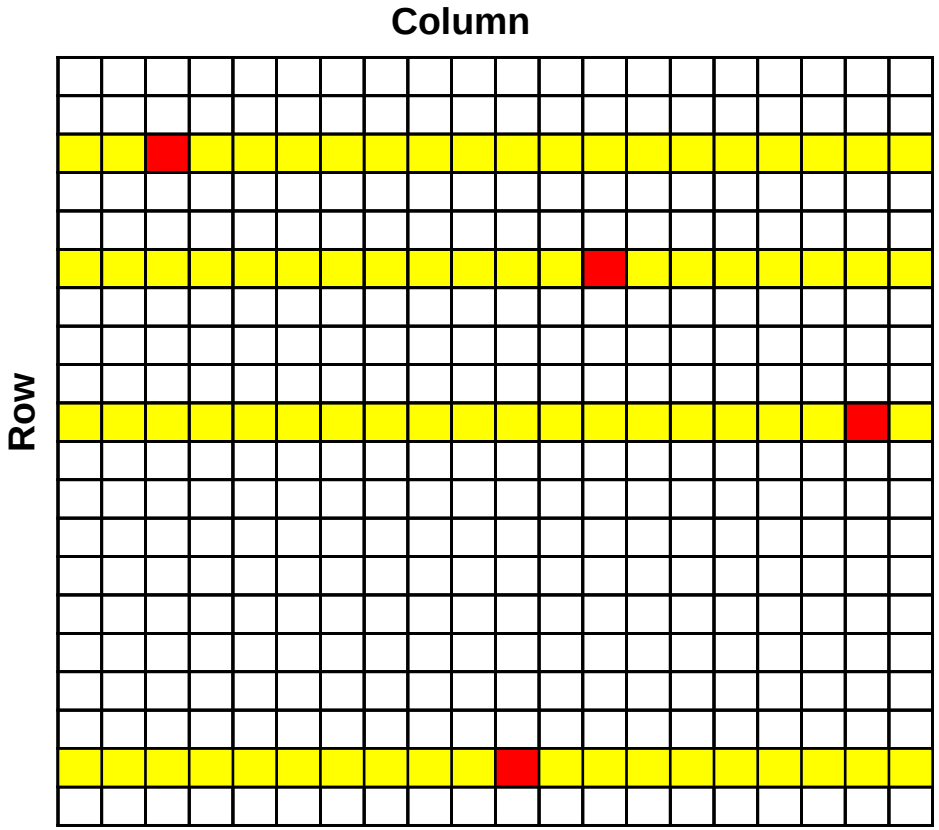
*Data Width * RTR*

# CALCULATING DDR3 RTR

- DDR3 has a penalty for switching between rows within a bank
- RTR calculations based on the Row Cycle Time: $T_{RC}$
  - Worst case parameter to access DDR3 in a completely random manner
- The DDR3 RTR formula is

$$RTR_{DDR3} = 1 / T_{RC}$$

- DDR3 typical $T_{RC}$ is 48ns
- ***$1/ T_{RC} = 1/48ns = 20.8$ MT/s***



# CALCULATING RLDRAM3 RTR

- 16 bank, DDR interface
- RTR calculations also based on the Row Cycle Time
- The RLDRAM3 RTR formula is

$$RTR_{RLDRAM3} = 1 / T_{RC}$$

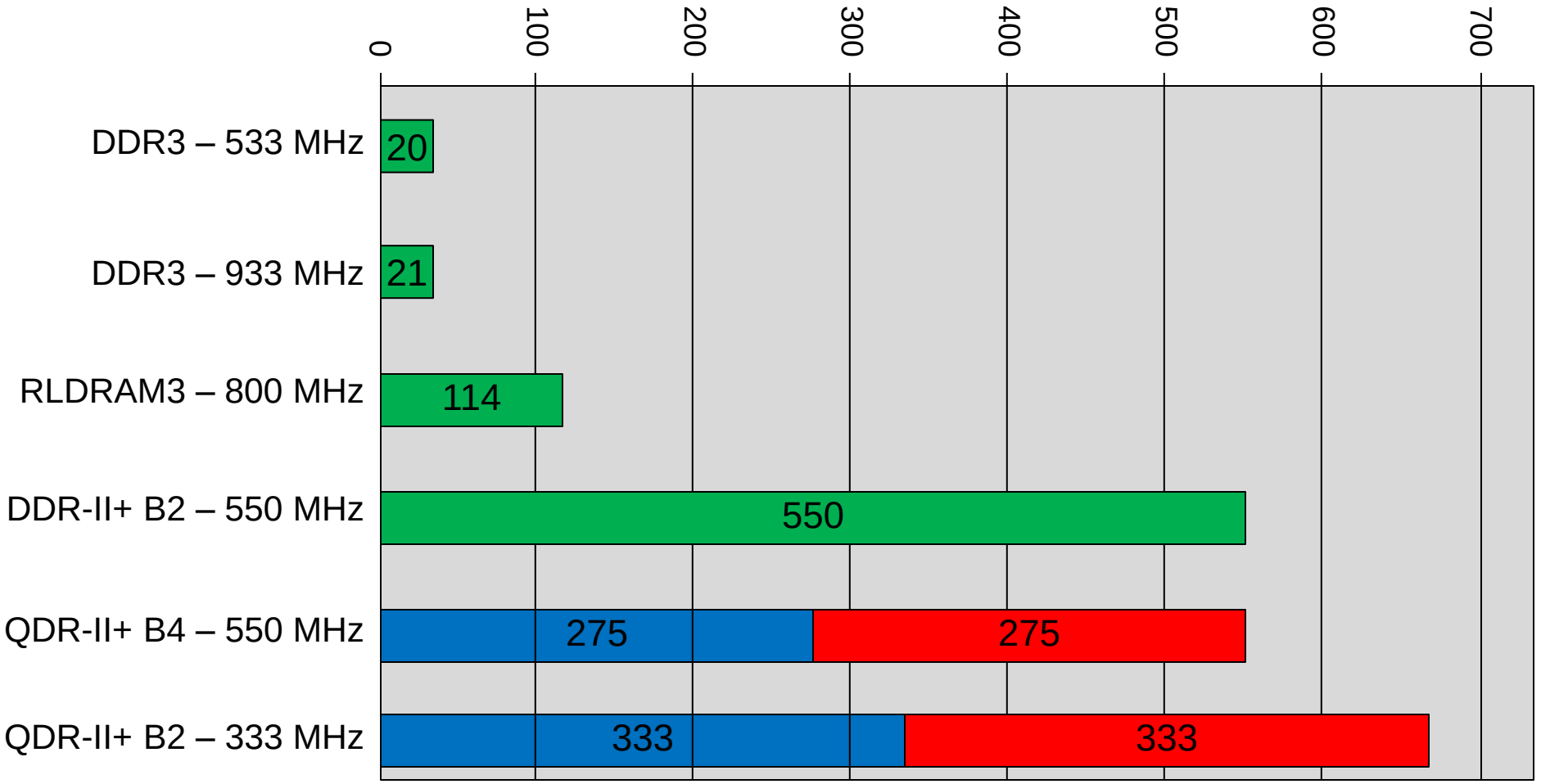
- For 800 MHz RLDRAM3, $T_{RC}$ is 8.8ns
- $1/ T_{RC} = 1/8.8ns = 114$ MT/s

# CALCULATING HIGH PERFORMANCE SRAM RTR

- No penalty for random access
- DDR-II+ SRAM
  - Single, shared bus
  - Burst of 2 (B2)
  - Maximum performance for imbalanced read/write applications
- QDR-II+ SRAM
  - Dedicated read and write busses
  - Burst of 2 (B2)
    - **Double address rate (DAR) – two addresses (1 read + 1 write) per clock**
    - Lower frequency but higher RTR
  - Burst of 4 (B4)
    - Single address rate (SAR) – one address per clock cycle
    - Higher clock rate and higher bandwidth

| SRAM Type | RTR Formula | RTR |
|---|---|---|
| DDR-II+ B2 @ 550 MHz | *RTR = FREQUENCY* | 550 MT/s R or W |
| QDR-II+ B4 @ 550 MHz | *RTR = FREQUENCY* | 550 MT/s R + W |
| QDR-II+ B2 @ 333 MHz | *RTR = FREQUENCY x 2* | 666 MT/s R + W |

# RANDOM TRANSACTION RATE



# MEMORY COMPARISON – PART 1

- Understand the nature of the data in your system
- Prioritize and weigh trade-offs

| Memory | Cost per Mbit | RTR* | Access Latency | Max Ideal Bandwidth on 7 series* | Max Density on 7 series* | Max Device Width |
|---|---|---|---|---|---|---|
| DDR3 | $0.0015 | 21 MT/s | 30-40 ns | 29.9 Gbps | 4 Gb | x16 |
| RLDRAM3 | $0.052 | 114 MT/s | 15 ns | 57.6 Gbps | 1 Gb | x36 |
| DDR-II+B2 | $0.90 | 550 MT/s | 4.5 ns | 39.6 Gbps | 144 Mb | x36 |
| QDR-II+ B2<br>QDR-II+ B4 | $0.90 | 666 MT/s<br>550 MT/s | 4.5 ns | 48.0 Gbps<br>79.2 Gbps | 144 Mb | x36 read<br>x36 write |

Single component, maximum supported 7 Series frequency, widest width

* Newer memories may be available but are not yet supported by Xilinx

# MEMORY COMPARISON – PART 2, POWER

## 1:1 READ-to-WRITE Operation

| Memory Type | Operating Voltage | Max Bandwidth | Actual Bandwidth | IDD | Power | mW per Gbps |
|---|---|---|---|---|---|---|
| DDR3 | 1.5V | 29.9 Gbps | 7.5 Gbps | 160 mA | 240 mW | 32 mW/Gbps |
| RLDRAM3 | 1.35V | 57.6 Gbps | 38.5 Gbps | 925 mA | 1248 mW | 32 mW/Gbps |
| QDR-II+ B4 | 1.8V | 79.2 Gbps | 79.2 Gbps | 1310 mA | 2350 mW | 30 mW/Gbps |

**RLDRAM3 Assumptions**

- Config = x36
- tCK = 1.25 ns (800 MHz)
- RL = 13 / WL = 14 clocks
- Continuous IDD1 Operation
- Burst Length = 2

**QDR-II+ SRAM Assumptions**

- Config = x36
- tCK = 1.8 ns (550 MHz)
- B4 device
- No other constraints

**DDR3 Assumptions**

- All banks already open (no activation current in calculation)
- No page misses (favorable assumption)
- Config = x16
- tCK = 1.07ns (933 MHz)
- tWTR = 7 clocks
- BL = BC4
- CL = 13 clocks ; CWL = 9 clocks
- 50% IDD4R / 50% IDD4W Operation
- Die Rev K

Note: Single device comparison is made with the widest configuration for each memory type

# MEMORY COMPARISON – PART 3, POWER

## 100% Random Reads (LUT) Operation

| Memory Type | Operating Voltage | Max Bandwidth | Actual Bandwidth | IDD | Power | mW per Gbps |
|---|---|---|---|---|---|---|
| DDR3 | 1.5V | 29.9 Gbps | 2.6 Gbps | 120 mA | 180 mW | 69.2 mW/Gbps |
| RLDRAM3 | 1.35V | 57.6 Gbps | 57.6 Gbps | 1895 mA | 2558 mW | 44.4 mW/Gbps |
| DDR-II+ B2 | 1.8V | 39.6 Gbps | 39.6 Gbps | 970 mA | 1746 mW | 44.1 mW/Gbps |

**RLDRAM3 Assumptions**

- **Config = x36**
- **tCK = 1.25 ns (800 MHz)**
- **Burst Length = 2**
- **Read Latency = 13 clocks**
- **Continuous IDD2R Operation**
- **8x data copies**
- **72 Mb effective density**

**DDR-II+ SRAM Assumptions**

- **144 Mb density**
- **Config = x36**
- **tCK = 1.8 ns (550 MHz)**

Note: A single device comparison is made with the widest configuration for each memory type

**DDR3 Assumptions**

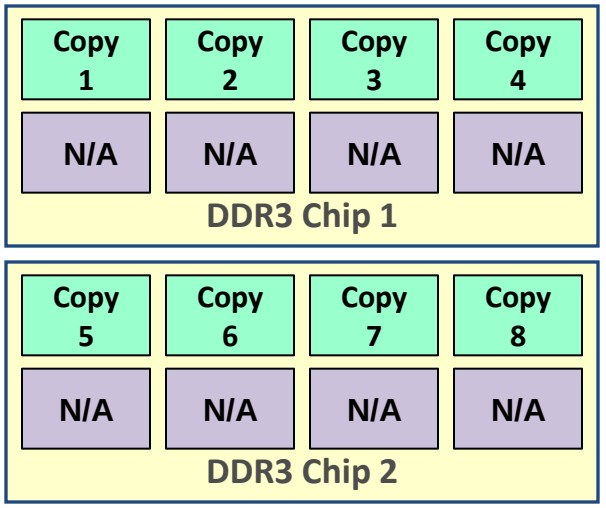
- **Config = x16**
- **tCK = 1.07ns (933 MHz)**
- **tRC = 48.91nS**
- **tRRD = 6 clocks**
- **tFAW = 35ns (33 clocks)**
- **CL = 13 clocks**
- **Continuous IDD1 Operation**
- **4x data copies**
- **512 Mb effective density**

# BALANCE PERFORMANCE AND TRADE-OFFS

- To achieve higher performance
  - Use higher performance (but more expensive) memory
  - Get more out of your DDR3
- Consider all trade-offs from a system perspective
  - Increasing number of components
    - Adds cost and design complexity
    - More memory controllers in FPGA
    - More pins on FPGA
  - PCB size and manufacturing complexity
  - Power and heat
  - Frequency of die shrinks

# GETTING MORE OUT OF YOUR DDR3

- Access data sequentially
- If data is random, close the row automatically
- Xilinx controller re-orders transactions
  - On by default
- Replicate data across banks (if transactions are predominantly read)
  - Can be done with 4 of 8 banks
  - Number of banks limited to 4 (see tFAW parameter)
  - Increases RTR by a factor of 4
  - Reduces density by a factor of 8
  - Queue transactions
    - DDR3 processes multiple activate commands simultaneously
    - 4 banks incur one tRC penalty
- Replicate data across chips



# EXAMPLE: 100 GIGABIT ETHERNET

- **Must handle 150 Million packets per second**
  - Up to eight 32-bit reads per packet
  - Need RTR of 1200 MT/s
  - 160 Mb worth of data
- ***Packet delivery must be guaranteed***
  - Must assume random addresses
  - Use RTR to evaluate options
- ***Calculate number of devices***

$$\frac{1200MT/s}{RTR \times (Replication\ Factor)} \times (I/O\ Width\ Factor)$$

| Technology | RTR | Replication Factor | I/O Width Factor | # of chips (RTR) | Actual # of chips | Density | Power (Core Only) | Chip Cost |
|---|---|---|---|---|---|---|---|---|
| DDR3, x16, 933 MHz | 21 | 4 | 2 | 28.6 | 32 | 4 Gb | 5.8 W | $96 |
| DDR-II+,B2, x36, 550 MHz | 550 | 1 | 1 | 2.2 | 3 | 216 Mb | 5.2 W | $195 |
| RLDRAM3, x36, 800 MHz | 114 | 8 (effective 7) | 1 | 1.5 | 2 | 288 Mb | 7.7 W | $120 |

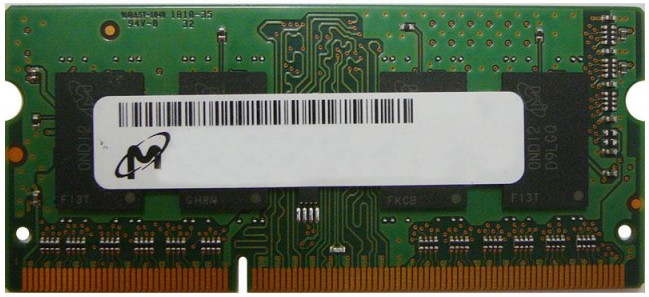
# EXAMPLE: 8 CAMERA SYSTEM

- Must handle 16 video streams
  - 8 transmitting, 8 receiving
  - 1920 x 1080 @ 75 Hz format
  - 32 data bits per pixel
  - 1 Frame = 66 Mbits
  - 16 streams × 66 Mb × 75 Hz
- Sustained bandwidth required is ~80 Gbps
- Data has a high sequential content
  - Line-by-line processing
  - Example: color correction

*Will DDR3 handle this?*

# EXAMPLE: 8 CAMERA SYSTEM

- Similar example created in Xilinx XAPP741
  - 64-bit DDR3 SODIMM @ 800 MHz on Xilinx KC705

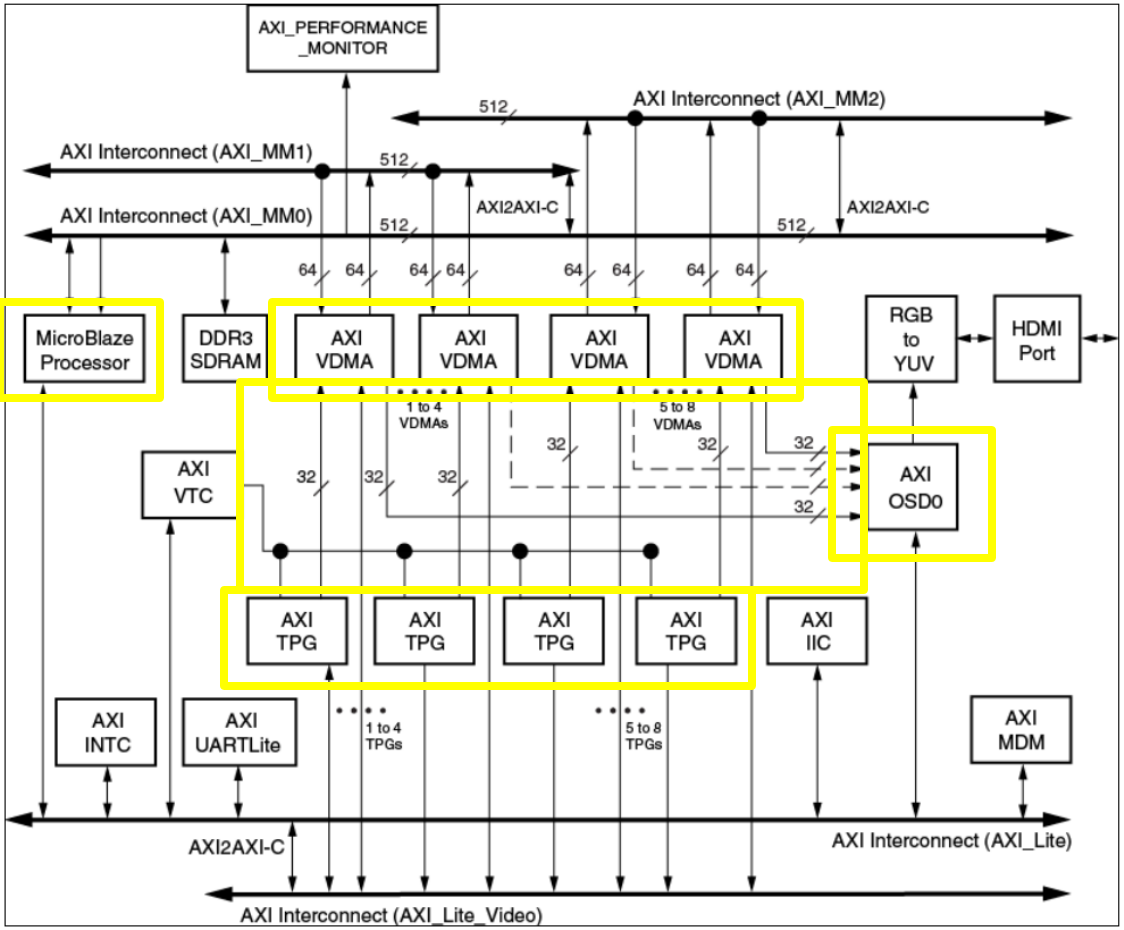


- Calculate DDR3 SODIMM performance potential
  - Worst-case is ~1.1 Gbps (totally random)
  - Best-case is ~92 Gbps (totally sequential)

- Conclusion: Data must be 90% sequential

# XAPP741 IMPLEMENTATION

- MicroBlaze-based design
- 16 video streams
- 8 AXI VDMA pipelines
- Video inputs generated by test pattern
- Outputs combined in OSD peripheral
- Built in EDK 13.4




*Actual Results = 79.8 Gbps or 77% of Theoretical Max*

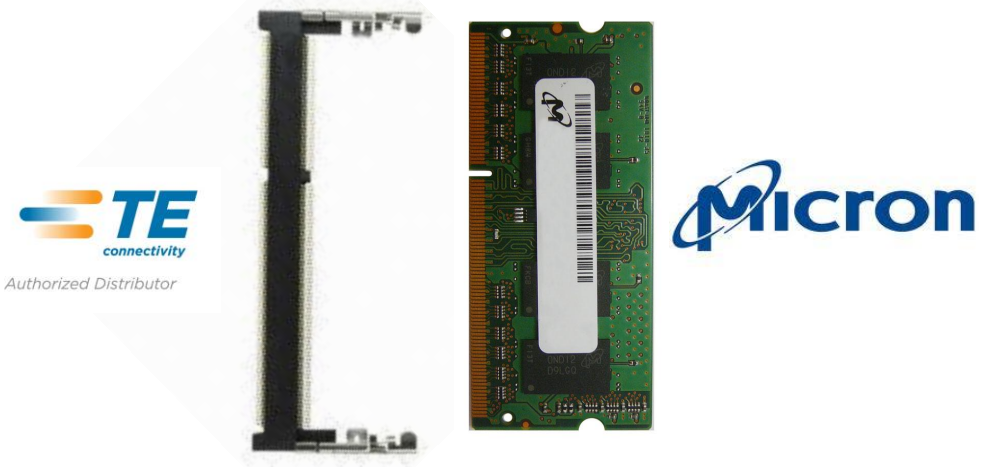
# CHOOSING THE MEMORY THAT BEST FITS

- What are the cost objectives?
  - DDR3 is lowest cost
- What density is required?
  - DRAM provides highest density
- How sequential is the data?
  - DDR3 does well with sequential accesses
- How often must the bus be turned-around?
  - QDR-II+ is ideal for read/modify/write scenarios

- Is guaranteed access time critical?
  - QDR-II+ has fast access time
- Is random addressing critical?
  - Use RTR to analyze access time requirement
  - Bank replication accelerates random reads for DRAM
  - SRAM has no random access penalty
- Is power critical?
  - Consider DDR3L or LPDDR2 for density
  - **Consider high performance memories for low mW per Gbps ratios**

# DDR3 IS A GOOD CHOICE IN MANY CASES

- Lowest cost per bit
- Largest density
- High sequential access bandwidth
- Modules
  - > On-DIMM termination
  - > Easy PCB design
  - > Upgradeable

# 7 SERIES DDR3 SUPPORT

## Device Support

| Component Width | Density | Max Interface Width | DIMMs | Rank | Voltage |
|---|---|---|---|---|---|
| x8, x16 | 1, 2, 4 Gb | 72 bit | UDIMM, RDIMM, SODIMM | Single and Dual (14.2) | 1.5V, 1.35V |

## Controller Features

| FPGA logic interface clock ratio | HDL | Bus | Re-order transactions |
|---|---|---|---|
| 2:1 (MemClk <400 MHz)<br>4:1 (MemClk >400 MHz) | Verilog, VHDL (14.1) | User, AXI | Yes (optional) |

# MICRON PRODUCT LONGEVITY PROGRAM (PLP)


Automotive


Industrial


Medical, Aerospace, Defense

- Targets markets requiring long life cycles
  - Automotive, industrial, medical, aerospace, and defense
- Ensures 10 years of support
  - DRAM, NOR, and NAND
- Provides stability
  - 2-year conversion timeline in the event of a die shrink

| | Product Family* | Density Range* | Temp Range* |
|---|---|---|---|
| DRAM | *DDR3 (MT41)* | 1–2Gb | IT, AT |
| | *DDR2 (MT47)* | 1–2Gb | IT, AT |
| | *DDR (MT46)* | 256–512Mb | IT, AT |
| | *SDRAM (MT48)* | 128–256Mb | IT, AT |

www.micron.com/support/plp

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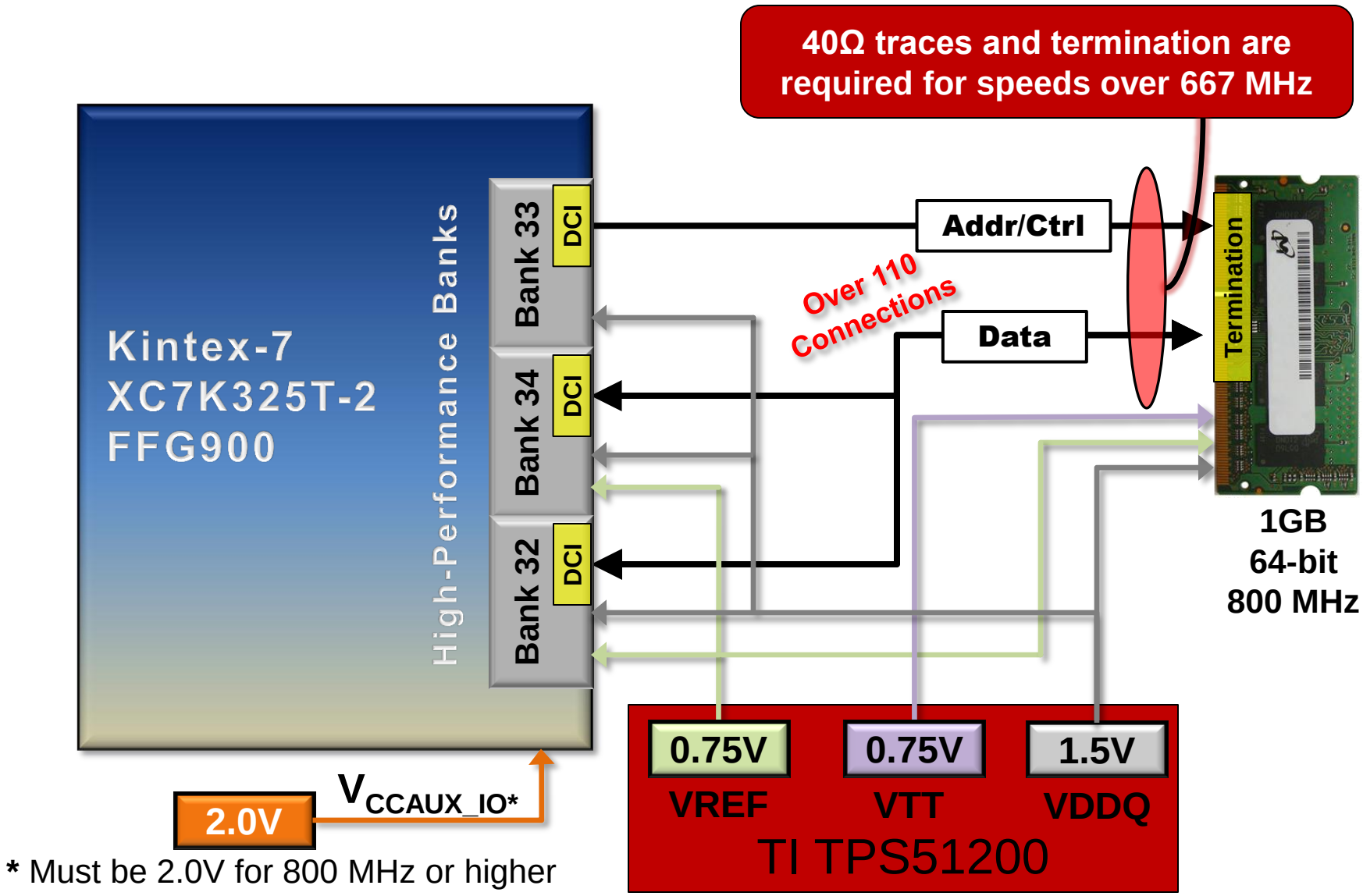
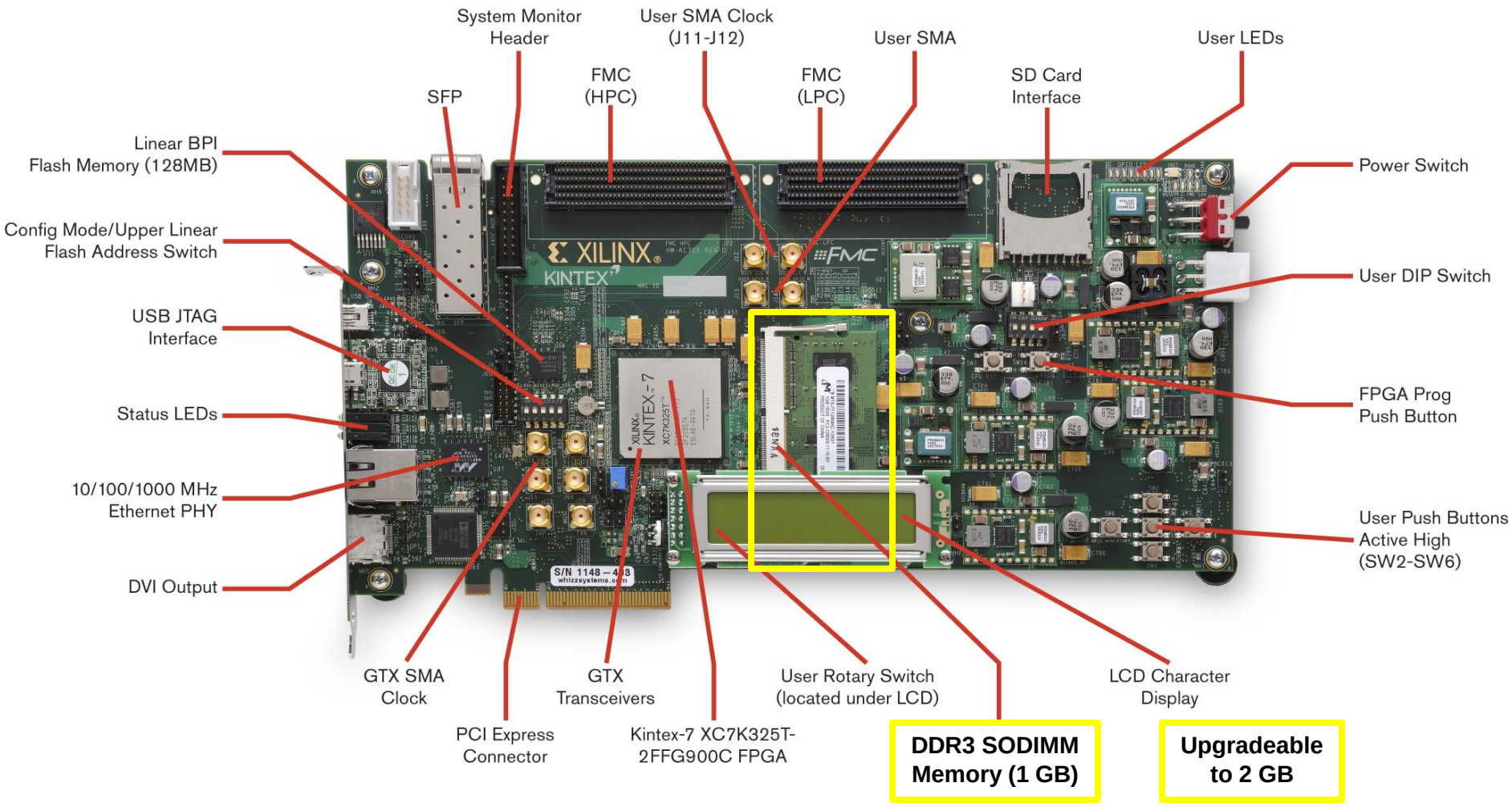
# KC705 DDR3 SODIMM INTERFACE DESIGN




* Must be 2.0V for 800 MHz or higher

# KC705 – FEATURE OVERVIEW



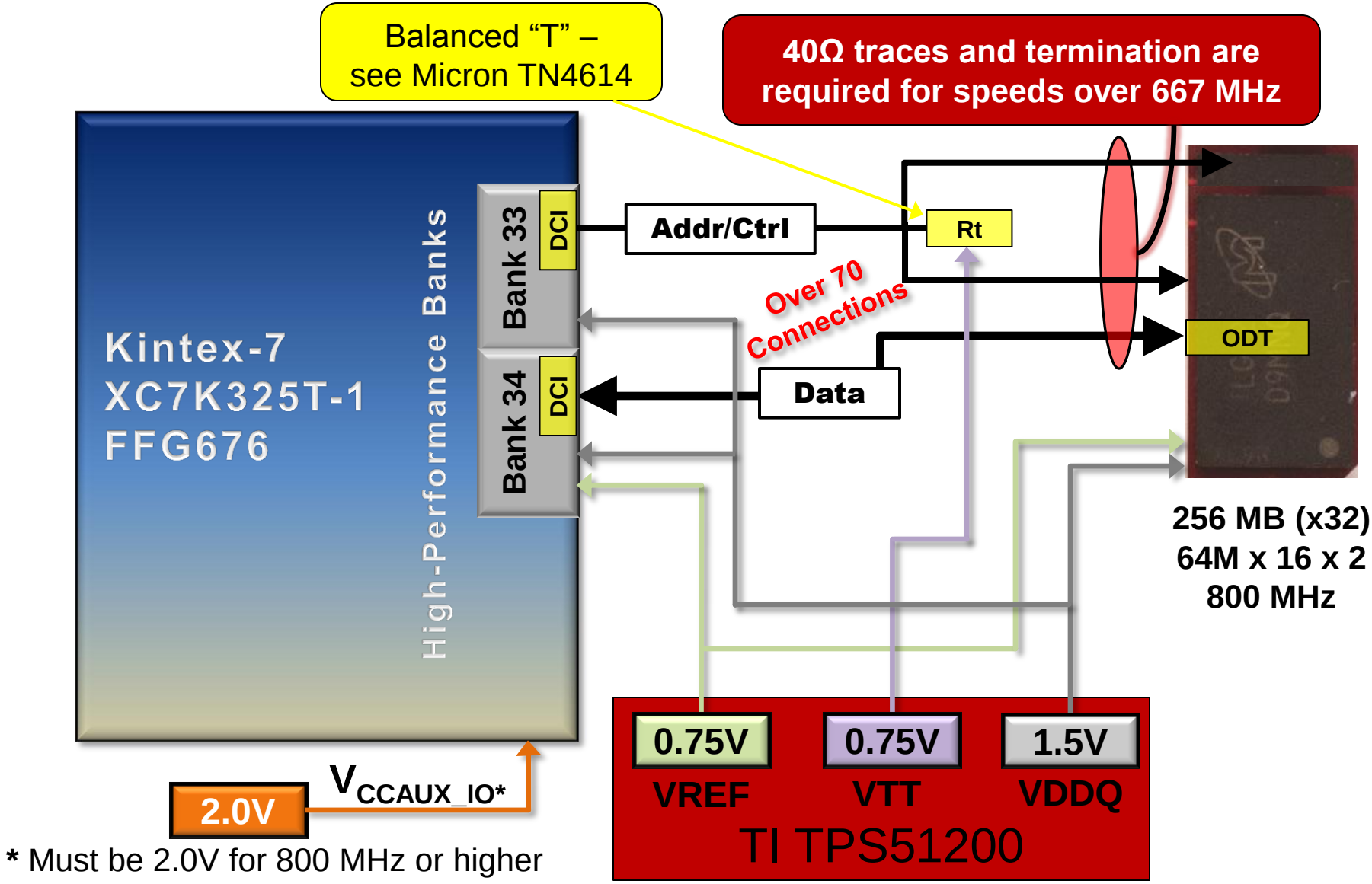
# KINTEX-7 FPGA KC705 EVALUATION KIT

- Hardware
  - KC705 evaluation board
  - AMS evaluation board
- Design Environment
  - Full seat ISE Design Suite Logic Edition
    - Device locked to the Kintex 325T
- Reference Designs
  - Full base reference and example designs and demos
    - Includes PCIe & ***DDR3 targeted reference design***
  - Board design files


www.xilinx.com/kc705

**Kintex-7 FPGA KC705 Evaluation Kit $1,695**

# K7-MMP DDR3 COMPONENT INTERFACE DESIGN

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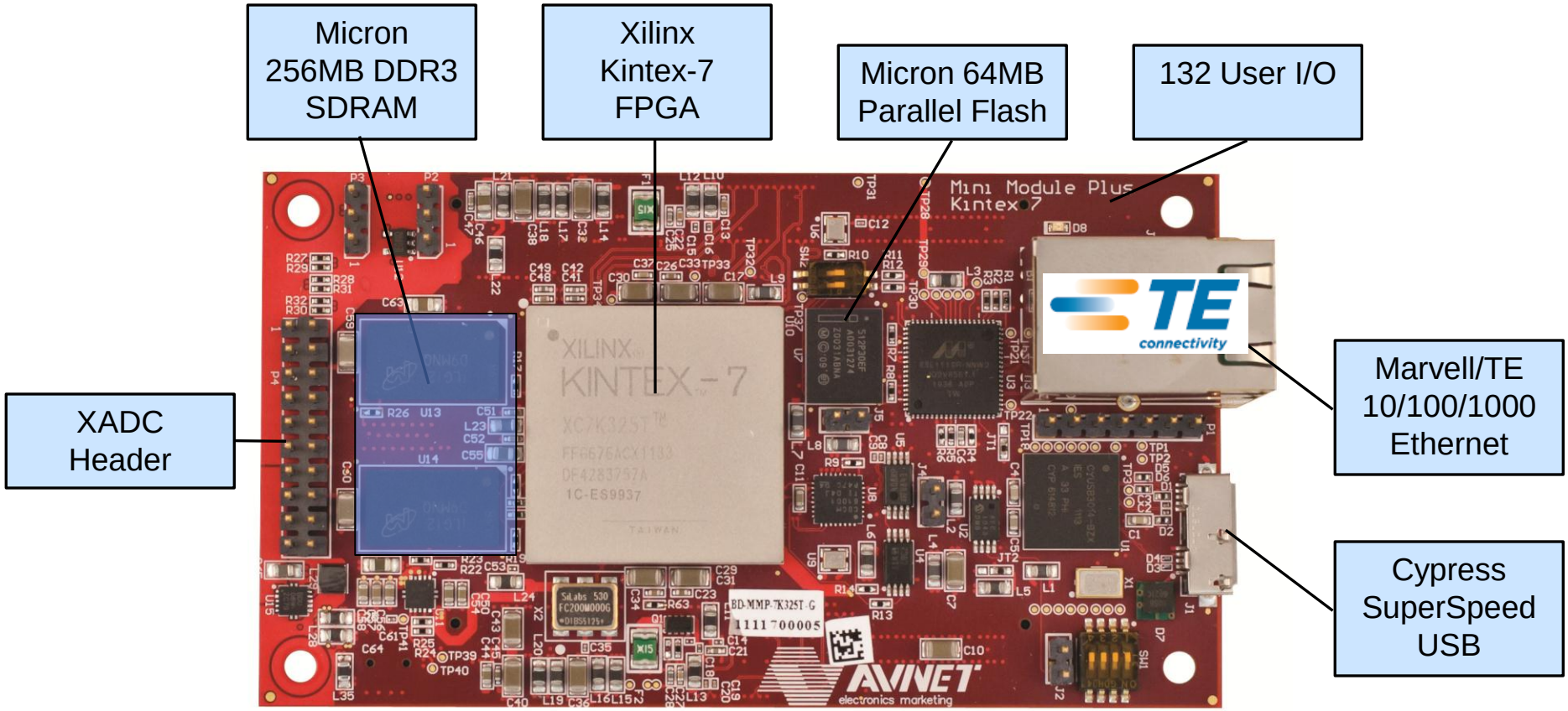
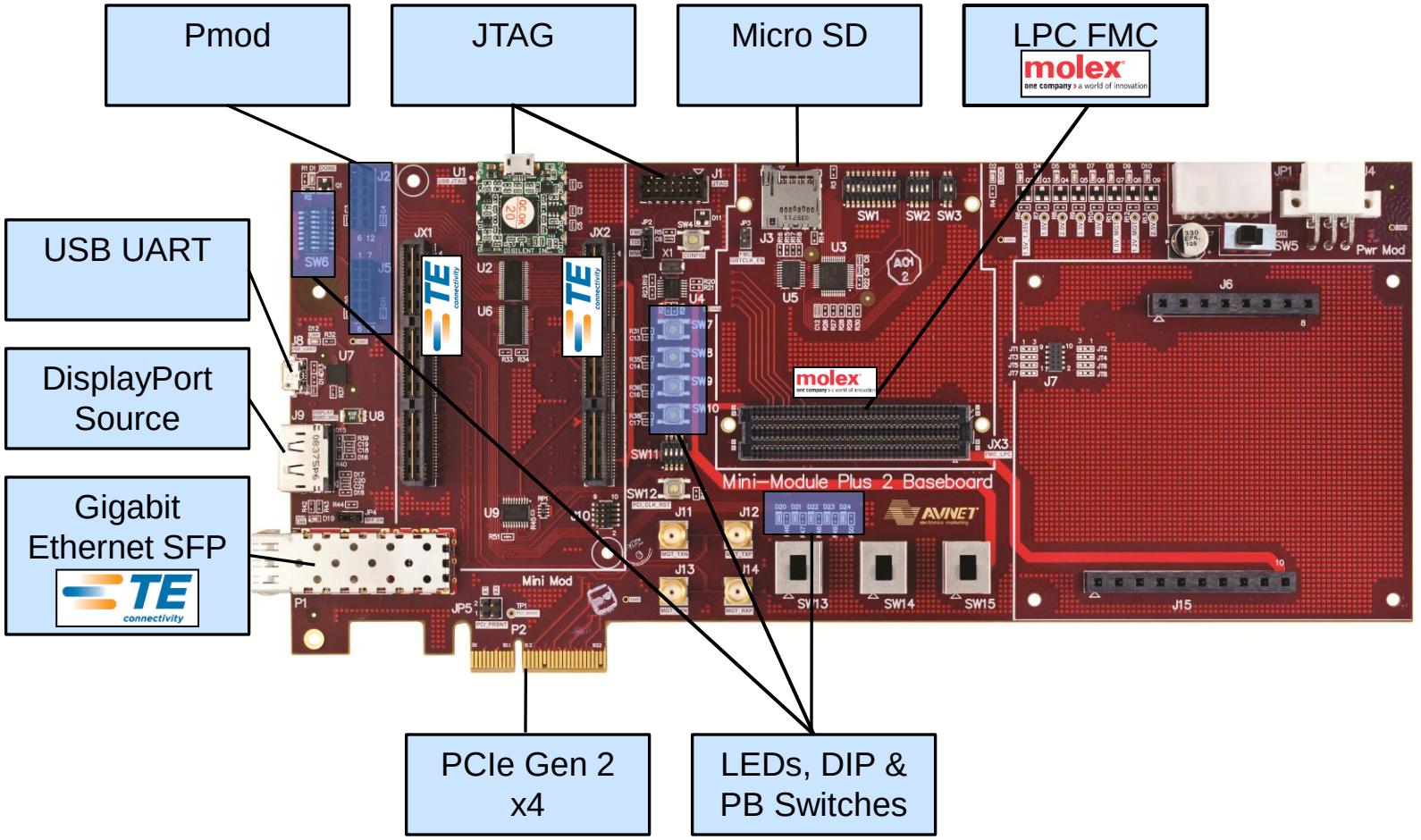
# K7-MMP FEATURES



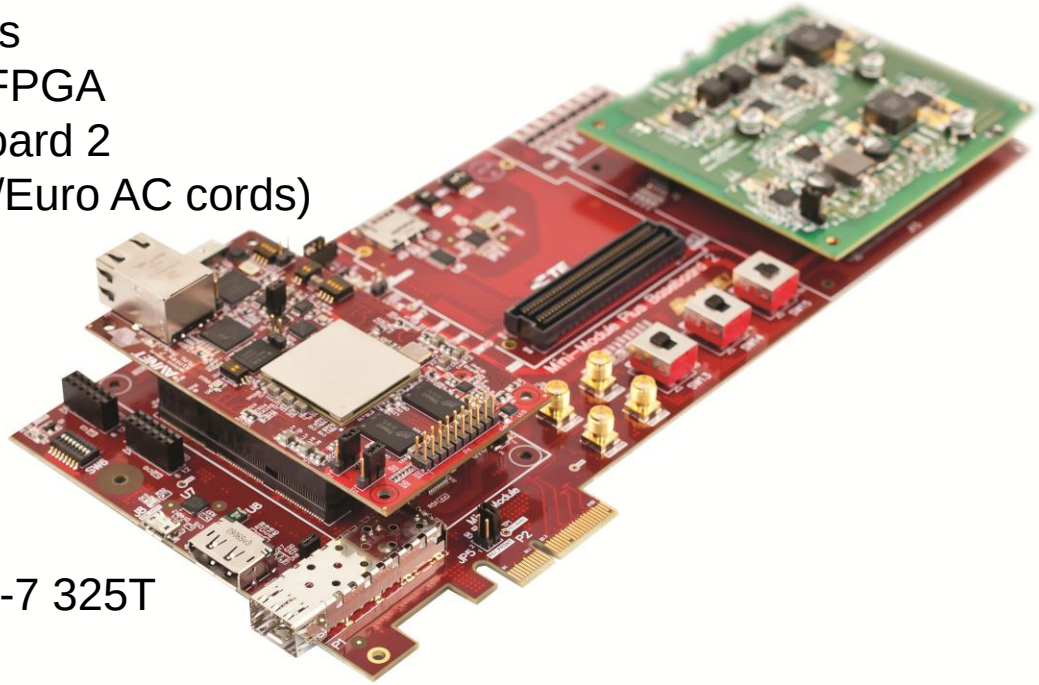

MMP = Mini-Module Plus

# MMP BASEBOARD 2 FEATURES



# WHAT IS INCLUDED IN THE K7-MMP KIT

- Hardware
  - Avnet Kintex-7 Mini Module Plus
    - Kintex-7 K325T-1FFG676 FPGA
  - Avnet Mini Module Plus Baseboard 2
    - 12V Power Supply (US/UK/Euro AC cords)
    - USB A-mini-B Cables (2)
    - Ethernet Cable
  - Power Module (user choice)



- Design Environment
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- Reference Designs
  - Full base reference and example designs and demos
    - Includes PCIe, MicroBlaze, Linux, and IBERT targeted reference design
  - Board design files

www.em.avnet.com/k7mmp

**Complete Kintex-7 MMP Kit $1,695**

# Pico Computing: M-Series Modules




## M-505

- Kintex-7 XC7K325T/K410T
- 4GB DDR3 SODIMM
- 128 MB NOR FLASH
- 34 LVDS
- 8 GTX Transceivers


## M-503

- Virtex-6 LX240T/LX365T/SX315T/ SX475T
- 2 x 4GB DDR3 SODIMM
- 3 x 9MB QDRII SRAM
- 80 LVDS
- x8 Gen2 PCIe Host Interface


## M-501

- Virtex-6 LX240T/LX365T/SX315T
- 512 MB DDR3
- x8 Gen2 PCIe Host Interface


## M-504

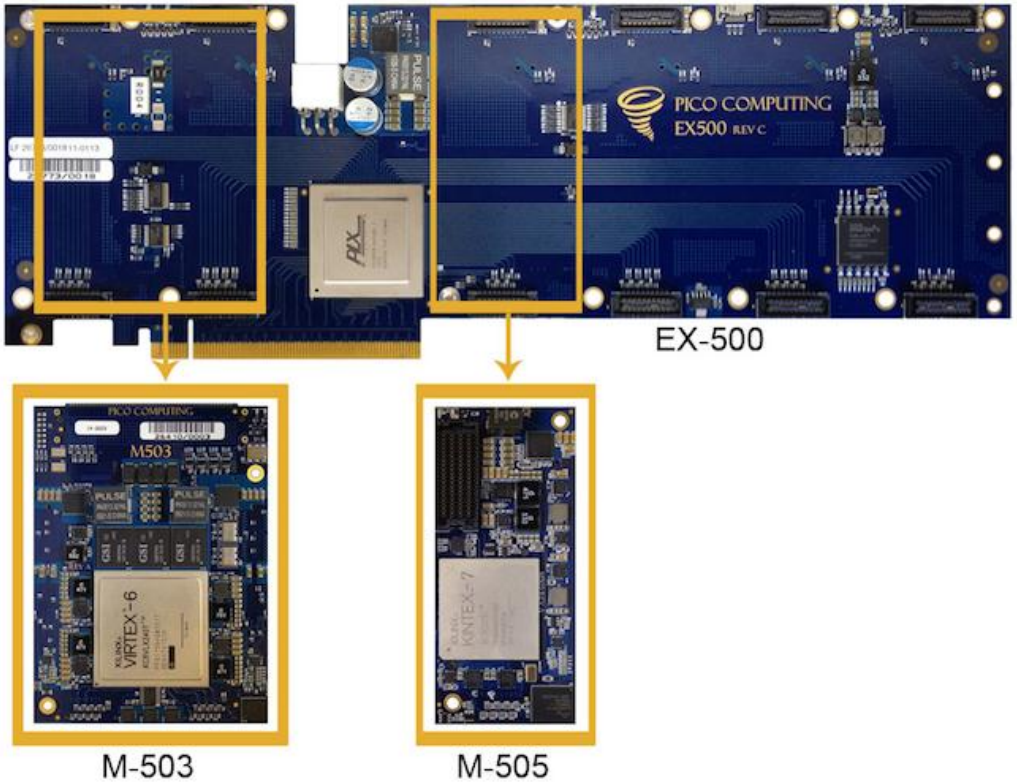
- Virtex-6 LX240T/LX365T/LX550T/ SX315T/SX475T
- 2 x 4GB DDR3 SODIMM
- 3 x 9MB QDRII SRAM
- 1GB Spansion Flash
- 63 LVDS
- 8GTX Transceivers
- X8 Gen2 PCIe Host Interface

# Pico Computing: EX-Series Backplanes




## EX-400

- Holds up to four M-Series Modules
- X16 Gen2 PCIe Interface to Host
- X8 Gen2 PCIe Interface to each M-Series Module




## EX-500

- Holds up to six M-Series Modules
- X16 Gen2 PCIe Interface to Host
- X8 Gen2 PCIe Interface to each M-Series Module

# DDR3 MEMORY MODULES & SOCKETS



| Form Factor | H x W (mm) | Number of Pins | Voltage(s) | Buffered/ Registrered | Bus Width(s) | JEDEC MO Number |
|---|---|---|---|---|---|---|
| Stardard DDR3 | 30 x 133.35 | 240 | 1.5V / 1.35V | Unbuffered or registered | x64/x72 | MO-269 |
| DDR3 Very Low Profile (VLP) | 18.75 x 133.35 | 240 | 1.5V / 1.35V | Unbuffered or registered | x64/x72 | MO-269 |
| DDR3 VLPx | 19.5 x 133.35 | 240 | 1.5V / 1.35V | Unbuffered or registered | x64/x72 | MO-269 |
| DDR3 SODIMM | 30 x 67.6 | 204 | 1.5V | Unbuffered | x64 | MO-268 |

TE connectivity

molex one company › a world of innovation

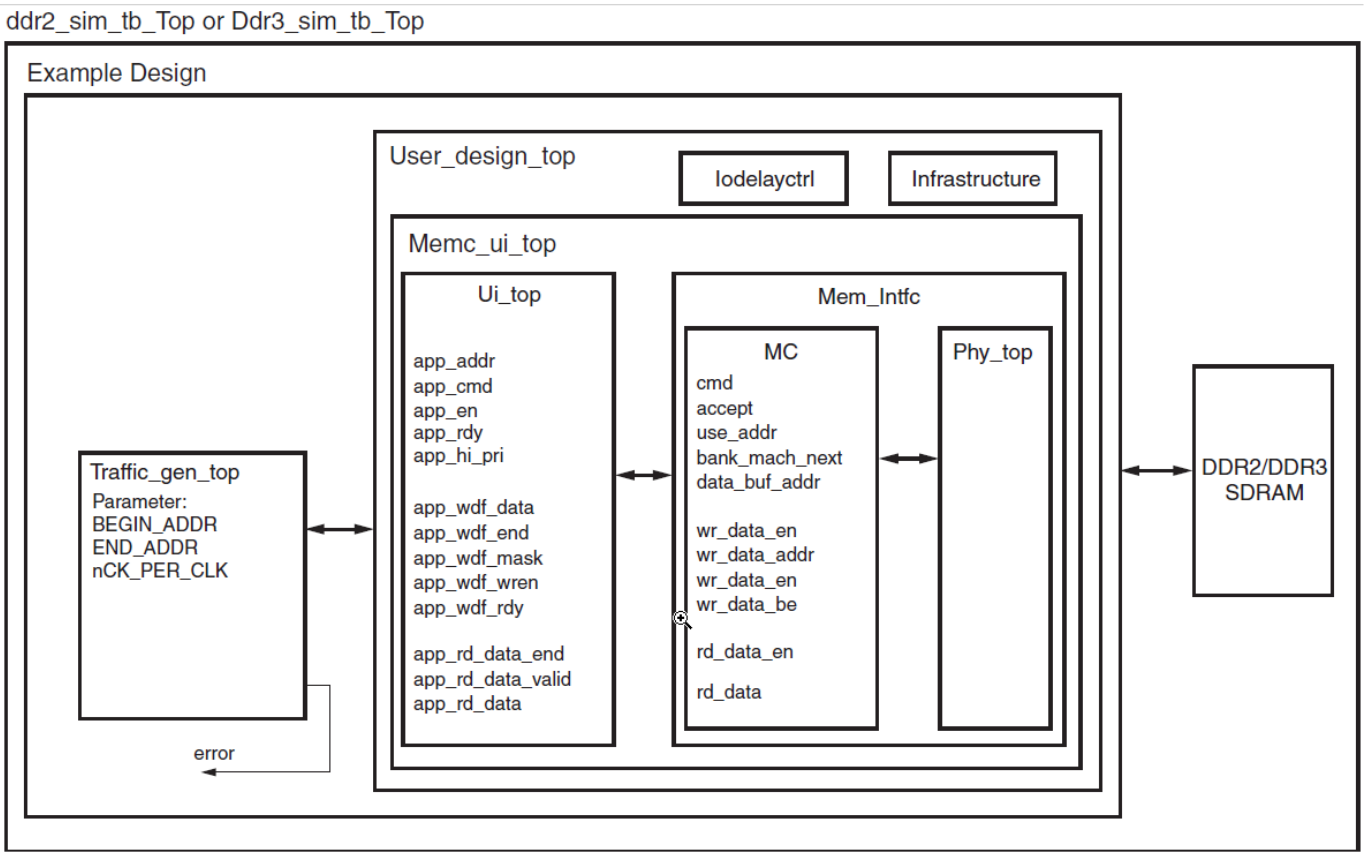
FCI

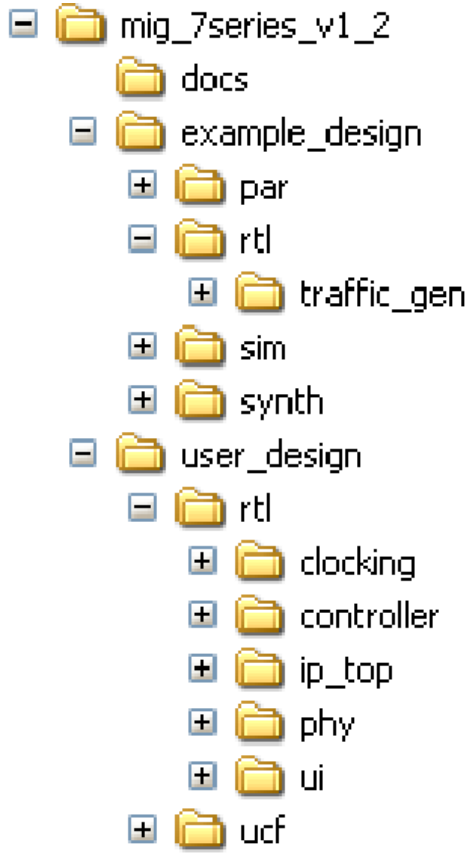
# GENERATING THE XILINX MIG DDR3 CONTROLLER

- Memory Interface Generator (MIG)
  - Launch from ISE/CORE Generator or
  - Launch from Vivado IP Catalog
  - Interface parameter selection
    - Device, burst length, data interleaving, re-ordering

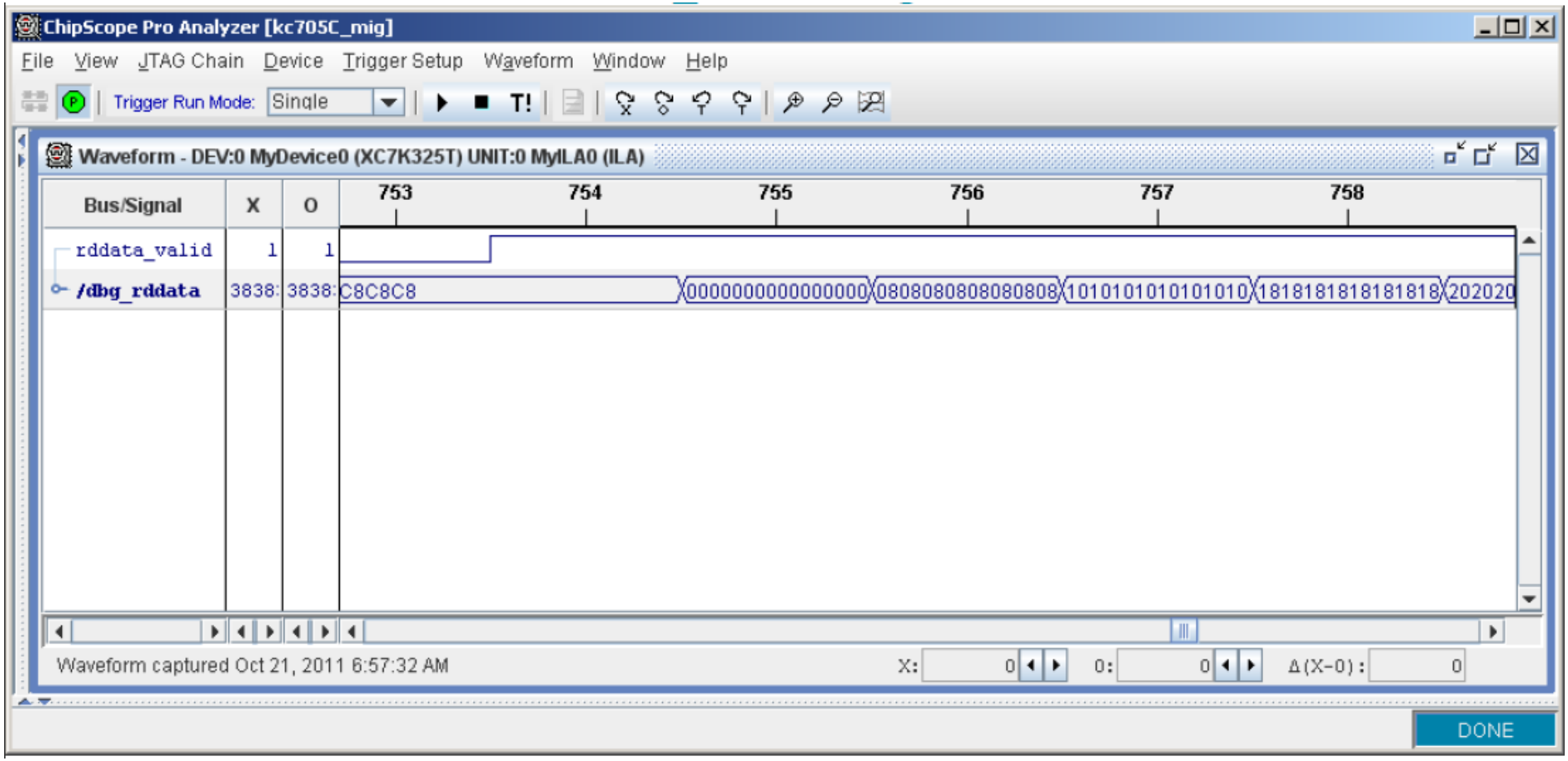
- Generated outputs
  - HDL Code: Verilog or VHDL
    - User interface: AXI or User
  - Simulation support
  - Build parameters
  - Example design
    - Simulate or synthesize


# MIG DEMO: VIVADO DESIGN FLOW



# EVALUATING MIG CONTROLLER IN CHIPSCOPE



# AGENDA

- DDR3 – Potential and Pitfalls
- Evaluating Memory Performance and Trade-offs
- Practical DDR3 design with 7 Series
- **Next Steps**

# NEXT STEPS – HIGH PERFORMANCE MEMORY

- View RLDRAM3 video demonstration online at www.avnetondemand.com
- Request Cypress white paper
  *MEMORY SUBSYSTEMS - THE MANY WORLDS*
  - Contact your local Avnet FAE
- To get information on Xilinx' validation platforms for RLDRAM3 or QDR-II+
  - Go to www.xilinx.com/support
  - Open a support case to request this information

# NEXT STEPS – DDR3

- View demonstrations
  - KC705 and K7-MMP X-fest exhibits (Xilinx and Avnet)
  - DDR3 video demonstration online at www.avnetondemand.com
- Memory Interface Generator
  - Follow the KC705 MIG Tutorial available on the web
- Purchase the K7-MMP or KC705
- Attend 2-day Xilinx training
  - *How to Design a High-Speed Memory Interface*

# NEXT STEPS

Evaluate trade-offs carefully!

Choose the best memory for your application


# THANK YOU
# PLEASE VISIT THE DEMO AREA

XILINX
ALL PROGRAMMABLE

AVNET
electronics marketing