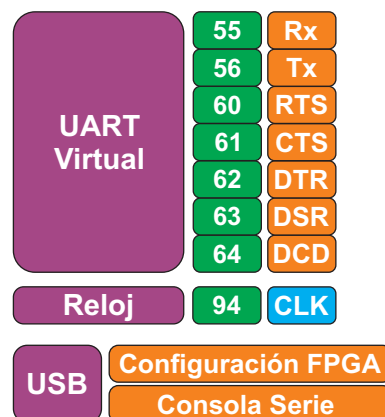
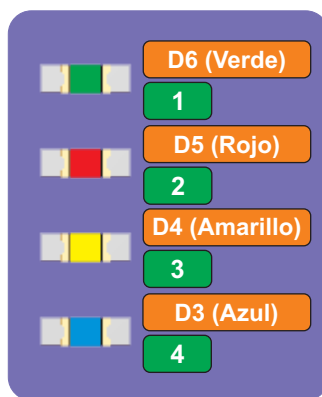
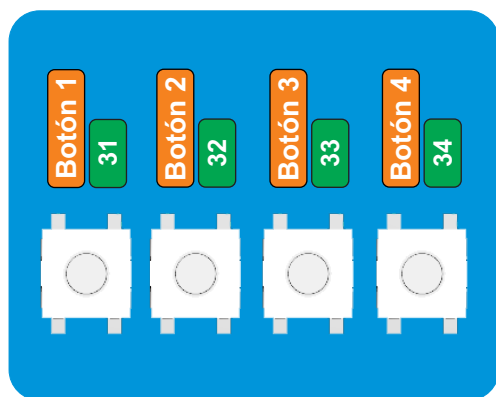
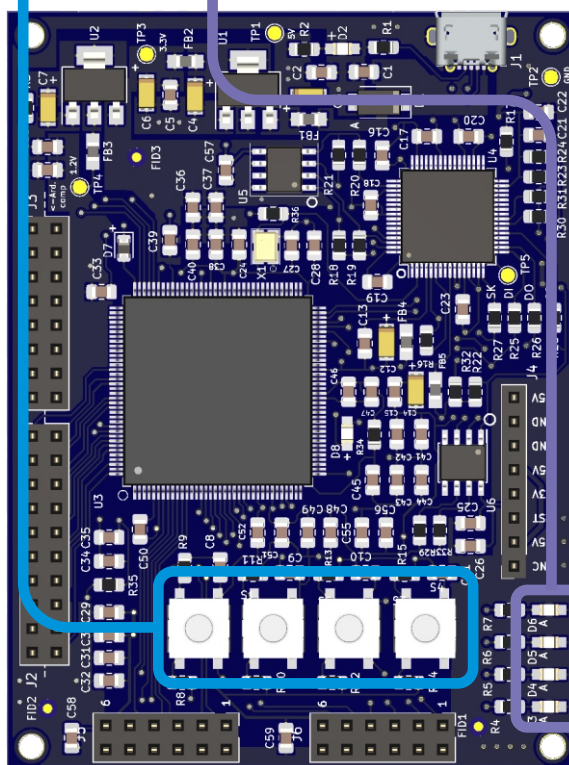


# Asignación de Pines



B1.21	107	1	•	2	106	B1.20
B1.19	105	3	•	4	104	B1.18
B1.17	99	5	•	6	98	B1.16
B1.15	97	7	•	8	96	B1.14
B1.13	95	9	•	10	85	B1.12
B1.11	84	11	•	12	83	B1.10
B1.9	89	13	•	14	81	B1.8
B1.7	80	15	•	16	79	B1.6

B0.1	122	1	•	2	124	B0.2
B0.3	125	3	•	4	128	B0.4
B0.5	129	5	•	6	130	B0.6
B0.7	134	7	•	8	135	B0.8
B0.9	136	9	•	10	137	B0.10
B0.11	138	11	•	12	139	B0.12
B0.13	141	13	•	14	GND	
B0.14	142	15	•	16	NC	
GND		17	•	18	143	B0.15
GND		19	•	20	144	B0.16



• 8	5V
• 7	GND
• 6	GND
• 5	5V
• 4	3.3V
• 3	37 RST
• 2	5V
• 1	NC

Alimentación
Masa
Pin FPGA
Port FPGA
Pin de Control
No Conectar
Descripción
Bloque Lógico

3.3V	GND	11	12	15	16
• 6	• 5	• 4	• 3	• 2	• 1
12	11	10	9	8	7
3.3V	GND	7	8	9	10
B3.1	B3.2	B3.3	B3.4	B3.5	B3.6
B3.7	B3.8				

3.3V	GND	21	22	23	24
• 6	• 5	• 4	• 3	• 2	• 1
12	11	10	9	8	7
3.3V	GND	17	18	19	20
B3.9	B3.10	B3.11	B3.12	B3.13	B3.14
B3.15	B3.16				