ID	Description	Actions to Take	Relevant Information	Status and Notes
1.1	**Xilinx Documentation**			
1.1.1	**Xilinx Documentation Navigator**			
	Are you using the Xilinx Documentation Navigator? Documentation Navigator provides an environment to view, search, and download Xilinx documentation and collateral. The environment can be filtered to quickly locate the desired information. Design Hubs are provided to quickly gather relevant information on specific design tasks.	The Documentation Navigator "DocNav" should be used to access all Xilinx documentation and collateral. The Documentation Navigator is installed with Vivado Design Suite.	UG949: UltraFast Design Methodology Guide for the Vivado Design Suite > Using the Documentation Navigator	
1.1.2	**Design Hubs**			
	Have you explored Design Hubs in Documentation Navigator?	Invoke Documentation Navigator and select the Design Hub View tab. Explore the various information made available with each one.	UG949: UltraFast Design Methodology Guide for the Vivado Design Suite > Using the Documentation Navigator	
	Do you know where to find the documentation for the cores and peripherals used in the Zynq Processing System?	Check Section A.3.8 of the Zynq-7000 AP SoC Technical Reference Manual (UG585) for a complete list of ARM documentations available.	UG585: Zynq-7000 All Programmable SoC Technical Reference Manual > Third-Party IP and Standards Documents	
1.1.3	**QuickTake Video and Software Tutorials, User Guides**			
	Have you explored the available Hardware training collateral? There are tutorials aimed at quickly bringing users up to speed with the Vivado Design Suite Development Tools. The Vivado User Guides provide detailed information about using the various features of the Vivado Design Suite.		UG898: Vivado Design Suite User Guide: Embedded Processor Hardware Design UG940: Vivado Design Suite Tutorial: Embedded Processor Hardware Design	
	Have you explored the available Software training collateral? There are a whole host of tutorials aimed at quickly bringing users up to speed with the SDK Development Tools.	There are five SDK tutorials: - How to Create a Board Support Package (BSP) - How to Create a New Software Application - How to Debug a Software Application - How to Profile a Software Application - How to Run a Software Application	SDK Tutorials	
	Have you watched the available Vivado Video Tutorials?	The following Vivado Videos are available: - Targeting Zynq Using Vivado IP Integrator - Designing with Vivado IP Integrator - Vivado Design Flows Overview	Xilinx.com > QuickTake landing page	
1.1.4	**Device and IP Notifications**			
	Have you subscribed to appropriate Design Advisories? Have you read all Customer Notices, Errata, and Answer Records related to the target device and IP? Have you subscribed to the appropriate Xilinx Technical Forums?	Get the latest information about the device and IP you are using in the design. Participate in the technical forums to seek help and to review past user experiences.	Zynq Solution Center	
	Have you submitted any web cases for your design project yet? If so, have you included the project name in any web cases you have submitted?	This allows you and Xilinx to search web cases by project name.	Xilinx.com > Support	
1.2	**Xilinx Training**			
1.2.1	**Xilinx Training Classes**			
	Are you and your team proficient with the Vivado Design Suite? Have you investigated the latest Vivado Training offerings? The Vivado Design Suite has evolved into a premier design environment with a lot of capabilities and user options. Proper training can ensure the design team quickly becomes efficient with the Vivado tools.	Attend a regularly scheduled Xilinx training class or request an onsite class. Perform Web-based online training classes.	Xilinx.com > Support - Training	
1.2.2	**Training - System Design**			
	Are the engineers familiar with the Zynq architecture?	Take the introduction to Zynq architecture class.	Xilinx Training Course: Introduction to Zynq Architecture	
	Are the engineers familiar with the Cortex-A9 MPCore?	Read the ARM Cortex-A Series Programmer's Guide.	ARM Cortex-A Series Programmer's Guide	
	Are the engineers familiar with ARM's AXI interface?	Read the AMBA AXI Specification.	ARM AMBA AXI Specification	
	Are the engineers familiar with Vivado IP Integrator?	Take the Embedded Systems Design class.	Xilinx Training Course: Embedded Systems Design	
	Are the engineers familiar with Vivado HLS?	Take the High-Level Synthesis with the Vivado HLS Tool class.	Xilinx Training Course: High-Level Synthesis with the Vivado HLS Tool	

ID	Description	Actions to Take	Relevant Information	Status and Notes
1.2.3	**Training - Software Design**			
	Are the engineers familiar with Zynq software development?	Take the Embedded Systems Software Design class	Xilinx Training Course: Embedded Systems Software Design	
	If using Linux, are the engineers familiar with PetaLinux?	Take the Embedded Design with PetaLinux Tools class	Xilinx Training Course: Embedded Design with PetaLinux Tools	
	Are the engineers familiar with the OS/RTOS chosen?	Check if the vendor offers training.	Vendor specific.	

ID	Description	Actions to Take	Relevant Information	Status and Notes
2.1	**Boot Device**			
2.1.1	**Flash Devices**			
	Which Flash device will be used for boot?	Choose between QSPI (single or Dual), NAND (ONFI 1.0), NOR, or SD	UG585: Zynq-7000 All Programmable SoC Technical Reference Manual > Quad SPI Boot NAND Boot NOR Boot SD Card Boot	
2.1.2	**Boot Requirements**		UG585: Zynq-7000 All Programmable SoC Technical Reference Manual > Boot and Configuration	
	How much space will be needed to store the boot images?	Choose the boot device based on density needs.	Answer Record 50991	
	Is there a boot time requirement?	Check the typical boot times based on the device type.	Answer Record 55572	
	Is the chosen device supported by the Xilinx tools?	Review AR 50991 to ensure the device selected will be supported by the Xilinx tools.	Answer Record 50991	
2.1.3	**Boot Device Connections and Settings**			
	Boot Device MIO connections	Review Peripheral and MIO selection guidelines for the boot device.	UG585: Zynq-7000 All Programmable SoC Technical Reference Manual > Quad SPI Boot NAND Boot NOR Boot SD Card Boot	
	Do you need eMMC support?	eMMC can be used as a secondary boot device. Review the eMMC guidelines from AR59999.	Answer Record 59999	
	Boot Mode settings	Consider providing the ability to easily switch the boot mode to JTAG.	UG585: Zynq-7000 All Programmable SoC Technical Reference Manual > Boot Mode Pin Settings	
	Do you plan on using QSPI devices > 16MB?	Extra circuitry might be required when using memory device's extended address register.	Answer Record 57744	
	Will the QSPI devices run > 40 MHz?	Plan on using the Feedback clock (MIO 8 pin).	UG585: Zynq-7000 All Programmable SoC Technical Reference Manual > Quad-SPI Flash Controller > Clocks	
	Are you using the XC7Z010 CLG225 Device?	The device does not support boot from SD or NOR.	UG585: Zynq-7000 All Programmable SoC Technical Reference Manual > MIO Pin Assignment Considerations	
2.2	**Secure Boot**			
2.2.1	**Authentication**			
	Is RSA authentication needed?	Become familiar with the RSA flow.	UG585: Zynq-7000 All Programmable SoC Technical Reference Manual > Device Secure Boot XAPP1175: Secure Boot of Zynq-7000 All Programmable SoC	
	Is AES/SHA encryption and authentication needed?	Become familiar with the AES/SHA flow.	UG585: Zynq-7000 All Programmable SoC Technical Reference Manual > Device Secure Boot XAPP1175: Secure Boot of Zynq-7000 All Programmable SoC	
2.2.2	**Storage**			
	Which key storage will be used; eFuse or BBRAM?	Understand the key programming flow for development and production.	UG821: Zynq-7000 All Programmable SoC Software Developers Guide > LibXil Skey for Zynq-7000 AP SoC Devices XAPP1175: Secure Boot of Zynq-7000 All Programmable SoC	
	What eFUSE settings will be used?	Select the features provided through the PL and PS eFuses.	UG585: Zynq-7000 All Programmable SoC Technical Reference Manual > eFuse Settings	
2.3	**Boot Stages**			
2.3.1	**Boot Stages**			

ID	Description	Actions to Take	Relevant Information	Status and Notes
	Will you be using an additional boot loader?	Review the Zynq boot stages and FSBL support. Review U-Boot support.	UG821: Zynq-7000 All Programmable SoC Software Developers Guide > U-Boot	
	Will the boot images be located outside of Flash?	Select a secondary interface: Ethernet, USB, UART, PCIe, or custom FPGA interface.	The FSBL, located in the primary boot device, could enable a secondary boot device.	
2.4	**Boot Features**			
2.4.1	**Features**			
	Is execute-in-place needed?	Execute-in-place is only available in QSPI and NOR modes	UG585: Zynq-7000 All Programmable SoC Technical Reference Manual > Boot and Configuration	
	Is PCIe enumeration required?	Calculate the estimated boot time based on the boot device. Review the Tandem PROM configuration feature.	PG054: 7 Series FPGAs Integrated Block for PCI Express Product Guide > Designing with the Core	
	Is there a need for multi-boot (golden image)?	Do the BootROM and FSBL support the intended use case?	UG821: Zynq-7000 All Programmable SoC Software Developers Guide UG585: Zynq-7000 All Programmable SoC Technical Reference Manual > BootROM Header Search	
	Is there a need for remote upgrade?	Select the upgrade path.		

ID	Description	Actions to Take	Relevant Information	Status and Notes
3.1	**Processor Peripherals Selection**			
3.1.1	**Gigabit Ethernet (1 or 2)**			
	Does the PS Ethernet Controller meet all of your design requirements?	Review the GEM specifications in the Technical Reference Manual and Data Sheet.	UG585: Zynq-7000 All Programmable SoC Technical Reference Manual > Gigabit Ethernet Controller	
	Are you using an RGMII PHY interface?	Available via MIO or EMIO. 3.3V I/O is not supported	PG160: GMII_to_RGMII IP v3.0 LogiCORE IP Product Guide	
	Are you using a GMII or MII PHY interface?	Available via EMIO only	Place the GMII RX clock on a clock capable IO	
	Are you using an SGMII or 1000 Base-X PHY interface?	Available via EMIO, only in devices with MGTs	PG047: LogiCORE IP Ethernet 1000BASE-X PCS/PMA or SGMII v14.2 Product Guide XAPP1082: PS and PL Ethernet Performance and Jumbo Frame Support with PL Ethernet in the Zynq-7000 AP SoC	
	Do you need jumbo frames support?	Use a PL-based Ethernet core	PG138: LogiCORE IP AXI Ethernet v6.1 Product Guide XAPP1082: PS and PL Ethernet Performance and Jumbo Frame Support with PL Ethernet in the Zynq-7000 AP SoC	
	Is IEEE-1588 support required?	Review the 1588 limitations of the GEM core.	UG585: Zynq-7000 All Programmable SoC Technical Reference Manual > IEEE 1588 Time Stamp Unit	
	Are you using the XC7Z010 CLG225 Device?	This device only supports 32 MIO pins. Ethernet 0 is not available via MIO.	UG585: Zynq-7000 All Programmable SoC Technical Reference Manual > MIO-at-a-Glance Table	
3.2	**Controllers**			
3.2.1	**USB Controller**			
	Does the USB controller meet all of your design requirements?	Review the USB peripheral specifications in the Technical Reference Manual and Data Sheet.	UG585: Zynq-7000 All Programmable SoC Technical Reference Manual > USB Host, Device, and OTG Controller	
	Do you have sufficient MIO pins to utilize the needed USB controllers?	USB Controllers require the use of the MIO pins.	UG585: Zynq-7000 All Programmable SoC Technical Reference Manual > USB Host, Device, and OTG Controller	
	Verify that the USB PHY meets the timing requirements for the Zynq device.	The Zynq Data Sheet specifies a min hold time requirement of 1ns. This must be verified against the PHY vendor data sheet.	Answer Record 53450	
	Are you using the XC7Z010 CLG225 Device?	This device only supports 32 MIO pins. USB 1 is not available.	UG585: Zynq-7000 All Programmable SoC Technical Reference Manual > MIO-at-a-Glance Table	
3.2.2	**UART Controller**			
	Does the UART Controller meet all of your design requirements?	Review the specifications in the Technical Reference Manual and Data Sheet.	UG585: Zynq-7000 All Programmable SoC Technical Reference Manual > UART Controller	
3.2.3	**SPI Controller**			
	Does the SPI Controller meet all of your design requirements?	Review the specifications in the Technical Reference Manual and Data Sheet.	UG585: Zynq-7000 All Programmable SoC Technical Reference Manual > SPI Controller	
3.2.4	**I2C Controller**			
	Does the I2C Controller meet all of your design requirements?	Review the specifications in the Technical Reference Manual and Data Sheet.	UG585: Zynq-7000 All Programmable SoC Technical Reference Manual > I2C Controller	
3.2.5	**CAN Controller**			
	Does the CAN Controller meet all of your design requirements?	Review the specifications in the Technical Reference Manual and Data Sheet.	UG585: Zynq-7000 All Programmable SoC Technical Reference Manual > CAN Controller	
	Do you need the two CAN controllers to run at different frequencies?	You will need to utilize MIO pin to bring in an external clock.	UG585: Zynq-7000 All Programmable SoC Technical Reference Manual > CAN Controller > Notices	
3.2.6	**GPIO Controller**			
	Does the GPIO meet all of your design requirements?	Review the specifications in the Technical Reference Manual and Data Sheet.	UG585: Zynq-7000 All Programmable SoC Technical Reference Manual > General Purpose I/O (GPIO)	
3.2.7	**SD/SDIO Controller**			
	Does the SD/SDIO Controller meet all of your design requirements?	Review the specifications in the Technical Reference Manual and Data Sheet.	UG585: Zynq-7000 All Programmable SoC Technical Reference Manual > SD/SDIO Controller	
3.3	**Peripherals**			

ID	Description	Actions to Take	Relevant Information	Status and Notes
3.3.1	**APU Peripherals**		UG585: Zynq-7000 All Programmable SoC Technical Reference Manual > Application Processing Unit	
	Do you plan on using an external clock for a watchdog timer?	Watchdog timer with external clock requires use of the SWDT.	UG585: Zynq-7000 All Programmable SoC Technical Reference Manual > Timers	
3.3.2	**Programmable Logic Peripherals**			
	Will PL peripherals be memory mapped to the PS?	The PS has a fixed 2GB address range to the PL.	UG585: Zynq-7000 All Programmable SoC Technical Reference Manual > System Addresses	
	Will PL masters have access to the OCM and DDR?	Make sure that the addressing does not conflict with the software code.	UG585: Zynq-7000 All Programmable SoC Technical Reference Manual > System Addresses	
	Are the peripherals needed available in the Xilinx library?	Xilinx offers an extensive list of AXI peripherals.	Xilinx IP Center	
	Are the peripherals available from a third-party vendor?	Contact the third-party vendor for information. Verify that Zynq software drivers are available.	Xilinx IP Center	
	Is there a need to design custom peripherals?	Review how to create and package IPs in Vivado.	UG1118: Vivado Design Suite User Guide: Creating and Packaging Custom IP	
	Is the ability to reset PS without clearing the PL required?	Contact your Xilinx FAE regarding the Zynq Processor System Reset Module (ZPSRM) solution.		
	Is the Anti-Tamper Security Monitor IP needed?	Check the support for the device/package selected.	Security solutions	
3.4	**Programmable Logic Performance**			
3.4.1	**Programmable Logic Performance**			
	Will software kernel be offloaded to a hardware accelerator?	Profile software and explore partition options for moving hot regions of software to PL.	UG1046: UltraFast Embedded Design Methodology Guide > System Level Considerations	
	Are there performance requirements for the PL design?	Explore best practices for choosing Zynq PL ports, masters and datapaths.	UG1046: UltraFast Embedded Design Methodology Guide > Hardware Design Considerations	
	Can PL performance be estimated before design started?	Explore SDK's System Performance Modeling toolkit for PL traffic sources.	UG1145: Xilinx Software Development Kit (SDK) User Guide, System Performance Analysis	
	Will ACP be used for data movement?	Explore best practices for using ACP for low latency shared memory with CPUs.	UG1046: UltraFast Embedded Design Methodology Guide > Hardware Design Considerations Chapter	
	Will HP ports be used for data movement?	Explore best practices for using HP for high throughput data movement to DRAM.	UG1046: UltraFast Embedded Design Methodology Guide > Hardware Design Considerations Chapter	
3.5	**General Questions**			
3.5.1	**General Questions**			
	Which peripherals will be using EMIO vs MIO? Are there enough MIO pins?	Review the MIO mappings. Using the EMIO requires a BIT file for software development.	UG585: Zynq-7000 All Programmable SoC Technical Reference Manual > MIO-at-a-Glance Table	

ID	Description	Actions to Take	Relevant Information	Status and Notes
4.1	**Memory Controller - Non Boot Usage**			
4.1.1	**DDR Controller**			
	Which memory type is required for your design?	Select between DDR3, DDR3L, DDR2, or LPDDR2.	UG585: Zynq-7000 All Programmable SoC Technical Reference Manual > DDR Memory Controller	
	What are the size and density needs?	The controller supports single rank devices up to 1 Gigabyte.	UG585: Zynq-7000 All Programmable SoC Technical Reference Manual > DDR Memory Types, Densities, and Data Widths	
	Is ECC needed?	Memory width will be limited to 16-bit up to 512 Megabytes.	UG585: Zynq-7000 All Programmable SoC Technical Reference Manual > Error Correction Code	
	Has the DDR memory space been partitioned?	Partition the memory for CPU0, CPU1, PS masters, and PL masters.		
	Are you using the XC7Z010 CLG225 Device?	This device/package supports a 16-bit interface.	UG585: Zynq-7000 All Programmable SoC Technical Reference Manual > MIO-at-a-Glance Table	
4.1.2	**Static Memory Controller**			
	Which memory type is required for your design?	Select between NOR Flash, NAND Flash, or Asynchronous SRAM. QSPI Flash is not available when using the SMC.	UG585: Zynq-7000 All Programmable SoC Technical Reference Manual > Static Memory Controller	
	Does the Static Memory Controller meet all your design requirements?	Review the specifications in the TRM and Data Sheet.	UG585: Zynq-7000 All Programmable SoC Technical Reference Manual > Static Memory Controller	
	Are you using the XC7Z010 CLG225 Device?	This device/package does not support the NOR/SRAM interfaces. The NAND interface is supported in the 8-bit interface, but not the 16-bit interface.	UG585: Zynq-7000 All Programmable SoC Technical Reference Manual > MIO-at-a-Glance Table	

ID	Description	Actions to Take	Relevant Information	Status and Notes
5.1	**Software Configuration**			
5.1.1	**Processor Implementation**			
	Is the system Single or Dual core?	Select based on the software requirements.	A Bare Metal implementation uses a single core by default. Some OS/RTOS offer dual core SMP support.	
	For a dual core system, will it be AMP or SMP?	Check if the OS/RTOS offers SMP support. Check if the OS/RTOS has been used in an AMP configuration.	Vendor specific.	
	Will a Hypervisor/Supervisor be used?	Check the available Hypervisor solutions.	Multi-OS Support Wiki page	
	Is there a need for TrustZone support?	Review how the software will be used to manage TrustZone.	WP429: TrustZone Technology Support in Zynq-7000 All Programmable SoC	
	Will PL masters have access to the PS IO peripherals?	Consider if the resources will be shared with multiple masters. Plan a mutual exclusion scheme if needed.	OS/RTOS specific.	
	Will the NEON engine be enabled?	Will the code be optimized for NEON? Use of intrinsics or libraries?	XAPP1206: Boost Software Performance on Zynq-7000 AP SoC with NEON Application Note	
	Is there a need for hardware acceleration of the software?	Review the use of the ACP and Vivado HLS.	Vivado High Level Synthesis Product Page	
	Will the On Chip Memory (OCM) be used by the PS and/or PL?	Define how the OCM will be mapped and used.	UG585: Zynq-7000 All Programmable SoC Technical Reference Manual > On-Chip Memory (OCM)	
5.1.2	**RTOS/OS Selection**			
	Are you using RTOS/OS for Core 0?	Verify that the OS/RTOS supports Zynq.	Vendor specific.	
	Have changes been made to Core 1 RTOS/OS to be used in AMP mode?	Verify that the OS/RTOS has been modified to be used as an AMP configuration on the second core.	Vendor specific. The Xilinx Bare Metal BSP supports an AMP configuration.	
	If you are using Linux, will PetaLinux be used?	Review the Xilinx PetaLinux offering.	PetaLinux Tools Product Page	
	For Linux, where will the root file system be located?	Select the filesystem type and location.	System specific.	
	Are there real-time requirements, hard or soft?	Select an OS/RTOS based on the RT requirements.	RTOS/OS specific.	
	Does the RTOS/OS have support for the Zynq peripherals selected?	Verify that the available BSP supports the peripherals needed.	RTOS/OS specific.	
	Does the RTOS/OS have support for the PL based peripherals (Xilinx, Third Party, or Custom)?	If not, does the customer have the expertise to create them and/or are they available through Third Parties?	RTOS/OS specific.	
	Is the Board Support Package dependent on a particular development board?	Verify the amount of work required to port the BSP to another board.	RTOS/OS specific.	
5.1.3	**Middleware Selection**			
	Is an Ethernet stack needed?	Verify that the stack has been ported to Zynq.	RTOS/OS specific.	
	Is a USB stack needed?	Verify that the stack has been ported to Zynq.	RTOS/OS specific.	
	Is a CAN stack needed?	Verify that the stack has been ported to Zynq.	RTOS/OS specific.	
	Is a File System needed?	Verify that the RTOS/OS has a compatible Zynq file system.	RTOS/OS specific.	
	Is there a need for Graphics?	Verify that the graphic library is compatible with the video IPs used in the design.	RTOS/OS specific.	
	Is there a need for specific libraries?	Verify that the libraries are available for Zynq.	RTOS/OS specific.	
5.2	**Performance**			
5.2.1	**Performance**			
	Does the system need to meet a performance target?	Define performance goals.	UG1046: UltraFast Embedded Design Methodology Guide > System Considerations	

ID	Description	Actions to Take	Relevant Information	Status and Notes
	Can system performance be estimated before design started?	Explore the SDK System Performance Modeling toolkit to model Zynq PS & PL performance	UG1145: Xilinx Software Development Kit (SDK) User Guide, System Performance Analysis	
	Is live system performance monitoring required?	Explore Zynq performance monitor points in both PS and PL.	UG1046: UltraFast Embedded Design Methodology Guide > System Considerations	
	Are there performance requirements for offchip interfaces?	Use a development board to verify if the requirements can be met based on the OS/RTOS.	XAPP1082: PS and PL Ethernet Performance and Jumbo Frame Support with PL Ethernet in the Zynq-7000 AP SoC	
	Do you need to optimize the final system for performance goals?	Explore Zynq performance optimization techniques and benchmarks.	UG1145: Xilinx Software Development Kit (SDK) User Guide, System Performance Analysis	