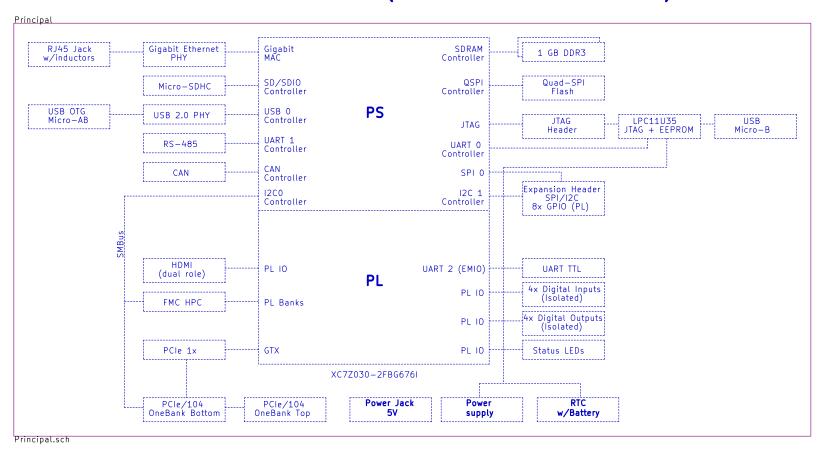
Computadora Industrial Abierta Argentina CIAA-ACC Xilinx XC7Z030 (2x Cortex A9 + Kintex-7 FPGA)







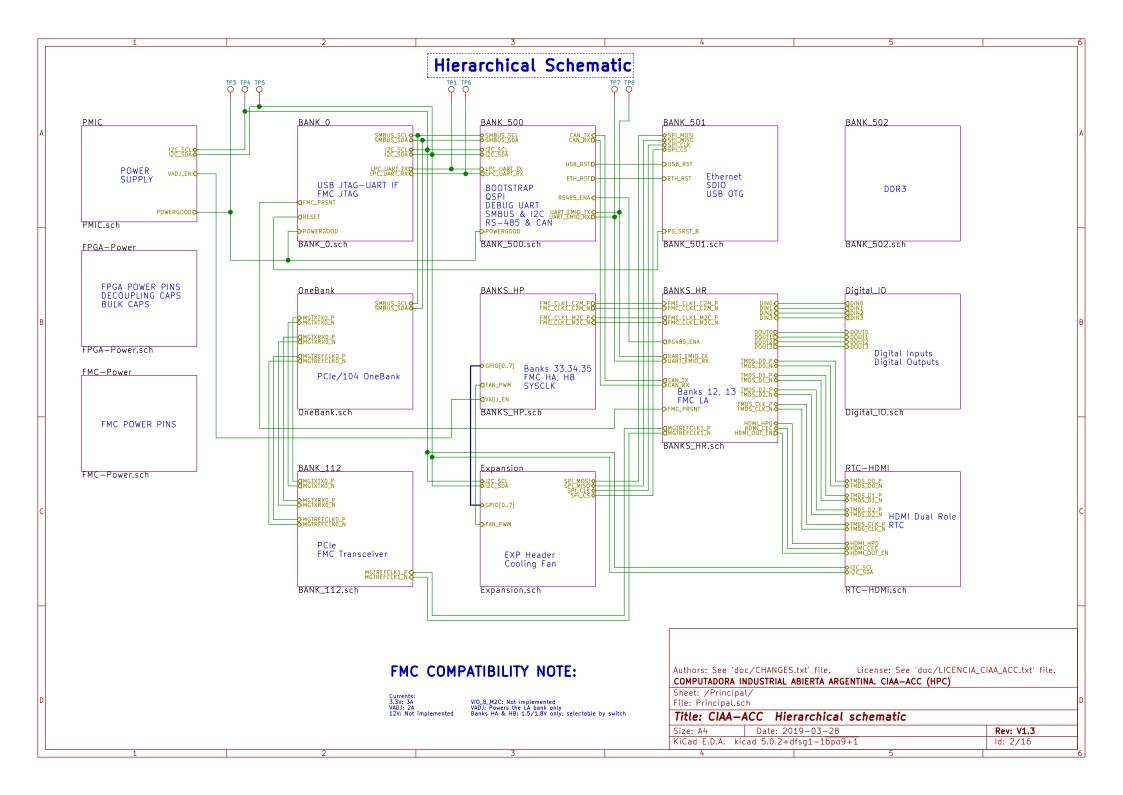


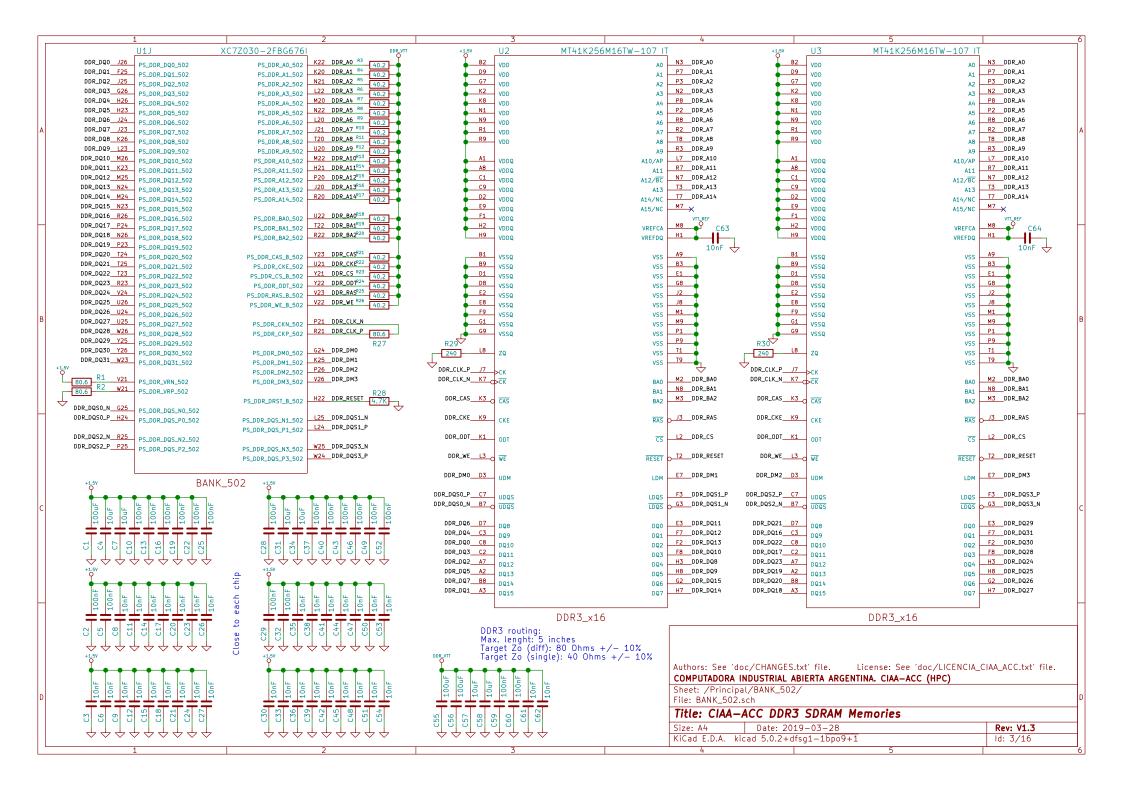
Authors: See 'doc/CHANGES.txt' file. License: See 'doc/LICENCIA_CIAA_ACC.txt' file. COMPUTADORA INDUSTRIAL ABIERTA ARGENTINA. CIAA—ACC (HPC)

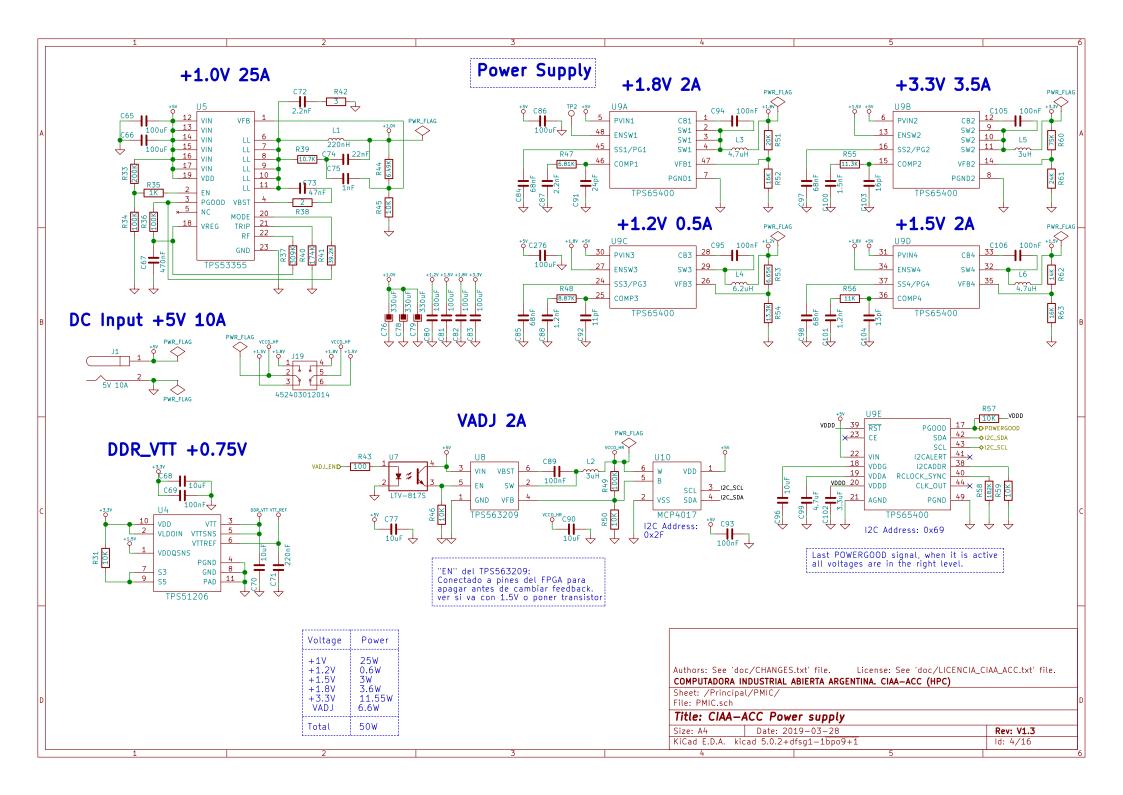
Sheet: / File: ciaa_acc.sch

Title: CIAA-A	ICC	Block	Diagram	
C1 1/	_			Т

Size: A4	Date: 2019-03-28	Rev: V1.3
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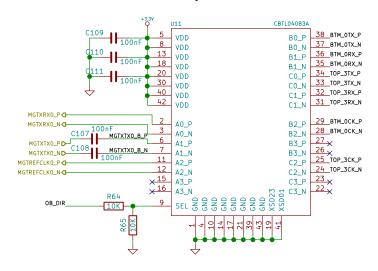


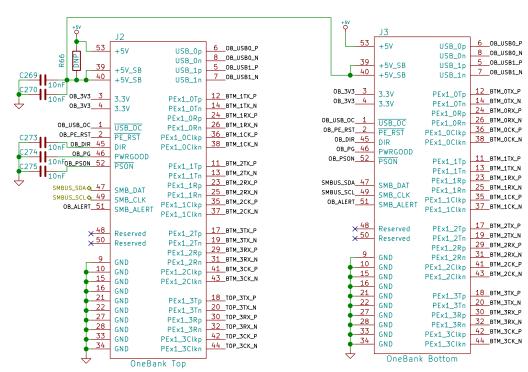


PCle/104 OneBank Connector

 $\begin{array}{ccc} & \text{H1} & \text{H3} \\ & \otimes & \otimes \\ & \text{H2} & \text{H4} \\ & \otimes & \otimes \\ & \text{Holes PCIe 104} \end{array}$

Mux/Demux Switch





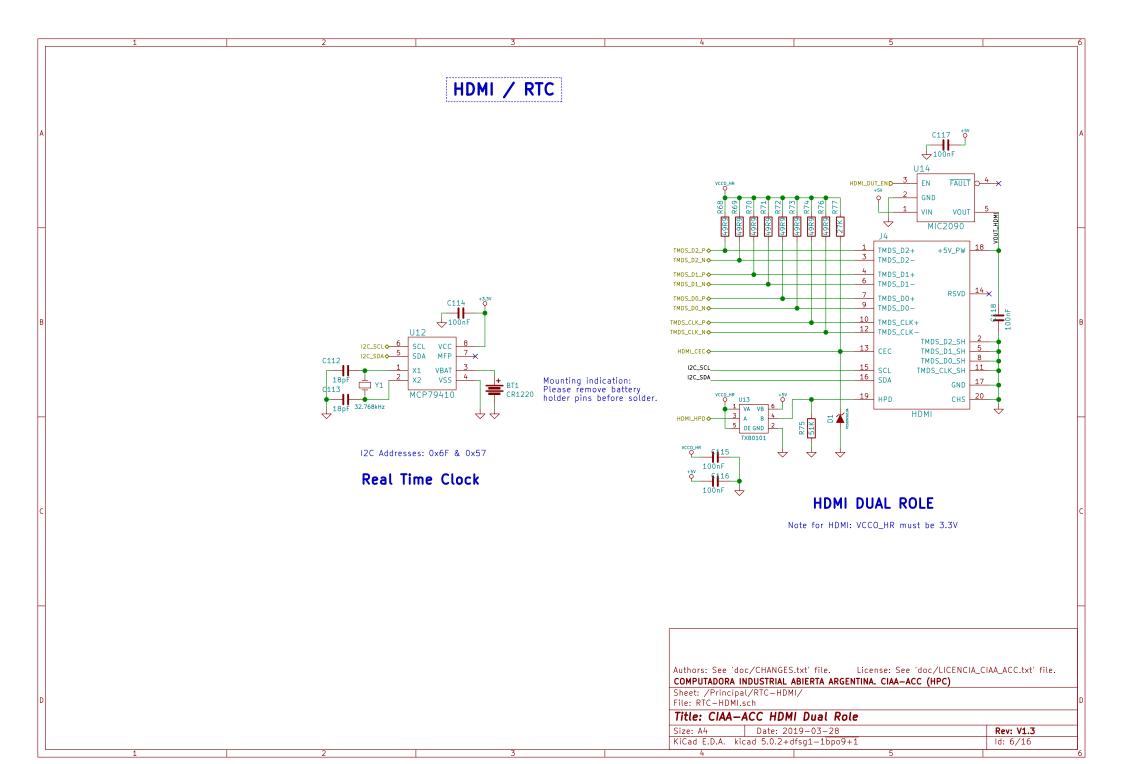
PCIe OneBank device routing:
Max. lenght: 4 inches
Target Zo (diff): 85 Ohms +/- 15%
Spacing between links: 20 mils
Matching tolerance (intra-pair): 5 mils
Matching tolerance (inter-pair): Not required

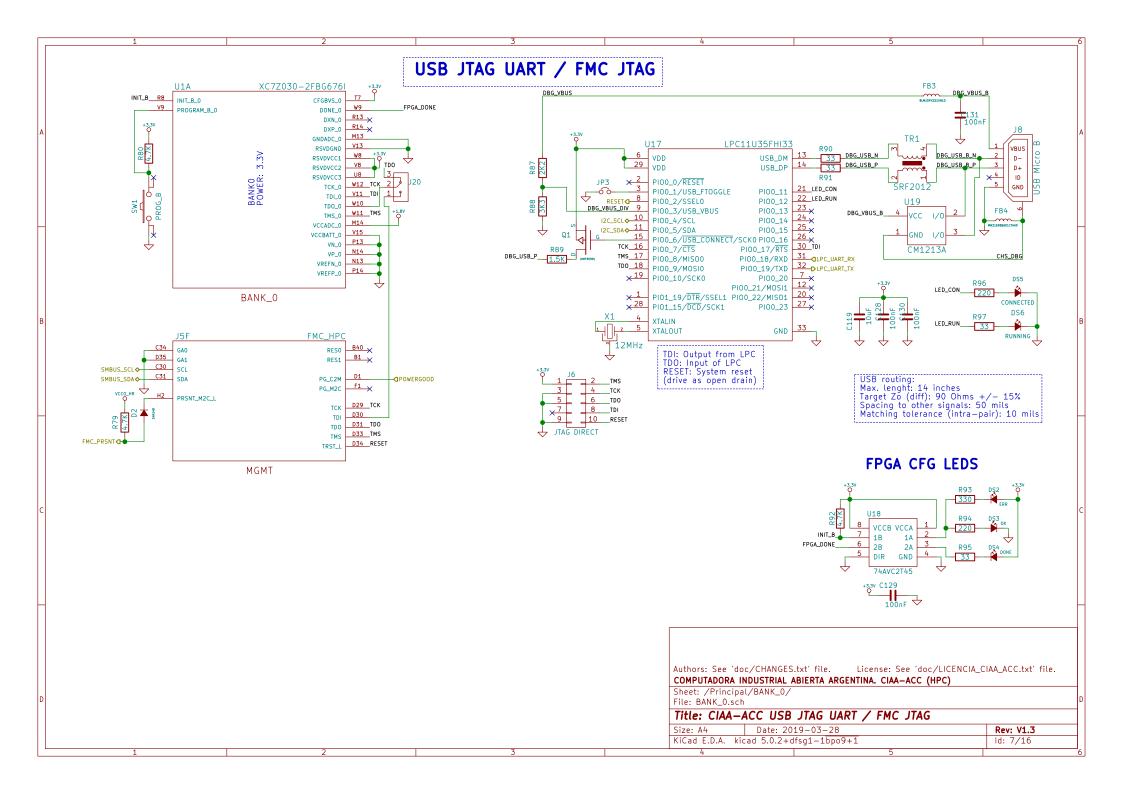
Authors: See 'doc/CHANGES.txt' file. License: See 'doc/LICENCIA_CIAA_ACC.txt' file. COMPUTADORA INDUSTRIAL ABIERTA ARGENTINA. CIAA—ACC (HPC)

Sheet: /Principal/OneBank/ File: OneBank.sch

Title: CIAA-ACC PCIe/104 OneBank Connector

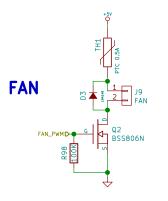
	Size: A4	Date: 20	19-03-28	Rev: V1.3	1	
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_	4		5		•	⁻ 6

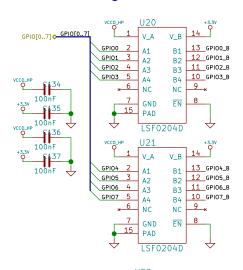


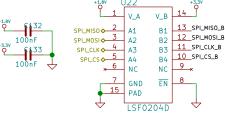


Expansion Header / FAN Connector

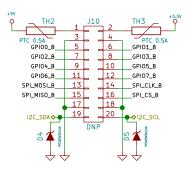
Voltage level translator







Expansion Header



GPIO Only available when VCCO_HP = 1.8V

○F1 ○F2 ○F3 ○F4

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Sheet: /Principal/Expansion/

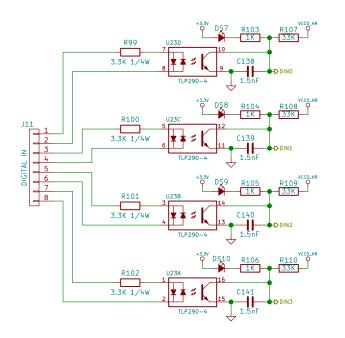
File: Expansion.sch

Title: CIAA-ACC Expansion Header (GPIO, SPI, I2C) / FAN Connector

 Size: A4
 Date: 2019-03-28
 Rev: V1.3

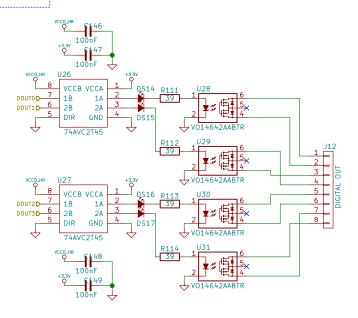
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 Id: 8/16

Digital Inputs and Outputs



ISOLATED DIGITAL INPUTS

Range: 12 to 24 V



ISOLATED DIGITAL OUTPUTS

Range: up to 60 V

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Sheet: /Principal/Digital_IO/ File: Digital_IO.sch

Title: CIAA-	ACC	Digital	Inputs	and	Outputs

Date: 2019-03-28 Rev: V1.3 KiCad E.D.A. kicad 5.0.2+dfsg1-1bpo9+1 ld: 9/16

PCIe / FMC Transceiver





FMC_HPC X A39 DP5_C2M_N C3 DP2_C2M_N DP0_C2M_N X A38 DP5_C2M_P C2_DP2_C2M_P DPO_C2M_P X A19 DP5_M2C_N X A18 DP5_M2C_P B37 DP6_C2M_N A23 DP1_C2M_N DP1_C2M_N DP1_C2M_P A22 DP1_C2M_P X B36 DP6_C2M_P DP1_M2C_N A3_DP1_M2C_N X B17 DP6_M2C_N A2 DP1_M2C_P X B16 DP6_M2C_P DP1_M2C_P DP2_C2M_N A27 DP0_C2M_N × B33 DP7_C2M_N DP2_C2M_P A26 DP0_C2M_P × B32 DP7_C2M_P A7 DPO_M2C_N X B13 DP7_M2C_N DP2_M2C_N DP2_M2C_P A6 DP0_M2C_P X B12 DP7_M2C_P X B29 DP8_C2M_N DP3_C2M_N A31 X X B28 DP8_C2M_P DP3_C2M_P A30 X X B9 DP8_M2C_N DP3_M2C_N A11 X DP3_M2C_P A10 X X B8 DP8_M2C_P × B25 DP9_C2M_N DP4_C2M_N A35 X X B24 DP9_C2M_P DP4_C2M_P A34 X DP4_M2C_N A15 X X B5 DP9_M2C_N X B4 DP9_M2C_P DP4_M2C_P A14 X

Coupling capacitor for transceivers must be in FMC mezzanine card.

PCIe routing: Target Zo (diff): 85 Ohms +/- 15% Spacing between links: 20 mils Matching tolerance (intra-pair): 5 mils Matching tolerance (inter-pair): Not required

TXRX

Authors: See 'doc/CHANGES.txt' file. License: See 'doc/LICENCIA_CIAA_ACC.txt' file. COMPUTADORA INDUSTRIAL ABIERTA ARGENTINA. CIAA—ACC (HPC)

Sheet: /Principal/BANK_112/

File: BANK_112.sch

Size: A4	Date: 20	19-03-28		Rev: V1.3
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