

SATURN SPARTAN-6 FPGA MODULE

User Guide

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Introduction

Saturn is an easy to use FPGA Development board featuring Xilinx Spartan-6 FPGA. Saturn is specially designed for experimenting and learning system design with FPGAs. This development board features Xilinx XC6SLX series FPGA with FTDI's FT2232H Dual-Channel USB device. The high speed USB 2.0 interface provides fast and easy configuration download to the on-board SPI flash. No programmer or special downloader cable is needed to download the bit stream to the board.

Applications

- Product Prototype Development
- Development and testing of custom embedded processors
- Signal Processing
- Communication devices development
- Educational tool for Schools and Universities

Board features

- FPGA: Spartan-6 XC6SLX9, LX16, LX25 or LX45 in CSG324 package
- DDR: 166MHz 512Mb LPDDR
- Flash memory: 128 Mb SPI flash memory (N25Q128A13ESE40E)
- 100MHz CMOS oscillator
- High Speed USB 2.0 interface for On-board flash programming. FT2232H
Channel A is dedicated for SPI Flash /JTAG Programming. Channel B can be used for custom applications.
- On-board voltage regulators for single power rail operation
- FPGA configuration via JTAG and USB
- Maximum 158 IOs for user defined purposes
 - XC6SLX9 - 118 IOs
 - XC6SLX16 - 150 IOs
 - XC6SLX25 - 144 IOs
 - XC6SLX45 - 136 IOs
 - FT2232H - 8 IOs

How to use the module

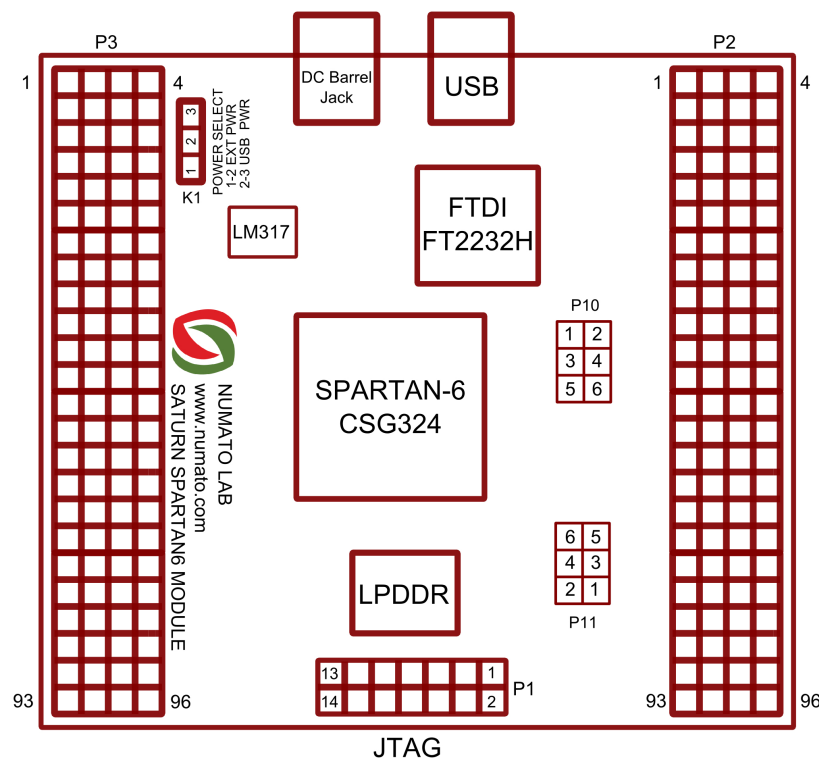
The following section describes how to use this module.

Components/Tools required

Along with the module, you may need the items in the list below for easy and fast installation.

1. USB A to Mini B cable.
2. DC Power supply (Optional).

Connection Diagram



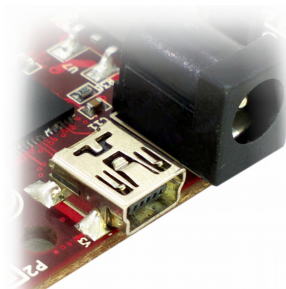
This diagram should be used as a reference only. For detailed information, see Saturn schematics at the end of this document. Details of individual connectors are as below.

USB Interface

The on board full speed USB controller helps a PC/Linux/Mac computer to communicate with this module. Use a USB A to Mini B cable to connect with a PC. By default the module is powered from USB so make sure not to overcrowd unpowered USB hubs. (the picture on the right shows USB Mini connector)

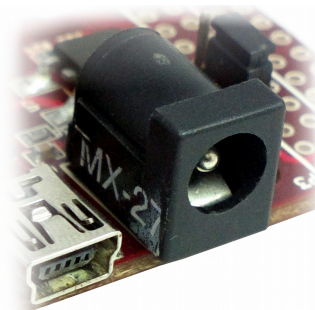


Visit <http://numato.com/cables-accessories> to buy cables and accessories for this product.



DC Power Supply

This module uses +5V power supply to function properly. **By default the board is configured to use +5V supply from USB. So an external +5V power is not required unless USB port is unable to supply enough current. In most cases USB ports are capable of providing enough current for the module. Current requirement for this board largely depends on your application. Please consult FPGA data sheet for more details on power requirements.** If for any reason, an external 5V power supply needs to be used for the module, the Power select jumper should be configured properly before connecting the power supply. Please refer to the marking on the board for more details.



Power Select

The Power Select header K1 is used to configure the power source for the board. The jumper in pin 2 and 3 is shorted to switch the power source to on board USB port and pin 1 and 2 to use the external DC power.

JTAG Connector

JTAG connector provides access to FPGA's JTAG pins. A XILINX platform cable can be used to for JTAG programming.

GND	GND	GND	GND	GND	GND	GND
13	11	9	7	5	3	1
14	12	10	8	6	4	2
NC	NC	TDI	TDO	TCK	TMS	VREF

JTAG/SPI Configuration on FT2232H channel A

Channel A of FT2232H can be connected to the SPI bus that connects the SPI Flash chip to the FPGA or to the JTAG pins of the FPGA. By connecting SPI bus to FT2232H channel A, the SPI flash can be directly programmed to save the configuration permanently. This is the default configuration set when Saturn is shipped. When FT2232H channel A is connected to SPI, Saturn Configuration Downloader utility can be used to program the board.

When FT2232H channel A is connected to FPGA JTAG, the JTAG signals can be accessed directly through FT2232H. Saturn Configuration Downloader utility currently does not support programming FPGA SRAM through JTAG.

Please see the tables below for information about selecting SPI or JTAG for FT2232H channel A. SPI must be selected for Saturn Configuration Downloader utility to work.

Header P10

Jumper Configuration for SPI	Jumper Configuration for JTAG
1 - 2	2 - 4
5 - 6	3 - 5

Header P11

Jumper Configuration for SPI	Jumper Configuration for JTAG
1 - 2	2 - 4
5 - 6	3 - 5

GPIOs

This device is equipped with a maximum 158 user IO pins that can be used for various custom applications. Out of 158 user IOs 56 are length matched which can be used as differential pairs.

Header P3

Pin No. On The Header	Spartan-6 (CSG324) Pin No.	Pin No. On The Header	Spartan-6 (CSG324) Pin No.
1	GND	2	3V3
3	VCCIN	4	GND
5	G13	6	H12
7	K14	8	J13
9	H16	10	H15
11	H14	12	H13
13	G14	14	F14
15	G18	16	G16
17	F16	18	F15
19	F18	20	F17
21	E18	22	E16
23	D18	24	D17
25	C18	26	C17
27	A16	28	B16
29	A15	30	C15
31	C14	32	D14
33	A14	34	B14
35	E13	36	F13
37	A13	38	C13
39	E12	40	F12
41	C12	42	D12
43	A12	44	B12
45	E11	46	F11

47	C11	48	D11
49	GND	50	GND
51	GND	52	GND
53	F10	54	G11
55	A11	56	B11
57	A10	58	C10
59	F9	60	G9
61	C9	62	D9
63	A9	64	B9
65	F8	66	G8
67	E8	68	E7
69	C8	70	D8
71	A8	72	B8
73	E6	74	F7
75	A7	76	C7
77	A6	78	B6
79	C6	80	D6
81	A5	82	C5
83	A4	84	B4
85	A3	86	B3
87	A2	88	B2
89	GND	90	GND
91	GND	92	GND
93	3V3	94	3V3
95	3V3	96	3V3





Header P2

Pin No. On The Header	Spartan-6 (CSG324) Pin No.	Pin No. On The Header	Spartan-6 (CSG324) Pin No.
1	ACBUS0*	2	ACBUS1
3	3V3	4	GND

5	ACBUS2	6	ACBUS3
7	K12	8	K13
9	ACBUS4	10	ACBUS5
11	L14	12	M13
13	ACBUS6	14	ACBUS7
15	M14	16	N14
17	L12	18	L13
19	L15	20	L16
21	K15	22	K16
23	N15	24	N16
25	T17	26	T18
27	P15	28	P16
29	U16	30	V16
31	U17	32	U18
33	T14	34	V14
35	U15	36	V15
37	T12	38	V12
39	U13	40	V13
41	R11	42	T11
43	M11	44	N11
45	GND	46	GND
47	GND	48	GND
49	GND	50	GND
51	GND	52	GND
53	N10	54	P11
55	U11	56	V11
57	R10	58	T10
59	M10	60	N9
61	T9	62	V9
63	R8	64	T8

65	N7	66	P8
67	M8	68	N8
69	U7	70	V7
71	U8	72	V8
73	R7	74	T7
75	N6	76	P7
77	N5	78	P6
79	T6	80	V6
81	R5	82	T5
83	U5	84	V5
85	R3	86	T3
87	T4	88	V4
89	INITB	90	3V3
91	PROGB	92	3V3
93	GND	94	GND
95	GND	96	GND

* ACBUS0 - ACBUS7 are pins of FTDI FT2232H Dual-Channel USB device.

	VCC
	Ground
	GPIO
	FTDI IO

No Connect Pins In LX9(CSG324)

SL No.	Pin No On The Header P3	Spartan-6 (CSG324)
1	37	A13
2	38	C13
3	39	E12
4	40	F12
5	41	C12

6	42	D12
7	45	E11
8	46	F11
9	53	F10
10	54	G11
11	65	F8
12	66	G8
13	67	E8
14	68	E7
15	73	E6
16	74	F7
SL No.	Pin No On The Header P2	Spartan-6 (CSG324)
1	35	U15
2	36	V15
3	37	T12
4	38	V12
5	43	M11
6	44	N11
7	53	N10
8	54	P11
9	59	M10
10	60	N9
11	65	N7
12	66	P8
13	67	M8
14	68	N8
15	75	N6
16	76	P7

No Connect Pins In LX25 (CSG324)

SL No.	Pin No On The HeaderP3	Spartan-6 (CSG324)
1	65	F8
2	66	G8
3	67	E8
4	68	E7
5	73	E6
6	74	F7

No Connect Pins In LX45(CSG324)

SL No.	Pin No On The Header P3	Spartan-6 (CSG324)
1	39	E12
2	40	F12
3	41	C12
4	42	D12
5	45	E11
6	46	F11
7	53	F10
8	54	G11
9	65	F8
10	66	G8
11	67	E8
12	68	E7
13	73	E6
14	74	F7

FT2232H – Spartan-6 (CSG324) FPGA Connection Details

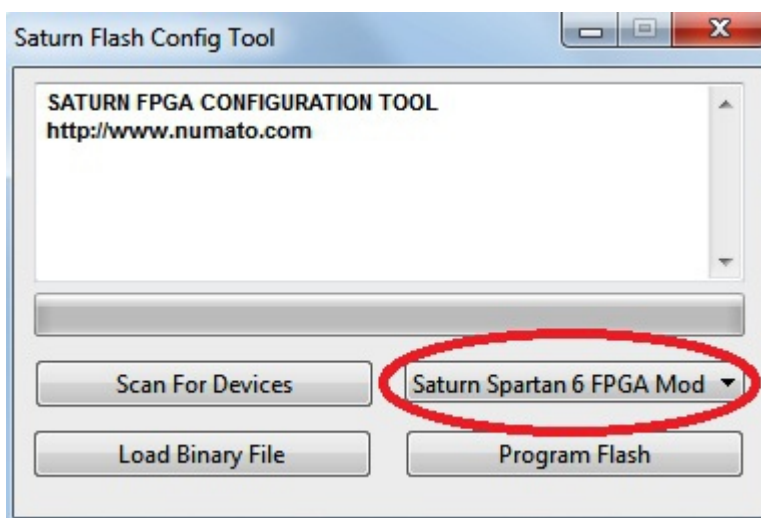
FTDI Pin No.	Pin Function (245 FIFO)	Spartan-6 Pin No.
38	D0	L17
39	D1	L18

40	D2	M16
41	D3	M18
43	D4	N17
44	D5	N18
45	D6	P17
46	D7	P18
48	RXF#	K18
52	TXE#	K17
53	RD#	J18
54	WR#	J16
55	SIWUB	H18

Driver Installation

Windows

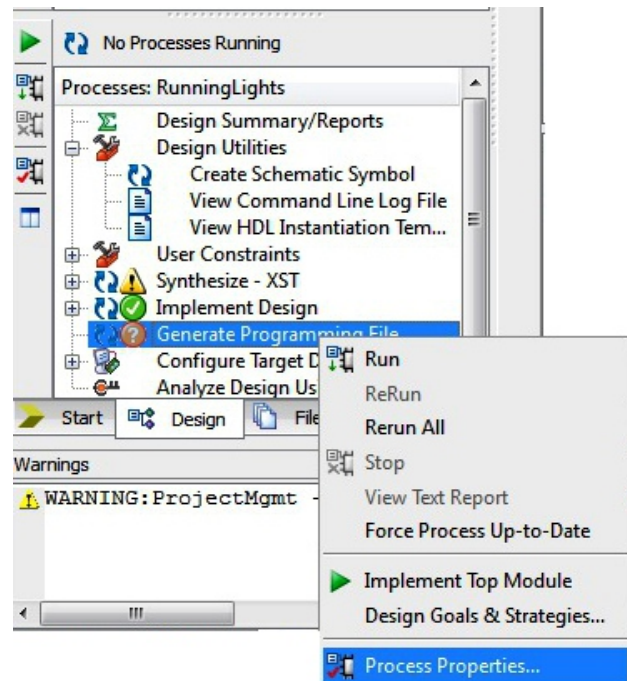
This product requires a driver to be installed for proper functioning when used with Windows. The D2XX driver can be downloaded from <http://www.ftdichip.com/Drivers/D2XX.htm>. Windows Users run the CDM v2.08.30 WHQL Certified.exe application that will prompt to install the FTDI CDM drivers. When driver installation is complete, the module should appear in Saturn Flash Config Tool as Saturn Spartan 6 FPGA Module (see the picture).



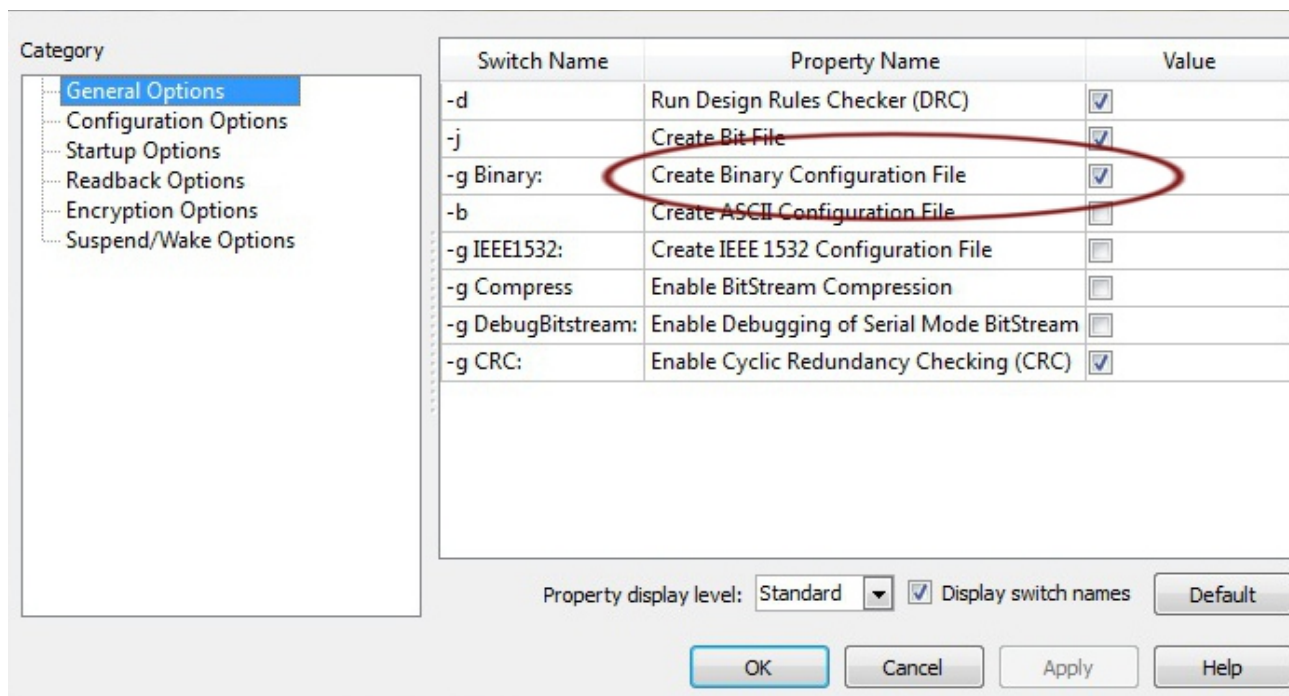
Generating Bit Stream for Saturn

HDL design needs to be converted to bit stream before it can be programmed to FPGA. Saturn at this time accepts only binary (.bin) bit stream created by XILINX ISE (<http://www.xilinx.com/tools/webpack.htm>). Once the HDL is synthesized, it is easy to create a binary bit stream out of it. Please follow the steps below to generate binary bit stream from your design using ISE Web Pack.

Step 1: Right click on the “Generate Programming File” option in “Processes” window.



Step 2: Select “Process Properties” from the pop up menu. In the dialog box, check “Create Binary Configuration File” Check box and click “Apply”.



Step 3: Click “OK” to close the dialog box. Right click on “Generate Programming File” option again and select “Run”. Now you will be able to find a “.bin” file in the project directory and that file can be used for Saturn configuration.

Powering Up Saturn

Saturn is factory configured to be powered directly from USB port so make sure that you are using a USB port that can power the board properly. It is recommended to connect the board directly to the PC instead using a hub. It is practically very difficult to estimate the power consumption of the board, as it depends heavily on your design and the clock used. XILINX provides tools to estimate the power consumption. In any case if power from USB is not enough for your application, external supply can be applied to the board. Jumper PWRSEL should be set up properly (short pin 1-2) to use the board on external power. Saturn requires three different voltages, a 3.3V, a 1.8V supplies and a 1.3V supply. On-board regulators derive these voltages from the USB/Ext power supply.

Configuring Saturn Spartan6 Module

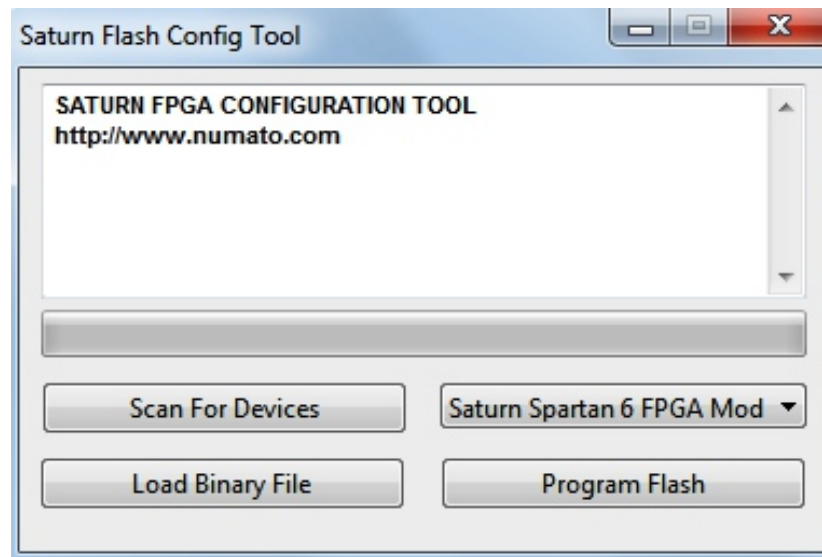
The Saturn Spartan6 module can be configured by two methods,

- a) Using Spartan configuration tool through USB.
- b) Using the Xilinx programming cable.

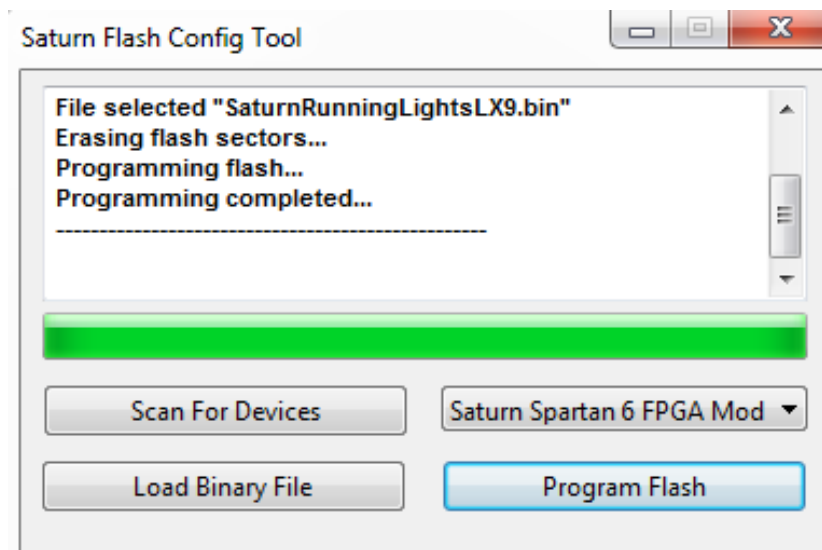
Configuring Saturn using configuration tool

Saturn has an on-board FTDI FT2232 device which facilitates easy reprogramming of on-board SPI flash through USB interface. The FTDI receives bit stream from the host application and program it in to the SPI Flash and lets the FPGA boot from the flash. The Saturn configuration application can be downloaded from www.numato.com for free.

Step 1: Open Saturn Config Tool. Click “Scan for Devices” if “Saturn Spartan 6 FPGA Module” is not detected automatically.



Step 2: Click on “Load Binary” Select the “.bin” file, then click on “Program Flash” button. Wait till “Programming Completed” appears on the screen.

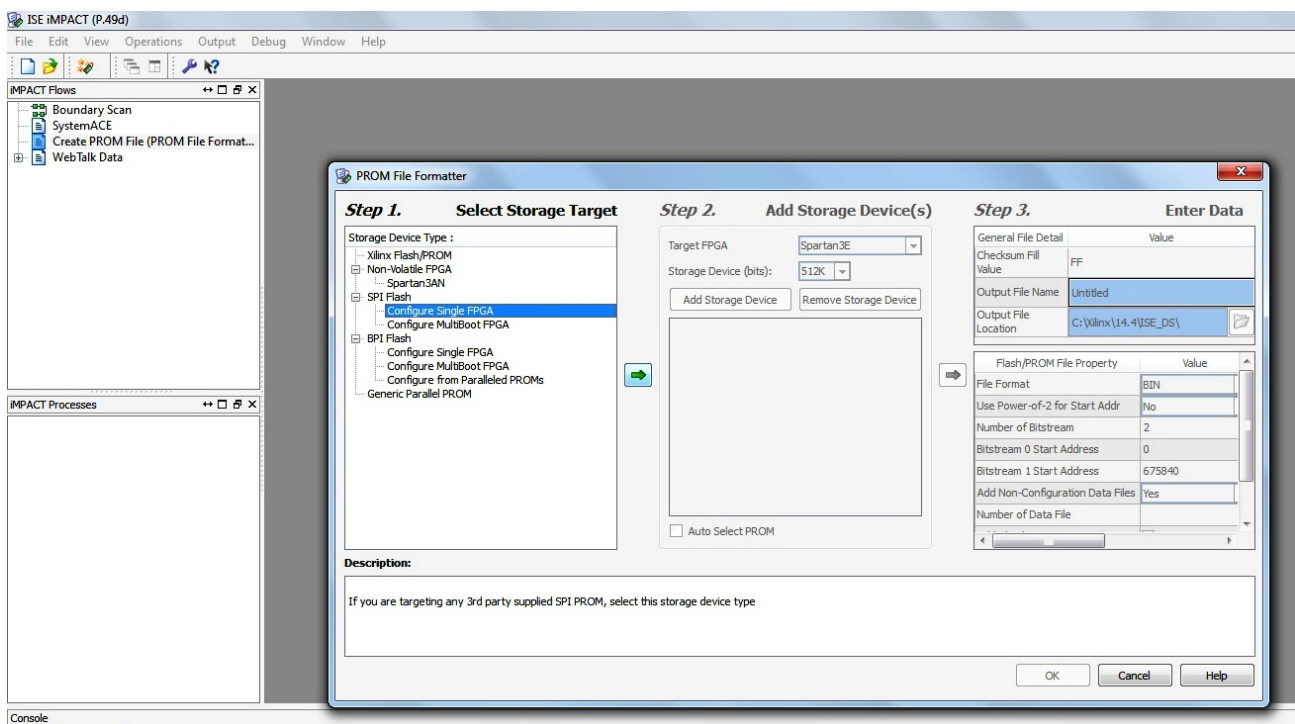


Configuring Saturn using JTAG

Saturn Spartan6 module features an on-board JTAG connector which facilitates easy reprogramming of SRAM and on-board SPI flash through JTAG programmer like “XILINX Platform-cable usb”. Programming Saturn using JTAG requires “XILINX ISE iMPACT” software which is bundled with XILINX ISE Design Suite. To program the SPI flash we need a “.mcs” file needs to be generated from the “.bit” file. Steps for generating “.mcs” file are as below. Programming FPGA SRAM does not require a “.mcs” file to be generated.

Generating “.mcs” file for Saturn

Step 1: Open ISE iMPACT. Click on “Create PROM file(PROM file formatter)”. In the dialog box, select “Configure Single FPGA” in storage device type. Then click on the green arrow on the right side.



Step 2: Select 128M in Storage Device (bits). Now click on “Add Storage Device”, then the green arrow on the right side.

Step 2. Add Storage Device(s)


Storage Device (bits) 128K ▼

☐ Auto Select PROM


128K
256K
512K
1M
2M
4M
8M
16M
32M
64M
128M
256M
512M

Step 3: Set an output file name and the output file location (the ".mcs" file will be generated at this location which will be required later for programming the FPGA), then click OK twice, then select the ".bit" file we already generated then click Open and click NO when it prompts to add another device file.

Step 3. Enter Data

General File Detail	Value
Checksum Fill Value	FF
Output File Name	Saturn
Output File Location	C:\Xilinx\14.4\ISE_DS\ 

Flash/PROM File Property	Value
File Format	MCS
Add Non-Configuration Data Files	No

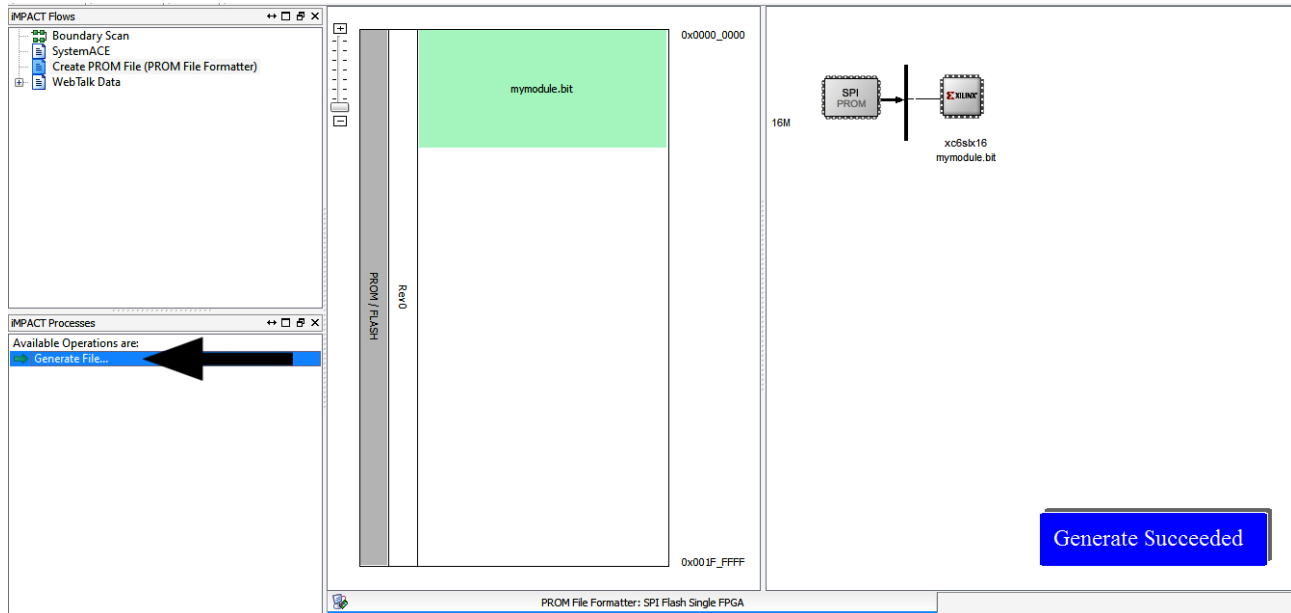


d mode.

ed to calculate the checksum of the unused portions.

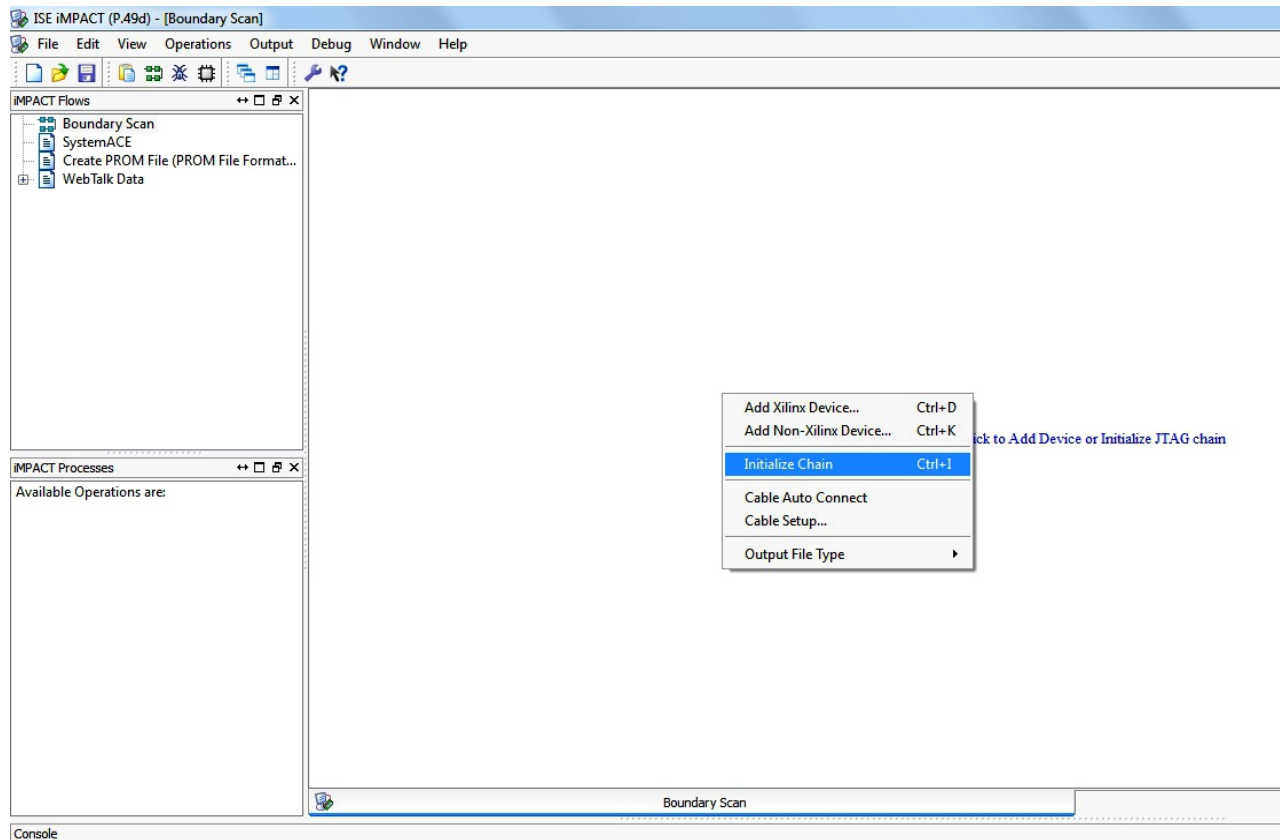
le format your PROM programmer uses, you output a MCS

Step 4: Double click on “Generate File”. “Generate Succeeded” will be displayed as shown in fig below if the “.mcs” the file is generated successfully.

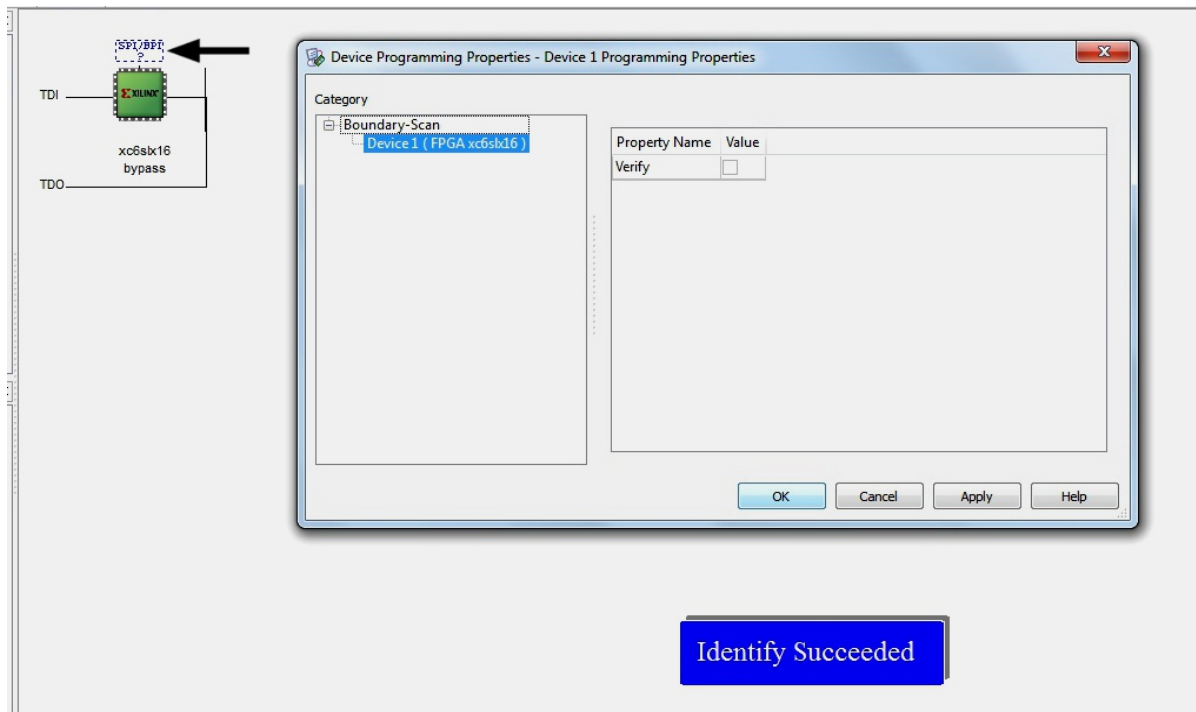


Programming FPGA using ISE iMPACT

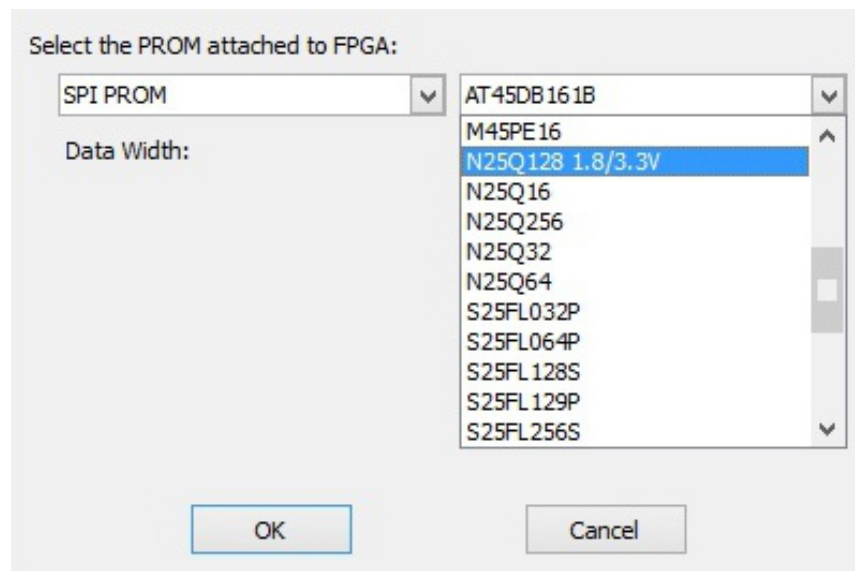
Step 1: Open ISE iMPACT. Click on “Boundary Scan” in the iMPACT flows window on the left top corner. Then right click on the window panel on the right. Select “Initialize Chain”.



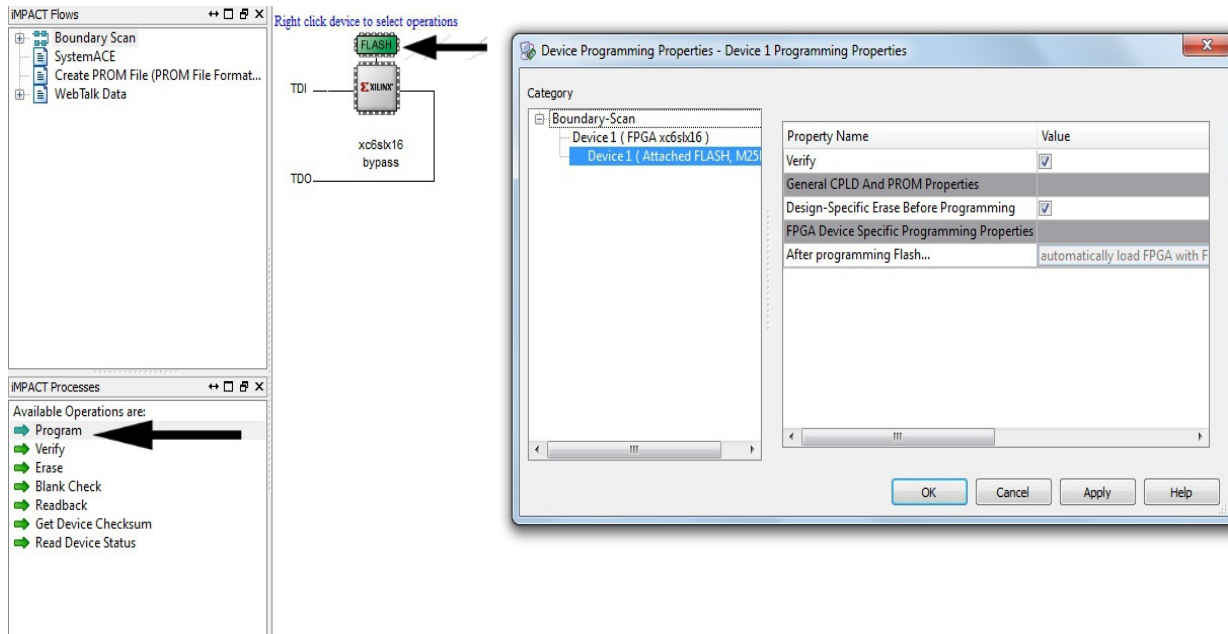
Step 2: If the device is detected properly you will get a pop up window as shown below, Click OK. Then right click on the SPI/BPI (next to the black arrow in the below fig.), select Add SPI/BPI Flash.



Step 3: Select the ".mcs" file we already created and click OK. Now choose "N25Q128" in the dialogue box appeared, then click OK.



Step 4. Click on “Flash”, Double Click on Program, select OK. If the programming is successful, a confirmation message will be displayed.



Length matched GPIOs Pairs

This device is equipped with a maximum of 158 user IOs. Of those, 45 IO pairs are length matched which can be used as differential pairs.

Pin No. on the Header P3	Spartan-6 Differential Pair
9-10	H15-H16
17-18	F16-F15
19-20	F17-F18
21-22	E16-E18
23-24	D17-D18
25-26	C17-C18
27-28	B16-A16
31-32	C14-D14
33-34	B14-A14
37-38	C13-A13
41-42	D12-C12
43-44	B12-A12
47-48	D11-C11
53-54	G11-F10
55-56	B11-A11
57-58	C10-A10
59-60	F9-G9
61-62	D9-C9
63-64	B9-A9
69-70	D8-C8
71-72	B8-A8
75-76	C7-A7

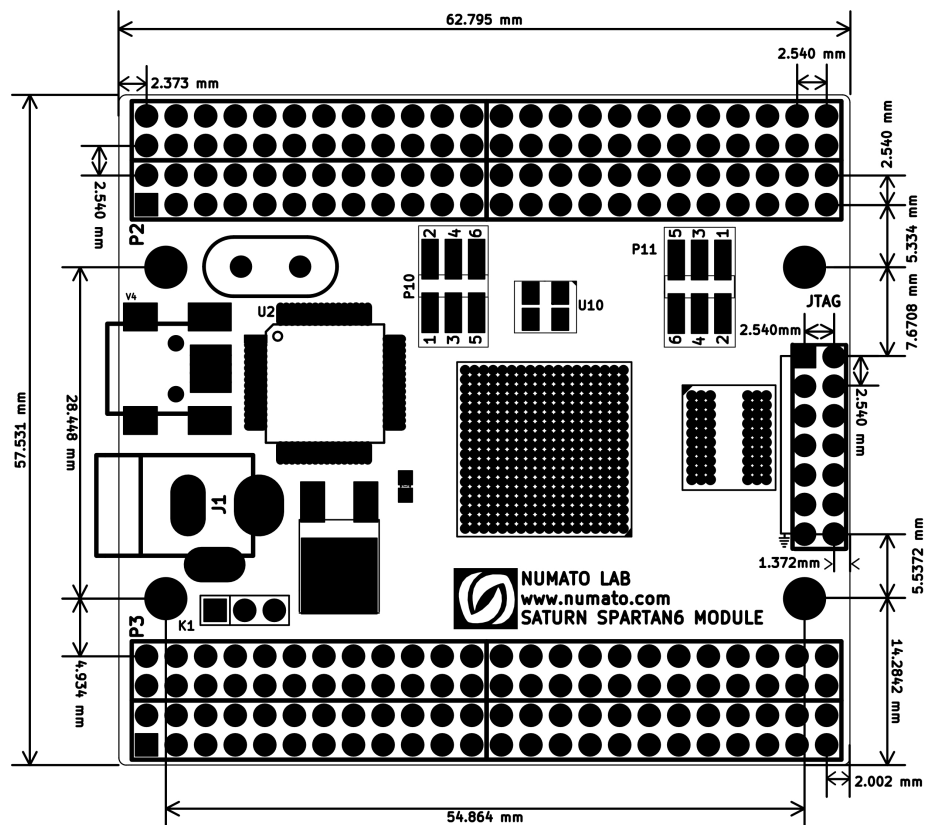
77-78	B6-A6
79-80	C6-D6
81-82	C5-A5
83-84	A4-B4
85-86	B3-A3
87-88	B2-A2
Pin No. on the Header P2	Spartan-6 Differential Pair
7-8	K13-K12
17-18	L12-L13
19-20	L15-L16
21-22	K15-K16
23-24	N15-N16
33-34	T14-V14
57-58	R10-T10
61-62	T9-V9
63-64	R8-T8
69-70	U7-V7
71-72	U8-V8
73-74	R7-T7
79-80	T6-V6
81-82	R5-T5
83-84	U5-V5
85-86	R3-T3
87-88	T4-V4

Technical Specifications

Parameter *	Value	Unit
Basic Specifications		
Number of GPIOs	158 (Max)	
On-board oscillator frequency (FXO-HC536R)	100	MHz
LPDDR Capacity	512	Mb
LPDDR Clock	166	MHz
SPI Flash Memory (N25Q128A13ESE40E)	128	Mb
Power supply voltage (USB or external)	5 – 6	V
FPGA Specifications		
Internal supply voltage relative to GND	–0.5 to 1.32	V
Auxiliary supply voltage relative to GND	–0.5 to 3.75	V
Output drivers supply voltage relative to GND	–0.5 to 3.75	V

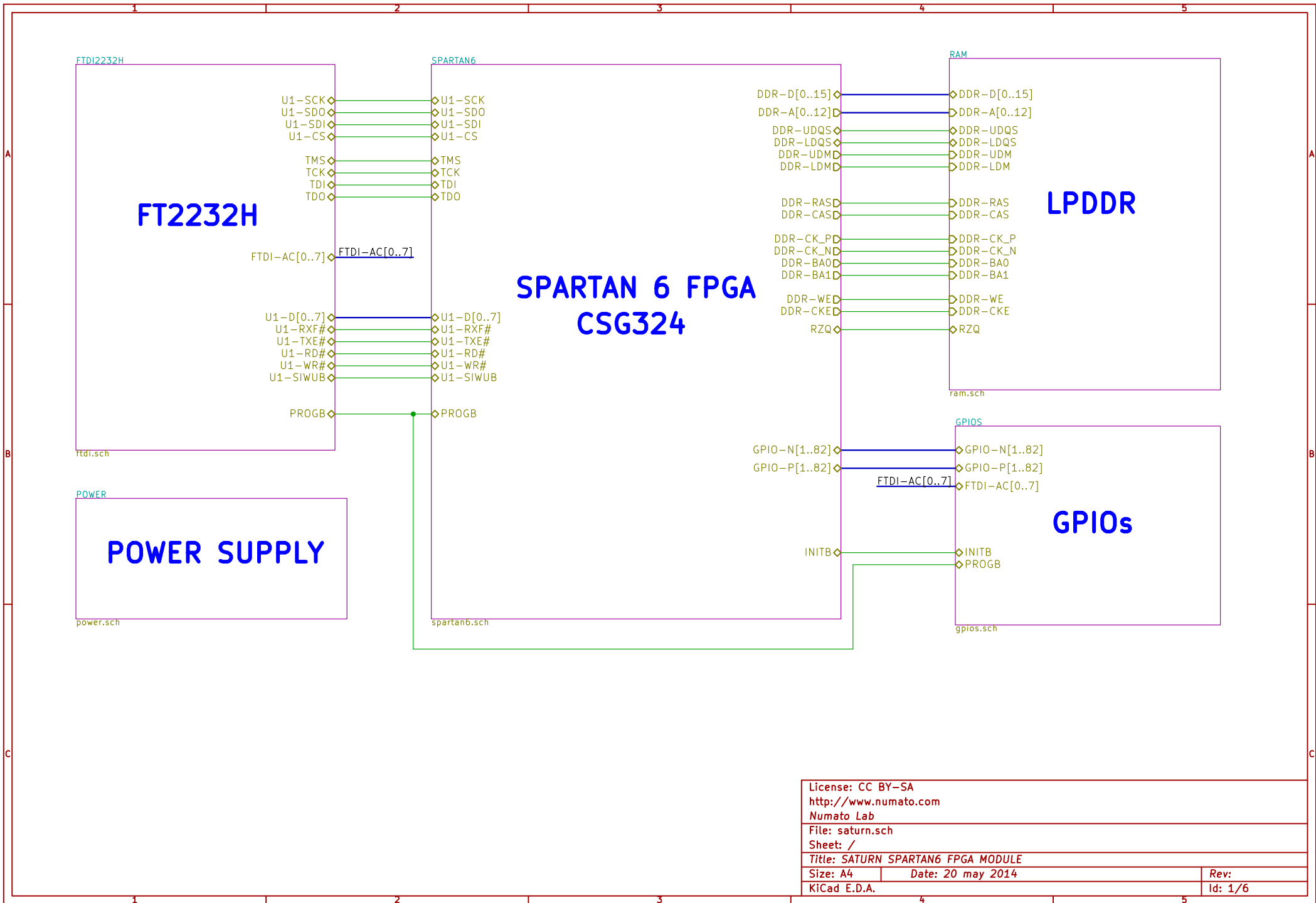
All parameters considered nominal. Numato Systems Pvt Ltd reserve the right to modify products without notice.

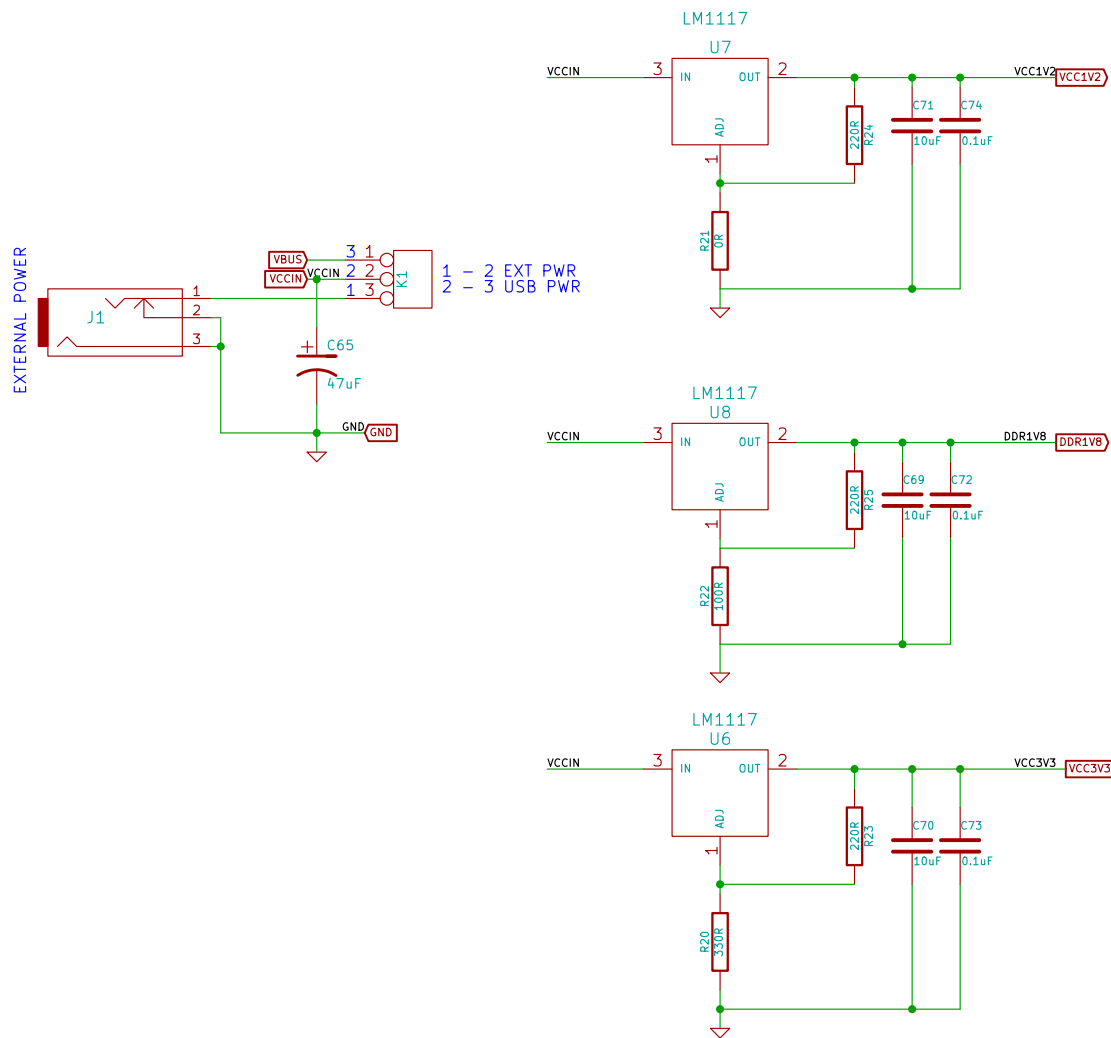
Physical Dimensions



Schematics

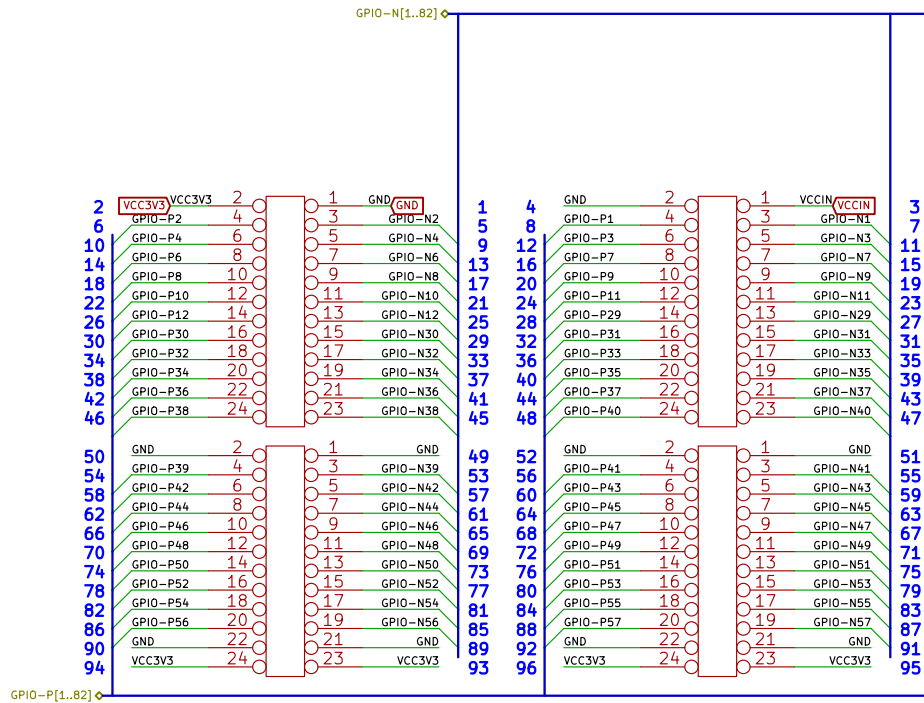
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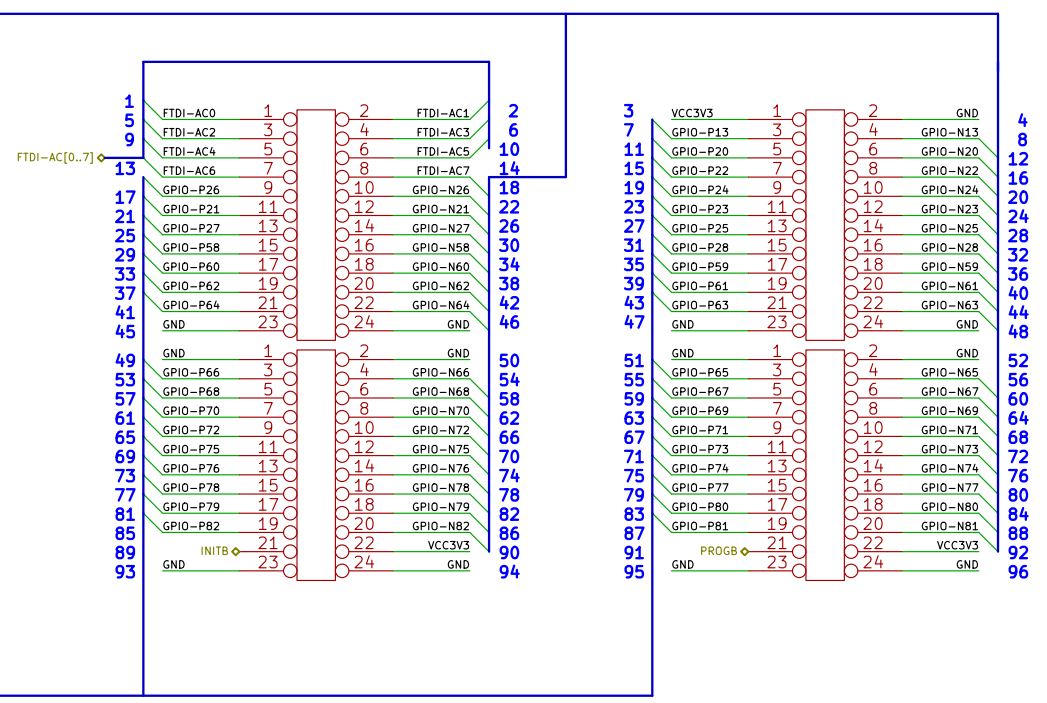


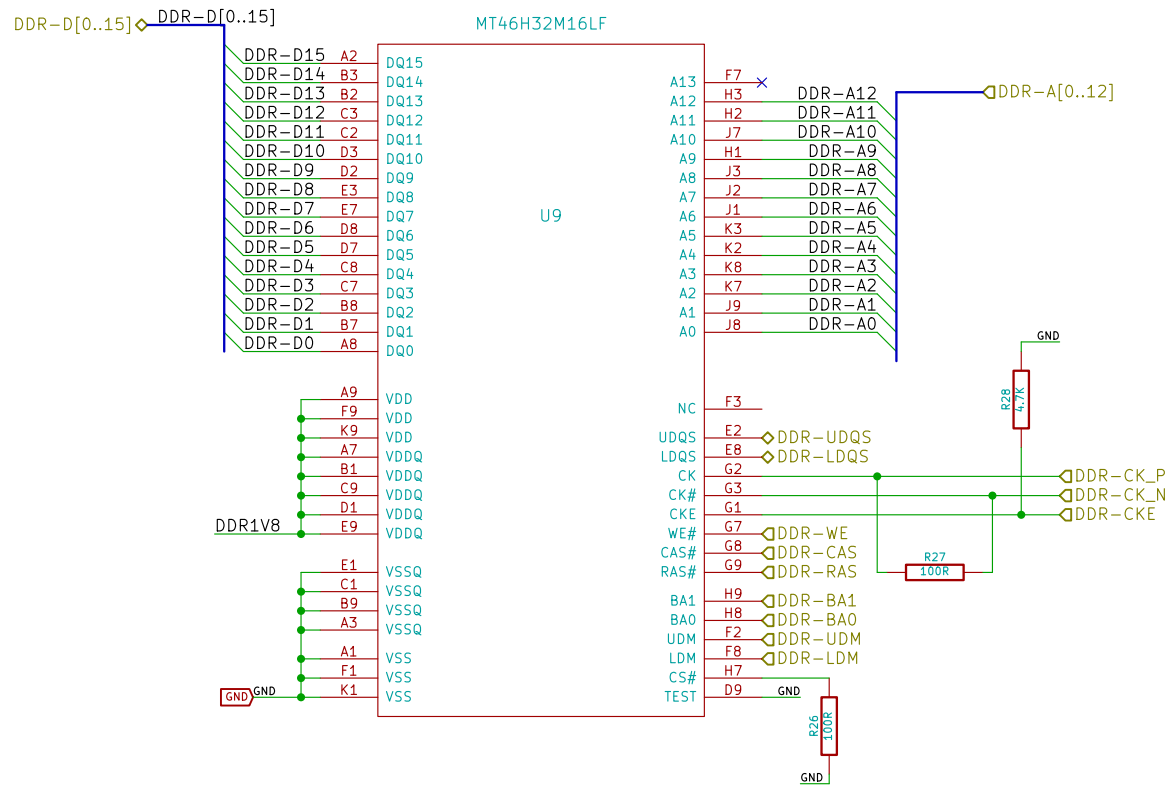
License: CC BY-SA		
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Numato Lab		
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Size: A4	Date: 20 may 2014	Rev:
KiCad E.D.A.		Id: 2/6

HEADER P3

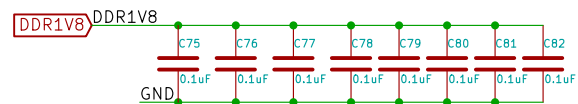


HEADER P2

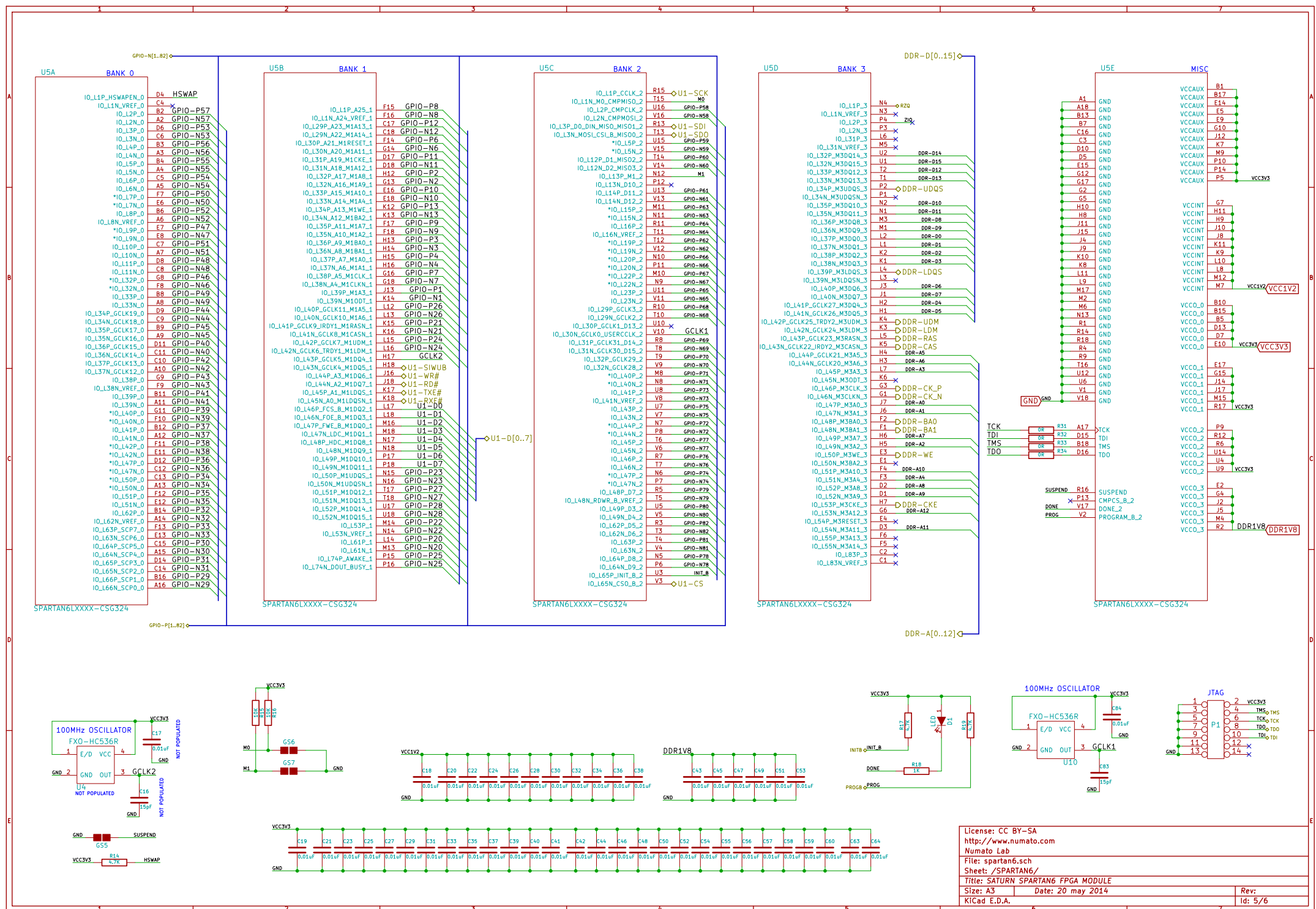


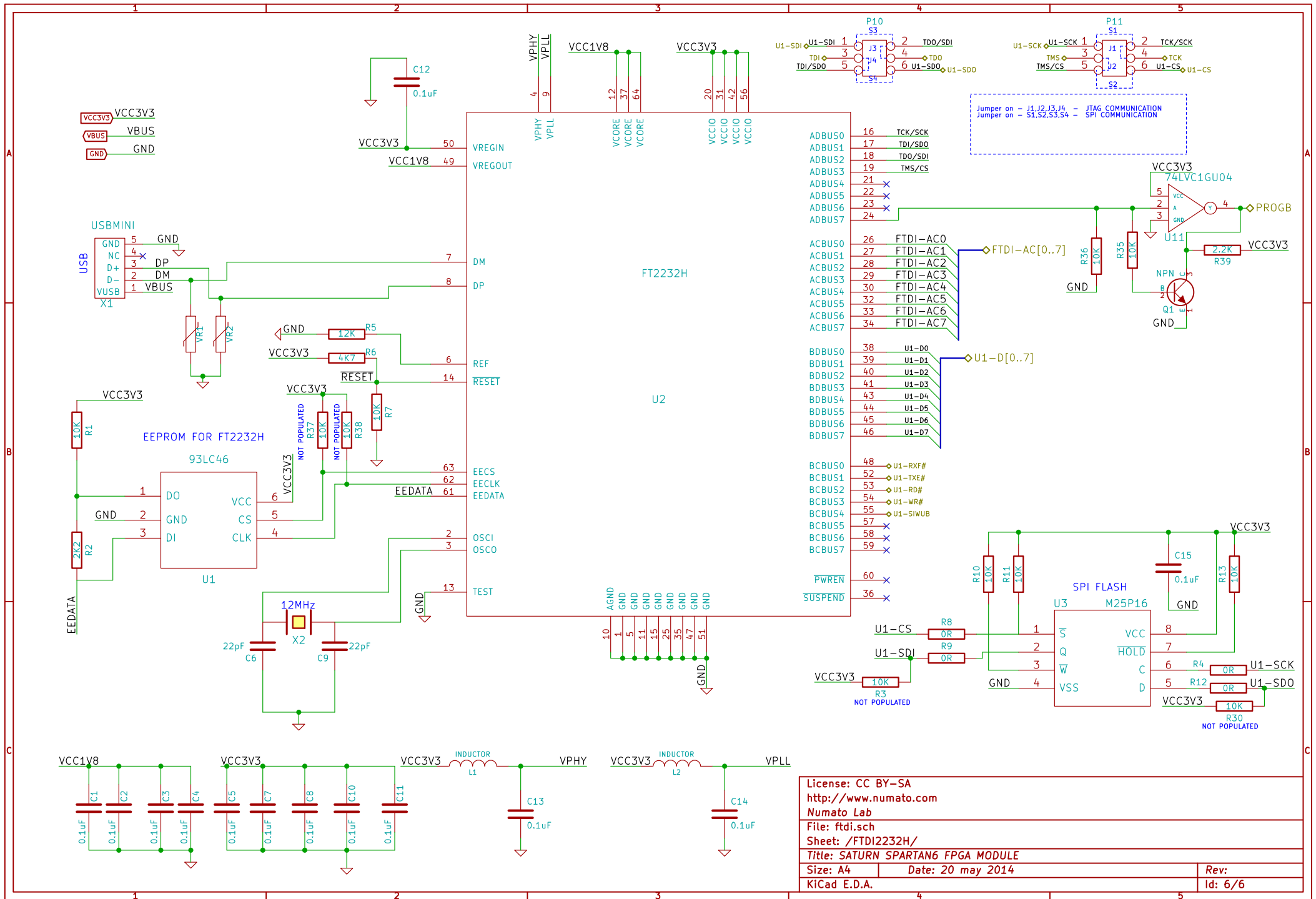


RZQ 100R R29 GND

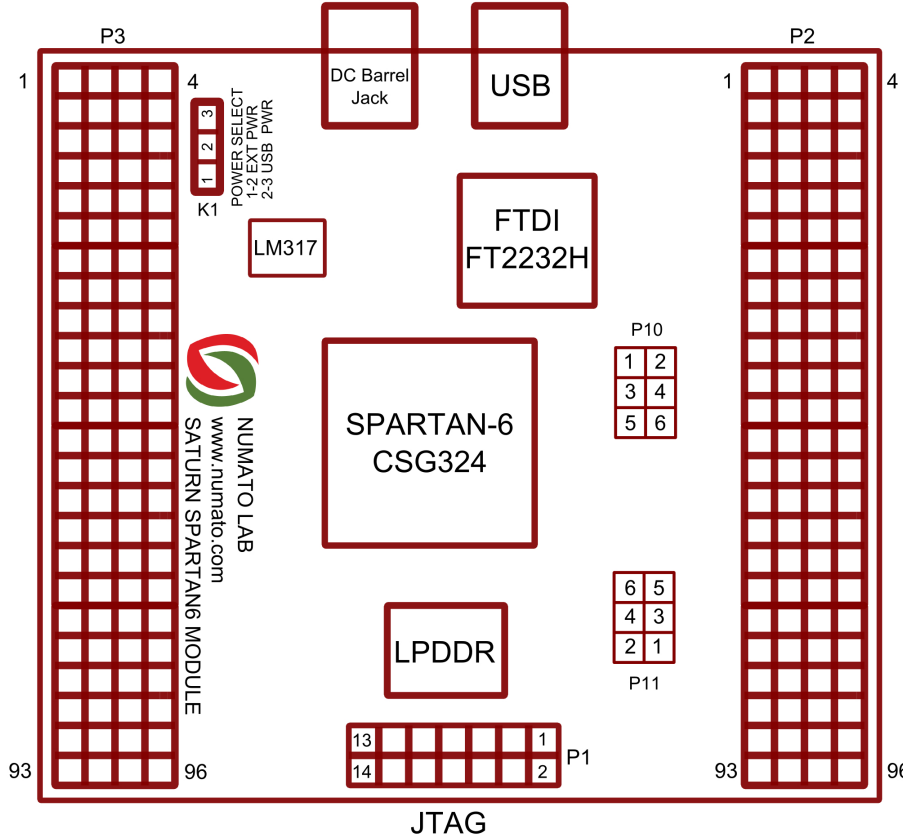


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http://www.numato.com		
Numato Lab		
File: ram.sch		
Sheet: /RAM/		
Title: SATURN SPARTAN6 FPGA MODULE		
Size: A4	Date: 20 may 2014	Rev:
KiCad E.D.A.		Id: 4/6





Saturn V4 GPIO Easy Reference



HEADER P3

Pin No. On The Header	Spartan-6 (CSG324) Pin No.	Pin Description	Pin No. On The Header	Spartan-6 (CSG324) Pin No.	Pin Description	Pin No. On The Header	Spartan-6 (CSG324) Pin No.	Pin Description	Pin No. On The Header	Spartan-6 (CSG324) Pin No.	Pin Description
1	GND	NA	2	3V3	NA	3	VCCIN	NA	4	GND	NA
5	G13	IO_L32N_A16_M1A9_1	6	H12	IO_L32P_A17_M1A8_1	7	K14	IO_L39N_M1ODT_1	8	J13	IO_L39P_M1A3_1
9	H16	IO_L37N_A6_M1A1_1	10	H15	IO_L37P_A7_M1A0_1	11	H14	IO_L36N_A8_M1BA1_1	12	H13	IO_L36P_A9_M1BA0_1
13	G14	IO_L30N_A20_M1A11_1	14	F14	IO_L30P_A21_M1RESET_1	15	G18	IO_L38N_A4_M1CLKN_1	16	G16	IO_L38P_A5_M1CLK_1
17	F16	IO_L1N_A24_VREF_1	18	F15	IO_L1P_A25_1	19	F18	IO_L35N_A10_M1A2_1	20	F17	IO_L35P_A11_M1A7_1
21	E18	IO_L33N_A14_M1A4_1	22	E16	IO_L33P_A15_M1A10_1	23	D18	IO_L31N_A18_M1A12_1	24	D17	IO_L31P_A19_M1CKE_1
25	C18	IO_L29N_A22_M1A14_1	26	C17	IO_L29P_A23_M1A13_1	27	A16	IO_L66N_SCP0_0	28	B16	IO_L66P_SCP1_0
29	A15	IO_L64N_SCP4_0	30	C15	IO_L64P_SCP5_0	31	C14	IO_L65N_SCP2_0	32	D14	IO_L65P_SCP3_0
33	A14	IO_L62N_VREF_0	34	B14	IO_L62P_0	35	E13	IO_L63N_SCP6_0	36	F13	IO_L63P_SCP7_0
37	A13	IO_L50N_0	38	C13	IO_L50P_0	39	E12	IO_L51N_0	40	F12	IO_L51P_0
41	C12	IO_L47N_0	42	D12	IO_L47P_0	43	A12	IO_L41N_0	44	B12	IO_L41P_0
45	E11	IO_L42N_0	46	F11	IO_L42P_0	47	C11	IO_L36N_GCLK14_0	48	D11	IO_L36P_GCLK15_0
49	GND	NA	50	GND	NA	51	GND	NA	52	GND	NA
53	F10	IO_L40N_0	54	G11	IO_L40P_0	55	A11	IO_L39N_0	56	B11	IO_L39P_0
57	A10	IO_L37N_GCLK12_0	58	C10	IO_L37P_GCLK13_0	59	F9	IO_L38N_VREF_0	60	G9	IO_L38P_0
61	C9	IO_L34N_GCLK18_0	62	D9	IO_L34P_GCLK19_0	63	A9	IO_L35N_GCLK16_0	64	B9	IO_L35P_GCLK17_0
65	F8	IO_L32N_0	66	G8	IO_L32P_0	67	E8	IO_L9N_0	68	E7	IO_L9P_0
69	C8	IO_L11N_0	70	D8	IO_L11P_0	71	A8	IO_L33N_0	72	B8	IO_L33P_0
73	E6	IO_L7N_0	74	F7	IO_L7P_0	75	A7	IO_L10N_0	76	C7	IO_L10P_0
77	A6	IO_L8N_VREF_0	78	B6	IO_L8P_0	79	C6	IO_L3N_0	80	D6	IO_L3P_0
81	A5	IO_L6N_0	82	C5	IO_L6P_0	83	A4	IO_L5N_0	84	B4	IO_L5P_0
85	A3	IO_L4N_0	86	B3	IO_L4P_0	87	A2	IO_L2N_0	88	B2	IO_L2P_0
89	GND	NA	90	GND	NA	91	GND	NA	92	GND	NA
93	3V3	NA	94	3V3	NA	95	3V3	NA	96	3V3	NA

HEADER P2

Pin No. On The Header	Spartan-6 (CSG324) Pin No.	Pin Description	Pin No. On The Header	Spartan-6 (CSG324) Pin No.	Pin Description	Pin No. On The Header	Spartan-6 (CSG324) Pin No.	Pin Description	Pin No. On The Header	Spartan-6 (CSG324) Pin No.	Pin Description
1	FTDI-26	ACBUS0	2	FTDI-27	ACBUS1	3	3V3	NA	4	GND	NA
5	FTDI-28	ACBUS2	6	FTDI-29	ACBUS3	7	K12	IO_L34P_A13_M1WE_1	8	K13	IO_L34N_A12_M1BA2_1
9	FTDI-30	ACBUS4	10	FTDI-32	ACBUS5	11	L14	IO_L61P_1	12	M13	IO_L61N_1
13	FTDI-33	ACBUS6	14	FTDI-34	ACBUS7	15	M14	IO_L53P_1	16	N14	IO_L53N_VREF_1
17	L12	IO_L40P_GCLK11_M1A5_1	18	L13	IO_L40N_GCLK10_M1A6_1	19	L15	IO_L42P_GCLK7_M1UDM_1	20	L16	IO_L42N_GCLK6_TRDY1_M1LDM_1
21	K15	IO_L41P_GCLK9_IRDY1_M1RASN_1	22	K16	IO_L41N_GCLK8_M1CASN_1	23	N15	IO_L50P_M1UDQS_1	24	N16	IO_L50N_M1UDQSN_1
25	T17	IO_L51P_M1DQ12_1	26	T18	IO_L51N_M1DQ13_1	27	P15	IO_L74P_AWAKE_1	28	P16	IO_L74N_DOUT_BUSY_1
29	U16	IO_L2P_CMPCLK_2	30	V16	IO_L2N_CMPMOSI_2	31	U17	IO_L52P_M1DQ14_1	32	U18	IO_L52N_M1DQ15_1
33	T14	IO_L12P_D1_MISO2_2	34	V14	IO_L12N_D2_MISO3_2	35	U15	IO_L5P_2	36	V15	IO_L5N_2
37	T12	IO_L19P_2	38	V12	IO_L19N_2	39	U13	IO_L14P_D11_2	40	V13	IO_L14N_D12_2
41	R11	IO_L16P_2	42	T11	IO_L16N_VREF_2	43	M11	IO_L15P_2	44	N11	IO_L15N_2
45	GND	NA	46	GND	NA	47	GND	NA	48	GND	NA
49	GND	NA	50	GND	NA	51	GND	NA	52	GND	NA
53	N10	IO_L20P_2	54	P11	IO_L20N_2	55	U11	IO_L23P_2	56	V11	IO_L23N_2
57	R10	IO_L29P_GCLK3_2	58	T10	IO_L29N_GCLK2_2	59	M10	IO_L22P_2	60	N9	IO_L22N_2
61	T9	IO_L32P_GCLK29_2	62	V9	IO_L32N_GCLK28_2	63	R8	IO_L31P_GCLK31_D14_2	64	T8	IO_L31N_GCLK30_D15_2
65	N7	IO_L44P_2	66	P8	IO_L44N_2	67	M8	IO_L40P_2	68	N8	IO_L40N_2
69	U7	IO_L43P_2	70	V7	IO_L43N_2	71	U8	IO_L41P_2	72	V8	IO_L41N_VREF_2
73	R7	IO_L46P_2	74	T7	IO_L46N_2	75	N6	IO_L47P_2	76	P7	IO_L47N_2
77	N5	IO_L64P_D8_2	78	P6	IO_L64N_D9_2	79	T6	IO_L45P_2	80	V6	IO_L45N_2
81	R5	IO_L48P_D7_2	82	T5	IO_L48N_RDWR_B_VREF_2	83	U5	IO_L49P_D3_2	84	V5	IO_L49N_D4_2
85	R3	IO_L62P_D5_2	86	T3	IO_L62N_D6_2	87	T4	IO_L63P_2	88	V4	IO_L63N_2
89	U3	IO_L65P_INIT_B_2	90	3V3	NA	91	V2	PROGRAM_B_2	92	3V3	NA
93	GND	NA	94	GND	NA	95	GND	NA	96	GND	NA