Building Generic Bus Properties

Daniel E. Gisselquist, Ph.D.
March, 2023

Gisselquist Technology, LLC
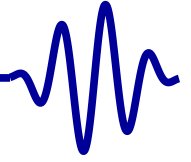
AXIN Protocol

Signals

Global Signals	AXI Stream	AXIN
ACLK	TVALID	VALID
ARESETN	TREADY	READY
	TDATA	DATA
	TSTRB	BYTES
	TKEEP	
	TLAST	LAST
		ABORT
	TUSER	

Signals

Global Signals	AXI Stream	AXIN
ACLK ARESETN	TVALID TREADY	VALID READY
	TDATA	DATA
	TSTRB	BYTES
	TKEEP	
	TLAST	LAST ABORT
	TUSER	

These signals arean't really needed

Signals

Global Signals	AXI Stream	AXIN
ACLK ARESETN	TVALID TREADY	VALID READY
	TDATA	DATA
	~~TSTRB~~	BYTES
	~~TKEEP~~	
	TLAST	LAST
		ABORT
	~~TUSER~~	

We'll add these two new ones

ABORT

1. ABORT may be raised at any time
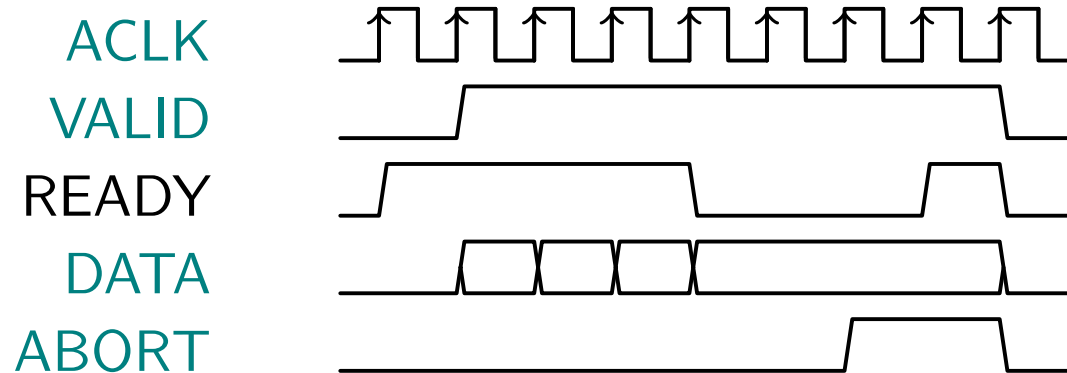
It may be raised while `VALID && !READY`.
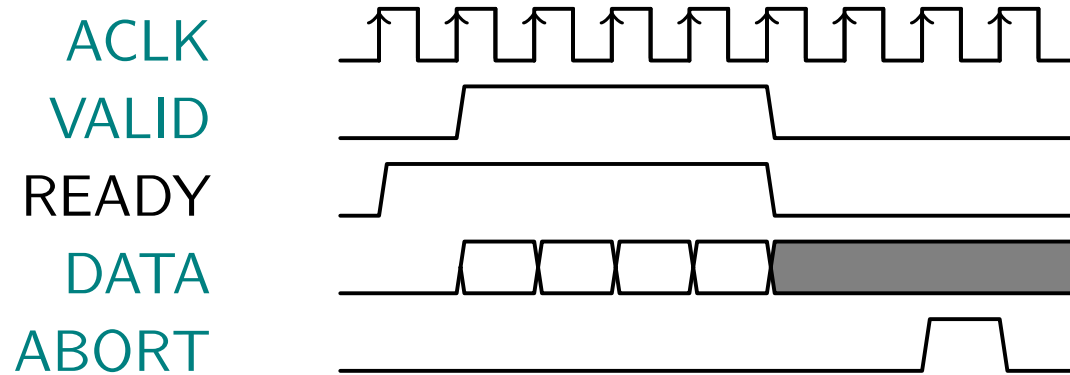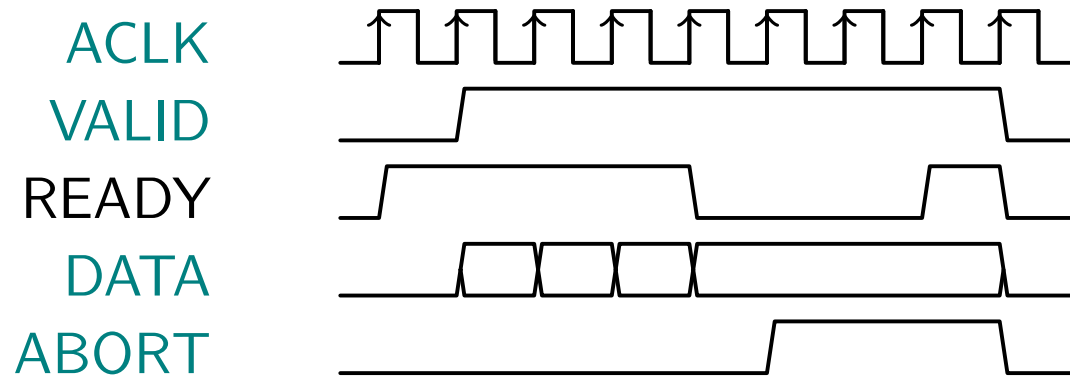
ABORT

1. ABORT may be raised at any time

It may be raised even without raising VALID.

ABORT

1. ABORT may be raised at any time
2. ABORT may be only be released if not stalled


```
property assert (@(posedge ACLK)
        disable iff (!ARESETN)
        (VALID && !READY && ABORT)
                |=> VALID && ABORT);
```

ABORT

1. ABORT may be raised at any time
2. ABORT may be only be released if not stalled
3. While legal, it doesn't make sense to raise ABORT if `VALID && LAST`.
4.

If `VALID && LAST` are both true, the packet has successfully, entered the downstream registers. Raising ABORT at this point makes little sense.
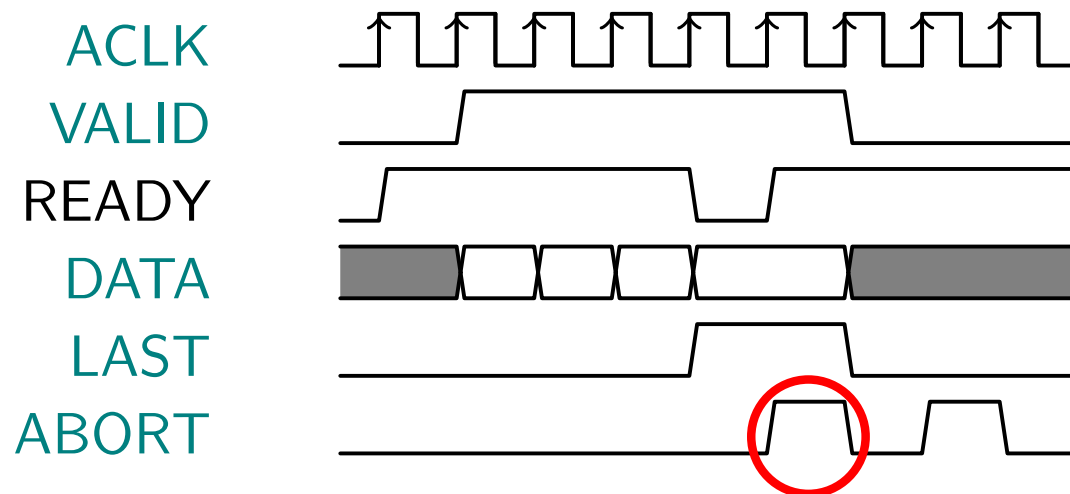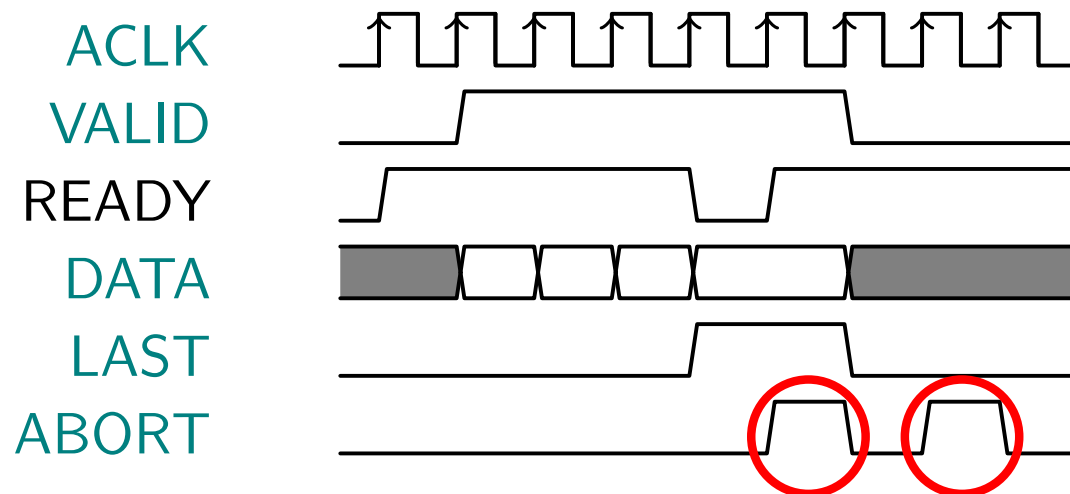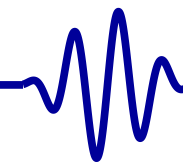
ABORT

1. ABORT may be raised at any time
2. ABORT may be only be released if not stalled
3. While legal, it doesn't make sense to raise ABORT if `VALID && LAST`.
4. Nor does it make sense to raise ABORT if a packet hasn't started.

If `VALID && LAST` are both true, the packet has successfully, entered the downstream registers. Raising ABORT at this point makes little sense.
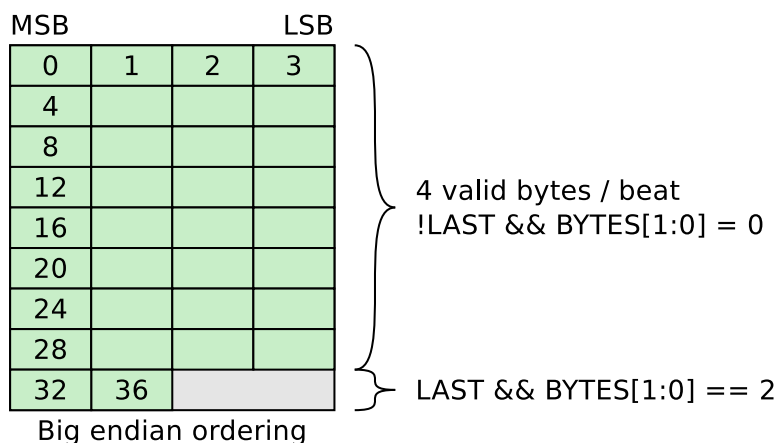
BYTES

1. All beats are packed
2. The BYTES field contains $clog2(DW/8)$ bits.
   If ever BYTES $== 0$, then there are $DW/8$ valid bytes implied.
3. Only the last beat can contain fewer than DW/8 bytes
4. The last beat cannot be empty. It must have at least one byte.
5. Ordering can be big   endian

MSB			LSB
0	1	2	3
4			
8			
12			
16			
20			
24			
28			
32	36		

4 valid bytes / beat
!LAST && BYTES[1:0] = 0

LAST && BYTES[1:0] == 2

Big endian ordering

BYTES

1. All beats are packed
2. The BYTES field contains $clog2(DW/8)$ bits.
   If ever BYTES $== 0$, then there are $DW/8$ valid bytes implied.
3. Only the last beat can contain fewer than DW/8 bytes
4. The last beat cannot be empty. It must have at least one byte.
5. Ordering can be big or little endian

MSB			LSB
3	2	1	0
			4
			8
			12
			16
			20
			24
			28
		36	32

4 valid bytes / beat
!LAST && BYTES[1:0] = 0

LAST && BYTES[1:0] == 2

Little endian ordering