bq77915 3-Series to 5-Series Stackable Ultra-Low Power Primary Protector with Autonomous Cell Balancing and HIBERNATE Mode

1 Features

- Ultra-Low Quiescent Current: 8 µA typ. (NORMAL Mode), 2 µA (HIBERNATE Mode)
- Full Suite of Voltage, Current, and Temperature Protections
- Smart Passive Cell Balancing Removes Cell-to-Cell Imbalance
- Scalable Cell Count from 3 Series to 20 Series or More
- Voltage Protection (Accuracy ±10 mV for OV, ±18 mV for UV)
  - Overvoltage: 3 V to 4.575 V
  - Undervoltage: 1.2 V to 3 V
- Open Cell and Open Wire Detection (OW)
- Current Protection
  - Overcurrent Discharge 1: –10 mV to –85 mV
  - Overcurrent Discharge 2: –20 mV to –170 mV
  - Short Circuit Discharge: –40 mV to –340 mV
- Temperature Protection
  - Overtemperature Charge: 45°C or 50°C
  - Overtemperature Discharge: 65°C or 70°C
- Additional Features
  - Independent Charge (CHG) and Discharge (DSG) FET Drivers
  - Smart Cell Balancing Algorithm with Integrated FETs (up to 50-mA Balancing Current), also Supports External FETs for Higher Cell-Balancing Current
  - Ultra-Low Power HIBERNATE Mode
  - High 36-V Absolute Maximum Rating Per Cell Input
  - Resistor Programmable Overcurrent (OCD1/2) Delay
- SHUTDOWN Mode: 0.5-µA Maximum

2 Applications

- Power Tools, Garden Tools
- Robotic Cleaners, Vacuum Cleaners, Hoverboards
- eBikes
- 10.8-V to 72-V Packs

3 Description

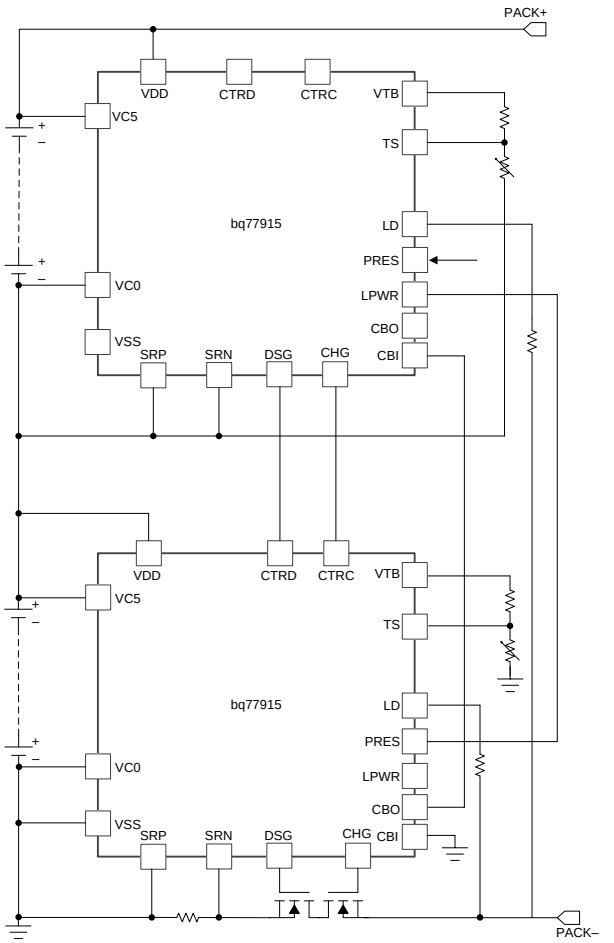
The bq77915 device is a low-power battery pack protector that implements a suite of voltage, current, and temperature protections and a smart cell balancing algorithm without microcontroller (MCU) control. The device's stackable interface provides simple scaling to support battery cell applications from 3 series to 20 series or more. Protection thresholds and delays are factory-programmed and available in a variety of configurations. Separate overtemperature and undertemperature thresholds for discharge (OTD and UTD) and charge (OTC and UTC) are provided for added flexibility.

Device Information(1)

Part Number	Package	Body Size (NOM)
bq77915	TSSOP–24	7.70 mm × 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic



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4 Revision History

DATE	REVISION	NOTES
March 2018	*	Advance Information

5 Description (continued)

The device achieves pack protection via the integrated independent CHG and DSG low-side NMOS FET drivers, which may be disabled through two control pins. These control pins may also be used to achieve cell protection solutions for higher series (6 series and beyond) in a simple and economical manner. To do this, simply cascade a higher device CHG and DSG outputs to the immediate lower device control pins. For added flexibility, discharge overcurrent protection delays can be programmed using a resistor connected from the OCDP pin to VSS.

The bq77915 protector achieves a smart passive cell-balancing algorithm via integrated FETs for cell balancing currents up to 50 mA. For higher cell-balancing current requirements, external FETs can be connected. A HIBERNATE mode intended for shipping and storage of the battery packs enables ultra-low power operation.

The bq77915 protector is intended for battery packs where no host monitoring is required.

6 Device Comparison Table

Unless otherwise specified, the device has, by default, a state comparator enabled with a 1.875-mV threshold. A filtered fault detection is used by default. Contact Texas Instruments for future configuration options or PRODUCT PREVIEW devices.

Part Number	OV			UV				OW	OCD1		OCD2		SCD		OCC	Current Fault Recovery		Temperature (°C)(1)				Cell Balancing	
	Threshold (mV)	Delay (s)	Hyst (mV)	Thresh (mV)	Delay (s)	Hyst (mV)	Load Removal Recovery (Y/N)	Current (nA)	Threshold (mV)	Delay (ms)	Threshold (mV)	Delay (ms)	Threshold (mV)	Delay (ms)	Threshold (mV)	Delay (ms)	Method	OTD	OTC	UTD	UTC	VOV – VFC (mV)	VCBTH – VCBTL (mV)
bq7791500	4200	1	200	2900	1	400	Y	100	60	180	60	180	120	0.96	60	N/A	Load Removal only (OCD1, OCD2, SCD)/Load Detection Only (OCC)	65	45	–10	0	100	100

(1) These thresholds are targets, based on temperature, but they are dependent on external components that could vary based on customer selection. The circuit is based on a 103AT NTC thermistor connected to TS and VSS, and a 10-kΩ resistor connected to VTB and TS. Actual thresholds must be determined in mV; refers to the over- and undertemperature mV threshold in the *Electrical Characteristics* table.

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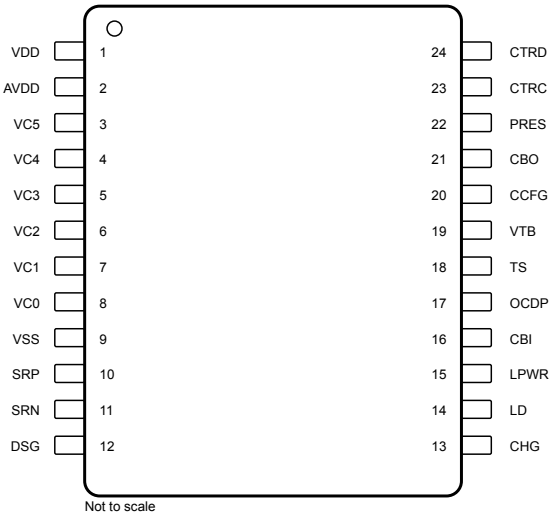
7 Pin Configuration and Functions

PW Package
24-Pin TSSOP
Top View



Not to scale

Pin Functions

NUMBER	NAME	I/O	DESCRIPTION
1	VDD	P(1)	Supply voltage
2	AVDD	O	Analog supply (only connect to a capacitor)
3	VC5	I	Cell voltage sense inputs
4	VC4	I	
5	VC3	I	
6	VC2	I	
7	VC1	I	
8	VC0	I	
9	VSS	P	Analog ground
10	SRP	I	Current sense input connecting to the battery side of the sense resistor
11	SRN	I	Current sense input connecting to the pack side of the sense resistor
12	DSG	O	DSG FET driver output
13	CHG	O	CHG FET driver output
14	LD	I	PACK– load removal detection
15	LPWR	O	HIBERNATE mode communication pin. Connect to the PRES pin of the lower device in a stack configuration. For a single device, leave LPWR pin floating.
16	CBI	I	Cell balancing input. Leave the CBI pin floating to disable cell balancing. Drive the pin low to enable cell balancing. In a stacked configuration, connect the CBI pin of an upper devices to the CBO pin of the immediate lower device.
17	OCDP	I	Connecting a resistor from this pin to VSS programs the OCD1/2 fault detection delay. Connect to a 10-MΩ resistor to VSS for the upper devices in a stack.
18	TS	I	Thermistor measurement input. Connect a 10-kΩ resistor to VSS pin if the function is not used.
19	VTB	O	Thermistor bias output
20	CCFG	I	Cell in series-configuration input
21	CBO	O	Cell balancing output, connect through a 10-k resistor to the CBI pin of the upper device in a stacked configuration. For a single device, leave CBO pin floating.

(1) I = Input, O = Output, P = Power

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Pin Functions (continued)

NUMBER	NAME	I/O	DESCRIPTION
22	PRES	I	HIBERNATE mode input. Drive high for NORMAL mode operation. Leave the PRES pin floating for HIBERNATE mode. Connect to the LPWR pin of the upper device in a stack configuration.
23	CTRC	I	CHG and DSG override inputs
24	CTRD	I	

8 Specifications

8.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted). All values are referenced to VSS unless otherwise noted.(1)

			MIN	MAX	UNIT
V_I	Input voltage	VDD, VC5, VC4, VC3, VC2, VC1, CTRD, CTRC	–0.3	36	V
		LD	–30	20	V
		PRES	–0.3	36	V
		VC0, SRN, SRP, TS, AVDD, CCFG, CBI	–0.3	3.6	V
V_O	Output voltage range	DSG	–0.3	20	V
		CHG	–30	20	V
		LPWR	–30	3.6	V
		VTB	–0.3	3.6	V
		CBO	–0.3	36	V
I_I	Input current	LD, CHG		500	µA
		DSG		1	mA
I_O	Output current	CHG, DSG		1	mA
		Cell Balancing current (VC5, VC4, VC3, VC2, VC1, VC0)		50	mA
Storage temperature, T_{STG} (Storage Temperature Range)			–65	150	°C
Lead temperature, T_{SOLDER} (Soldering, 10s)				300	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

8.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS–001(1)	±1000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±250	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

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8.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted).

			MIN	MAX	UNIT
V_{BAT}	Supply voltage	VDD	3	25	V
V_I	Input voltage	VC5-VC4, VC4-VC3, VC3-VC2, VC2-VC1, VC1-VC0	0	5	V
		CTRD, CTRC	0	(VDD + 5)	
		CCFG, CBI	0	AVDD	
		PRES	0	16	
		SRN, SRP	–0.2	0.8	
		LD	0	16	
		TS	0	VTB	
V_O	Output voltage	CHG, DSG	0	16	V
		VTB, AVDD, LPWR	0	3	
		CBO	0	VDD	
T_{OPR}	Operating free-range temperature		–40	85	°C
R_{INE}	Cell monitor filter resistance (External Cell balancing)		1 kΩ +/–5%		
C_{INE}	Cell monitor filter capacitance (External Cell balancing)		0.1 µF +/–10%		
R_{INI}	Cell monitor filter resistance (Internal Cell balancing, 50-mA balancing current at 4.2-V cell voltage)		33 Ω +/–5%		
C_{INI}	Cell monitor filter capacitance (Internal Cell balancing)		1 µF +/–10%		
R_{VDD}	Supply voltage filter resistance		1 kΩ +/–5%		
C_{VDD}	Supply voltage filter capacitance		1 µF +/–20%		
R_{TS}	Thermistor		103AT 10 kΩ +/–3%		
R_{TS_PU}	Thermistor pullup resistor to VTB		10 kΩ +/–1%		
R_{GS_CHG}	CHG FET gate-source resistor		1 MΩ +/–5%		
R_{GS_DSG}	DSG FET gate-source resistor		1 MΩ +/–5%		
R_{DSG}	DSG gate resistor. System designers should adjust this parameter to meet the desirable FET rise/fall time.		4.5 kΩ +/–5%		
R_{CHG}	CHG gate resistor	System designers should adjust this parameter to meet the desirable FET rise/fall time.	1 kΩ +/–5%		
		If additional components are used to protect the CHG FET and/or to enable load removal detection for UV recovery	1 MΩ +/–5%		
R_{CTRC}	CTRC current limit resistor		10 MΩ +/–5%		
R_{CTRD}	CTRD current limit resistor		10 MΩ +/–5%		
R_{LD}	LD resistor for load removal detection		470 KΩ +/–5%		
R_{CB}	Resistor between CBO of lower device and CBI of upper device		10 kΩ +/–5%		
R_{HIB}	Resistor between LPWR of upper device and PRES of lower device		10 kΩ +/–5%		
R_{SNS}	Current sense resistor for current protection. System designers should change this parameter according to the application current protection requirement.		1 mΩ +/–1%		

8.4 Thermal Information

THERMAL METRIC[1]		bq77915 PW (TSSOP) 24 PINS	UNITS
$R_{\theta JA}$	Junction-to-ambient thermal resistance	88.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	26.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	43.5	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

Thermal Information (continued)

THERMAL METRIC(1)		bq77915 PW (TSSOP) 24 PINS	UNITS
ψ_{JT}	Junction-to-top characterization parameter	1.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	43	°C/W

8.5 Electrical Characteristics

Typical values stated at T_A = 25ºC and VDD = 20 V. MIN and MAX values stated with T_A = –40ºC to +85ºC and VDD = 3 to 25 V unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE						
V_{POR}	POR threshold	VDD rising, 0 to 6 V			4	V
V_{SHUT}	Shutdown threshold	VDD falling, 6 to 0 V	2		3.25	V
V_{AVDD}	AVDD voltage	C_{VDD} = 1 µF	2.1		3.6	V
SUPPLY AND LEAKAGE CURRENT						
I_{CC}	NORMAL mode current	Cell1 through Cell5 = 4 V, VDD = 20 V, No Cell Balancing		8	13	µA
		Cell Balancing Cells 3, 4 or 5		48		µA
I_{HIB}	HIBERNATE mode current	Cell1 through Cell5 = 4 V, VDD = 20 V, HIBERNATE mode		2	3	µA
I_{CFAULT}	Fault condition current	State comparator on		10	15	µA
I_{OFF}	SHUTDOWN mode current	VDD < V_{SHUT}			0.5	µA
$I_{LKG\_OW\_DIS}$	Input leakage current at VCx pins	All cell voltages = 4 V, Open-wire disable configuration	–100	0	+100	nA
I_{OW_100nA}	Open wire sink current at VCx pins	All cell voltages = 4 V, 100-nA configuration	30	110	175	nA
I_{OW_200nA}	Open wire sink current at VCx pins	All cell voltages = 4 V, 200-nA configuration	95	210	315	nA
I_{OW_400nA}	Open wire sink current at VCx pins	All cell voltages = 4 V, 400-nA configuration	220	425	640	nA
I_{OWA}	Open wire sink current accuracy	cell voltage = 4 V	–50%		+50%	
PROTECTION ACCURACIES						
V_{OV}	Overvoltage programmable threshold range		3000		4575	mV
V_{UV}	Undervoltage programmable threshold range		1200		3000	mV
V_{VA}	OV, UV detection accuracy	T_A = 25ºC, OV detection accuracy	–10		10	mV
		T_A = 25ºC, UV detection accuracy	–18		18	mV
		T_A = 0 to 60ºC	–28		26	mV
		T_A = –40 to 85ºC	–40		40	mV
V_{HYS_OV}	OV hysteresis programmable threshold range		0		400	mV
V_{HYS_UV}	UV hysteresis programmable threshold range		0		800	mV
V_{OTD}	Overtemperature in discharge programmable threshold	Threshold for 65°C	19.71%	20.56%	21.86%	VTB
		Threshold for 70°C	17.36%	18.22%	19.51%	
$V_{OTD(REC)}$	Overtemperature in discharge recovery	Recovery threshold at 55°C for when V_{OTD} is at 65°C	25.24%	26.12%	27.44%	VTB
		Recovery threshold at 60°C for when V_{OTD} is at 70°C	22.12%	23.20%	24.24%	
V_{OTC}	Overtemperature in charge programmable threshold	Threshold for 45°C	32.14%	32.94%	34.54%	VTB
		Threshold for 50°C	29.15%	29.38%	31.45%	

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Electrical Characteristics (continued)

Typical values stated at T_A = 25ºC and VDD = 20 V. MIN and MAX values stated with T_A = –40ºC to +85ºC and VDD = 3 to 25 V unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{OTC(REC)}$	Overtemperature in charge recovery	Recovery threshold at 35°C for when V_{OTD} is at 45°C	38.63%	40.97%	40.99%	VTB
		Recovery threshold at 40°C for when V_{OTD} is at 50°C	36.18%	36.82%	38.47%	
V_{UTD}	Undertemperature in discharge programmable threshold	Threshold for –20°C	86.41%	87.14%	89.72%	VTB
		Threshold for –10°C	80.04%	80.94%	83.10%	
$V_{UTD(REC)}$	Undertemperature in discharge recovery	Recovery threshold at –10°C for when V_{UTD} is at –20°C	80.04%	80.94%	83.10%	VTB
		Recovery threshold at 0°C for when V_{UTD} is at –10°C	71.70%	73.18%	74.86%	
V_{UTC}	Undertemperature in charge programmable threshold	Threshold for –5°C	75.06%	77.22%	78.32%	VTB
		Threshold for 0°C	71.70%	73.18%	74.86%	
$V_{UTC(REC)}$	Undertemperature in Charge Recovery	Recovery threshold at 5°C for when V_{UTC} is at –5°C	68.80%	69.73%	71.71%	VTB
		Recovery threshold at 10°C for when V_{UTC} is at 0°C	64.67%	65.52%	67.46%	
V_{OCC}	Overcurrent charge programmable threshold range, (V_{SRP} – V_{SRN})		5		80	mV
V_{OCD1}	Overcurrent discharge 1 programmable threshold range, (V_{SRP} – V_{SRN})		–85		–10	mV
V_{OCD2}	Overcurrent discharge 2 programmable threshold range, (V_{SRP} – V_{SRN})		–170		–20	mV
V_{SCD}	Short circuit discharge programmable threshold range, (V_{SRP} – V_{SRN})		–340		–40	mV
V_{CCAL}	OCC, OCD1 detection accuracy at lower thresholds	V_{OCD1} > –20 mV, V_{OCC} < 20 mV	–30%		30%	
V_{CCAH}	OCC, OCD1, OCD2, SCD detection accuracy	V_{OCD1} ≤ –20 mV; V_{OCC} > 20 mV; all OCD2 and SCD threshold ranges	–20%		20%	
V_{OW}	Open-wire fault voltage threshold at VCx per cell with respect to $VC_{x–1}$	Voltage falling on VCx, 3.6 V to 0 V	450	500	550	mV
V_{OW_HYS}	Hysteresis for open wire fault	Voltage rising on VCx, 0 V to 3.6 V		100		mV
CHARGE AND DISCHARGE FET DRIVERS						
V_{FETON}	CHG/DSG on	VDD ≥ 12 V, CL = 10 nF	11	12	14	V
		VDD < 12 V, CL = 10 nF	VDD – 1.5		VDD	V
V_{FETOFF}	CHG/DSG off	No load when CHG/DSG is off.			0.5	V
R_{CHGOFF}	CHG off resistance	CHG off for > t_{CHGPDN} and pin held at 100 mV	0.4	0.5	0.6	kΩ
R_{DSGOFF}	DSG off resistance	DSG off and pin held at 100 mV		10	16	Ω
$I_{CHG(CLAMP)}$	CHG clamp current	CHG off and pin held at 18 V			450	µA
$V_{CHG(CLAMP)}$	CHG clamp voltage	$I_{CHG(CLAMP)}$ = 300 µA	16	18	20.5	V
t_{CHGON}	CHG on rise time	CL = 10 nF, 10% to 90%		50	150	µs
t_{DSGON}	DSG on rise time	CL = 10 nF, 10% to 90%		2	75	µs
t_{CHGOFF}	CHG off fall time	CL = 10 nF, 90% to 10%		15	30	µs
t_{DSGOFF}	DSG off fall time	CL = 10 nF, 90% to 10%		5	15	µs
CELL BALANCING						

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Electrical Characteristics (continued)

Typical values stated at T_A = 25ºC and VDD = 20 V. MIN and MAX values stated with T_A = –40ºC to +85ºC and VDD = 3 to 25 V unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{HYST}	Hysteresis between overvoltage and Full Charge Voltage Range (4 steps of 50mV)	T_A = 25ºC	50		200	mV
V_{STEP}	Difference between the cell balancing threshold voltages (4 steps of 50mV)	T_A = 25ºC	50		200	mV
$V_{(CBIL)}$	CBI low threshold to enable Cell Balancing				0.5	V
t_{CBI_DEG} (1)	CBI deglitch period			100		ms
t_{BAL}	Odd and Even Cell group Balancing Duration at a time			521		ms
R_{BAL}	Cell Balancing Internal FET Resistance	T_A = 0 to 60ºC, Cell1 through Cell5 = 4 V, VDD = 20 V	8	12	20	Ω
D_{BAL}	Cell Balancing duty cycle	Only Odd cell group or Only Even cell group		90%		
CTRC AND CTRD CONTROL						
V_{CTR1}	Enable FET driver (VSS)	With respect to VSS. Enabled < MAX			0.6	V
V_{CTR2}	Enable FET driver (Stacked)	Enabled > MIN	VDD + 2.2			V
$V_{CTR(DIS)}$	Disable FET driver	Disabled between MIN and MAX	2.04		VDD + 0.7	V
$V_{CTR(MAXV)}$	CTRC and CTRD clamp voltage	I_{CTR} = 600 nA	VDD + 2.8	VDD + 4	VDD + 5	V
t_{CTRDEG_ON} (1)	CTRC and CTRD deglitch for ON signal	From solid off to solid on		7		ms
t_{CTRDEG_OFF} (1)	CTRC and CTRD deglitch for OFF signal	From solid on to solid off		7		ms
CURRENT STATE COMPARATOR						
$V_{(STATE\_D1)}$	Discharge qualification threshold1	Measured at SRP–SRN		–1.875		mV
$V_{(STATE\_D1\_HYS)}$	Discharge qualification threshold1 hysteresis	Measured at SRP–SRN		–1.25		mV
$V_{(STATE\_C1)}$	Charge qualification threshold1	Measured at SRP–SRN		1.875		mV
$V_{(STATE\_C1\_HYS)}$	Charge qualification threshold1 hysteresis	Measured at SRP–SRN		1.25		mV
$V_{(STATEA)}$	State detection accuracy		–50%		50%	
t_{STATE} (1)	State detection qualification time				1.2	ms
LD PIN						
$V_{LD(CLAMP)}$	LD clamp voltage	$I_{(LDCLAMP)}$ = 300 µA	16	18	20.5	V
$I_{LD(CLAMP)}$	LD clamp current	$V_{(LDCLAMP)}$ = 18 V			450	µA
V_{LDT}	LD threshold	Open PACK terminals	1.25	1.3	1.35	V
$R_{LD(INT)}$	LD input resistance when enabled	Measured to VSS		250		kΩ
t_{LD_DEG}	LD detection deglitch		1	1.5	2.3	ms
CCFG PIN						
$V_{(CCFGL)}$	CCFG threshold low (ratio of V_{AVDD})	3-cell configuration			10%	AVDD
$V_{(CCFGH)}$	CCFG threshold high (ratio of V_{AVDD})	4-cell configuration	65%		100%	AVDD
$V_{(CCFGHZ)}$	CFG threshold high-Z (ratio of V_{AVDD})	5-cell configuration, CCFG floating, internally biased	25%	33%	45%	AVDD
t_{CCFG_DEG} (1)	CCFG deglitch			6		ms
HIBERNATE MODE						

(1) Not production tested parameters. Specified by design.

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Electrical Characteristics (continued)

Typical values stated at T_A = 25ºC and VDD = 20 V. MIN and MAX values stated with T_A = –40ºC to +85ºC and VDD = 3 to 25 V unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{(PRESH)}$	PRES high threshold		1.25	1.5	1.75	V
$t_{PRES\_DEG\_ENT}$ (1)	PRES deglitch time (HIBERNATE entry)			4.5		s
$t_{PRES\_DEG\_EXT}$ (1)	PRES deglitch time (HIBERNATE exit)			10		ms
CUSTOMER TEST MODE						
$V_{(CTM)}$	Customer test mode entry voltage at VDD	VDD > VC5 + $V_{(CTM)}$, T_A = 25°C	8.5		10	V
t_{CTM_ENTRY} (2)	Delay time to enter and exit customer test mode	VDD > VC5 + $V_{(CTM)}$, T_A = 25°C	50			ms
t_{CTM_DELAY} (2)	Delay time of faults while in customer test mode	T_A = 25°C			200	ms
$t_{CTM\_OC\_REC}$ (2)	Fault recovery time of OCC, OCD1, OCD2, and SCD faults while in customer test mode	250-ms and 500-ms options, T_A = 25°C			100	ms

(2) The device is in a no-fault state prior to entering Customer Test Mode.

8.6 Timing Requirements

			MIN	TYP	MAX	UNIT
PROTECTION DELAYS (1)						
t_{OVn_DELAY}	Overvoltage detection delay time	0.5-s Delay Option	0.4	0.5	0.8	s
		1-s Delay Option	0.8	1	1.4	
		2-s Delay Option	1.8	2	2.7	
		4.5-s Delay Option	4	4.5	5.2	
t_{UVn_DELAY}	Undervoltage detection delay time	1-s Delay Option	0.8	1	1.5	s
		2-s Delay Option	1.8	2	2.7	
		4.5-s Delay Option	4	4.5	5.5	
		9-s Delay Option	8	9	10.2	
t_{OWn_DELAY}	Open-wire detection delay time		3.6	4.5	5.3	s
t_{OTC_DELAY}	Overtemperature charge detection delay time		3.6	4.5	5.3	s
t_{UTC_DELAY}	Undertemperature charge detection delay time		3.6	4.5	5.3	s
t_{OTD_DELAY}	Overtemperature discharge detection delay time		3.6	4.5	5.3	s
t_{UTD_DELAY}	Undertemperature discharge detection delay time		3.6	4.5	5.3	s
t_{OCD1_DELAY}	Overcurrent 1 detection delay time	10-ms delay option	8	10	15	ms
		20-ms delay option	17	20	26	
		45-ms delay option	36	45	52	
		90-ms delay option	78	90	105	
		180-ms delay option	155	180	205	
		350-ms delay option	320	350	405	
		700-ms delay option	640	700	825	
		1420-ms delay option	1290	1420	1620	

(1) Not production tested parameters. Specified by design.

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Timing Requirements (continued)

			MIN	TYP	MAX	UNIT
t_{OCD2_DELAY}	Overcurrent 2 detection delay time	5-ms delay option	4	5	8	ms
		10-ms delay option	8	10	15	
		20-ms delay option	17	20	26	
		45-ms delay option	36	45	52	
		90-ms delay option	78	90	105	
		180-ms delay option	155	180	205	
		350-ms delay option	320	350	405	
		700-ms delay option	640	700	825	
t_{OCC_DELAY}	Overcurrent charge detection delay time		8	10	12	ms
t_{SCD_DELAY}	Short-circuit detection delay time	400-µs delay option	220	400	610	µs
		960-µs delay option	528	960	1450	
t_{CD_REC}	Overcurrent 1, Overcurrent 2, and Short-circuit recovery delay time	250-ms option	225	250	275	ms
		500-ms option	450	500	550	

9 Detailed Description

9.1 Overview

The bq77915 device is a full-feature stackable primary protector for Li-Ion/Li-Polymer batteries with a smart cell-balancing algorithm. The device implements a suite of protections including:

- Cell voltage: overvoltage, undervoltage
- Current: overcurrent charge, overcurrent discharge 1 and 2, short circuit discharge
- Temperature: overtemperature and undertemperature in charge and discharge
- PCB: cell open-wire connection
- FET body diode protection

Protection thresholds and delays are factory-programmed and available in a variety of configurations.

The bq77915 supports 3-series to 5-series cell configurations. Up to four devices can be stacked to support ≥6-series cell configurations, providing protections up to a 20-series cell configuration.

The device has an ultra-low current HIBERNATE mode for shipping and storage. The device also features a smart cell-balancing algorithm to minimize cell-to-cell imbalance. The device has built-in CHG and DSG drivers for low-side N-channel FET protection, which automatically opens up the CHG and/or DSG FETs after protection delay time when a fault is detected. A set of CHG/DSG overrides is provided to allow disabling of CHG and/or DSG driver externally. Although the host system can use this function to disable the FET control, the main usage of these pins is to channel down the FET control signal from the upper device to the lower device in a cascading configuration in ≥6-series battery packs.

9.1.1 Device Functionality Summary

Table 1. Device Functionality Summary

FAULT DESCRIPTOR		FAULT DETECTION THRESHOLD and DELAY OPTIONS		FAULT RECOVERY METHOD and SETTING OPTIONS	
OV	Overvoltage	3 V to 4.575 V (25-mV step)	0.5, 1, 2, 4.5 s	Hysteresis	0, 100, 200, 400 mV
UV	Undervoltage	1.2 V to 3 V (100-mV step for < 2.5 V, 50-mV step for ≥ 2.5 V)	1, 2, 4.5, 9 s	Load Removal + Hysteresis	0, 200, 400, 800 mV
OW	Open Wire (cell to pcb disconnection)	0 (disabled), 100 nA, 200 nA, 400 nA	4.5 s	Restore bad VCx to pcb connection	VCx > V_{OW}

ADVANCE INFORMATION

Overview (continued)

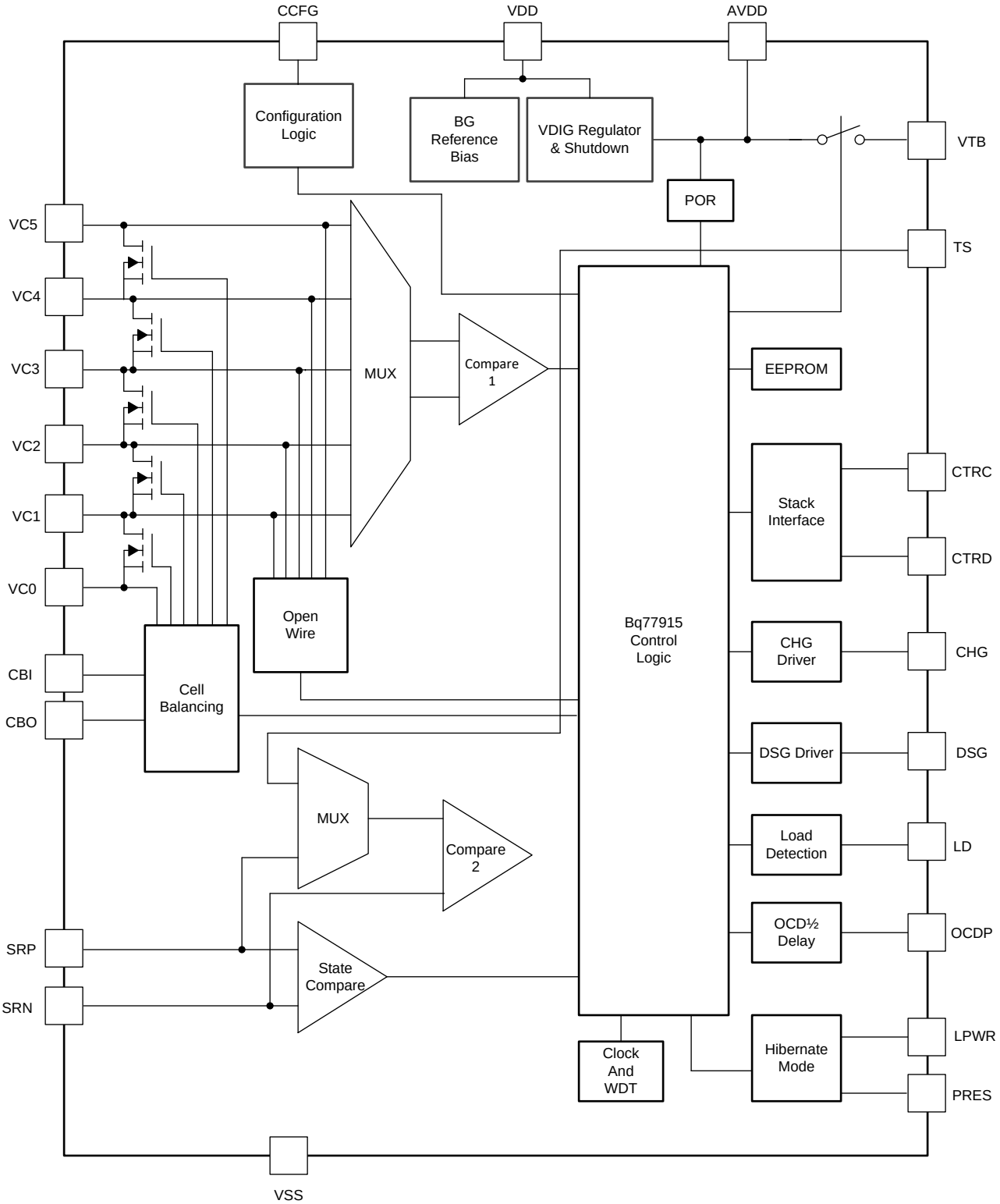
Table 1. Device Functionality Summary (continued)

FAULT DESCRIPTOR		FAULT DETECTION THRESHOLD and DELAY OPTIONS		FAULT RECOVERY METHOD and SETTING OPTIONS	
OTD(1)	Overtemperature during discharge	65°C or 70°C	4.5 s	Hysteresis or Load Removal + Hysteresis	10°C
OTC(1)	Overtemperature during charge	45°C or 50°C	4.5 s	Hysteresis	10°C
UTD(1)	Undertemperature during discharge	–20°C or –10°C	4.5 s	Hysteresis	10°C
UTC (1)	Undertemperature during charge	–5°C or 0°C	4.5s	Hysteresis	10°C
OCC	Overcurrent during charge	5 mV to 80mV (5-mV step)	10 ms	Timer auto-release and load detection, timer auto-release only, load detection only	250 ms or 500 ms
OCD1	Overcurrent1 during discharge	–10 mV to –85 mV (5-mV step)	10, 20, 45, 90, 180, 350, 700, 1420 ms	Timer auto-release and load removal, timer auto-release only, load removal only	
OCD2	Overcurrent1 during discharge	–20 mV to –170 mV (10-mV step)	5, 10, 20, 45, 90, 180, 350, 700 ms		
SCD	Short circuit discharge	–40 mV to –340 mV (20-mV step)	400, 960 µs		
CTRC	CHG signal override control	Disable via external control or via CHG signal from the upper device in stack configuration	t_{CTRDEG_ON}	Enable via external control or via CHG signal from the upper device in stack configuration	t_{CTRDEG_OFF}
CTRD	DSG signal override control	Disable via external control or via DSG signal from the upper device in stack configuration	t_{CTRDEG_ON}	Enable via external control or via DSG signal from the upper device in stack configuration	t_{CTRDEG_OFF}

(1) These thresholds are target-based on temperature, but they are dependent on external components that could vary based on customer selections. The circuit is based on a 103AT NTC thermistor connected to TS and VSS, and a 10-kΩ resistor connected to VTB and TS. Actual thresholds must be determined in mV; refers to the over- and undertemperature mV threshold in the *Electrical Characteristics* table.

ADVANCE INFORMATION

9.2 Functional Block Diagram



ADVANCE INFORMATION

9.3 Feature Description

9.3.1 Protection Summary

Two comparators are time-multiplexed to detect all of the protection fault conditions and to measure cell voltages for balancing. Each of the comparators runs on a time-multiplexed schedule and cycles through the assigned protection fault checks and voltage measurements. Comparator 1 checks for OV, UV, OW, OTC, OTD, UTC, and UTD protection faults and measure individual cell voltages for balancing. Comparator 2 checks for OCD1, OCD2, SCD, and OCC protection faults. For OV, UV, and OW protection faults and cell balancing, every cell is checked individually in a round-robin fashion, starting with cell 1 and ending with the highest selected cell. The number of the highest cell is configured using the CCFG pin.

Devices can be ordered with various timing and hysteresis settings. See Table 1 for more details.

9.3.2 Fault Operation

9.3.2.1 Operation in OV

An OV fault detection is when at least one of the cell voltages is measured above the OV threshold, V_{OV} for a time of OV delay, t_{OVn_DELAY}. The CHG FET is turned off. The OV fault recovers when the voltage of the cell in fault is below the (OV threshold – OV hysteresis, V_{HYS_OV}) for a time of OV delay.

The device assumes an OV fault after reset, and clears automatically after OV delay if all cell voltages are below the OV threshold minus hysteresis. In the event of an overvoltage fault condition on a particular cell, the balancing FET corresponding to that cell is turned on until the cell voltage drops to the full charge voltage or until the cell has recovered from overvoltage fault condition, whichever occurs earlier. See *Cell Balancing* for more details.

The state comparator is turned on when CHG is turned off. If a discharge current is detected, the device immediately switches the CHG back on. The response time of the state comparator is typically in 700 µs and should not pose any disturbance in the discharge event.

9.3.2.2 Operation in UV

An UV fault detection is when at least one of the cell voltages is measured below the UV threshold, V_{UV}, for a duration of UV delay, t_{UVn_DELAY}. The DSG FET is turned off. The UV fault recovers when:

- The voltage of the cell in fault goes above the (UV threshold + UV hysteresis, V_{HYS_UV}) for a time of UV delay OR
- The voltage of the cell in fault goes above the (UV threshold + UV hysteresis, V_{HYS_UV}) for a time of UV delay and the load is removed.

The state comparator might decide the turn on the DSG FET before the cell voltage recovers to protect the body diode.

To minimize device supply current when a UV fault has occurred or CTRD was driven to the DISABLED state, the bq77915 disables all discharge overcurrent detection blocks. Upon recovery from the fault or when CTRD is no longer externally driven, all discharge overcurrent detection blocks are reactivated.

9.3.2.3 Operation in OW

An OW fault detection is when at least one of the cell voltages is measured below the OW threshold, V_{OW}, for a duration of OW delay, t_{OWn_DELAY}. CHG and DSG are turned off. The OW fault recovers when the cell voltage in fault is above the OW threshold + OW hysteresis, V_{OW_HYS}, for a time of OW delay.

The t_{OWn_DELAY} time starts when the voltage at a given cell is detected below the V_{OW} threshold and is not from the time that the actual event of an open wire occurs. During an open-wire event, it is common that the device detects an undervoltage and/or overvoltage fault before detecting an open-wire fault. This may occur due to the differences in fault thresholds, fault delays, and the VCx pin filter capacitor values. To ensure that CHG and DSG return to normal operation mode, the OW, OV, and UV faults' recovery conditions must be met.

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Feature Description (continued)

9.3.2.4 Operation in OCD1

An OCD1 fault is when the discharge load is high enough that the voltage across the R_{SNS} resistor (V_{SRP}–V_{SRN}) is measured below the OCD1 voltage threshold, V_{OCD1}, for a duration of OCD1 delay, t_{OCD1_DELAY}. CHG and DSG are turned off.

The OCD1 fault recovers when:

- Load removal is detected only, $V_{LD} < V_{LDT}$, OR
- Overcurrent Recovery Timer, t_{CD_REC}, expiration only OR
- Overcurrent Recovery Timer expiration and load removal is detected.

9.3.2.5 Operation in OCD2

An OCD2 fault is when the discharge load is high enough that the voltage across the R_{SNS} resistor (V_{SRP}–V_{SRN}) is measured below the OCD2 voltage threshold, V_{OCD2}, for a duration of OCD2 delay, t_{OCD2_DELAY}. CHG and DSG are turned off.

The OCD2 Fault recovers when:

- Load removal detected only, $V_{LD} < V_{LDT}$, OR
- Overcurrent Recovery Timer, t_{CD_REC}, expiration only OR
- Overcurrent Recovery Timer expiration and load removal is detected.

9.3.2.6 Programming the OCD1/2 Delay Using the OCDP Pin

OCD1 and OCD2 detection delays are programmed by the resistor connected from the OCDP pin to VSS. The device checks for the resistor value at power-up. For the bottom device in a stack, Table 2 shows how the resistor values should be chosen.

Table 2. OCD1/2 Delay Using OCDP Pin

Resistor Value	OCD1 Delay	OCD2 Delay
750 kΩ±1%	1420 ms	700 ms
604 kΩ±1%	700 ms	350 ms
487 kΩ±1%	350 ms	180 ms
383 kΩ±1%	180 ms	90 ms
294 kΩ±1%	90 ms	45 ms
196 kΩ±1%	45 ms	20 ms
100 kΩ±1%	EEPROM Delay Options (EC Table)	

The OCD2 delay is roughly half of the OCD1 delay when any of the first six resistors are connected from the OCDP pin to VSS. However, if a 100-kΩ resistor is connected, the OCD1 and OCD2 delays are independent of each other and can be chosen to have any value provided in the EC table.

For any device other than the bottom device in a stacked configuration, a 10-MΩ resistor must be connected from the OCDP pin of that device to the VSS pin of the device.

If the OCDP pin is left open, the OCD1 and OCD2 delays are determined by the EEPROM settings.

9.3.2.7 Operation in SCD

An SCD fault is when the discharge load is high enough that the voltage across the R_{SNS} resistor, (V_{SRP}–V_{SRN}), is measured below the SCD voltage threshold, V_{SCD} for a duration of SCD delay, t_{SCD_DELAY}. CHG and DSG are turned off.

The SCD Fault recovers when:

- Load removal detected only, $V_{LD} < V_{LDT}$, OR
- Overcurrent Recovery Timer, t_{CD_REC}, expiration only OR
- Overcurrent Recovery Timer expiration and load removal is detected.

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9.3.2.8 Operation in OCC

An OCC fault is when the charging current is high enough that the voltage across the R_{SNS} resistor, (V_{SRP}-V_{SRN}), is measured above the OCC voltage threshold, V_{OCC}, for a duration of OCC delay, t_{OCC_DELAY}. CHG and DSG are turned off.

The OCC Fault recovers when:

- Load detected only, $V_{LD} > V_{LDT}$, OR
- Overcurrent Recovery Timer, t_{CD_REC}, expiration only OR
- Overcurrent Recovery Timer expiration and load is detected.

9.3.2.9 Overcurrent Recovery Timer

The timer expiration method activates an internal recovery timer as soon as the initial fault condition exceeds the OCD1/OCD2/SCD/OCC time. When the recovery timer reaches its limit, both of the CHG and DSG drivers are turned back on. If the combination option of timer expiration AND load removal/detection is used, then the load removal/detection condition is only evaluated upon expiration of the recovery timer, which can have an expiration period of t_{CD_REC}.

9.3.2.10 Load Detection and Load Removal Detection

The load detection and removal detection features are implemented with the LD pin. When no undervoltage fault and current fault conditions are present, the LD pin is held in an open-drain state. Once any UV, OCD1, OCD2, OCC, or SCD fault occurs and load removal or detection is selected as device of the recovery conditions, a high impedance pull-down path to VSS is enabled on the LD pin. With an external load still present, the LD pin will be externally pulled high: It is internally clamped to $V_{LDCLAMP}$ and should also be resistor-limited through R_{LD} externally to avoid conducting excessive current. If the LD pin voltage exceeds V_{LDT} for t_{LD_DEG}, it is interpreted as a *load present condition* and is one of the recovery mechanisms selectable for an OCC fault. When the load is eventually removed, the internal high-impedance path to VSS should be sufficient to pull the LD pin below V_{LDT} for t_{LD_DEG}. This is interpreted as a *load removed condition* and is one of the recovery mechanisms selectable for UV, OCD1, OCD2, and SCD faults.

Table 3. Load State

LD PIN	LOAD STATE
≥ V_{LDT} for t_{LD_DEG}	Load present
< V_{LOT} for t_{LD_DEG}	Load removed

9.3.2.11 Operation in OTC

An OTC fault occurs when the temperature increases such that the voltage across an NTC thermistor goes below the OTC voltage threshold, V_{OTC}, for an OTC delay time, t_{OTC_DELAY}. CHG is turned off. The state comparator is turned on when CHG is turned off. If a discharge current is detected, the device immediately switches the CHG back on. The response time of the state comparator is typically in 700 µs and should not pose any disturbance in the discharge event. The OTC fault recovers when the voltage across thermistor gets above OTC recovery threshold, V_{OTC_REC}, for OTC delay time.

9.3.2.12 Operation in OTD

An OTD fault is when the temperature increases such that the voltage across an NTC thermistor goes below the OTD voltage threshold, V_{OTD}, for an OTD delay time, t_{OTD_DELAY}. CHG and DSG are turned off.

The OTD Fault recovers when:

- The voltage across thermistor gets above OTD recovery threshold, V_{OTD_REC}, for a time of OTD delay OR
- The voltage across thermistor gets above OTD recovery threshold, V_{OTD_REC}, for a time of OTD delay and load is removed.

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9.3.2.13 Operation in UTC

A UTC fault occurs when the temperature decreases such that the voltage across an NTC thermistor gets above the UTC voltage threshold, V_{UTC}, for a time of UTC delay, t_{UTC_DELAY}. CHG is turned off. The state comparator is turned on when CHG is turned off. If a discharge current is detected, the device will immediately switch the CHG back on. The response time of the state comparator is typically in 700 µs and should not pose any disturbance in the discharge event. The UTC fault recovers when the voltage across thermistor gets below UTC recovery threshold, V_{UTC_REC}, for a time of UTC delay.

9.3.2.14 Operation in UTD

A UTD fault occurs when the temperature decreases such that the voltage across an NTC thermistor goes above the UTD voltage threshold, V_{UTD}, for a UTD delay time, t_{UTD_DELAY}. CHG and DSG are turned off. The UTD fault recovers when the voltage across thermistor gets below UTD recovery threshold, V_{UTD_REC}, for a time of UTD delay.

9.3.3 Protection Response and Recovery Summary

Table 4 summarizes how each fault condition affects the state of the DSG and CHG output signals, as well as the recovery conditions required to resume charging and/or discharging. As a rule, the CHG and DSG output drivers are enabled only when no respective fault conditions are present. When multiple simultaneous faults (such as an OV and OTD) are present, all faults must be cleared before the FET can resume operation.

Table 4. Fault Condition, State, and Recovery Methods

FAULT	FAULT TRIGGER CONDITION	CHG	DSG	RECOVERY METHOD	TRIGGER DELAY	RECOVERY DELAY
CTRC disabled	CTRC disabled for delgitch delay time	OFF	—	CTRC must be enabled for delgitch delay time	t_{CTRDEG_ON}	t_{CTRDEG_OFF}
CTRD disabled	CTRD disabled for delgitch delay time	—	OFF	CTRD must be enabled for delgitch delay time		
OV	V(Cell) rises above V_{OV} for delay time	OFF	—	V(Cell) drops below $V_{OV} – V_{HYS\_OV}$ for delay	t_{OVn_DELAY}	
UV	V(Cell) drops below V_{UV} for delay time	—	OFF	DSG FET turned on after Load is removed and V(Cell) rises above $V_{UV} + V_{HYS\_UV}$ for delay.	t_{UVn_DELAY}	
OW	$VC_X – VC_{X–1} < V_{OW}$ for delay time	OFF	OFF	Bad VC_X recovers such that $VC_X – VC_{X–1} > V_{OW} + V_{OW\_HYS}$ for delay	t_{OWn_DELAY}	
OCC	(VSRP - VSRN) > VOCC for delay time	OFF	OFF	Recovery delay expires, OR LD detects > V_{LDT}, OR Recovery delay expires + LD detects > V_{LDT}	t_{OCC_DELAY}	t_{CD_REC}
OCD1, OCD2, SCD	(VSRP - VSRN) < VOCD1, VOCD2, or VSCD for delay time	OFF	OFF	Recovery delay expires, OR LD detects < V_{LDT}, OR Recovery delay expires + LD detects < V_{LDT}	t_{OCD1_DELAY} , t_{OCD2_DELAY}, t_{SCD_DELAY}	t_{CD_REC}
OTC(1)	Temperature rises above T_{OTC} for delay time	OFF	—	Temp drops below $T_{OTC} – T_{OTC\_REC}$ for delay	t_{OTC_DELAY}	
OTD(1)	Temperature rises above T_{OTD} for delay time	OFF	OFF	Temp drops below $T_{OTD} – T_{OTD\_REC}$ for delay, OR Temp drops below $T_{OTD} – T_{OTD\_REC}$ for delay and Load is removed	t_{OTD_DELAY}	
UTC(1)	Temperature drops below T_{UTC} for delay time	OFF	—	Temperature rises above $T_{UTC} + T_{UTC\_REC}$ for delay	t_{UTC_DELAY}	
UTD(1)	Temp drops below T_{UTD} for delay time	OFF	OFF	Temp rises above $T_{UTD} + T_{UTD\_REC}$ for delay	t_{UTD_DELAY}	

(1) T_{UTC}, T_{UTD}, T_{UTC_REC}, and T_{UTD_REC} correspond to the temperature produced by V_{UTC}, V_{UTD}, V_{UTC_REC}, and V_{UTD_REC} of the selected thermistor resistance.

To prevent FET damage, there are times when the CHG or DSG FET may be enabled even though a fault event has occurred. See the *State Comparator* section for details.

9.3.4 Cell Balancing

Cell balancing is performed by comparing the cell voltages with respect to cell balancing threshold voltages, evaluating the results of the comparison and controlling the cell balancing FET, which over a period of time will allow for closer cell voltages, thereby extending battery pack life. The conditions for performing cell balancing are: CBI is connected to VSS, no device in the stack is in a fault condition, and the pack is charging.

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CBI is the cell balancing input pin. It enables cell balancing function for the device.

- Leave the CBI pin floating to disable cell balancing. An internal circuit pulls up the CBI pin to AVDD in this case.
- Connect CBI to VSS to enable cell balancing.

In a single device, cell balancing of all the odd numbered cells can happen at the same time, and balancing of all the even numbered cells can also happen at the same time, but odd and even cells are not balanced at the same time. When devices are stacked on top of each other, it must be ensured in the PCB layout that the trace from VC5 pin to a cell and the trace from the VC0 pin of the next upper device to the immediately higher cell are kept separate.

All cell balancing FETs are turned off during voltage measurements. If odd numbered and even numbered cells need balancing at the same time, one single cycle time t_{BAL} is dedicated for odd numbered cells alone followed by the next t_{BAL} dedicated for even numbered cells alone.

In a stacked configuration, the CBO pin of the bottom device should be connected to the CBI pin of the next upper device through a 10-kΩ resistor and so forth.

When a cell is in OV, its corresponding balancing FET will be turned on if CBI is connected to VSS and if there are no discharge faults anywhere in the stack. The balancing FET will be ON until the cell voltage drops to V_{FC} or $V_{OV} – V_{HYS\_OV}$, whichever occurs earlier.

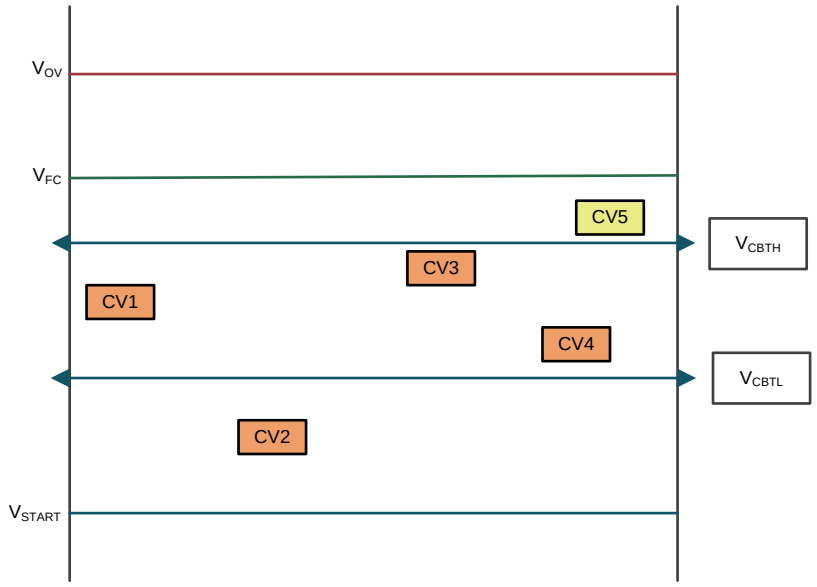

Figure 1. Cell-Balancing Algorithm

V_{CBTL} is the lower cell balancing threshold and V_{CBTH} is the upper cell balancing threshold. In the figure shown above, the balancing FET will be turned on only for the cell CV5. V_{START} is set at 3.8 V, therefore, cell balancing starts only when individual cell voltages exceed 3.8 V. The difference between V_{CBTH} and V_{CBTL} can be programmed in the EEPROM to be between 50 mV and 200 mV, in steps of 50 mV. The difference between the V_{OV} and V_{FC} can also be programmed in the EEPROM to be between 50 mV and 200 mV, in steps of 50 mV.

When using the integrated MOSFETs for cell balancing, the cell monitor filter resistance R_{INI} controls the amount of cell balancing current the device can supply to the cells. Internal cell balancing should be used for cell balancing currents up to 50 mA. External MOSFETs have to be used if higher cell balancing currents are required. In the case of external balancing, the balancing current is controlled by the resistor R_{CB} in series with the external MOSFET, as shown in Figure 2. The pin filter resistance R_{INE} should be 1 kΩ and the capacitance C_{INE} should be 0.1 µF. The gate bias voltage necessary to turn on the FET connected to Cell(n) is generated by the resistor R_{INE} connected to the $VC_{(n–1)}$ pin. The external MOSFET must be selected with a threshold voltage less than 1.7 V.

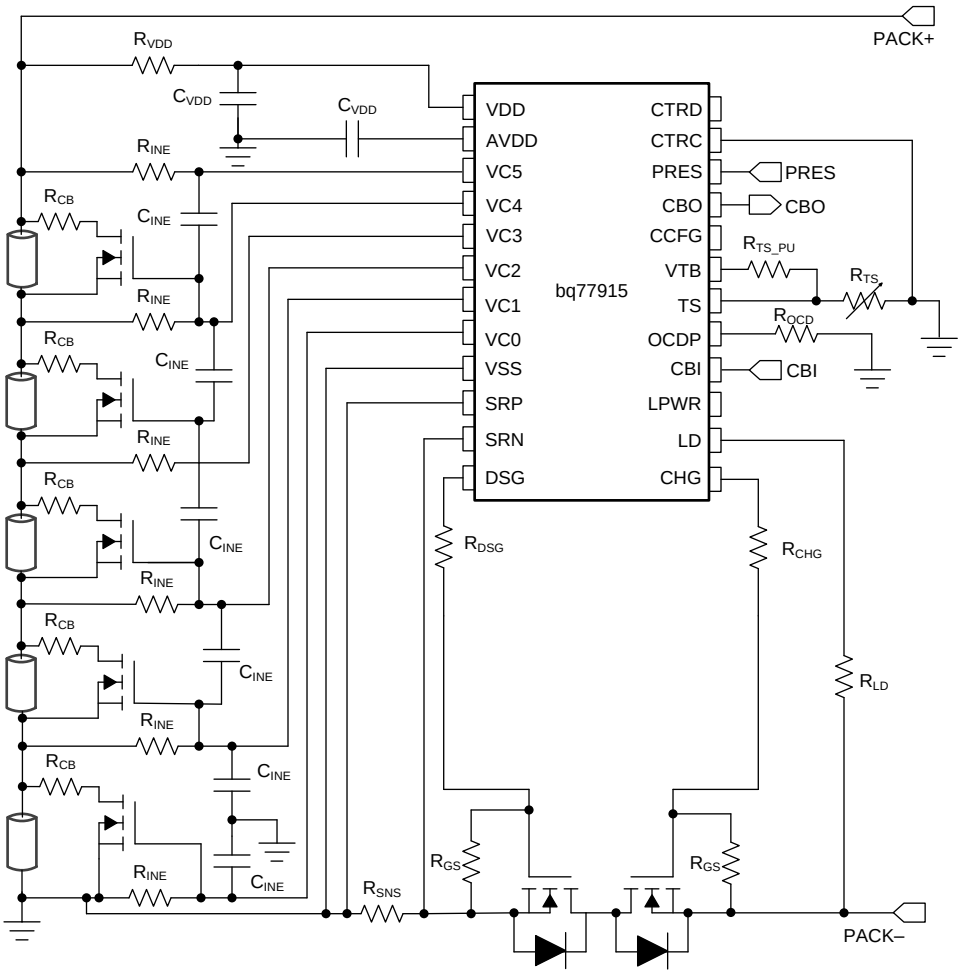

Figure 2. Cell Balancing with External MOSFETs

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9.3.5 HIBERNATE Mode Operation

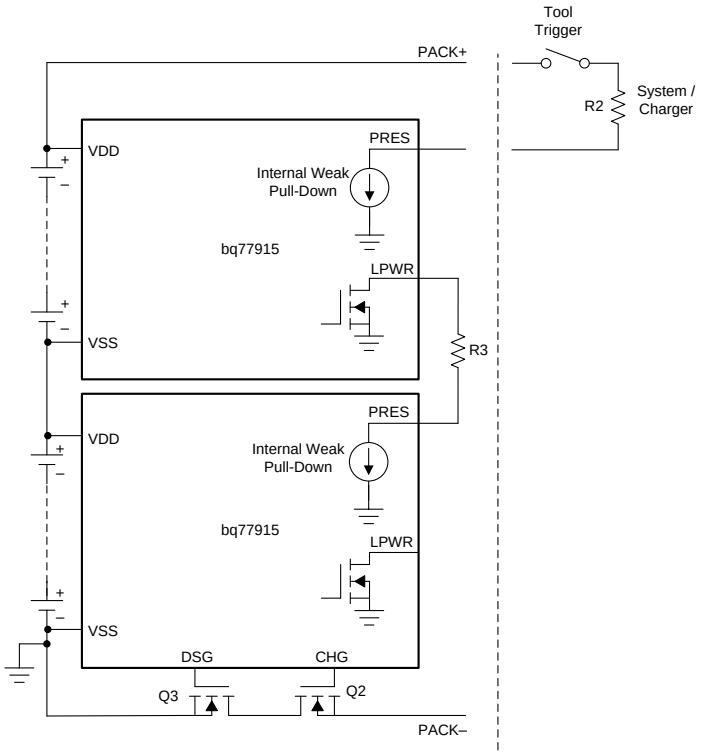

Figure 3. HIBERNATE Mode Simplified Schematic 1

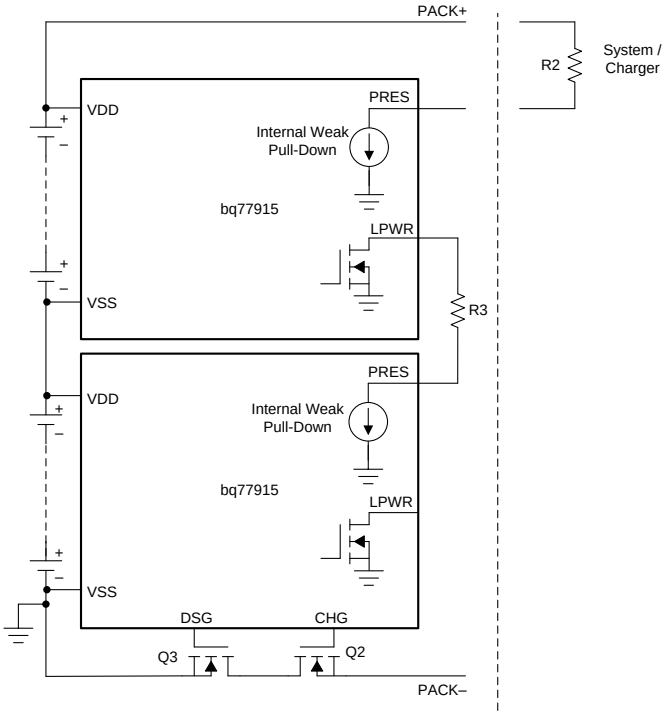

Figure 4. HIBERNATE Mode Simplified Schematic 2

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The bq77915 has two dedicated pins (PRES and LPWR) for HIBERNATE mode operation. Most of the internal circuitry is turned off in HIBERNATE mode to save power. Charge and discharge FETs are turned off and all fault protections are disabled.

The PRES pin has an internal pull-down connected to the pin, which pulls PRES low. When the PRES pin is left floating (the system or charger is not connected to the pack), the load is not connected, and the device is not in any fault condition, the device enters HIBERNATE mode after $t_{PRES\_DEG\_ENT}$ time. Once in HIBERNATE mode, the system or the charger should drive this pin high ($>V_{PRESH}$) through the resistor R2 for NORMAL mode operation. When the battery pack (in HIBERNATE mode) is inserted to the tool/system or when a charger is connected to the pack, the system has to provide a pull-up to the PRES pin, which puts the device back to NORMAL mode. The device will exit HIBERNATE mode after a $t_{PRES\_DEG\_EXT}$ deglitch time.

In a stacked configuration, connect the LPWR pin of an upper device to the PRES pin of a lower device through the resistor R3.

9.3.6 Configuration CRC Check and Comparator Built-In-Self-Test

To improve reliability, the device has a built-in CRC check for all the factory-programmable configurations, such as the thresholds and delay time settings. When the device is set up in the factory, a corresponding CRC value is also programmed to the memory. During normal operation, the device compares the configuration setting against the programmed CRC periodically. A CRC error will reset the digital circuitry and increment the CRC fault counter. The digital reset forces the device to reload the configuration as an attempt to correct the configurations. A correct CRC check reduces the CRC fault counter. Three CRC fault counts will turn off both the CHG and DSG drivers. If FETs are opened due to a CRC error, only a POR can recover the FET state and reset the CRC fault.

In addition to the CRC check, the device also has built-in-self-test (BIST) on the comparators. The BIST runs in a scheduler, and each comparator is checked for a period of time. If a fault is detected for the entire check period, the particular comparator is considered at fault, and the CHG and DSG FETs are turned off. The BIST continues to run by the scheduler even if a BIST fault is detected. If the next BIST result is good, the FET driver resumes normal operation.

The CRC check and BIST check do not affect the normal operation of the device. However, there is not specific indication when a CRC or BIST error is detected besides turning off the CHG and DSG drivers. If there is no voltage, current, or temperature fault condition present, but CHG and DSG drivers remain off, it is possible either CRC or BIST error is detected. Users can POR the device to reset the device.

9.3.7 Fault Detection Method

9.3.7.1 Filtered Fault Detection

The device detects a fault once the applicable fault is triggered after accumulating sufficient trigger sample counts. The filtering scheme is based on a simple add/subtract. Starting with the Triggered Sample Count cleared, the counts go up for a sample that is taken across the tested condition (for example, above the fault threshold when looking for a fault) and the counts go down for a sample that is taken before the tested condition (that is, below the fault threshold). Figure 5 shows an example of a signal that triggers a fault when accumulating five counts above the fault threshold. Once a fault has been triggered, the trigger sample counts reset.

NOTE

With a filtered detection, when the input signal falls below the fault threshold, the sample count does not reset but only counts down as shown in Figure 5. Therefore, it is normal to observe a longer delay time if a signal is right at the detection threshold. The noise can push the delay count to be counting up and down, resulting in a longer time for the delay counter to reach its final accumulated trigger target.

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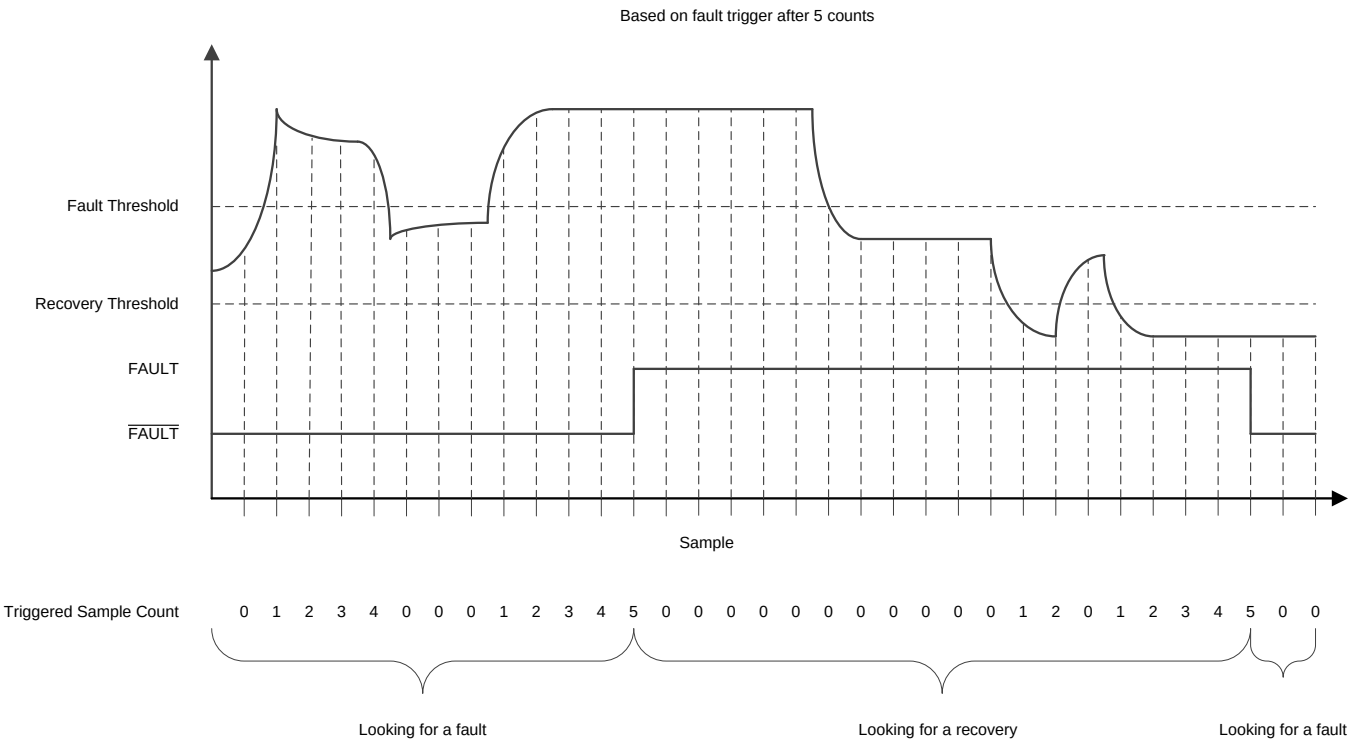

Figure 5. Filtered Fault Detection

9.3.8 State Comparator

A small, low-offset analog state comparator monitors the sense resistor voltage (SRP–SRN) to determine when the pack is in a DISCHARGE state less than a minimum threshold, V_{STATE_D}, or a CHARGE state greater than a maximum threshold, V_{STATE_C}. The state comparator is used to turn the CHG FET on to prevent damage/overheating during discharge in fault states that call for having only the CHG FET off, and vice versa for the DSG FET during charging in fault that call for having only the DSG FET off. Also, the state comparator is turned on in NORMAL mode (CHG and DSG FETs on) during cell balancing to ensure that cell balancing is performed only when the pack is charging.

Table 5 summarizes when the state comparator is operational. The state comparator is only on during faults detected that call for only one FET to be turned off, and also in NORMAL mode during cell balancing to ensure that cell balancing is performed only when the pack is charging.

Table 5. State Comparator Operation Summary in Fault Conditions

MODE	CHG	DSG	STATE COMP
NORMAL mode, No Cell Balancing	ON	ON	OFF
NORMAL mode, Cell Balancing	ON	ON	V_{STATE_C} Detection
UV, CTRD	ON	OFF	V_{STATE_C} Detection
OV, UTC, OTC, CTRC	OFF	ON	$_{STATE\_D}$ Detection
OCD1, OCD2, SCD, OCC, UTD, OTD, OW	OFF	OFF	OFF

ADVANCE INFORMATION

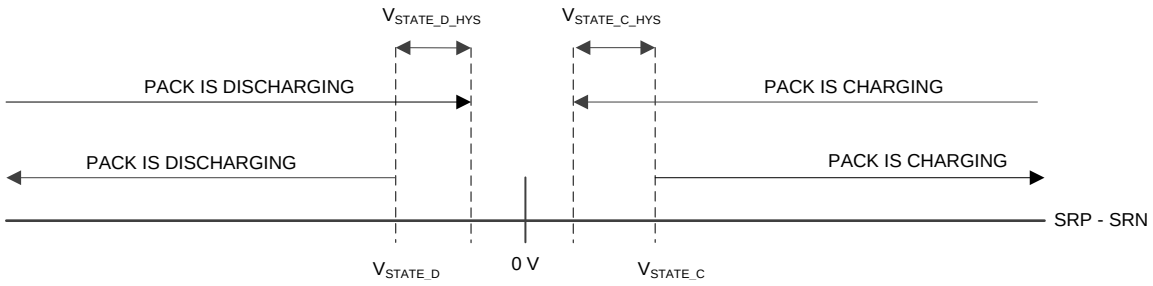

Figure 6. State Comparator Thresholds

Any time a CHG fault is present and a DSG fault is not present, the device will enable the state comparator. If the pack is in a fault state where charging is prohibited but discharging is permitted (OV, OTC, UTC, and CTRC), a discharge may occur. When this happens, the CHG FET driver will be turned on to avoid damage, as it will otherwise carry the discharge current through its body diode. The state comparator (with the V_{STATE_D} threshold and $V_{STATE\_D\_HYS}$ hysteresis) remains on for the entire duration of a CHG fault with no DSG fault event.

If there is a DSG fault under CTRD conditions, the DSG FET would be turned on if charge is detected. The state comparator (with V_{STATE_C} threshold and $V_{STATE\_C\_HYS}$ hysteresis) remains on for the entire duration of a DSG fault with no CHG fault event.

9.3.9 DSG FET Driver Operation

The DSG pin is driven high only when no related faults (UV, OW, OTD, UTD, OCD1, OCD2, SCD, OCC, and CTRD disabled) are present and the device is not in HIBERNATE mode of operation. It is a fast switching driver with a target on resistance of about 15 Ω–20 Ω and an off resistance of R_{DSGOFF}. It is designed to enable customers to select the optimized R_{GS} value to archive the desirable FET rise and fall time per the application requirement and the choice of FET characteristics. When the DSG FET is turned off, the DSG pin drives low and all discharge overcurrent protections (OCD1, OCD2, SCD) are disabled to better conserve power. These resume operation when the DSG FET is turned on. The device provides FET body diode protection through the state comparator if one FET driver is on and the other FET driver is off.

The DSG driver may be turned on to prevent FET damage if the battery pack is charging while a discharge inhibit fault condition is present. This is done by the state comparator. The state comparator (with V_{STATE_C1} or V_{STATE_C2} threshold and $V_{STATE\_C1\_HYS}$ or $V_{STATE\_C2\_HYS}$ hysteresis) remains on for the entire duration of a DSG fault with no CHG fault event.

- If (SRP–SRN) ≤ (V_{STATE_C} – $V_{STATE\_C\_HYS}$) and no charge event is detected, the DSG FET output will remain OFF due to the presence of a DSG fault.
- If (SRP–SRN) > V_{STATE_C} and a charge event is detected, the DSG FET output will turn ON for body diode protection.

See the *State Comparator* section for details.

The presence of any related faults, as shown in Figure 7, results in the DSGFET_OFF signal.

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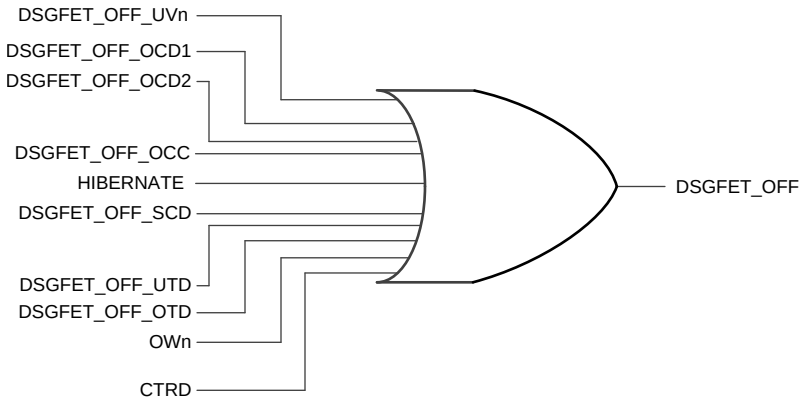

Figure 7. Faults That Can Qualify DSGFET_OFF

9.3.10 CHG FET Driver Operation

The CHG pin is driven high only when no related faults (OV, OW, OTC, UTC, OTD, UTD, OCD1, OCD2, SCD, OCC, and CTRC disabled) are present and the pack is not in HIBERNATE mode of operation. The CHG pin is used to drive the CHG FET, which is designed to be used on the single device configuration or used by the bottom device in a stack configuration.

Turning off the CHG pin has no influence on the overcurrent protection circuitry. The CHG pin is designed to turn on very quickly; the internal on resistance is about 2 kΩ. The CHG FET turn off relies on the external resistor connected in parallel to the gate-source nodes of the NCH power FET.

The CHG FET may be turned on to protect the FET's body diode if the pack is charging, even if a charging inhibit fault condition is present. This is done through the state comparator. The state comparator (with V_{STATE_D1} or V_{STATE_D2} threshold and $V_{STATE\_D1\_HYS}$ or $V_{STATE\_D2\_HYS}$ hysteresis) remains on for the entire duration of a DSG fault with no CHG fault event.

- If (SRP–SRN) > (V_{STATE_D} + $V_{STATE\_D\_HYS}$) and no discharge event is detected, the CHG FET output will remain OFF due to the present of a CHG fault.
- If (SRP–SRN) ≤ V_{STATE_D} and a discharge event is detected, the CHG FET output will turn ON for body diode protection.

The CHGFET_OFF signal is a result of the presence of any related faults as shown in Figure 8.

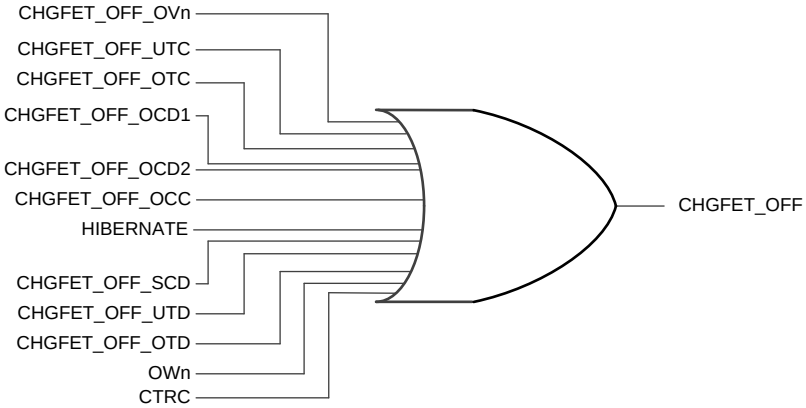

Figure 8. Faults That Can Qualify CHGFET OFF

9.3.11 External Override of CHG and DSG Drivers

The device allows direct disabling of the CHG and DSG drivers through the CTRC and CTRD pins, respectively. Figure 9 shows the operation of the CTRC and CTRD pins. To support the simple-stack solution for higher-cell count packs, these pins are designed to operate above the device's VDD level. Connect a 10-MΩ resistor between a lower device CTRC and CTRD input pins to an upper device's CHG and DSG output pins (see the schematics in *Stacking Implementations*).

CTRC only enables or disables the CHG pin, while CTRD only enables or disables the DSG pin. When the CTRx pin is in the DISABLED region, the respective FET pin will be off, regardless of the state of the protection circuitry. When the CTRx pin is in either ENABLED region, the protection circuitry determines the state of the FET driver.

NOTE

In any event where CTRC is disabled, CTRD is enabled, no DSG FET related faults are present, and (SRP–SRN) < V_{STATE_D}, the CHG output pin will be held high regardless. In any event where CTRD is disabled, CTRC is enabled, no charge FET related faults present, and (SRP–SRN) > V_{STATE_C}, the DSG output pin will be held high regardless.

Both CTRx pins apply the fault-detection filtered method to improve the robustness of the signal detection. The counter counts up if an ENABLED signal is sampled; the counter counts down if a DISABLED signal is sampled. When the counter counts up from 0% to > 70% of its full range, which takes about 7-ms typical of a solid signal, the CTRx pins take the signal as ENABLED. If the counter counts down from 100% to < 30% of its full range, which takes about 7-ms typical of a solid signal, the CTRx pins take the signal as DISABLED. From a 0 count counter (solid DISABLE), a solid ENABLE signal takes about t_{CTRDEG_ON} time to deglitch. From a 100% count (solid ENABLE), a solid DISABLE signal takes about t_{CTRDEG_OFF} time to deglitch. Although such a filter scheme provides a certain level of noise tolerance, it is highly recommended to shield the CTRx traces and keep the traces as short as possible in the PCB layout design. The CTRx deglitch time will add onto the FET response timing on OV, UV, and OW faults in a stack configuration. The t_{CTRDEG_OFF} time adds an additional delay to the fault detection timing and the t_{CTRDEG_ON} time adds an additional delay to the fault recovery timing.

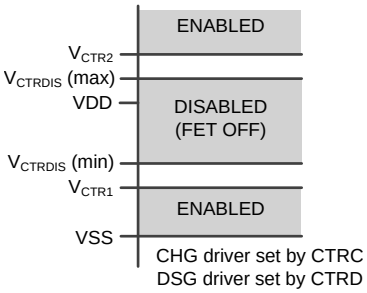

Figure 9. CTRC, CTRD Voltage Levels

9.3.12 Configuring 3-Series, 4-Series, or 5-Series Modes

The bq77915 supports 3-series, 4-series, or 5-series packs. To avoid accidentally detecting a UV fault on unused (shorted) cell inputs, the device must be configured for the specific cell count of the pack. This is set with the configuration pin, CCFG, which is mapped as shown in Table 6. The device periodically checks the CCFG status and takes t_{CCFG_DEG} time to detect the pin status.

Table 6. CCFG Configurations

CCFG	CONFIGURATION	CONNECT TO
< V_{CCFGL} for t_{CCFG_DEG}	3 cells	VSS
Within V_{CCFGM} for t_{CCFG_DEG}	4 cells	AVDD
> V_{CCFGH} for t_{CCFG_DEG}	5 cells	Floating

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The CCFG pin should be tied to the recommended net from Table 6. The device compares the CCFG input voltage to the AVDD voltage and should never be set above the AVDD voltage. When the device configuration is for 5 series, leave the CCFG pin floating. The internal pin bias is approximately 33% of the AVDD voltage for 5-series configuration.

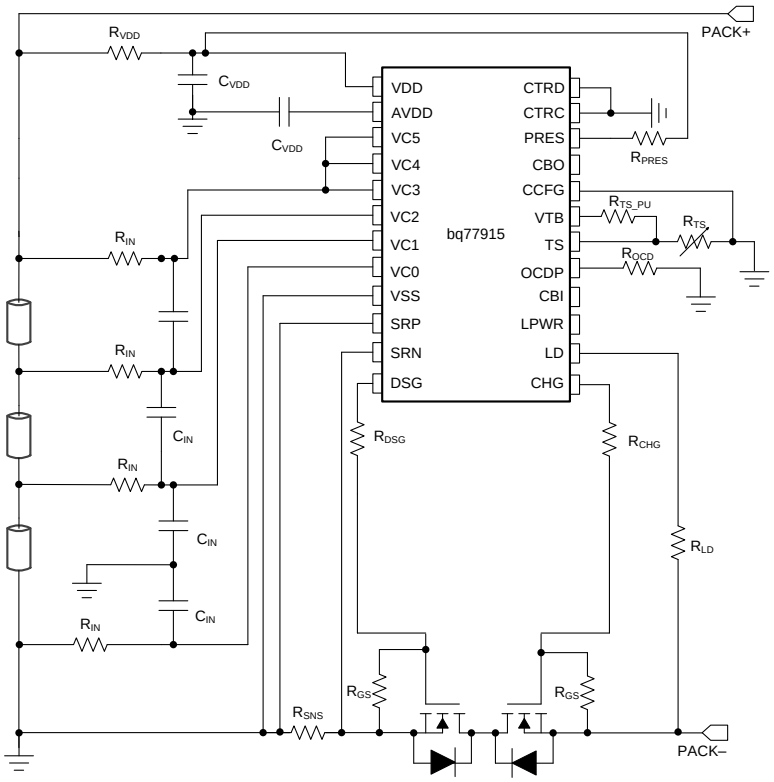

Figure 10. 3-Series Configuration with Cell Balancing and HIBERNATE Mode Disabled

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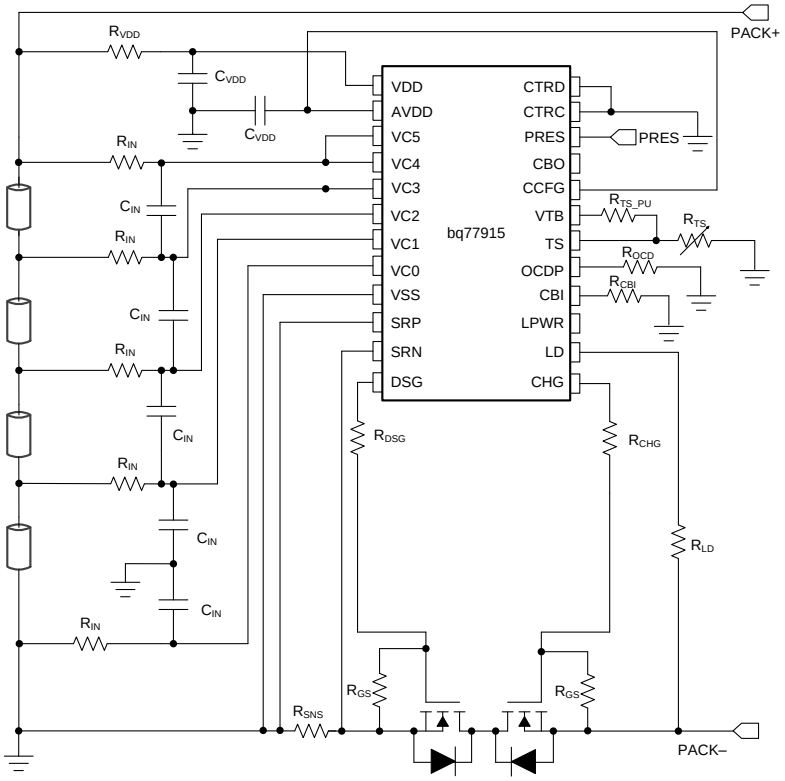

Figure 11. 4-Series Configuration with Internal Cell Balancing and HIBERNATE Mode Enabled

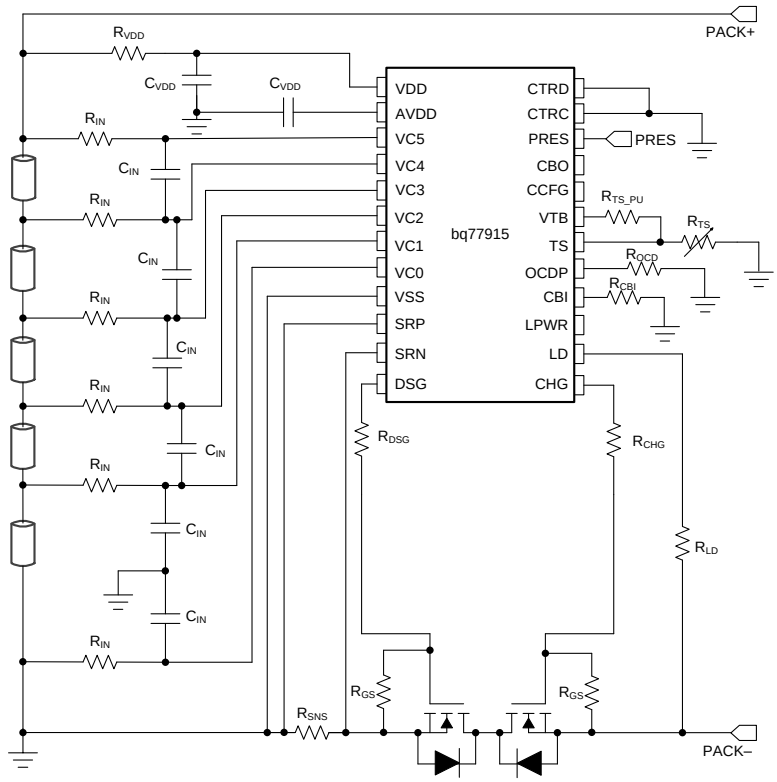

Figure 12. 5-Series Configuration with Internal Cell Balancing and HIBERNATE Mode Enabled

ADVANCE INFORMATION

9.3.13 Stacking Implementations

Higher than 5-series cell packs may be supported by daisy-chaining multiple devices. Each device ensures OV, UV, OW, OTC, OTD, UTC, and UTD protections of its directly monitored cells, while any fault conditions automatically disable the global CHG and/or DSG FET driver.

NOTE

Upper devices do not provide OCC, OCD1, OCD2, or SCD protections, as these are based on pack current. For the bq77915 used on the upper stack, the SRP and SRN pins should be shorted to prevent false detection.

To configure higher-cell packs, follow this procedure:

- Each device must have a connection on at least each of its three lowest cell input pins.
- It is highly recommended to connect higher cell count to the upper devices (for example, for a 7-series configuration, connect four cells on the upper device and three cells on the bottom device). This is to provide stronger CTRx signal to the bottom device.
- Ensure that each device's CCFG pin is configured appropriately for its specific number of cells (that is, three, four, or five cells).
- Connect the upper CHG pins with an RCTRx to the immediate lower device CTRC pin.
- Connect the upper DSG pins with an RCTRx to the immediate lower device CTRD pin.
- All upper devices should have their SRP and SRN pins shorted to their VSS pins.
- Connect the upper CBI pins with an R_{CB} to the immediate lower device CBO pin.
- Connect the upper LPWR pins with an R_{HIB} to the immediate lower device PRES pin.
- Connect the upper OCDP pins with a 10-MΩ resistor to VSS. Use the lower OCDP pin to program the OCD1/2 delay.

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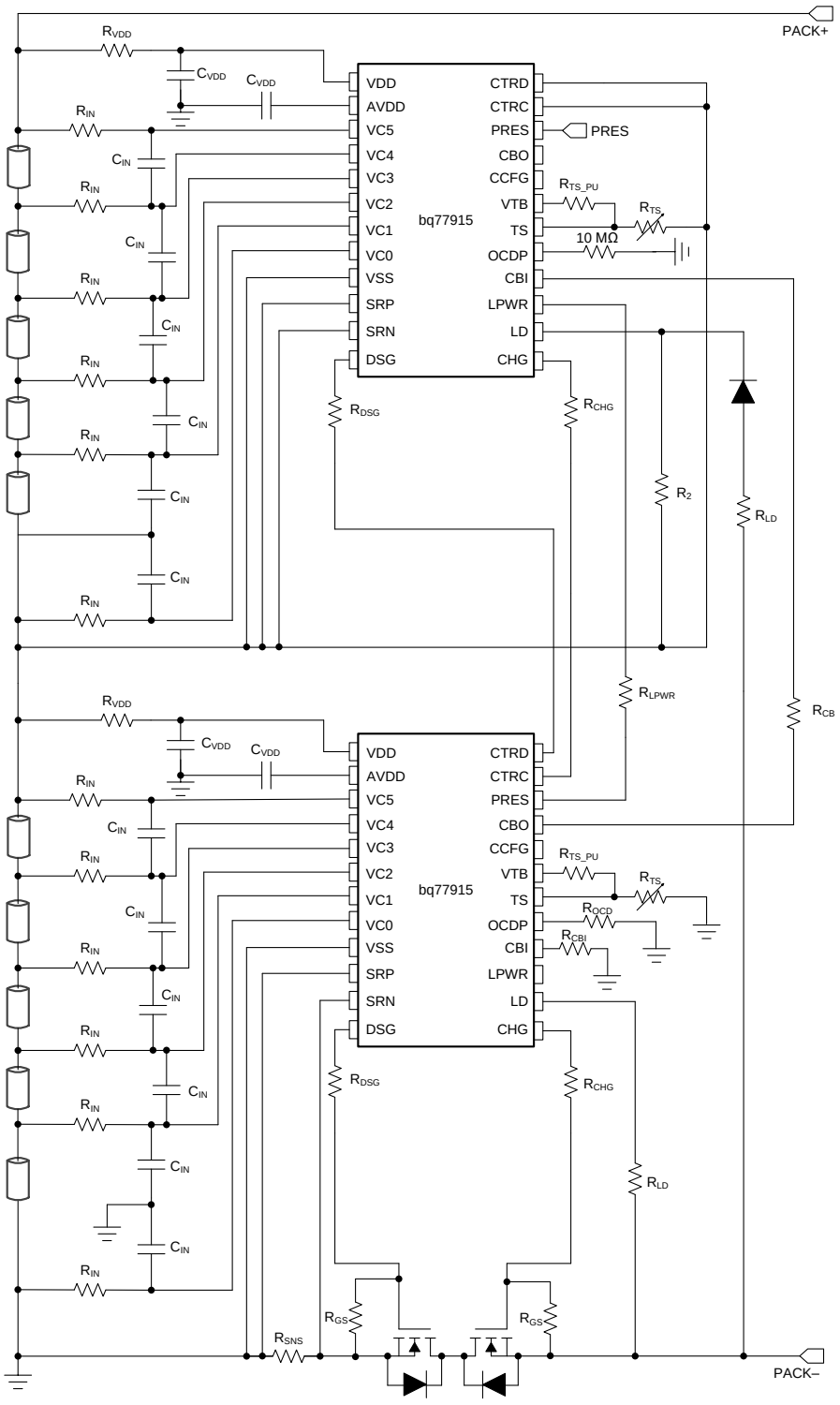

Figure 13. 10-Series Configuration with Internal Cell Balancing and HIBERNATE Mode Enabled

ADVANCE INFORMATION

9.3.14 Zero-Volt Battery Charging Inhibition

Once the device is powered up, it can pull the CHG pin up if the VDD ≥ V_{SHUT}, which varies from about 1 V per cell on a 3-series configuration to about 0.6 V per cell on a 5-series configuration. If the battery stack voltage falls below V_{SHUT}, the device is in SHUTDOWN mode and the CHG driver is no longer active and charging is not allowed unless VDD rises above V_{POR} again.

9.4 Device Functional Modes

9.4.1 Power Modes

9.4.1.1 Power On Reset (POR)

The device powers up when VDD ≥ V_{POR}. At POR, the following events occur:

- A typical of 5-ms hold-off delay applies to both CHG and DSG drivers, keeping both drivers in the OFF state. This is to provide time for the internal LDO voltage to ramp up.
- The CTRC and CTRD deglitch occurs. During the deglitch time, the CHG and DSG driver remains off. Note that deglitch time masks out the 5-ms hold-off delay.
- The device assumes an OV fault at POR; thus, the CHG driver is off for OV recovery time if all the cell voltages are < (V_{OV} – V_{HYS_OV}). The OV recovery time starts after the 5-ms hold-off delay. If device reset occurs when any cell voltage is above the OV hysteresis range, the CHG driver will remain off until an OV recovery condition is met.

9.4.1.2 NORMAL Mode

This is the normal operation mode. All configured protections are active, no fault is detected, and both CHG and DSG drivers are enabled. HIBERNATE mode is deactivated. While the device is in NORMAL mode, cell balancing occurs if all the necessary conditions for balancing are valid. Refer to the *Cell Balancing* section for details.

9.4.1.3 FAULT Mode

If any configured protection fault is detected, the device enters the FAULT mode. In this mode, the CHG and/or DSG driver can be turned off depending on the fault. Refer to *Fault Condition, State, and Recovery Methods* for details. When one of the FET drivers (either CHG or DSG) is turned off, while the other FET driver is still on, the state comparator is activated for FET body diode protection.

9.4.1.4 HIBERNATE Mode

If the PRES pin is left floating, the device enters HIBERNATE mode operation. In this mode, all fault detection and cell balancing is deactivated and the CHG and DSG drivers are turned off to reduce power consumption to ultra-low levels. This mode of operation is recommended when the battery packs are in shipping or storage. The device can be brought back to NORMAL mode by driving PRES high.

9.4.1.5 SHUTDOWN Mode

This is the lowest power consumption state of the device when VDD falls below V_{SHUT}. In this mode, all fault detections, CHG and DSG drivers are disabled. The device will wake up and enter NORMAL mode when VDD rises above V_{POR}.

ADVANCE INFORMATION

Device Functional Modes (continued)

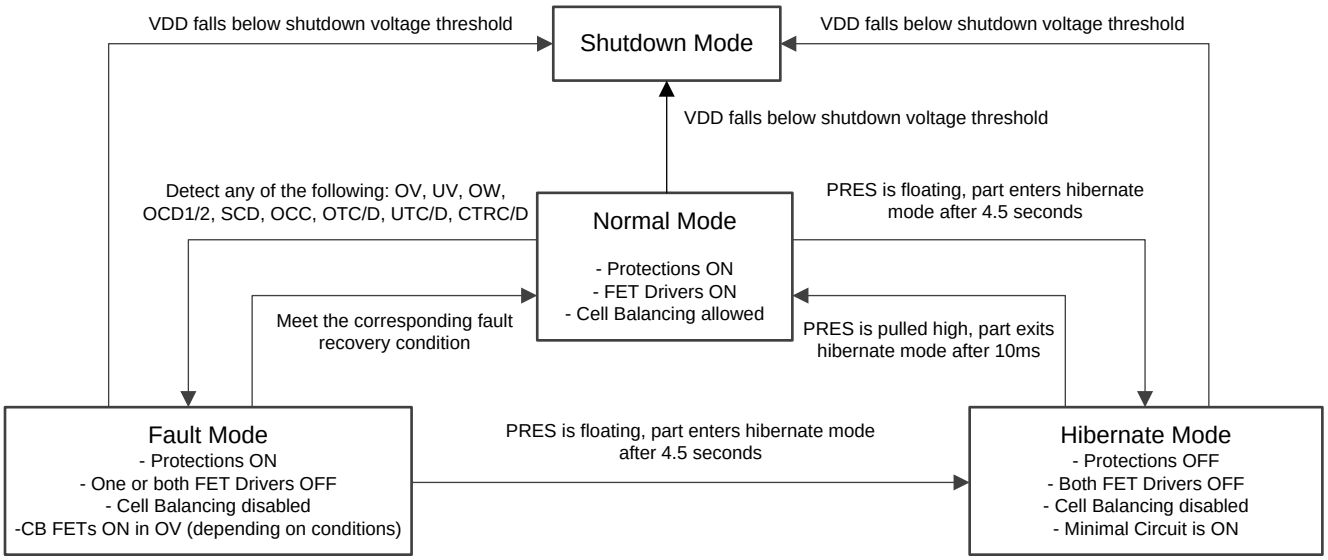

Figure 14. Various Operational Modes

9.4.1.6 Customer Fast Production Test Modes

The bq77915 device supports the ability to greatly reduce production test time by cutting down on protection fault delay times. To shorten fault times, place the bq77915 device into Customer Test Mode (CTM). CTM is triggered by raising VDD to V_{CTM} voltage above the highest cell input pin (that is, VC5) for t_{CTM_ENTRY} time.

The CTM is expected to be used in single-chip designs only. CTM is not supported for stacked designs. Once the device is in CTM, all fault delays and non-current fault's recovery delay times reduce to a value of t_{CTM_DELAY}. The fault recovery time for overcurrent faults (OCD1, OCD2, OCC, and SCD) is reduced to $t_{CTM\_OC\_REC}$.

Verification of protection fault functionality can be accomplished in a reduced timeframe in CTM. Reducing the VDD voltage to the same voltage applied to the highest-cell input pin for t_{CTM_ENTRY} will exit CTM.

In CTM, with reduced time for all internal delays, qualification of all faults will be reduced to a single instance. Thus, in this mode, fault-condition qualification is more susceptible to transients, so take care to have fault conditions clearly and cleanly applied during test mode to avoid false triggering of fault conditions during CTM.

ADVANCE INFORMATION

10 Power Supply Recommendations

The recommended cell voltage range is up to 5 V. If three cells in series are connecting to bq77915, the unused VCx pins should be shorted to the highest unused VCx pin. The recommended VDD range is from 3 V to 25 V. This implies the device is still operational when cell voltage is depleted down to the ~1.5-V range.

11 Layout

11.1 Layout Guidelines

1. Match SRN and SRP traces.
2. R_{IN} filters, VDD, AVDD filters, and the C_{VDD} capacitor should be placed close to the device pins.
3. Separate the device ground plane (low current ground) from the high current path. Filter capacitors should reference to the low current ground path or device Vss.
4. In a stack configuration, the R_{CTRD} and R_{CTRC} should be placed closer to the lower device CTRD and CTRC pins.
5. R_{GS} should be placed near the FETs.
6. In a stacked configuration, it must be ensured in the PCB layout that the trace from the VC5 pin to a cell and the trace from the VC0 pin of the next upper device to the immediately higher cell are kept separate.

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation see the following:

- *bq77915 3–5S Low-Power Protector Evaluation Module User's Guide* SLUUBU2

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Community Resources

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12.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

ADVANCE INFORMATION

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

ADVANCE INFORMATION

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
BQ7791500PWR	PREVIEW	TSSOP	PW	24	2000	TBD	Call TI	Call TI	-40 to 85		
BQ7791500PWT	PREVIEW	TSSOP	PW	24	250	TBD	Call TI	Call TI	-40 to 85		
PBQ7791500PWT	PREVIEW	TSSOP	PW	24	250	TBD	Call TI	Call TI	-40 to 85		

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

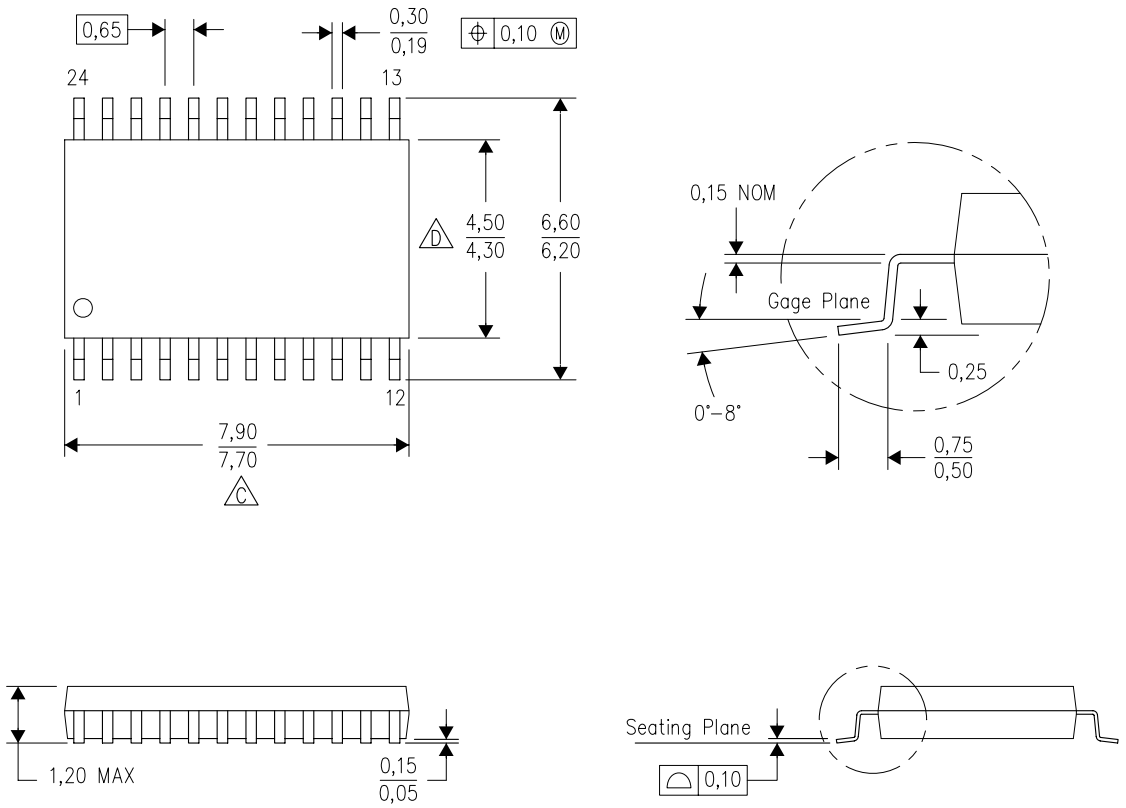
(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

PW (R–PDSO–G24) PLASTIC SMALL OUTLINE



4040064–6/G 02/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

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TI may expressly designate certain products as completing a particular qualification (e.g., Q100, Military Grade, or Enhanced Product). Designers agree that it has the necessary expertise to select the product with the appropriate qualification designation for their applications and that proper product selection is at Designers' own risk. Designers are solely responsible for compliance with all legal and regulatory requirements in connection with such selection.

Designer will fully indemnify TI and its representatives against any damages, costs, losses, and/or liabilities arising out of Designer's non-compliance with the terms and provisions of this Notice.

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