Advanced Logic Design

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0.1 Introduction

- exam:
  - written exam 50
  - project: worth the other 50
  - oral: optional, +-3
- material
  - slides on moodle
  - CMOS VLSI Design, A circuits and Systems Perspective, 4th ed, Addison-Wesley
  - Computer Architecture: a quantitative approach, Morgan Kaufmann

Chapter 1

Design Methodologies

1.1 Abstraction in IC Design

1.1.1 Transistor Level

- Design: devices litterally draw on the IC
- Transistor-Level layout
- Analysis: Transistor-level device simulation

1.1.2 Transistor schematics level

- Design: schematics drawn
- Synthesis: actual layout automatically generated through transistor-level layout compaction
- Analysis: Transistor-level device simulation
- can handle from 10's to few thousand transistors

1.1.3 Logic gates level

- Design: Logic schematics drawn using a gate-level layout editor
- synthesis: transistor schematics and layout generated
- automated place and route and compaction
- analysis: Gate-level simulator, and device level simulator

1.1.4 Standard cells level

- Draw schematics from pre-defined cells
- synthesis: layout generated using cell-based place and route
- analysis: Logic-level and gate-level simulation
- analysis: Static Timing Analysis

1.1.5 Register-transfer lebel (RTL)

- Design: provide a description of the state (registers) and how it changes during operations
- synthesis: standard cell synthesized and layout automatically generated
- analysis: behavioral and gate-level simulation
- analysis: static timing analysis using abstracted gate level models

1.1.6 Model-based design

- Design: cenceive a mathematical model of the system
- synthesis: derive algorithms that implement the mathematical model
- analysis: formal mathematical analysis of the model
- analysis: model simulation
- can handle milions of gates