## VAR-AM33CustomBoard



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#### Disclaimer:

SchematicS are for reference only. Variscite LTD provides no warranty for the use of these schematics. Schematics are subject to change without notice.

## Revision History

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Rev 1.0	Initial
Rev 1.02	Major changes:     LCD buffer added for SOM protection     GPMC mux changed     Back light connector added     LVDS connector pinout change
Rev 1.02A	Compatible to DVK with wired 1.02 PCB , refer to Ver 1.1 as a design reference
Rev 1.11	Major changes: VAR-SOM-AMM33 GPIO3_9 Replaced with GPIO3_4 USB Power limiter to 5V G.PHY 125Mhz clock topology update BUS Mux IC changed to resistor assembly option User button added G.PHY external delay lines added
Rev 1.11 A	10K pull up on GPMC CLK , added . Indicating 1.11 PCB revision
Rev 1.11 B	VAR-SOM-AM33 Pin 105,130- connected to GND Adding RX1 in parallel to D4 - Setting USB ID pin to 1.8V Max Do not use UART1 / MMC1 in case of on-som Wifi/BT module presense notification USB power distribution pull ups removed. USB port 4 power distribution fixed.
Rev 1.11 C	VAR-SOM-AM33 symbol pin 72 updated SPI1 muxing recommendation fix
Rev 1.11 D	VAR-SOM-AM33 pin 60 is N.C
Rev 1.11 E	I2C1 pull-ups not required MMC0_CMD pulled-up
Rev 1.11 F	L3 changed to 15uH
Rev 1.11 G	R11 / R12 changed to 100nf. Working as diffrential pairs fits TI original Alsamixer settings, both in Linux and Android
Rev 1.21	USB OTG scheme chagned, according to revised TI datasheet





# 02 - Block Diagram





















