TECHNICAL PUBLICATION

HDI Layer Stackups

for Large Dense PCBs

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INTRODUCTION

This paper is intended to help those who are doing large dense PCBs with multiple high pin-count BGAs and are finding standard laminate stackups inadequate to meet their cost and performance goals. Maybe your laminate board has too many layers, or the feature sizes prevent effective breakout and routing of the BGAs. HDI (High Density Interconnect) stackups are a viable alternative and can provide lower cost with higher performance if designed properly.

Hopefully from this paper you will be able to determine which stackup methodology is best for your designs and why the alternatives may not be appropriate. If you just want to find out which stackups are recommended, you can just skip to the end of the document. However, if you want to understand the reasons why these stackups are recommended and the impact of choosing one of the alternatives, then it would be best to read the whole paper.

Defining the appropriate stackup should be considered as one of the most important aspects of initial design work. Since there are so many variables involved with stackups, this paper will focus on stackups that will enable effective design of boards with multiple large and dense BGAs. Typically this includes boards for the networking, computer, server and emulation marketplace. It is assumed that even though handheld devices and consumer electronic products will likely have dense BGAs, it is unusual for them to have multiple instances exceeding 1500 pins and as such do not present the kind of design challenges of concern herein.

Fabrication Vendors

Stackups should be designed in conjunction with the fabrication vendor to minimize cost and meet signal integrity requirements. The board fabrication vendor ultimately builds a board that meets your requirements for cost, reliability, overall thickness, and impedance control. There may be additional requirements related to plating and specific materials. As a general rule, the vendor will adjust all the stackup variables as needed during their process to meet your goals. The most productive method is to agree with the vendor on a stackup prior to designing the board; and then the fabricator will need to make minimal adjustments to meet your goals.

A good example is impedance control. Regardless of how carefully the stackup is defined with trace widths, material choices, dielectric and copper thicknesses, the fabrication process is not so exact. Each vendor has different equipment and methods. The lamination process shrinks the dielectrics and materials may be changed if not in stock or readily available. The tolerances in all areas add up and ultimately a reliable vendor has to make the right combination of adjustments in-process so that when measuring impedance on the test coupon, it fulfills your spec. Trace widths and material thicknesses may change a little but if the measured impedance is within spec then it really doesn't matter what changes were made - as long as the other requirements are not fatally compromised of course.

If the initial stackup is not defined properly, minor acceptable adjustments by the fabrication vendor will not be adequate to fulfill your overall requirements. A wise and experienced vendor will not accept the risk of making major changes to the design data.

Dependencies

Unfortunately there are many dependencies, some of them circular when defining a stackup. The process of determining an effective stackup can be overwhelming. Forgive the next meandering and confusing paragraph; but it is a good example of the difficult process of deciding which variables need to be compromised or emphasized to reach your goals: It is necessary to reduce the layer count to keep costs down. On some of the largest PCBs, there are well over ten thousand nets which require many layers for routing. To control crosstalk, you need to increase the spacing between traces which will likely necessitate even more layers. You may also want to run the diff pairs together through the via array under the BGA, which means the via must be small enough to not only allow the diff pair to run together, but also space the traces far enough apart to attain the desired coupling. These traces also need to be the appropriate width in correlation to the thickness of the dielectrics and their material attributes to provide the desired impedance. But if you have too many layers, then the via needs to be bigger otherwise the aspect ratio of hole size to length becomes too great to drill with a good yield. If you make the via hole smaller, you can enable more dense routing but may sacrifice manufacturing yields. If you make the via hole larger, you may have to split the diff pairs through the BGA fanout via array, negatively impacting the signal

integrity. If you have more layers because you have to split the diff pairs, you will need an even larger via. On top of that, all these factors may require you to develop special fanout patterns in the context of the stackup to support the manufacturing, signal integrity and routing goals. This paragraph just touches a few of the dependencies; yet even so, it describes a daunting task.

Where does one start then? Later in this paper you will see a number of example stackups with the advantages and disadvantages plus a basic description of which via models, design rules work best. Some signal and power integrity concerns will also be addressed.

Overview of Stackup Types

In the context of boards that have high pin-count BGAs, there are three stackup types of interest:

1. **Standard Lamination with Through Vias**

Advantages

- Low cost (until layer count becomes too high)
- Simple via models
- Simple dielectrics - Primarily FR-4
- Mature process, "everybody does it"
- High reliability (until layer count becomes too high)

Disadvantages

- If layer count becomes too high
- Fewer fabrication vendors can obtain good yields, costs skyrocket
- Can delaminate under high temperatures required for ROHS lead-free soldering
- Via has to be large, reducing route-ability, increasing layers
- Difficult to implement for BGA pin-pitches below 1mm
- Through hole vias capacitively couple to every plane layer and signal losses increase with thickness
- Long via stubs create impedance mismatches, reflections on single-ended nets
- Large via pads often force diff pairs to be split under BGAs

Recommendations

There are a number of tipping points where standard lamination with through vias is not viable

- Once the board is over 28 layers, it becomes difficult to manufacture with acceptable yields and therefore can become cost prohibitive.
- If the board is over 28 layers, the dielectrics can be so thin that delamination can occur under the higher temperatures required for lead-free soldering.
- Generally when using a few BGAs with less than 1500 pins and a 1mm pin-pitch, the breakout and routing of these devices is feasible using through vias.
  - However, if you have a large number these on a single design, then the route density may force the layer count up high enough to limit the effectiveness of this stackup.
  - If you have multiple BGAs with over 1500 pins and 0.8mm pin-pitch (or less) it is likely that through vias will make it very difficult to route these devices.
- When the thickness of the board due to the number of layers forces the via to be so large that it inhibits route-ability.
  - Via length to hole diameter should be <10x otherwise reliability declines significantly.
  - Pad diameter should be hole size plus 0.01"
  - If the via pad is so large that it prevents diff pairs or multiple single-ended traces from being routed between the BGA via arrays, then more layers will be required to complete the routing.
    - Vias can be shifted off the standard matrix under BGAs; however, with through vias, not much is gained.

2. **Sequential Lamination with Blind & Buried Vias**

Advantages

- Potentially shorter via stubs
- Fairly simple via models
- Generally smaller vias than required for through hole vias
  - Minimum size for mechanically drilled vias are the same as for standard laminate; however blind and buried vias will likely have a smaller aspect ratio enabling more use of minimum via hole size, which is 8th.

- Simple dielectrics - Primarily FR-4
- Effective use of blind & buried vias opens up routing channels, potential for fewer layers

Disadvantages

- Not a widely adopted process, more and more fabricators do HDI instead
- Minimum size for drilled vias is 8th
- Costs more than through hole laminated, yet minimum trace widths are still the same
- Practical reliability limits the number of sequential laminations to 2 or 3

Recommendations

- Sequentially laminated boards have the same tipping points as standard laminates; however, since the via length to hole size aspect ratio will be less and pad sizes can be smaller, route-ability improves and it is less likely that the design would exceed 28 layers.
- Since the feature sizes for traces can vias are still the same as with standard laminate, designing with multiple large BGAs of < 1mm is very difficult.

3. Buildup with Micro-Vias (HDI)

Advantages

- Smaller feature sizes for vias and traces enables higher route density and fewer layers
- Effective use of micro-via patterns opens up routing channels, potential for fewer layers
- Only practical way to design with multiple large BGAs having <0.8 mm pitch
- Lowest cost for high density boards
- Improved signal and power integrity
  - With appropriate stackup definition
- Materials do well in processes requiring ROHS
- Newer materials available of higher performance and lower costs
  - These new materials are not suitable for standard or sequential lamination

Disadvantages

- Complex via models
  - Many variations and still evolving
- Complex stackup definition
- Effective design methods on large dense designs have not been widely understood and documentation is sparse
- Predictive design guides and cost estimates not yet available
- Although HDI fabrication is pervasive in PAC Rim and China, North America slow to adopt

Recommendations

- HDI is the best alternative to high layer-count and expensive standard laminate or sequentially laminated boards.
- The trend is for higher pin-count and finer pin-pitch. The tipping point will occur when the >1500 pin BGAs use a .8mm pitch.
  - The only way to effectively breakout and route multiple instances of these devices on a single board will be with the smaller HDI feature sizes.
- HDI currently dominates the fabrication technology for handheld and consumer electronics. For large board designs, it will continue to grow.

HDI Stackup Details

This section is provided as a reference describing the relevant HDI stackup information based on the Institute of Printed Circuits (IPC) standard.

In this section Types I, II & III are described. Type III is the recommended configuration for large dense boards with multiple high pin-count BGAs.

IPC-2315 Design Guide for High Density Interconnects & Microvias

Published jointly with the Japan Printed Circuits Association, IPC/JPCA-2315 provides an easy to follow tutorial on the selection of HDI and microvia design rules and structures. Addresses various considerations when designing an HDI printed wiring board including design examples and processes, selection of materials, general descriptions, and various microvia technologies. Offers designers and manufacturers one source for reliable design and manufacturability information for commonly produced HDI boards. Includes over 30 full color illustrations. 33 pages. Released June 2000.

HDI Type I

This construction uses both micro-vias and through-vias in a structure consisting of a laminated core and a single micro-via layer on at least one side.

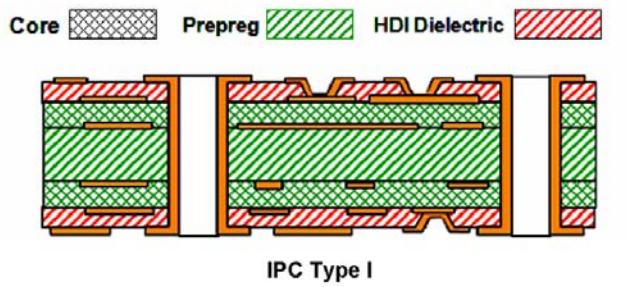

Figure 1

Notes:

1. The number of layers in the laminated core varies and is limited by two factors
   a. The through-via should have an aspect ratio (total length to hole size) less than 10x to maintain reasonable reliability.
   b. If the FR-4 dielectrics become too thin, they will delaminate under higher temperatures required for lead-free soldering.

Recommendations

- In the context of large dense boards with multiple high pin-count BGAs, this stackup will not be significantly better than laminate.
  - The through via pads will need to be large.
  - Using only a single micro-via layer will limit the ability to benefit from the smaller via and trace feature sizes.

HDI Type II

This construction uses micro-vias, buried-vias, and may have through-vias.

- There is a single micro-via layer on at least one side.
- Via holes are drilled in a laminated core and become buried when the dielectric material is added for the micro-vias.
- Micro-vias are staggered from other micro-vias and may be stacked or staggered relative to the buried vias.

Additional Notes:

1. See Type I note above on limiting the number of laminated core layers which applies to all variations of Type II through and buried vias.

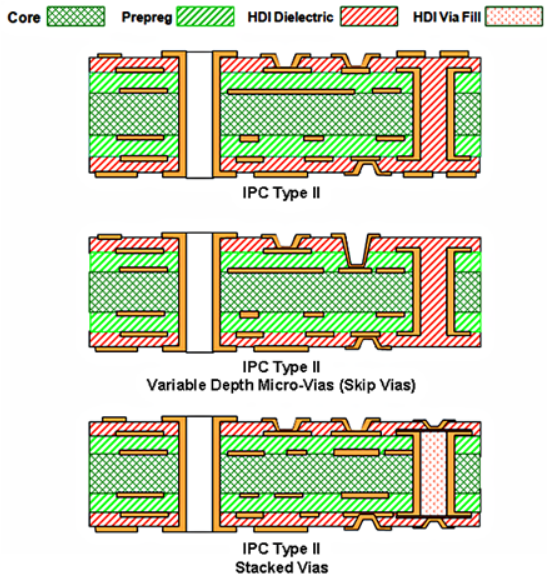

Figure 2

Recommendations

- In the context of large dense boards with multiple high pin-count BGAs, this stackup is better than Type I; however, is not adequate for the more difficult designs.
  - Using buried vias instead of the through vias is a significant advantage.
  - Using only a single micro-via layer will limit the ability to benefit from the smaller via and trace feature sizes.
- The single micro-via layer also restricts the viability of using the outer layers for a GND plane. Having only one buildup layer for routing traces isn't nearly as effective as two.

HDI Type III

This construction uses microvias, buried vias, and may have through vias.

- There are at least two micro-via layers on at least one side.

- Via holes are drilled in a laminated core and become buried when the dielectric material is added for the microvias.
- Micro-vias may be staggered or stacked with themselves and the buried vias

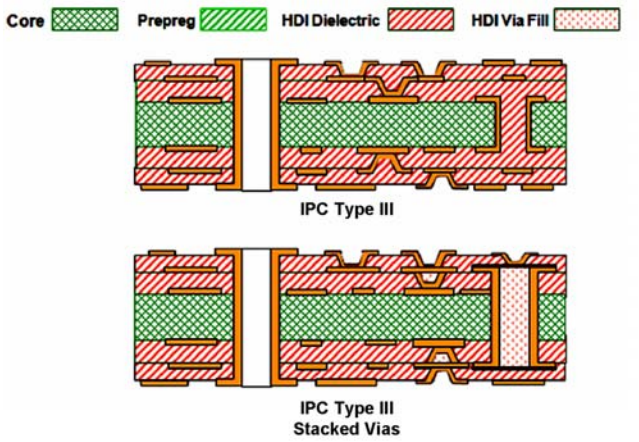

Figure 3

Additional Notes:

1. See Type I note above on limiting the number of laminated core layers which applies to all variations of Type III through and buried vias.

Recommendations

- HDI Type III is the best stackup configuration for large dense boards with multiple high pin-count BGAs.
- With two micro-via layers there is considerable routing area available using the smaller via and trace feature sizes.
- Using the outer layers for a GND plane is feasible because there are still enough micro-via layers available for signal routing.
- Using stacked vias will allow for greater route density; however, the cost will be higher.

HDI Type IV, V, VI

These additional HDI Types are defined in the IPC-2315 specification; however, they are not presented here simply because they are more expensive to fabricate and are probably not necessary for large dense PCBs with BGA breakout and routing challenges.

Via Models

HDI Type III accommodates numerous via models and spans. Ultimately the via model that suits your design best will be driven by finding the least expensive method that will still enable adequate route density within the constraints of signal integrity.

The graphic below represents some of the via models that may be used in HDI Type III.

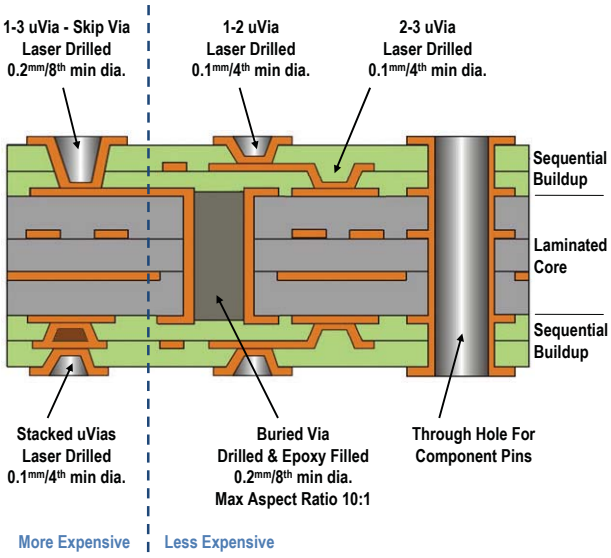

Figure 4

- Skip Vias - This via model is effective for transitioning layers (because it emulates the stacked via); however it is not as efficient as stacked vias for route space due to the fact that the minimum diameter is 8th.
- Buried-vias - As a general rule, all unused pads on the buried-vias should be removed. This will significantly reduce the crosstalk.
- Micro-via Pad Sizes - Although the pad size will vary by fabricator, using a pad .15mm/6th larger than the hole is adequate.
- Via Aspect Ratio - Hole length to diameter: Micro-vias 5:1, buried-vias 10:1

Alternative Via Spans

- Stacking Micro-Vias and Buried-Vias
  As shown below, the micro-vias may be stacked with themselves and/or with the buried-vias.

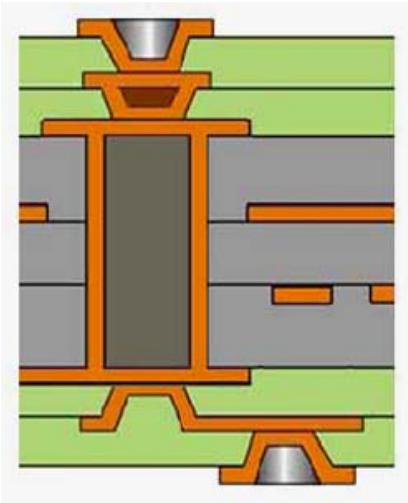

Figure 5

Advantages

- Using stacked vias enables the most flexible and efficient via configuration for routing.

Disadvantages

- Stacking vias generally costs more due to additional steps required to ensure a good connection between the vias.

- Extending Buried-Vias
  As shown below, you can extend the buried-via into the first micro-via layer.

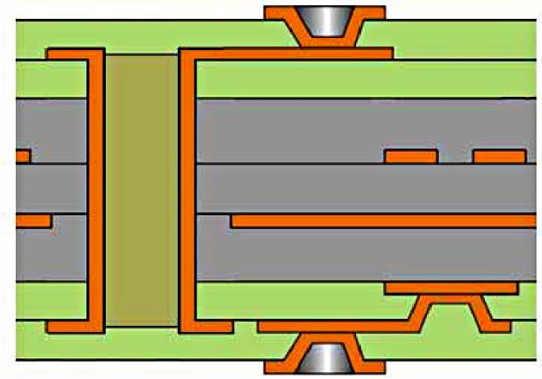

Figure 6

Advantages

- If you have power and ground nets that need to extend all the way through the board, using the extended buried-via uses less space.

Disadvantages

- Single-ended nets that use the extended blind via may suffer from additional via-stub effects; however, the additional stub length may be insignificant depending on the frequency.
- Depending on the fabricator, the cost of extending the buried-via may be slightly more than just having the buried-via in the laminated core.

Layer Count

The number of buildup and core layers required to route the board and fulfill the performance and signal integrity requirements will vary depending on the route density and manner in which you decide to manage the plane layer assignments. Determining the route density is a subject outside the scope of this paper; however, as a general rule for large dense boards start with 8-10 signal layers and increase them as needed during the routing process.

Since the thickness of the laminated core will be limited by the aspect ratio of the buried via (10:1), work with your board fabricator to determine core and prepreg thicknesses. Doing this in conjunction with trying to minimize via pad size for routing will enable you to determine the high-end number of layers available in the laminated core.

Design Rules

Throughout this paper, the minimum values for via hole sizes, pad sizes and the aspect ratios have been described. These minimums are used as a guide to enable high yields. Minimum trace widths and clearances are based upon the fabricator's capabilities; however, are more than likely to be set based on signal integrity requirements such as impedance control and minimizing crosstalk.

Fanout Patterns

The method used for fanout of BGAs is a worthy subject for its own paper and can significantly contribute to the success or failure of the design.

Here are some of the considerations:

- Via location relative to BGA pad
  - Adjacent (dog-bone)
  - Partial via-in-pad
  - Offset via-in-pad
  - Via-in-pad
- When using a combination of micro-vias and buried-vias, each via span can have its own pattern within the BGA and as such can affect the route-ability of the device.
  - Via-in-pad methods provide the greatest opportunity to increase route density.
  - Shifting and aligning the vias is likely to improve route-ability.
  - Using a complimentary patterns for the micro-vias and buried-vias can improve route-ability
  - Goal should be to reduce the overall "effective" number of pins by the time you get to the laminated core, thus reducing the number of layers required to breakout and route the BGA.

Recommended Stackup Criteria

A primary driver for going to HDI is to obtain sufficient route density to reduce layer count, thus lowering costs and improving reliability. Yet this must be done while maintaining power and signal integrity. Cost, density, power and signal integrity are the factors used in this paper to determine which stackups are recommended.

HDI Cost

There are four drivers that determine the fabrication cost for HDI boards.

- Materials - Not only the type of material used but also the amount. So obviously a larger board will cost more than a smaller one.
- Laminations - The more lamination steps, the higher the cost. When buildup layers and via spans are mirrored about the core, then they can be done in the same lamination step. As you will see in the recommended stackups, the manner in which the via spans are defined affects the number of laminations.
- Drills - The more drill setups required, the higher the cost. A thru hole, buried via and a uVia each count as single drill setup. When buildup layers and via spans are mirrored about the core, then the uVia drilling on both sides is considered as one drill setup. The manner in which the via spans are defined affects the number of drill setups.
- Plating - Plating steps affects the cost, the more steps the higher the cost. These steps are used to plate the via wall and to ensure a reliable connection at the bottom of the drill. Using stacked vias and additional buildup layers generally increases the number of plating steps.

Route Density

Micro-vias and smaller trace widths on buildup layers can significantly improve route density. Via-in-pad and stacking vias is also very good for improving route density. Using micro-vias and blind vias in certain patterns can open considerable space for routing on the laminate core layers. Ultimately increasing route density will reduce your layer count and overall fabrication costs.

Power Integrity

In the context of an HDI Type III stackup, location of the planes will impact your power distribution and integrity along with signal integrity. The appropriate location of planes is a much deeper and more complicated subject than can be addressed in this paper; however, certain methodologies are recognized as effective and will be described at a high level herein.

In the stackups shown below, the number of layers in the laminated core is variable of course. 16 layers is just convenient for the purpose of showing plane layer assignments graphically.

- Outer Layer GND
  A stackup such as this one is typical when GND is assigned to the outer layers.

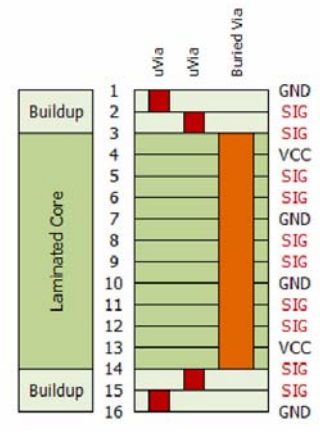

Figure 7

Advantages

- GND on the outer layers provide an excellent EMI shield.
- If you can place the bypass capacitors for the BGA on the same layer as the BGA, then you can minimize the number of vias used for GND underneath the BGA. This will open routing channels which may be critical for an extremely dense board.
  - You my still want vias for some of the GND pins to improve the return paths

Disadvantages

- If you manage your return paths with an appropriate but not excessive number of GND vias under the BGA, then there really isn't a downside to using this method.
- Some may say that using the outer layers for GND will limit the number of buildup (smaller features) layers for routing signals. Although this is true, it is also important to consider that controlling the signal integrity of those nets will be more difficult and burying the first GND plane in the laminate structure will result in the routing on the micro-via layers to not have a good reference plane.

- **Outer Layer GND & VCC**
  A stackup such as this one is typical when GND is assigned to the outer layers.

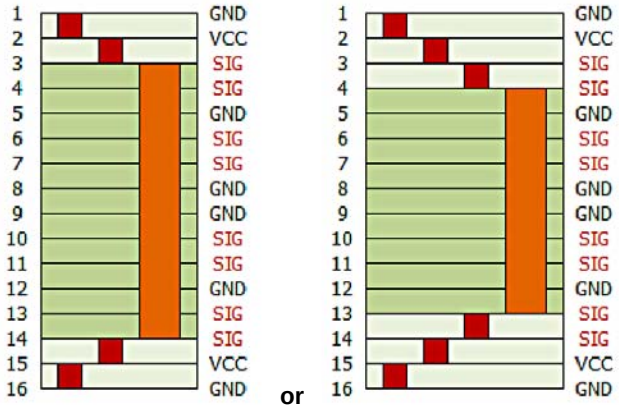

Figure 8

Notes:

- Using stacked-vias would be good for this kind of stackup if it can be cost justified.
  Advantages
- Same advantages as listed for "Outer Layer GND" above plus these additional ones:
- The capacitive coupling between the GND and VCC layers will be excellent minimizing the bypass capacitors needed for the BGA (assuming you use a relatively thin dielectric - less than .05mm or 2th).
- This is also an opportunity to use embedded capacitors and pull-up resistors effectively.
  - Considerable routing space would be opened on all the signal layers.

Disadvantages

- If you manage your return paths with an appropriate but not excessive number of GND vias under the BGA, then there really isn't a downside to using this method.

- Split Planes

  Often large BGAs require multiple voltage supplies. You can use split planes or dedicated voltage layers for this power distribution. It would be best to add a couple voltage supply layers in the center of the board surrounded by GND planes to avoid having signal layers affected by crossing the splits or different voltages.

Signal Integrity

This is a subject that has many dependencies, variables and thousands of articles. No attempt here to do anything but point out a few design methods related to large board HDI stackups that will positively affect signal integrity.

- Remove unused pads on buried vias. This will reduce crosstalk significantly.
- Route the high-speed single-ended nets on the buildup layers closest to the component. Stub effects are eliminated because buried-vias are not used.
- Route diff pairs on the laminated core layers. The via stubs affect the diff pairs less than the single-ended nets and the crosstalk between the diff pair vias (if the unused pads are removed) is likely to be insignificant.
- A stripline configuration where pairs of signal layers are sandwiched between plane layers

not only provide the best return paths but also reduce crosstalk. This supports the notion that using a GND plane on the outer layers is a good practice.

Recommended HDI Type III Stackups

What are the best HDI stackups? It depends on your priorities. These stackups were analyzed for relative cost, route density, power integrity and signal integrity. The following three are rated at the top with the priority given to route density with good power and signal integrity:

Stackup A

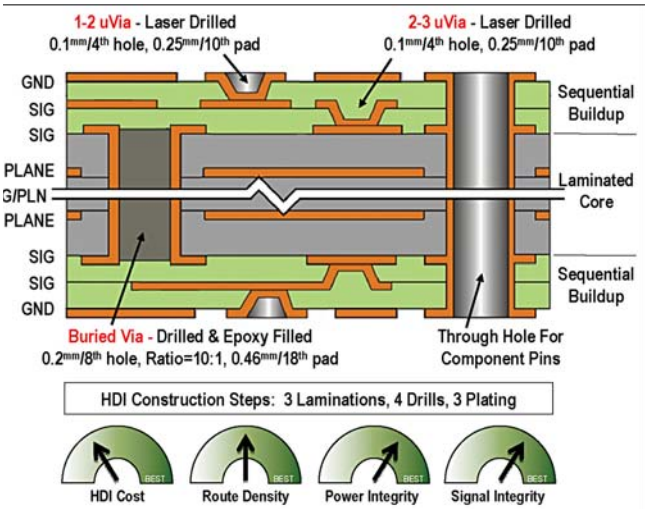

Figure 9

Comments:

- This is a good average of the variables and a great stackup to start with if this is your first attempt at HDI.
- The via models are simple and it won't be difficult to find vendors who can fabricate it.
- The GND plane on the outer layers provides the igh rating for power and signal integrity.

Stackup B

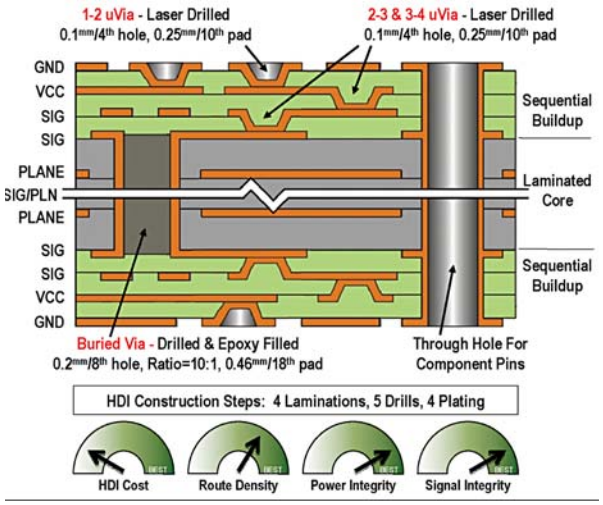

Figure 10

Comments:

- The GND and VCC on the outer layers provide the best power and signal integrity.
- The additional buildup layer increases the cost (more laminations, drills and plating steps) but also improves the route density as opposed to losing an HDI routing layer due to the VCC plane.
- The via models are simple and it won't be difficult to find vendors who can fabricate it.

Stackup C

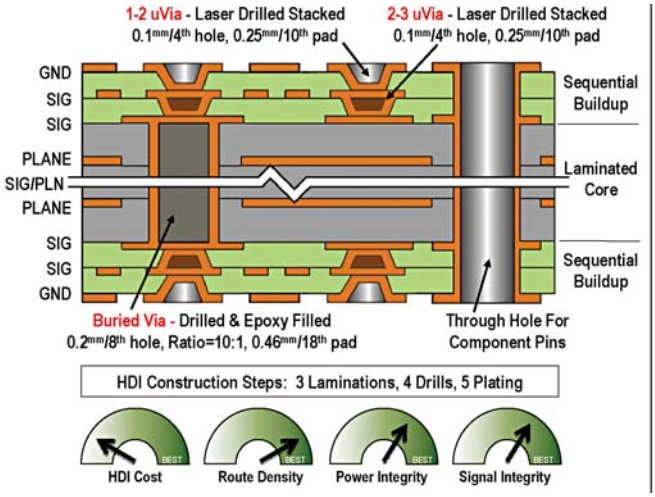

Figure 11

Comments:

- The stacked vias enable the best route density but also increases the cost and may limit the number of vendors who can fabricate this stackup.
- The GND plane on the outer layers provides the high rating for power and signal integrity.

Secondary HDI Stackups

These stackups are useful in their own way depending on priorities; but they not as good overall as the Top 3.

Stackup D

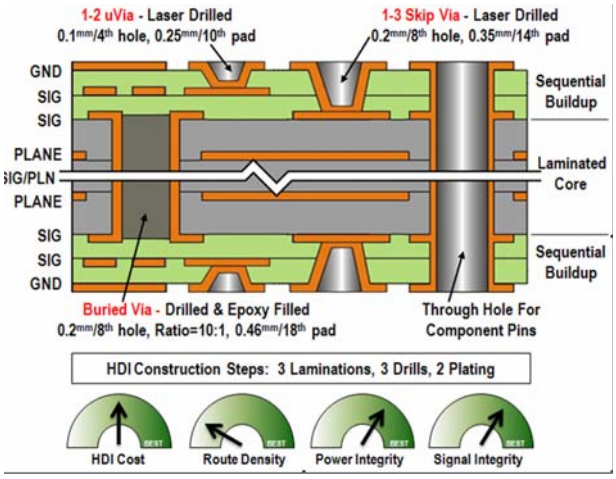

Figure 12

Comments:

- The GND plane on the outer layers provides the high rating for power and signal integrity.
- The skip via reduces laminations and plating steps which lowers cost; however, contributes to a relatively low route density.

Stackup E

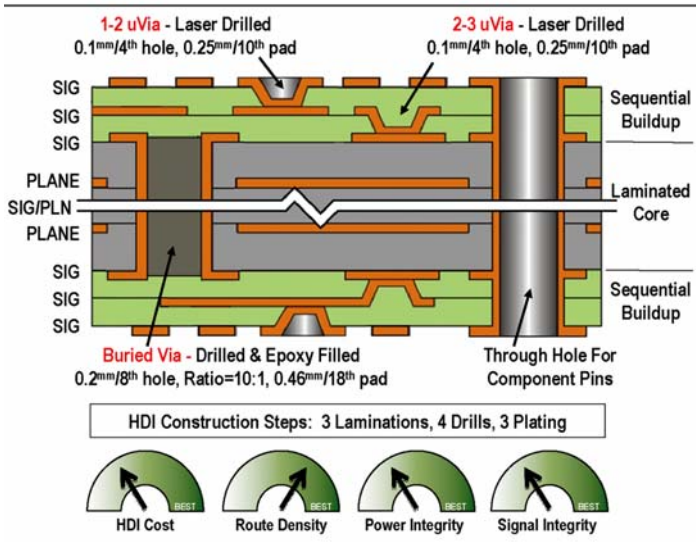

Figure 13

Comments:

- The via models are simple and it won't be difficult to find vendors who can fabricate it.
- The lack of a GND plane on the outer layers reduces power and signal integrity; however it does provide for improved route density assuming routing would be done on the outer layers.

Stackup F

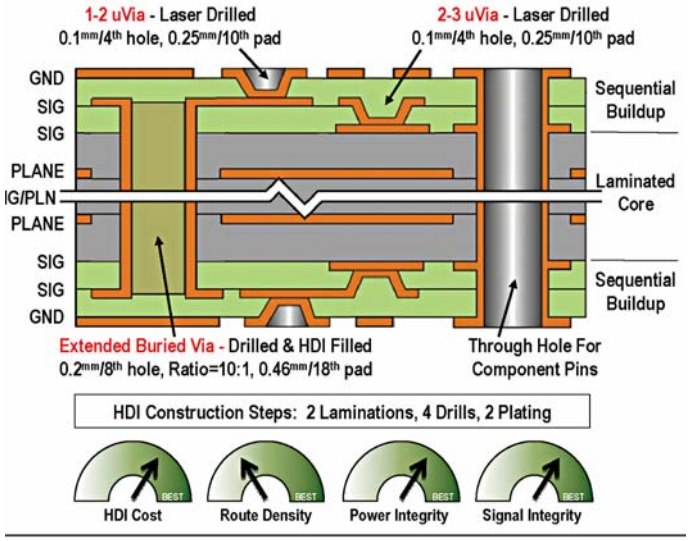

Figure 14

Comments:

- The GND plane on the outer layers provides the high rating for power and signal integrity.
- The extended buried via reduces the lamination and platin steps which lowers cost; however it reduces route density.

Stackup G

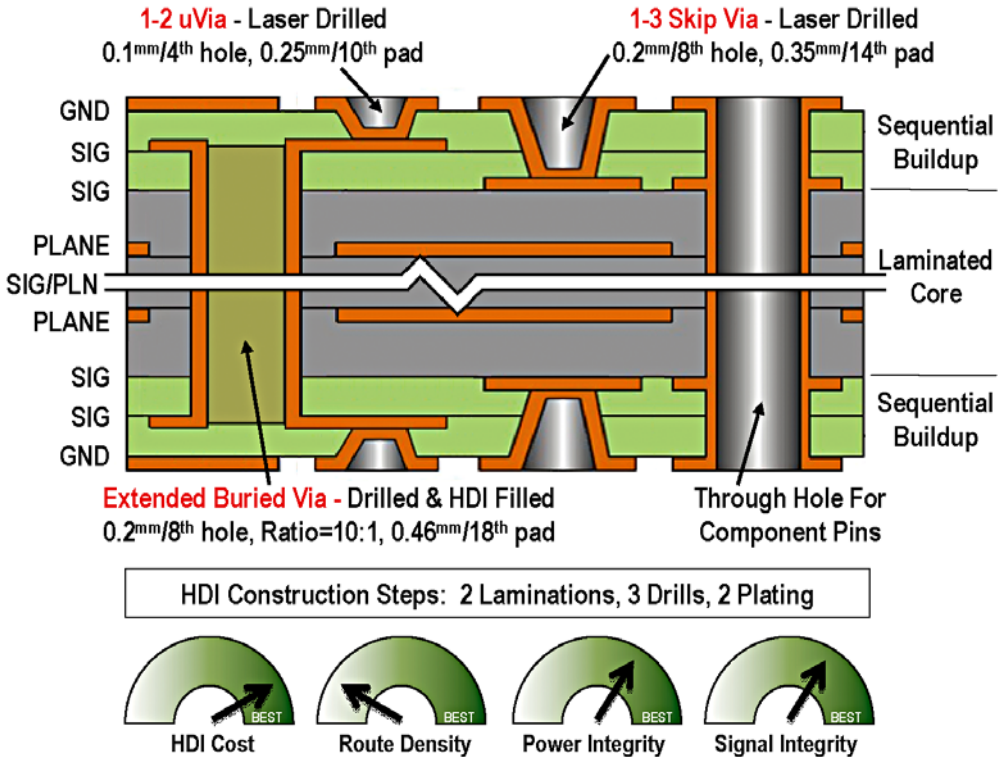

Figure 15

Comments:

- The GND plane on the outer layers provides the high rating for power and signal integrity.
- The extended buried via and the skip via reduces the lamination and plating steps which lowers cost; however it also reduces route density.

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