# Overview

iVCP1 is an encoder IP (Intellectual Property) which provides low-latency encoding capability on the basis of H.264 video coding scheme. iVCP1 operates at sequence unit, once iVCP1 starts, it can continue operating without the host CPU. Moreover, iVCP1 can encode maximum 1080p30 at 133MHz low frequency without frame memory.



Table 1‑3: Sub-module Description

| Abbr. | Description | Abbr. | Description |
| --- | --- | --- | --- |
| PBC | Picture Buffer Control module | IME | Intra Mode Estimation module |
| TRF | Quantization, conversion, inverse quantization, inverse conversion and intra prediction | VLC | Variable Length Coding module |
| RATE | Rate control module | CTRL | Control module |

iVCP1 encoding process is the sequence unit, once iVCP1 is kicked after initial setting by CPU, iVCP1 continues encoding process accoding to input image timing from camera interface

## Interfaces

APB Target Ports: A 32-bit APB bus is connected to iVCP1.

Camera Interface: iVCP1 has camera interface which input pixel data.

Stream Interface: iVCP1 has stream interface which output encoded stream

## Clock Distribution

iVCP1 has three clock domains, camera clock domain from external camera clock(clk\_p), IP main clock domain and APB bus clock domain. Camera clock domain and IP main clock domain (clk\_m) can be driven asynchronously. APB clock domain should be synchronized clock with IP main clock domain, but APB clock is permitted integer ratio to IP main clock, such as 1:2, 1:3 or 1:4 with clock synchronized signal control. The clock synchronized signal is described in 5.3.4.



## Start setting for iVCP1



## Reset Operation

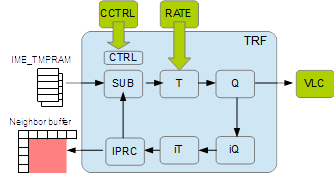
iVCP1 has a hardware reset controlled by input port and a software reset controlled by register setting. The software reset is separated to each modules, it should be set simultaneously. These register is switched back to “0” automatically.

**TRF module**

**1.1. Main function.**

Encoding

* Get picture parameter/MB parameter / template data (TMP) from SRAM (Written by IME)
* Create residual data by template data and intra prediction data
* Get quantization parameter (QP) from RATE via direct connection.
* Do Transform (T) operation.
* Do Quantization (Q) operation.

Figure 1-2: TRF block diagram

*Table 1-2: TRF Sub-modules*

| **Module** | **Function000----------p** | **Description** |
| --- | --- | --- |
| TCTRL | Controller | Control whole TRF.  Control pipelines in sub modules.  Control the MB/picture parameter. |
| IPRC | Intra prediction  Reconstruction  Subtraction | Predict according to block parameter.  Create reconstruct image and store for next MB IP enc  Create residual image for transform |
| T | Transformation | Transform data from IPRC horizontally and vertically. |
| Q | Quantization | Quantize data in from T and output them to IQ and VLC |
| IQ | Inverse Quantization | Inverse quantize data from Q (ENC) |
| IT | Inverse Transformation | I-transform residual coef from iQ H/V to make reconstruct data for next MB prediction |

**iVCP1**

**Overview**

**Features**

**Main Functions**

**Block Diagram**

**Interfaces**

**Input & Output**

**iVCP1 Operation**

**Reset Operation**

**iVCP1/TRF Module**

**Position**

**Block diagram**

***TRF SRAM list***

***TRF Sub-modules***

**IPRC Sub-module**

**Function  
Interfaces**

**MB preparation**

**INTRA Prediction**

**RC operation (Reconstruct data)**

**T Sub-module**

**T horizontal processing**

**T vertical Processing**

**Q Sub-module**

**Q operation**

**iQ Sub-module**

**IQ Stages**

**IT Sub-module**

**IT horizontal processing**

**IT vertical processing**

**Internal Data ranges**