TANK REFILLING ALARM

Digital Logic Design
Project Report

Abstract: The purpose of this project is to design and develop a control system of water tank refilling based on logic gates. The system contains logic gates, input , outputs and LED light which indicates the alarm.

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Motivation (Background)

This project idea came in my mind when I was sitting with my family members and one of my cousin discuss about the big loss in his water plant. where the all water tanks become empty and the staff was not aware about the vacant tanks because they didn't have any system or device connected with water tanks which indicate them about the level of water in the tanks.

Then I discuss this loss with my group members So we came with an idea to make a circuit which alarms the company when approximately 60% of the tanks need refill so that the company will safe from a big loss

For this purpose we make this project.

Circuit is attached below.

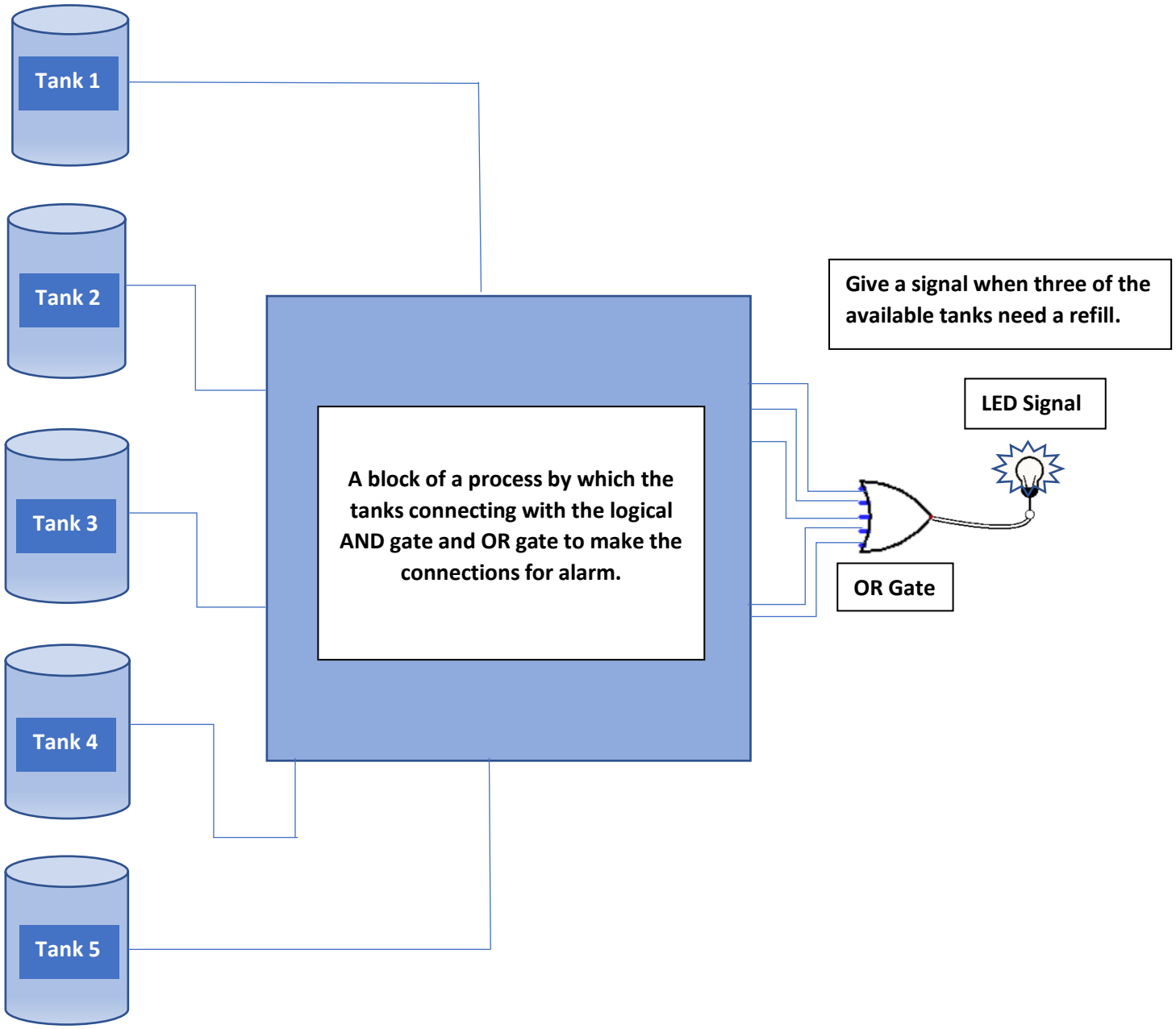
➢ I/Os Assignment Table (Truth Table)

We make the truth table in which we use the concept of our project that when any 3 or more than 3 tanks needs refill means their value become low(0) so at that time our led should glow means high(1)

A	B	C	D	E	Output
0	0	0	0	0	1
0	0	0	0	1	1
0	0	0	1	0	1
0	0	0	1	1	1
0	0	1	0	0	1
0	0	1	0	1	1
0	0	1	1	0	1
0	0	1	1	1	0
0	1	0	0	0	1
0	1	0	0	1	1
0	1	0	1	0	1
0	1	0	1	1	0
0	1	1	0	0	1
0	1	1	0	1	0
0	1	1	1	0	0
0	1	1	1	1	0
1	0	0	0	0	1
1	0	0	0	1	1
1	0	0	1	0	1
1	0	0	1	1	0
1	0	1	0	0	1
1	0	1	0	1	0
1	0	1	1	0	0

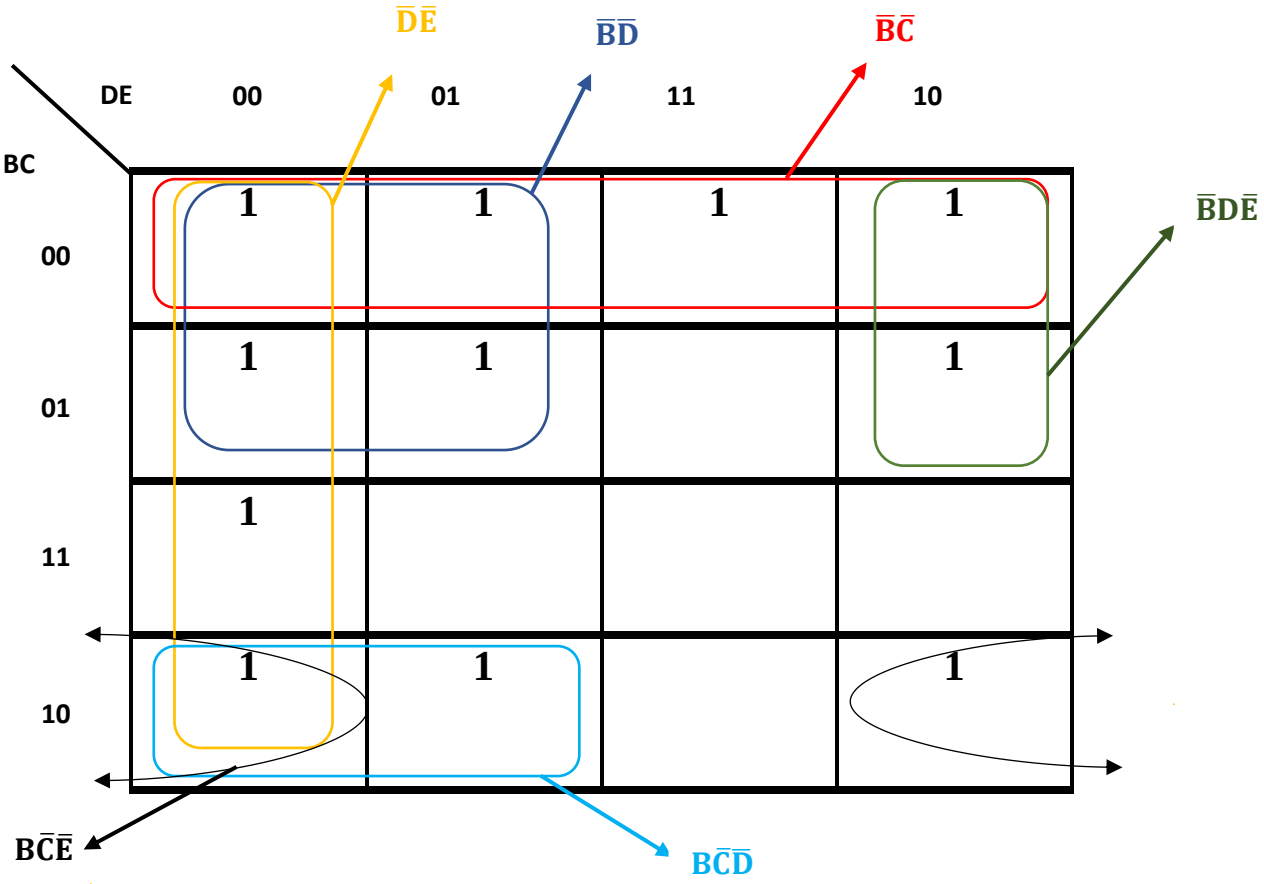
1	0	1	1	1	0
1	1	0	0	0	1
1	1	0	0	1	0
1	1	0	1	0	0
1	1	0	1	1	0
1	1	1	0	0	0
1	1	1	0	1	0
1	1	1	1	0	0
1	1	1	1	1	0

➢ Project Block Diagram



➢ Project Description

For the proper working of the project, first we draw a Karnaugh map for A= 0



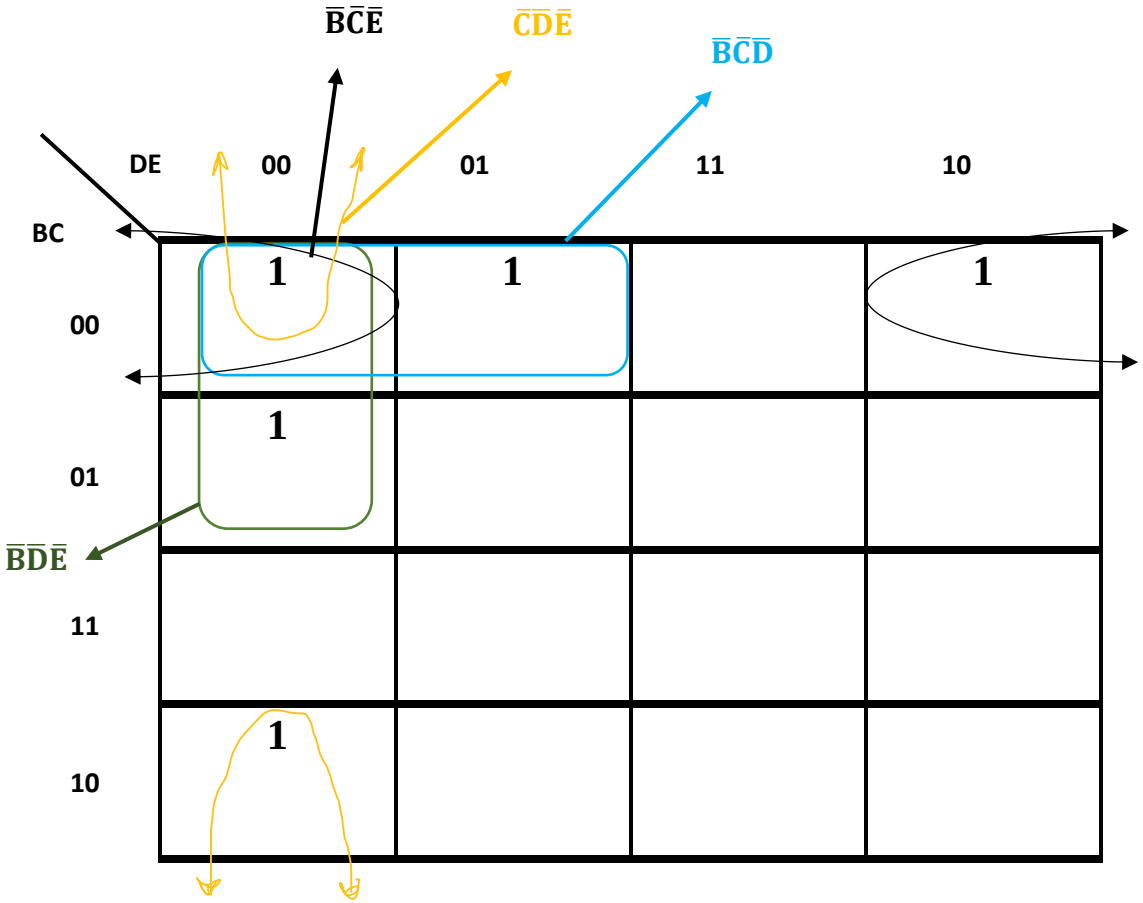
➔ Expression For A = 0 :

$\bar{B}\bar{C} + \bar{B}\bar{D} + \bar{D}\bar{E} + \bar{B}D\bar{E} + B\bar{C}\bar{D} + B\bar{C}\bar{E}$

$\bar{A}\,(\,\bar{B}\bar{C} + \bar{B}\bar{D} + \bar{D}\bar{E} + \bar{B}D\bar{E} + B\bar{C}\bar{D} + B\bar{C}\bar{E}\,)$

$\bar{A}\bar{B}\bar{C} + \bar{A}\bar{B}\bar{D} + \bar{A}\bar{D}\bar{E} + \bar{A}\bar{B}D\bar{E} + \bar{A}B\bar{C}\bar{D} + \bar{A}B\bar{C}\bar{E}$

Then we draw a Karnaugh map for A = 1



➔ **Expression For A = 1 :**

$\bar{B}\bar{D}\bar{E} + \bar{B}\bar{C}\bar{D} + \bar{B}\bar{C}\bar{E} + \bar{C}\bar{D}\bar{E}$

$A(\bar{B}\bar{D}\bar{E} + \bar{B}\bar{C}\bar{D} + \bar{B}\bar{C}\bar{E} + \bar{C}\bar{D}\bar{E})$

$A\bar{B}\bar{D}\bar{E} + A\bar{B}\bar{C}\bar{D} + A\bar{B}\bar{C}\bar{E} + A\bar{C}\bar{D}\bar{E}$

➔ **Final Expression:**

Then we combine both the expressions to make the final expression,

$$\bar{A}\bar{B}\bar{C} + \bar{A}\bar{B}\bar{D} + \bar{A}\bar{D}\bar{E} + \bar{A}\bar{B}\bar{D}\bar{E} + \bar{A}\bar{B}\bar{C}\bar{D} + \bar{A}\bar{B}\bar{C}\bar{E} + \bar{A}\bar{B}\bar{D}\bar{E} + \bar{A}\bar{B}\bar{C}\bar{D} + \bar{A}\bar{B}\bar{C}\bar{E} + \bar{A}\bar{C}\bar{D}\bar{E}$$

$$\bar{B}\bar{C}(\bar{A} + \bar{A}\bar{D} + \bar{A}\bar{E}) + \bar{B}\bar{D}(\bar{A} + \bar{A}\bar{E}) + \bar{D}\bar{E}(\bar{A} + \bar{A}\bar{C}) + \bar{A}\bar{B}\bar{C}(\bar{D} + \bar{E}) + \bar{A}\bar{B}\bar{D}\bar{E}$$

$$\bar{B}\bar{C}(\bar{A} + \bar{A}\bar{D} + \bar{A}\bar{E}) + \bar{B}\bar{D}(\bar{A} + \bar{E})\bar{A}\bar{B}\bar{D} + \bar{D}\bar{E}(\bar{A} + \bar{C}) + \bar{A}\bar{B}\bar{C}(\bar{D} + \bar{E}) + \bar{A}\bar{B}\bar{D}\bar{E}$$

Using Rule: 11

to the 2nd and 3rd term

$$A + \bar{A}B = A + B$$

$$\because \bar{A} + A\bar{B} = \bar{A} + \bar{B}$$

$$\bar{B}\bar{C}(\bar{A} + \bar{D} + \bar{E}) + \bar{B}\bar{D}(\bar{A} + \bar{E}) + \bar{D}\bar{E}(\bar{A} + \bar{C}) + \bar{A}\bar{B}\bar{C}(\bar{D} + \bar{E}) + \bar{A}\bar{B}\bar{D}\bar{E}$$

Using Rule: 11

to the 1st term

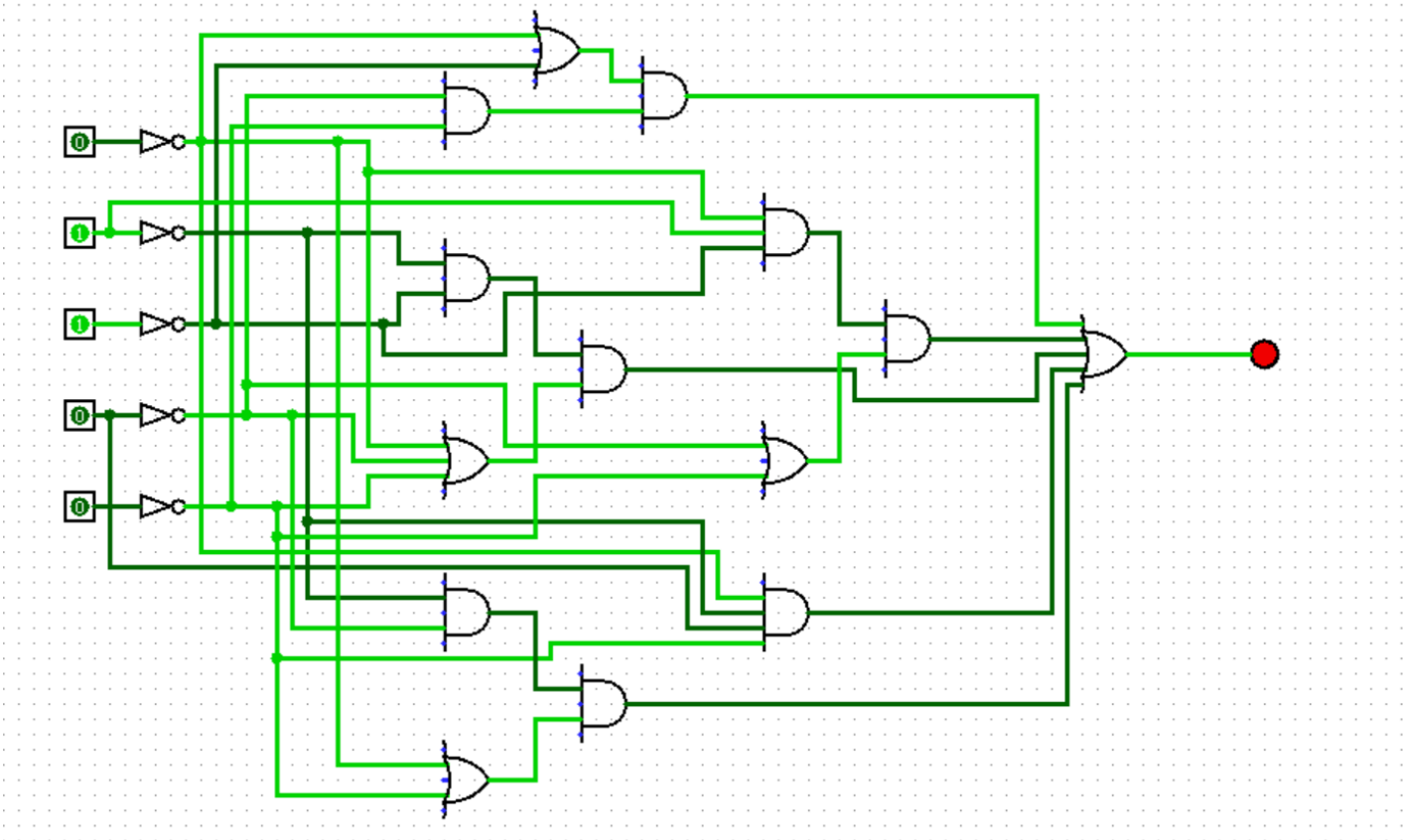
$$A + \bar{A}B = A + B$$

$$\because \bar{A} + A\bar{B} = \bar{A} + \bar{B}$$

By the above final expression, we construct the logic circuit of the project,

The circuit is shown below,

➢ **Logisim Circuit of Tank Refilling Alarm:**

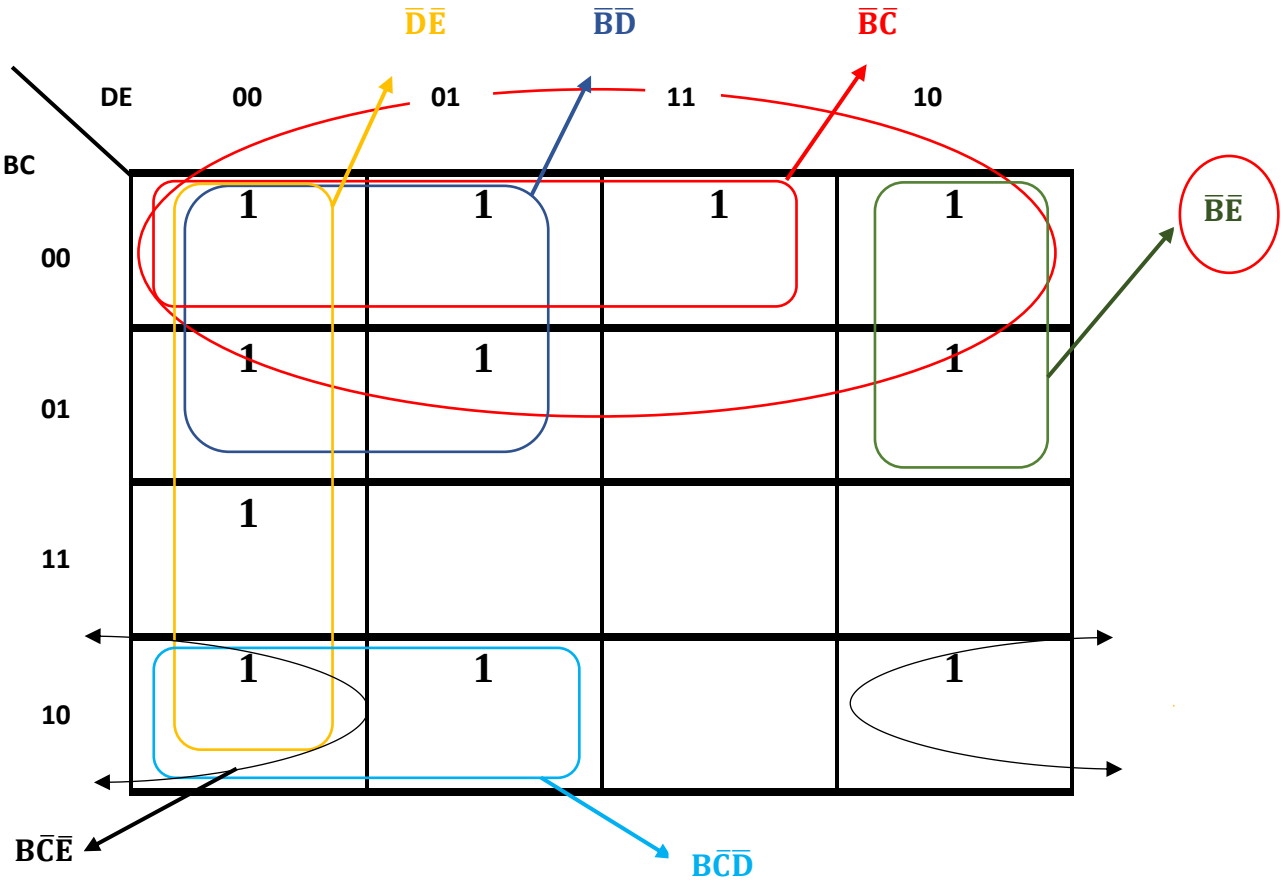


➢ Troubleshooting Description

Karnaugh map

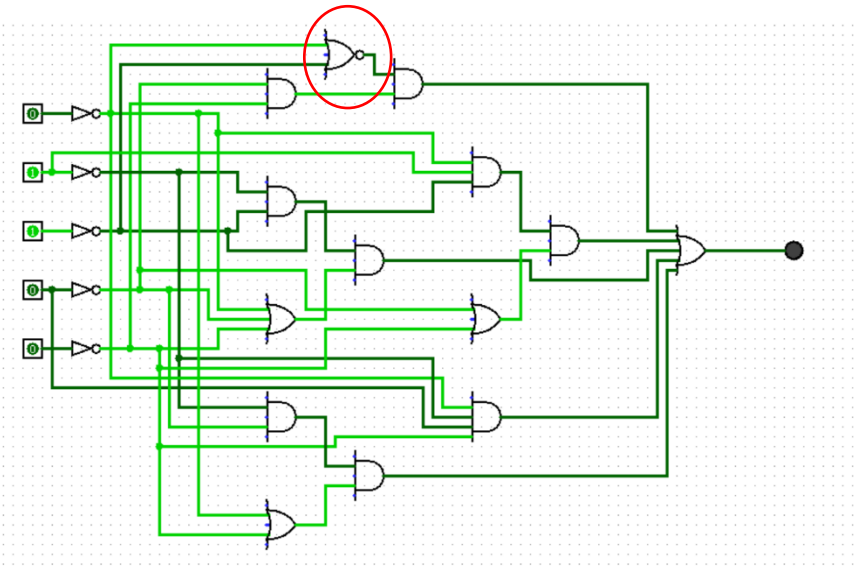
When we were making karnaug map we have to face some minor errors like we mistakenly make the group of 3 ones instead of 4 then we made wrong equation due to which circuit diagram doesn't give input according to our truth table. Then we have do the same work again which is very time consuming.

So we learn from this mistake that we should be very careful while making Karnaugh map.

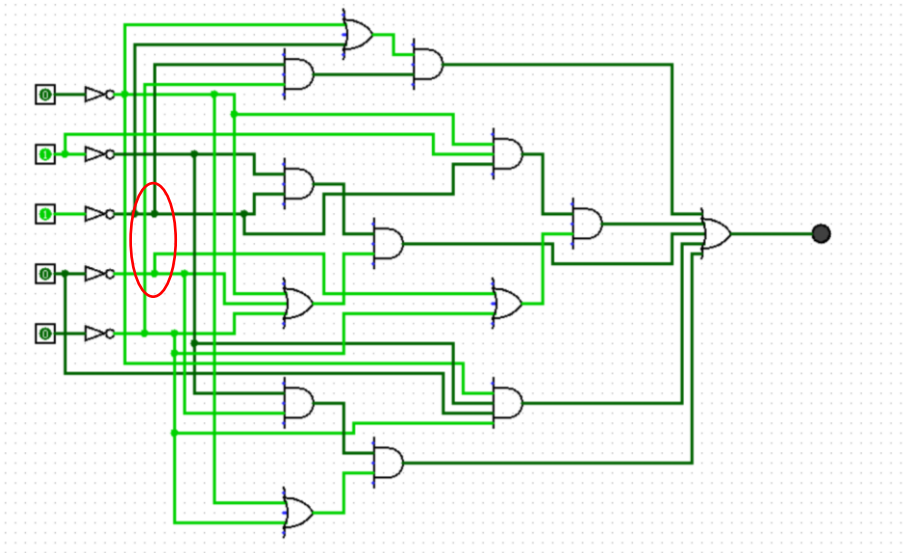


Logisim Circuit

- When we made the circuit in the Logisim, we were facing many errors like mistakenly we use nor gate instead of Or gate due to which circuit gives the wrong output.



- Also we didn't notice that, while doing $\bar{D}\bar{E}$ instead of connecting $\bar{D}$ pin with AND gate , we mistakenly connect $\bar{C}$ because of which the circuit didn't give output according to our truth table.



Simulations