CPSC 410 Midterm1

Name: _____

Please rate this exam 1 – 10, with 1 being the easiest.
Rating: _____

1. (15 pts) Match the following event with the type of interrupt it generates

Event	**Hardware**	**System Call**	**Exception**	**None of these**
User presses a key	x			
Divide by 0			x	
CPU executes a read() instruction		x		
MMU notifying CPU that data is ready	x			
Page table physical address lookup				x

2. (5 pts) For a multi-level feedback queue, choose the answer that best describes where a highly user interactive process runs.

a) In a queue with a long time slice and high priority
b) In a queue with a short time slice and high priority
c) In a queue with a short time slice and low priority
d) In a queue with a long time slice and low priority
e) In a queue with no restrictions on amount of time the process runs
f) In the readyQ
g) It's not g

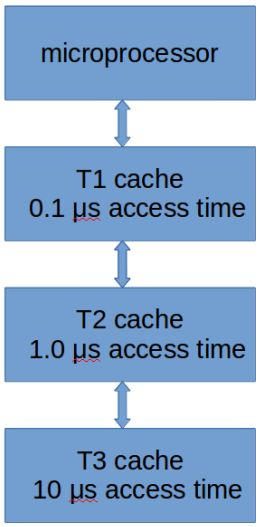
3. (10 pts) In a cooperative multitasking operating system; assume a process is running the following loop.

```
1. int i=0;
2. while (true){
3.     i++;
4.     if (i==32000)
5.         i=0;
6. }
```

Choose all answers that describe the conditions under which this process yields control to the OS and, if applicable, indicate the line(s) where this occurs.

a) when I equals 32000
b) when the memory holding i overflows
c) when it makes a system call for disk access
d) when the process time slice is up
e) it will never yield

4. (10 pts) The system illustrated below has 3 levels of cache with the given access times.
What is the average instruction access time if;
70% of data is in T1 and 20% is in T2 and 10% is in T3?
Please show all work



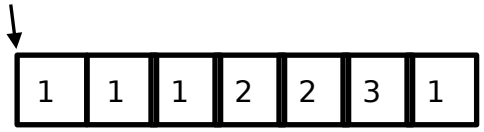
0.7 * 0.1µs + 0.2 * (0.1µs + 1µs) + 0.1 * (0.1µs + 1µs + 10µs) =1.4 µs

wrong
0.7 * 0.1µs + 0.2 * 1µs + 0.1 * 10µs =1.27 µs

5. (30 pts) A scheduler uses a preemptive Round Robin algorithm to run processes on a uniprocessor system. For the following processes, please indicate which process is running on the processor by placing its number in the blocks that follow. The time slice = 3 time units

Process	Arrival Time	Processor time
1	0	4
2	1	2
3	2	1

Time 0



(10 pts) Please fill each of the above boxes with the number of the currently running process.

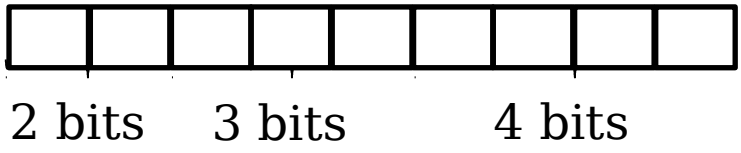
(5 pts) How many context switches are there? Show where they occur on the above diagram. Befor (0,3,5,6)
4

(5 pts) What is the average response time?
start_time – arrival_time
(0 +2+3)/4=1.25

(5 pts) What is the average turnaround time?
finish_time – arrival_time
7-0 + 5-1 + 6-2= 7+4+4=15/3=5

(5 pts) What is the average wait time?
finish_time – arrival_time-
required_CPU_time
7-0-4 + 5-1-2 + 6-2-1=(3+2+3)/3=8/3=2.6

6. (30 pts) For a 9 bit system using the following multilevel page table structure.



(3 pts) What is the size of the memory?

29 = 512 words**

(3 pts) What is the size of each frame (block) in memory?

24 = 16 words**

(3 pts) How many possible outer page tables are there and how many entries (rows) per outer page table?

1 and 22= 4 rows**

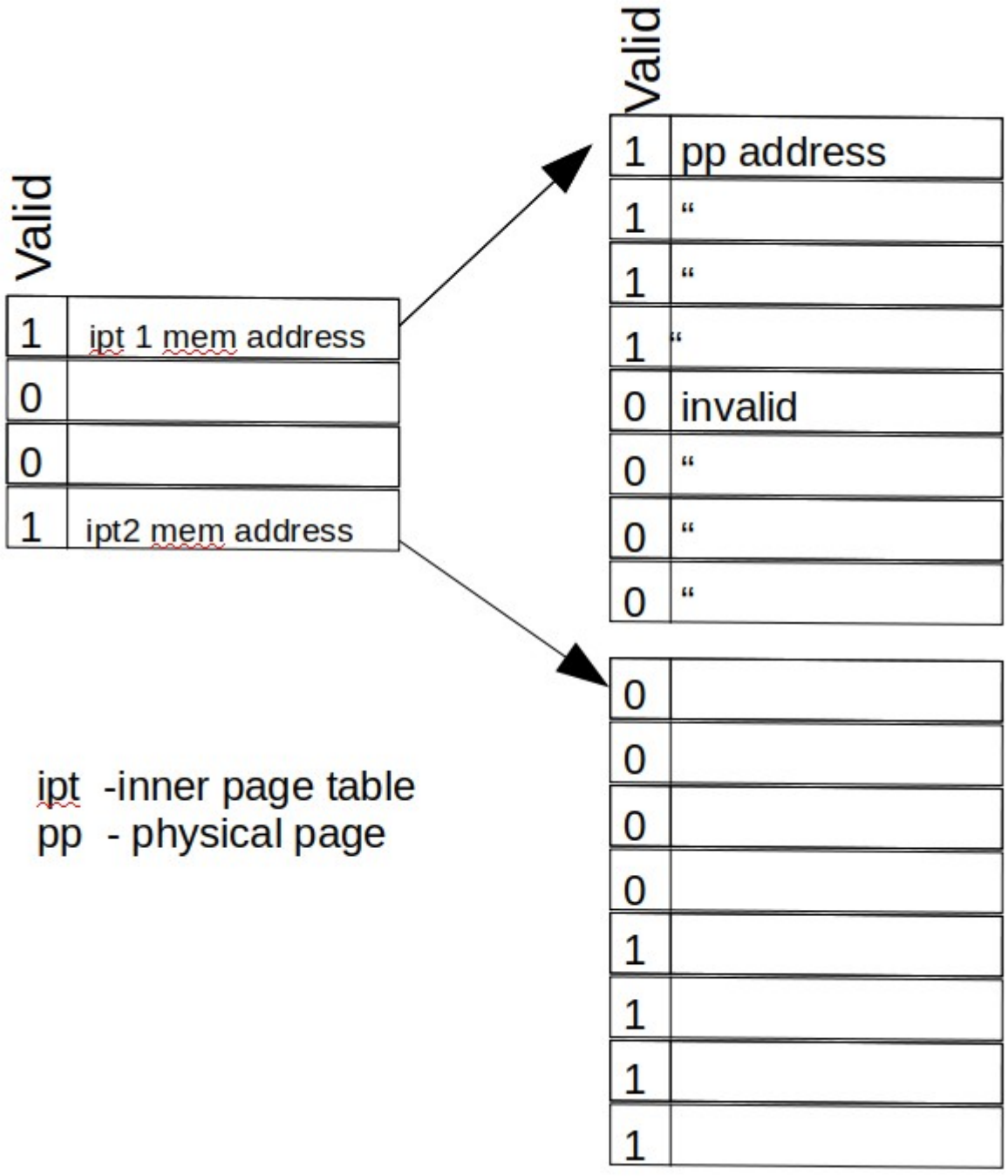
(3 pts) How many possible inner page tables are there and how many entries (rows) per inner page table?

4 and 23=8 rows**

(3 pts) What is a valid bit? What does it mean if it equals 1?

Means that the page table is needed

(15 pts) A process has exactly 128 instructions. 64 words at the beginning of its virtual address space and 64 words at the end. Please show all inner and outer page tables.


Valid
1 ipt 1 mem address
0
0
1 ipt2 mem address
Valid
1 pp address
1 “
1 “
1 “
0 invalid
0 “
0 “
0 “
0
0
0
0
1
1
1
1
ipt -inner page table
pp - physical page