Bansilal Ramnath Agarwal Charitable Trust's

Vishwakarma Institute of Information Technology

(Department of Electronics and Telecommunication)

Group No. - C18

Project Report

on

NOISE MODELING AND SIMULATION OF A SOURCE FOLLOWER CRYOGENIC AMPLIFIER

(IN COLLABORATION WITH - T. I. F. R.)

(DOMAIN - ANALOG CIRCUITS AND SYSTEMS)

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B. Tech E&TC

of

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Year 2020 - 2021

CERTIFICATE

This is to certify that final year project work entitled "Noise modeling and simulation of a source follower cryogenic amplifier" carried out in collaboration with T.I.F.R., Mumbai in the seventh semester by,

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Abstract

Objective

An analytical model has to be derived to understand how noise from different components and DC power supply in a source follower amplifier affects the overall noise performance of the amplifier.

Method/Chapters

1. Background and Literature Survey about different amplifier topologies and various types of noise in a junction field effect transistor (JFET).
2. Study of a source follower amplifier with passive and active load configuration. Advantages and disadvantages of both the configurations are also briefly discussed.
3. Developing an analytical model for noise in a source follower amplifier with passive load followed by its verification by simulating the small signal model in PSPICE.
4. Developing an analytical model for noise in a source follower amplifier with active load followed by its verification by simulating the small signal model in PSPICE.

Results

Based on the analytical model and PSPICE simulation, we tabulated and compared the output voltage noise density obtained from the analytical model and PSPICE simulation. Both the results are found to be in very good agreement with each other. The developed analytical model for noise will be extremely helpful to check and optimize the noise performance of a source follower amplifier.

Acknowledgements

Our mentors

1. Prof. (Dr) Chandrashekhar Garde[1]
2. Prof. (Dr) Vandana Nanal[2]
3. Prof. (Dr) Shrikant Joshi[3]
4. Dr Ashif Reza[4]

We would like to thank Prof. Chandrashekhar Garde from VIIT, Pune for giving us the opportunity to interact and connect us with great mentors from TIFR, Mumbai. Prof Garde's expertise in research, physics and cryogenics helped us understand our problem statement without any flaws and misconception. He mentored us for understanding the background of the project and motivated us to actively work on the project.

We thank Prof. Vandana Nanal from TIFR for giving us the great opportunity to work on the Neutrinoless double beta decay project.

We thank Prof. Shrikant Joshi (our final year project mentor) for interacting with us in every meeting and to solve all our queries related to the project. His expertise in core electronics helped us understand the fundamentals of analytical theorems and characteristics of microelectronics. He helped us analyse our models with utmost precision.

Lastly, we thank our mentor Dr Ashif Reza from TIFR. His experience at TIFR and his direct involvement in the Neutrinoless double beta decay project helped us understand the problem statement, develop and test the model and conclude with a positive and useful result. We thank him immensely to help us understand each and every aspect of designing and testing a mathematical model for noise characteristics in an amplifier.

Regards,
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Chapter 1: Introduction

1.1 Background

A prototype tin cryogenic bolometer detector operating at 10 mK is being developed to study a phenomenon known as neutrinoless double-beta decay (NDBD) at TIFR, Mumbai [1]. To detect a very tiny change in temperature (~ few tens to hundreds of microKelvin) due to an incident radiation, a neutron transmutation doped (NTD) Germanium temperature sensor is used due to its very high sensitivity (dR/dT) at such a low temperature.

In order to detect a weak electrical signal from an NTD Ge sensor (typical sensor resistance ~ 500 Mohm), a low noise amplifier with a very high input impedance is required. Currently, the sensor signal is amplified using a commercial differential amplifier [2] kept at room temperature. To reduce the EMI pickups and to minimize the signal integration due to long transmission line connecting NTD Ge sensor at 10 mK to differential amplifier outside the cryostat, it is planned to mount a preamplification stage inside the cryogen free dilution refrigerator (CFDR) [3]. For this purpose, a high input impedance front-end source follower preamplifier is already designed and tested at 120 K [4]. The Source follower preamplifier with active load configuration offers almost unity voltage gain and very stable performance as compared to a conventional source follower with passive load.

To achieve a high precision measurement, the design of the front-end source follower amplifier needs to be further optimized to accomplish very low noise, high gain stability and very low drift performance. In this project, we modeled the noise characteristics of this amplifier to attain optimised noise performance. The analytical model is derived to see how noise from the different components of the amplifier and DC power supply affects the overall noise performance of the amplifier. The analytical model is also independently verified using simulation tools.

1.2 Motivation

As mentioned in Chapter 1.1, an amplifier is to be designed to operate at 120K. At this temperature, an amplifier must have a very low noise characteristic to provide the desired signal to noise ratio (SNR). To understand the effect of various noise sources that affect the amplifier's performance, we were interested to mathematically derive the noise model of the amplifier circuit.

1.3 Task for team members

An analytical model has to be derived to see how noise from the different components of the amplifier and DC power supply affects the overall noise performance of the amplifier.

1.3.1 Sub-Tasks

1. Draw the small signal model of a source follower amplifier with various noise sources.
2. Select approach for noise modeling.
3. Reduce dependent sources to independent sources, if possible, to simplify modeling.
4. Derive effect of individual noise sources in the circuit using superposition theorem.
5. Add the effects of individual noise sources in the circuit to get total noise.
6. Simulate the complete small signal model and compare it with the analytical model.

Chapter 2: Literature Survey

2.1 Literature Survey on JFETs

2.1.1 Why to use JFET?

The front-end electronics to detect the bolometer signal requires an amplifier with a high input impedance. Therefore, Si JFETs have been chosen due to its high input impedance along with very low noise characteristics.

2.1.2 Source follower amplifier with passive load

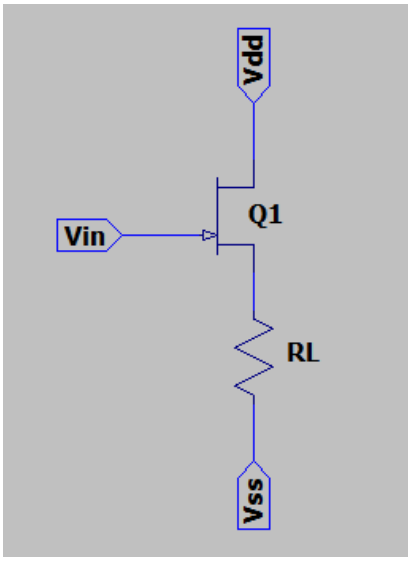

Fig. 2.1 Source follower amplifier with passive load

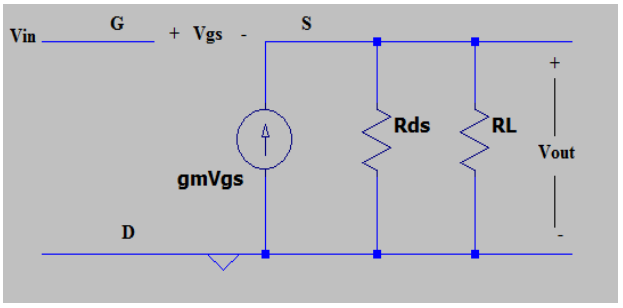

Fig. 2.2 Small signal model of source follower amplifier

A simple circuit schematic of a source follower (common drain) amplifier is shown in Fig. 2.1. In the above circuit, the circuit is configured in Common Drain mode. Load resistor is connected at the source terminal of JFET Q1.
The voltage gain and output impedance of an amplifier can be found by doing AC analysis of a circuit and using simple laws of network theory.

Voltage Gain

The output voltage of a source follower is,

$$V_{out} = g_m V_{gs} \times (R_{ds} || R_L) \qquad \dots (I)$$

Applying KVL in outer loop:

$$V_{in} - V_{gs} - V_{out} = 0$$

$$\therefore \quad Vgs = Vin - Vout \qquad \dots (II)$$

From (I) and (I I)

$$Av = \frac{Vout}{Vin} = \frac{gm\,(RL||rds)}{1+gm(RL||rds)}$$

Output Impedance

Output impedance of a circuit is found by making signal source equal to zero.

$$V_{in} = V_{gs} + V_{out}$$

$$0 = V_{gs} + V_{out}$$

$$V_{out} = I \times R_o \; (Here,\ I\ is\ current\ flowing\ through\ load)$$

$$V_{out} = (I_o - g_m V_{out}) \times r_{ds}||R_L \qquad \ldots (\text{I I I})$$

$Here\ I_o\ and\ R_o\ are\ output\ current\ and\ output\ impedance\ respectively.$

On solving equation (I I I), output impedance can be obtained as,

$$R_o = \frac{V_{out}}{I_o} = \frac{r_{ds} \times R_L}{r_{ds} + R_L + g_m \times r_{ds} \times R_L}$$

For $r_{ds} > R_L\ and\ g_m \times R_L >> 1$

$$R_o = 1/g_m$$

Thus, the output impedance of a source follower amplifier is $\frac{1}{g_m}$ (connected between source and ground, assuming input is shorted to ground). So, the dependent source $g_m V_{gs}$ can be modeled with $\frac{1}{g_m}$resistor connected between source and ground.

2.1.3 Source follower amplifier with active load

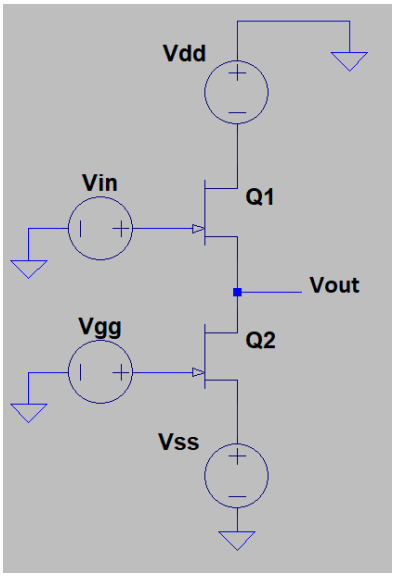

Fig. 2.3 Source follower amplifier

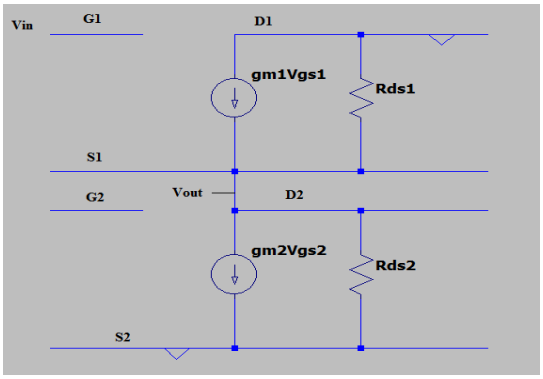

Fig. 2.4 Small signal model of source follower amplifier

In the above circuit, the circuit is configured in Common Drain topology with active load. JFET Q2 acts as an active load. The load Q2 is biased using V_{gg} power supply to provide high load resistance.
The voltage gain and output impedance of an amplifier can be found by doing AC analysis of the circuit and using simple laws of network theory.

Voltage Gain

The output voltage of a source follower with an active load can be found similar to an amplifier with passive load. Here, R_{ds_2} acts as a load resistor.

$$V_{out} = g_{m_1} V_{gs_1} \times (R_{ds_1} || R_{ds_2}) \qquad \dots (\mathrm{I})$$

Applying KVL in outer loop we get,

$$A_v = \frac{V_{out}}{V_{in}} = \frac{g_{m_1} \times R_{ds_2}}{1+(R_{ds_2}/R_{ds_1})+ g_{m_1} R_{ds_2}}$$

For $R_{ds_1} > R_{ds_2}$,

$$A_v = \frac{g_{m_1} R_{ds_2}}{1+g_{m_1} \times R_{ds_2}}$$

For larger values of $g_{m_1} \times R_{ds_2}$, gain A_v tends to unity.

Output Impedance

Output impedance of a circuit is found by making the signal source equal to zero, similar to an amplifier with passive load.

The output impedance of an amplifier with active load is given by,

$$R_o = \frac{1}{g_{m_1}} || R_{ds_1} || R_{ds_2}$$

2.1.4 Different configurations of JFET biasing

There are three basic configurations of a single-stage JFET amplifiers:

1. Common Source
2. Common Drain (Source Follower)
3. Common Gate

The different characteristics of these amplifiers are shown in the table below:

Characteristic	Common Source	C Source with R_S	Common Drain [Source Follower]	Common Gate
Voltage Gain [if $r_{ds} >> R_L$]	$A_v = -g_m R_L$	$A_v = \frac{-g_m R_L}{1 + g_m R_S}$	$A_v = \frac{g_m R_S}{1 + g_m R_S}$	$A_v = \frac{g_m R_L}{1 + g_m R_i + \frac{R_i}{R_S}}$ R_i = generator resistance
Current Gain	$\frac{I_D}{I_S}$ Very large!	$\frac{I_D}{I_S}$ Very large!	$\frac{I_D}{I_S}$ Very large!	$A_i = \frac{g_m R_S}{g_m R_S + 1}$
Input Impedance	R_G	R_G	R_G	$\frac{R_S}{g_m R_S + 1} = \frac{1}{g_m} // R_S$
Output Impedance	R_L [if $r_{ds} >> R_L$]	R_L [if $r_{ds} >> R_L$]	$\frac{R_S}{g_m R_S + 1} = \frac{1}{g_m} // R_S$	R_L [if $r_{ds} >> R_L$]
Phase Reversal	Yes	Yes	No	No

Table 2.1 Comparison of different configurations of JFET biasing

2.1.5 Advantages of active load over passive load in a source follower amplifier

- Active load provides a very high dynamic resistance by operating the Jfet in saturation region.
- The active load configuration provides a very stable voltage gain close to unity.
- In passive load configuration, using a large value of resistor would dissipate a larger amount of heat. Whereas JFET, as an active load, provides high dynamic resistance with less power dissipation.
- If we would implement this high resistance using physical resistance, it would take a very large area to implement integrated circuits. Implementing it as a simple JFET transistor as an active load will provide the required high resistance without the cost for such larger areas.

2.2 Types of noises

Following are the most relevant noise sources for this project:

1. Thermal Noise

The random motion of electrons in a conductor introduces fluctuations in the voltage measured across the conductor, even if the average current is zero. Thus, the spectrum of thermal noise is proportional to the absolute temperature. Refer Fig. 2.5.

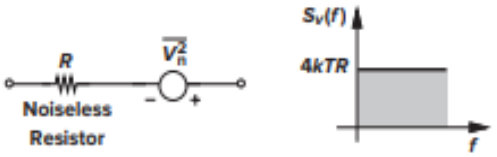

Fig. 2.5 Thermal noise

$$S_v(f) = 4kTR,\ f \geq 0$$

Every resistor generates a noise voltage across its terminals due to thermal fluctuations in the electron density within the resistor itself. These fluctuations give rise to an open-circuit noise voltage.

$$V_{noise}(rms) = (4kTR\Delta f)^{\frac{1}{2}}$$

where k=Boltzmann's constant (1.38 × 10−23 J/°K), T is the temperature in Kelvin, R is the resistance in ohms, and Δf is the bandwidth of the measurement in Hz.

2. Shot Noise

Electric current has noise due to the finite nature of the charge carriers. There is always some non-uniformity in the electron flow which generates noise in the current. This noise is called "shot noise". This can appear as voltage noise when current is passed through a resistor, or as noise in a current measurement. The shot noise, or current noise, is given by:

$$I_{noise}(rms) = (2qI\Delta f)^{\frac{1}{2}}$$

where q is the electron charge (1.6 × 10−19 Coulomb), I is the rms AC current or DC current depending upon the circuit, and Δf is the bandwidth.

3. 1/f (Flicker) Noise

Fluctuations in resistance due to the current flowing through a resistor is called 1/f noise. This noise has a 1/f spectrum and makes measurements at low frequencies more difficult. Other sources of 1/f noise include noise found in vacuum tubes and semiconductors. For carbon composition resistors, this is typically 0.1 µV to 3 µV of rms noise per volt applied across the resistor. Metal film and wirewound resistors have about 10 times less noise.

$$\overline{Id}^2 = \frac{KF \cdot I_d{}^{AF}}{f}\Delta f$$

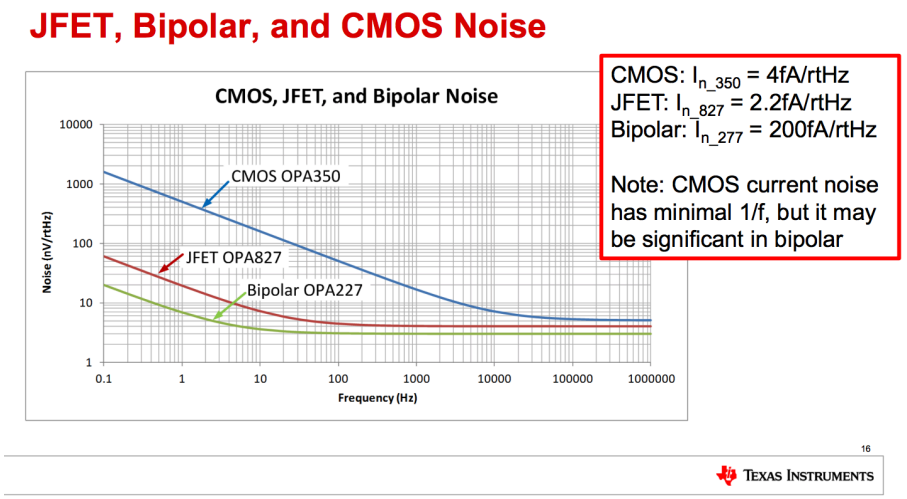

Fig. 2.6 Comparison of Integrated Noise Spectrum of JFET and BJT input Operational Amplifiers

2.3 Input referred and output referred noise

The equivalent input referred noise is the noise voltage or current, that when applied to the input of the noiseless circuit, generates the same output noise as the actual circuit does. The input referred noise indicates how much noise signal is corrupted by circuit's noise.

The output referred noise is the noise voltage or current spectral density which is a measurement of RMS noise voltage per square root hertz (or commonly nV/Hz½) at the output terminal. The output referred noise represents the RMS addition of individual response of all the noise sources taken each at a time.

2.4 Studying the Circuit Diagram

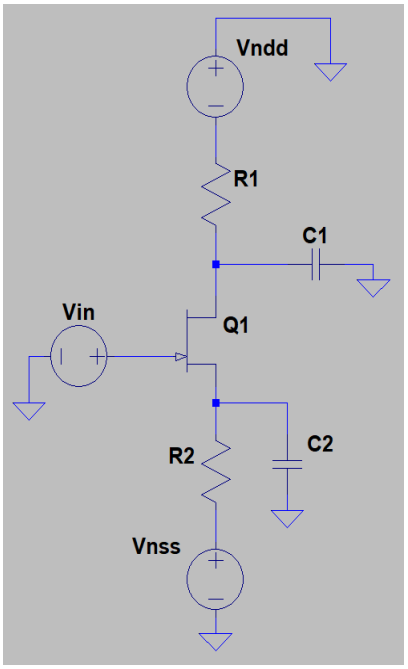

Fig. 2.7 Source follower with passive load with RC filter

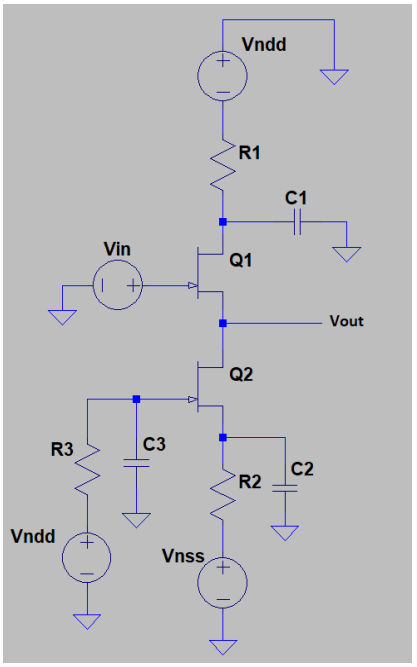

Fig. 2.8 Source follower with active load with RC filter

A source follower amplifier for a bolometer detector has already been designed and tested [4]. The circuit schematic of the source follower with passive and active load is shown in Fig.2.4. A single order low pass RC filter (R = 50 ohm, C = 100 nF, cut-off frequency ~ 30 kHz) is used to filter out high frequency noise, if any, from the power supply line. For noise modeling and analysis, we have not considered the effect of RC filter, as the thermal voltage noise density due to the 50 ohm resistor is ~ 1 nV/Hz½, which is very less compared to the power supply noise (usually greater than 10 nV/Hz½ for our case). So, the noise contributions from RC filter components are neglected in noise modeling of an active and passive load source follower amplifier.

Chapter 3: Noise Modeling of amplifier with passive load

3.1 Analytical modeling of noise for amplifier with passive load

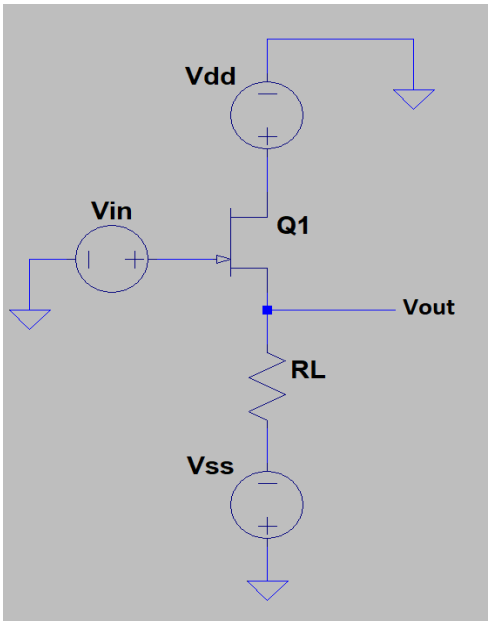

Fig.3.1 Source follower with passive load

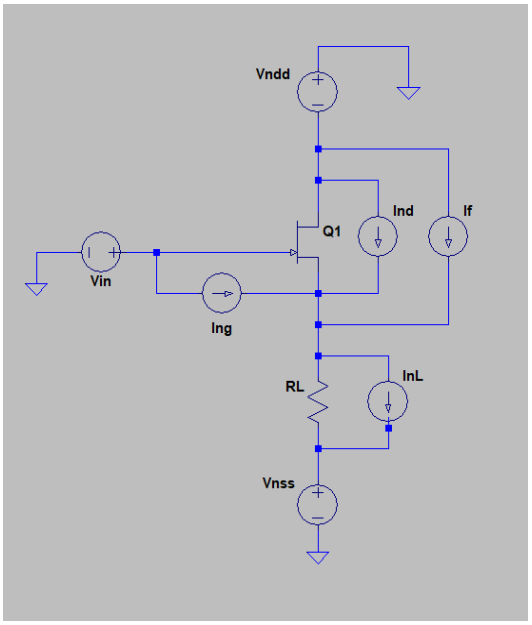

Fig. 3.2 Source follower with all noises

Fig. 3.1 shows a source follower amplifier with passive load configuration. In Fig. 3.2, we can see all the noise sources which are present in a typical circuit. Here, V_{ndd} and V_{nss} are power supply noises and I_{nL} is thermal noise of the load resistor. I_{nd} (thermal noise in drain-source channel), I_{ng} (shot noise) and I_f (flicker noise) are the internal noises of JFET. I_{ng} can be neglected as it is very insignificant at very low frequency. I_f can be neglected to reduce complexity; which can be later introduced as a future scope.

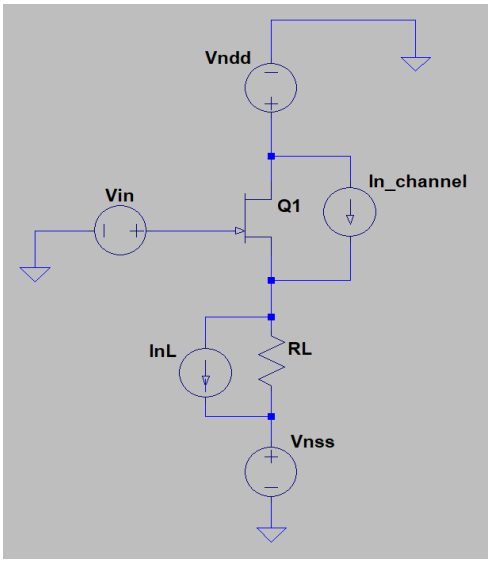

Fig. 3.3 Source follower amplifier with passive load with simplified noise source

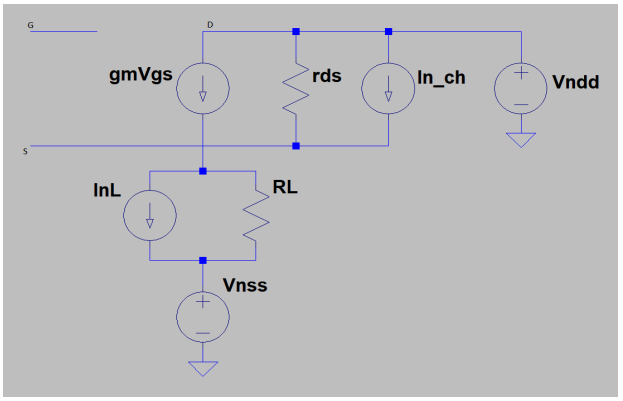

Fig. 3.4 Small signal model of Source follower amplifier with passive noise

According to the above mentioned assumptions and considerations, Fig. 3.3 represents the simplified circuit diagram. Fig. 3.4 represents the small signal model of the simplified circuit. We shall use this model to derive our analytical noise model.

3.1.1 Response of drain-source channel noise

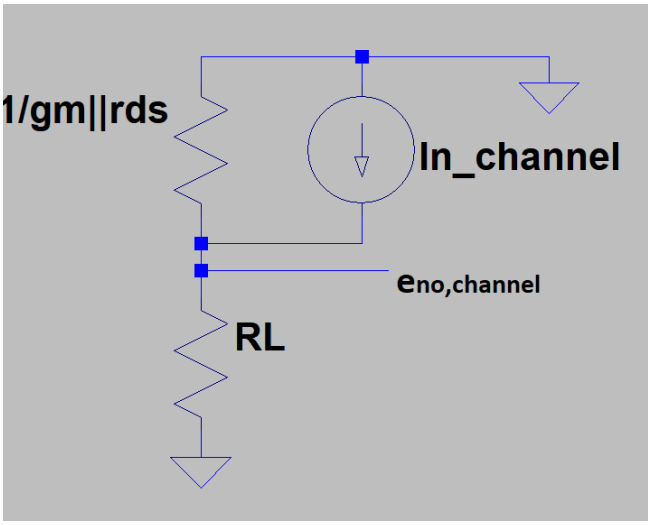

Fig. 3.5 Single JFET - Output referred noise due to drain-source channel noise

$$\vec{e^2_{no,channel}} = \vec{I^2_{n,channel}}(R_{op})^2$$

$$\therefore \quad \vec{e^2_{no,channel}} = \vec{I^2_{n,channel}}\left(\frac{R_{eq}}{1+g_m R_{eq}}\right)^2$$

$$where\ R_{eq} = r_{ds} \| R_L$$

$$Dividing\ by\ square\ of\ gain,$$

$$\vec{e^2_{ni,channel}} = \frac{\vec{e^2_{no,channel}}}{A_v^2}$$

$$= \frac{\vec{I^2_{n,channel}}\left(\frac{R_{eq}}{1+g_m R_{eq}}\right)^2}{\left(\frac{g_m R_{eq}}{1+g_m R_{eq}}\right)^2}$$

$$\therefore \quad \vec{e^2_{ni,channel}} = \frac{\vec{I^2_{n,channel}}}{(g_m)^2}$$

3.1.2 Response of load resistor noise

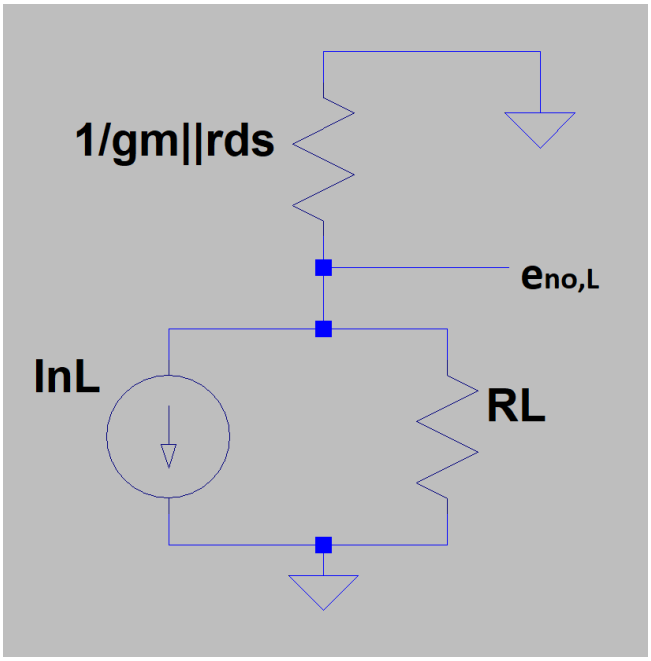

Fig. 3.6 Single JFET - Output referred noise due to load resistor noise

$$e_{no,L}^{2\,\rightarrow} = I_{nL}^{2\,\rightarrow}(R_{op})^2$$

$$R_{op}(output\ impedance) = \frac{1}{g_m} \parallel r_{ds} \parallel R_L = \frac{1}{g_m} \parallel R_{eq}$$

$$\ldots where\ R_{eq} = r_{ds} \parallel R_L \qquad I_{nL}^{2\,\rightarrow} = \frac{4k_B T}{R_L}$$

$$(Thermal\ noise\ from\ load\ resistor)$$

$$\therefore \quad e_{no,L}^{2\,\rightarrow} = \frac{4k_B T}{R_L}\left(\frac{1}{g_m} \parallel R_{eq}\right)^2$$

$$\therefore \quad e_{no,L}^{2\,\rightarrow} = \frac{4k_B T}{R_L}\left(\frac{R_{eq}}{1+g_m R_{eq}}\right)^2$$

$$Dividing\ by\ square\ of\ gain,$$

$$e_{ni,L}^{2\,\rightarrow} = \frac{e_{no,L}^{2\,\rightarrow}}{A_v^2}$$

$$= \frac{\frac{4k_B T}{R_L}\left(\frac{R_{eq}}{1+g_m R_{eq}}\right)^2}{\left(\frac{g_m R_{eq}}{1+g_m R_{eq}}\right)^2}$$

$$= \frac{4k_B T}{g_m{}^2 R_L}$$

$$\therefore \quad e^2_{ni,L}{}^{\rightarrow} = \frac{4k_B T}{g_m{}^2 R_L}$$

3.1.3 Response of supply noise V_{nss}

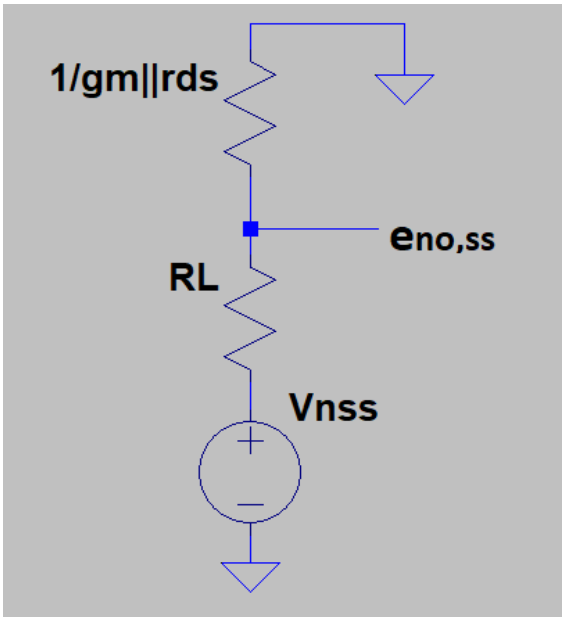

Fig. 3.7 Single JFET - Output referred noise from V_{nss} noise input

$$e^2_{no,ss}{}^{\rightarrow} = \left(\frac{(\frac{1}{g_m}\|r_{ds})}{R_L+(\frac{1}{g_m}\|r_{ds})}\right)^2 V^2_{nss}{}^{\rightarrow}$$

$$e^2_{ni,ss}{}^{\rightarrow} = \frac{e^2_{no,ss}{}^{\rightarrow}}{A^2_v} \ldots where, A^2_v = \left(\frac{g_m R_{eq}}{1+g_m R_{eq}}\right)^2 \left(Note:\ R_{eq} = R_L \parallel rds\right)$$

$$e^2_{ni,ss}{}^{\rightarrow} = \frac{\left(\frac{(\frac{1}{g_m}\|r_{ds})}{R_L+(\frac{1}{g_m}\|r_{ds})}\right)^2 V^2_{nss}{}^{\rightarrow}}{A^2_v}$$

3.1.4 Response of supply noise V_{ndd}

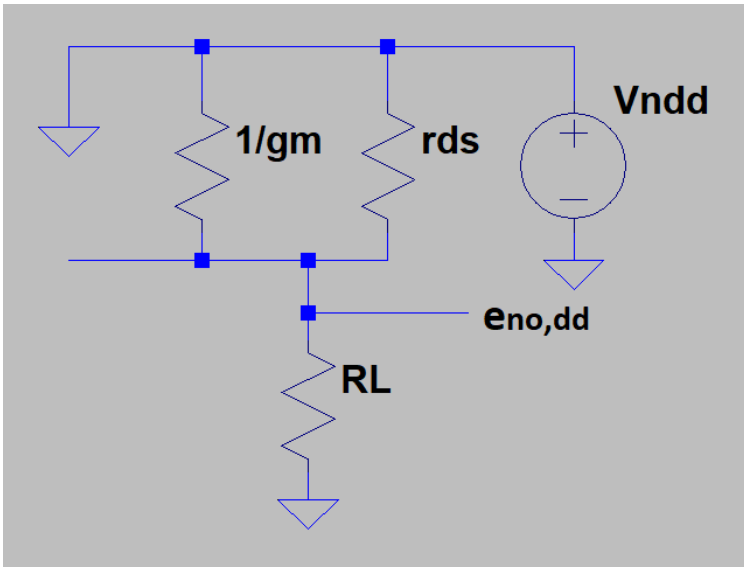

Fig. 3.8 Single JFET - Output referred noise due to V_{ndd} noise

$$e^2_{no,dd} \text{ can be found by a voltage divider network}$$

$$\vec{e^2_{no,dd}} = \left[\frac{R_L \| \frac{1}{g_m}}{(R_L \| \frac{1}{g_m}) + r_{ds}}\right]^2 \vec{V^2_{ndd}}$$

$$\vec{e^2_{ni,dd}} = \frac{\vec{e^2_{no,dd}}}{A_v^2} \text{where, } A_v^2 = \left(\frac{g_m R_{eq}}{1 + g_m R_{eq}}\right)^2 \left(Note:\ R_{eq} = R_L \parallel rds\right)$$

$$\therefore \quad \vec{e^2_{ni,dd}} = \frac{\left[\frac{R_L \| 1/gm}{(R_L \| 1/gm) + rds}\right]^2 \vec{V^2_{ndd}}}{A_v^2}$$

3.2 Output and Input Referred Voltage Noise Density

According to the Superposition theorem, equations of the response of individual noise sources can be summed up to find total noise densities. These densities can be later verified using simulation techniques.
Thus, the output voltage noise density is given by

$$\vec{e_{N,OUT}} = \sqrt{\vec{e^2_{no,L}} + \vec{e^2_{no,ch}} + \vec{e^2_{no,dd}} + \vec{e^2_{no,ss}}}$$

The input referred noise

$$\vec{e_{N,IN}} = \sqrt{\vec{e_{ni,L}^2} + \vec{e_{ni,ch}^2} + \vec{e_{ni,dd}^2} + \vec{e_{ni,ss}^2}}$$

3.3 Simulation and verification of model with passive load

For simulation, we generated the schematic of the small signal AC models as shown in Fig. 3.4. LTspice® is a high performance SPICE simulation software, schematic capture and waveform viewer with enhancements and models for easing the simulation of analog circuits[5]. Fig. 3.9 is a screenshot of the schematic drawn on LTSpice with some arbitrary values given to variables.

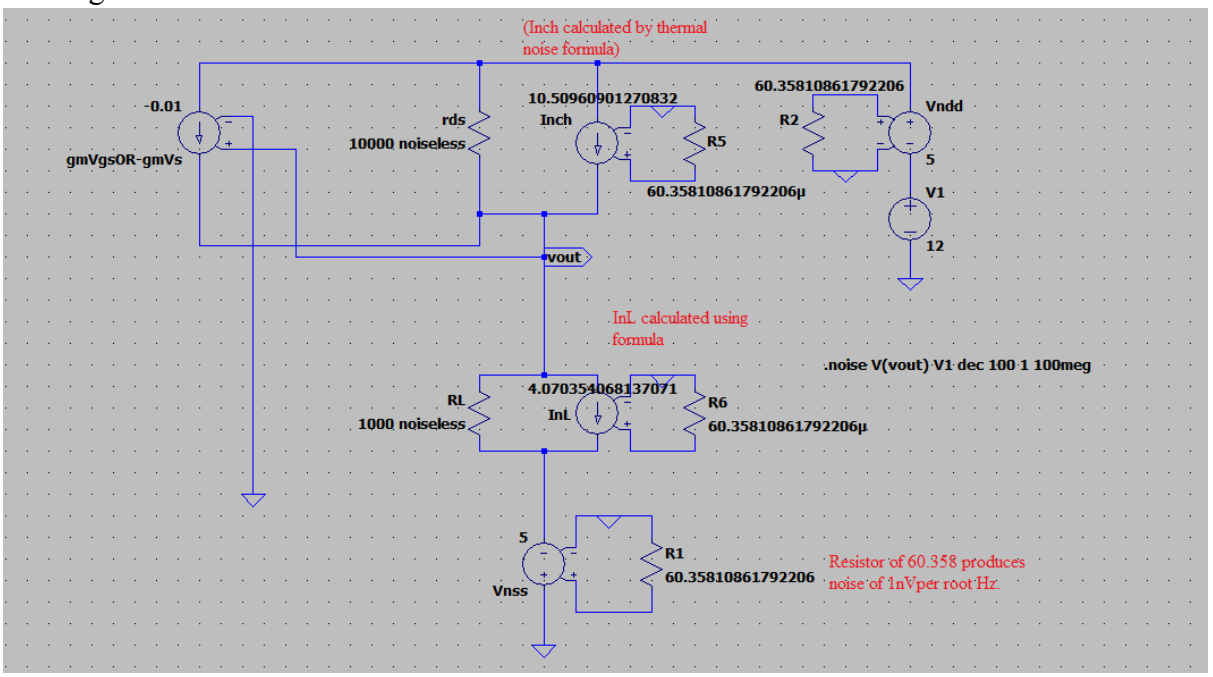

Fig. 3.9 LTSpice Schematic for Simulation of amplifier with passive load

LTSpice offers a way to add dependent current and voltage sources. This came handy to us when we wanted to recreate the noise sources shown in Fig 3.4. As seen in Fig. 3.9, V_{nss}, I_{nL}, I_{nch} and V_{ndd} are the noise sources.

To simulate output and input referred noise in LTSpice, a SPICE Directive (command) called *'.noise'* needs to be used. There does not seem to be a direct way of adding a voltage noise or current noise source to an LTSpice (or other kinds of Spice for that matter) circuit to be used in a *'.noise'* simulation. The only simple noise source (that affects .noise simulations) in LTspice is a simple resistor. An ideal resistor has a voltage noise described by:

$$v_n = \sqrt{4kTBR}$$

They were added as dependent sources in the LTSpice schematic. A very helpful blog helped us learn how to map the noise to be generated by adding resistors as dependencies to these LTSpice sources [6].

3.4 Simulation observations for amplifier with passive load

We simulated the model and verified our model derived based on Fig. 3.5 to Fig. 3.8 without considering gate noise (essentially grounding it). The rounded off results were as follows:

Table 3.1 Simulation of single JFET (Test case 1)

Case 1: g_m = 10mS, r_{ds} = 100kΩ, R_L = 1kΩ, I_{n_ch} = 10.509pA/Hz½			
V_{ndd} (nV/Hz½)	V_{nss} (nV/Hz½)	**Output Voltage Noise Density (nV/Hz½)**	
		Analytical Model	Simulation
0	0	1.023	1.023
5	0	1.023	1.023
10	0	1.023	1.023
25	0	1.024	1.024
50	0	1.024	1.024
100	0	1.027	1.027
0	5	1.120	1.120
0	10	1.368	1.368
0	25	2.490	2.490
0	50	4.655	4.655
0	100	9.140	9.140

As seen from above table, for $r_{ds} >> R_L$ the effect of V_{ndd}noise is negligible on the output voltage noise density. While the response of V_{nss}noise has considerable impact on output voltage noise density.

Table 3.2 Simulation of single JFET (Test case 2)

Case 2: g_m = 1mS, r_{ds} = 1kΩ, R_L = 1kΩ, I_{n_ch} = 3.324pA/Hz½			
V_{ndd} (nV/Hz½)	V_{nss} (nV/Hz½)	**Output Voltage Noise Density (nV/Hz½)**	
		Analytical Model	Simulation
0	0	1.751	1.751
5	0	2.417	2.417
10	0	3.765	3.765
25	0	8.515	8.515
50	0	16.758	16.758
100	0	33.379	33.379
0	5	2.417	2.417
0	10	3.765	3.765
0	25	8.515	8.515
0	50	16.758	16.758
0	100	33.379	33.379

It is observed from above table that, both V_{ndd} and V_{nss} affects in a similar way on output voltage noise density, when r_{ds} and R_L are comparable.

Chapter 4: Modeling of amplifier with active load

4.1 Analytical modeling of noise for an amplifier with active load

Similar to the modeling of a single JFET, for the analytical modeling of dual JFET, we used the Superposition theorem to calculate output referred noise for individual noise sources and then added them together, to find the total output referred noise. Fig. 4.4 represents the complete small signal model of the dual JFET amplifier. Here, Q1 acts as a source-follower amplifier and Q2 acts as an active load.

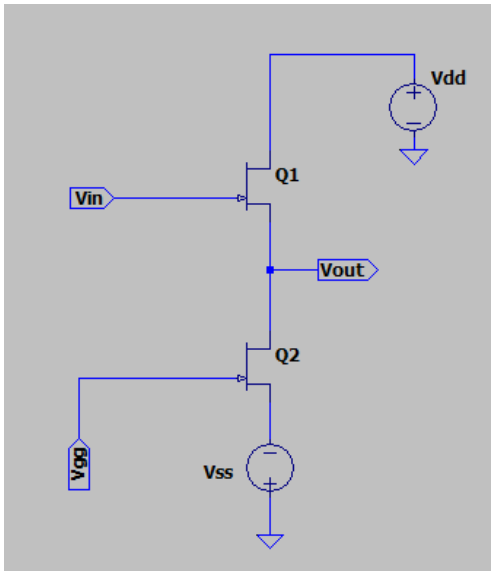

Fig. 4.1 Source follower amplifier with active load

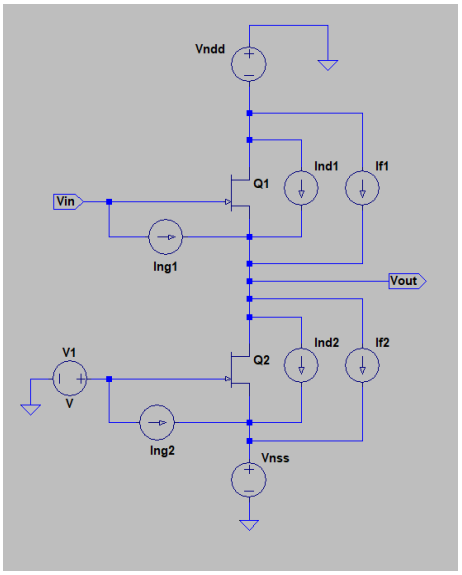

Fig. 4.2 Source follower amplifier with active load with all noise sources

As discussed in Chapter 3.1, we similarly simplify the circuit shown in Fig. 4.1 and design the small signal model. The small signal model shown in Fig. 4.4 shows the replacement of dependent sources as well. Refer Chapter 2.4.

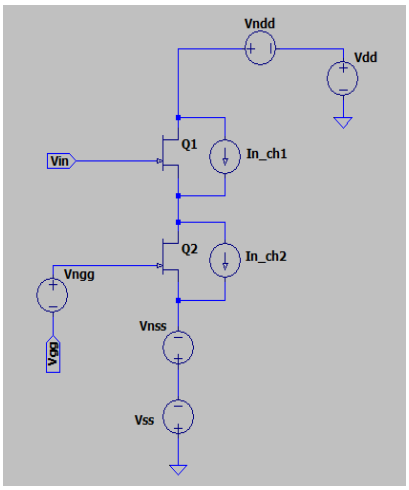

Fig. 4.3 Source follower amplifier with active load with simplified noise sources

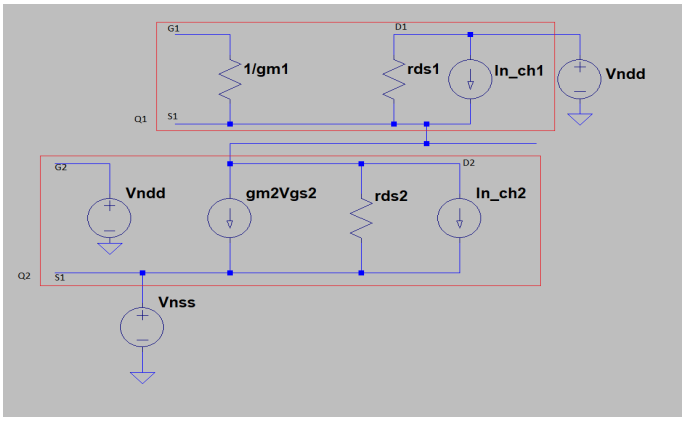

Fig. 4.4 Small signal model of amplifier with active load

4.1.1 Response of noise from V_{ndd}

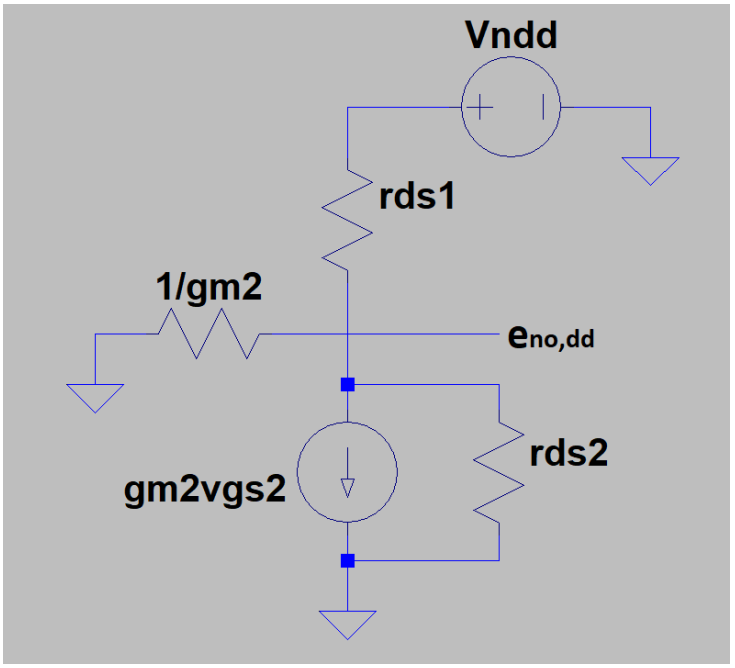

Fig. 4.5 Dual JFET - Output referred noise due to V_{ndd} noise

$e_{no,dd}$ *can be found by voltage divider network*

$$\vec{e^2_{no,dd}} = \left[\frac{\frac{1}{g_{m_1}} \| r_{ds_2}}{r_{ds_1} + (\frac{1}{g_{m_1}} \| r_{ds_2})}\right]^2 \vec{V^2_{ndd}}$$

$$\vec{e^2_{no,dd}} = \left[\frac{(r_{ds_2})}{(g_{m_1})(r_{ds_1})(r_{ds_2}) + r_{ds_1} + r_{ds_2}}\right]^2 \vec{V^2_{ndd}}$$

4.1.2 Response of noise from V_{ngg}

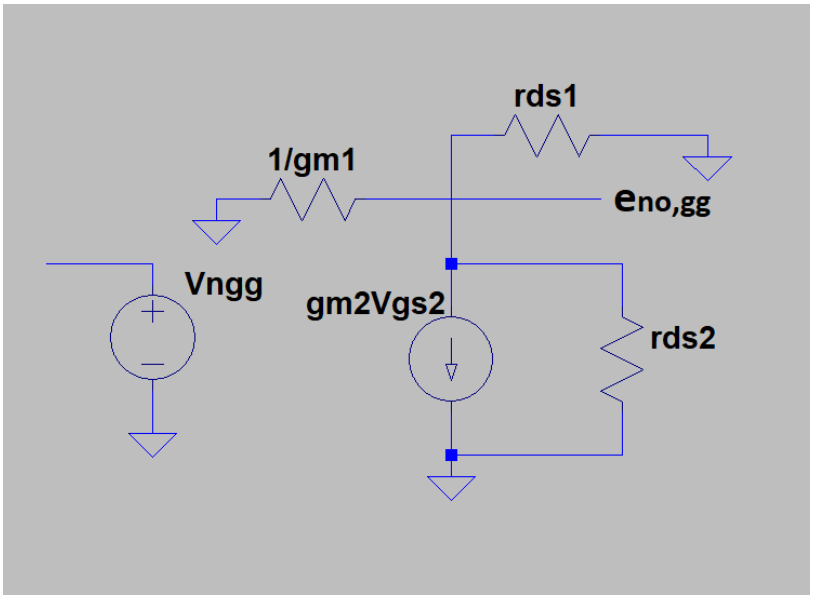

Fig. 4.6 Dual JFET - Output referred noise due to V_{ngg} noise

By Ohm's Law:

$$\vec{e^2_{no,gg}} = I^2_{n,g_{m_2}V_{gs_2}} (R_{op})^2$$

$$R_{op\ (output\ impedance)} = (\frac{1}{g_{m_1}} \| r_{ds_1} \| r_{ds_2})$$

$$\therefore \quad \vec{e^2_{no,gg}} = (g_{m_2} V_{gs_2})^2 \ (\frac{1}{g_{m_1}} \| r_{ds_1} \| r_{ds_2})^2$$

$$= (g_{m_2} V_{ngg})^2 \ (\frac{1}{g_{m_1}} \| r_{ds_1} \| r_{ds_2})^2$$

$$\therefore \quad \vec{e^2_{no,gg}} = [\frac{g_{m_2} r_{ds_1} r_{ds_2}}{(g_{m_1})(r_{ds_1})(r_{ds_2}) + r_{ds_1} + r_{ds_2}}]^2 \vec{V^2_{ngg}}$$

4.1.3 Response of noise from V_{nss}

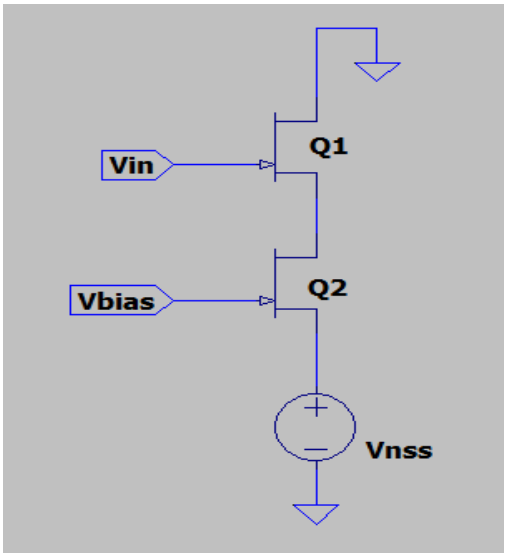

Fig. 4.7 Output referred noise due to V_{nss} noise with Q2 in common gate configuration

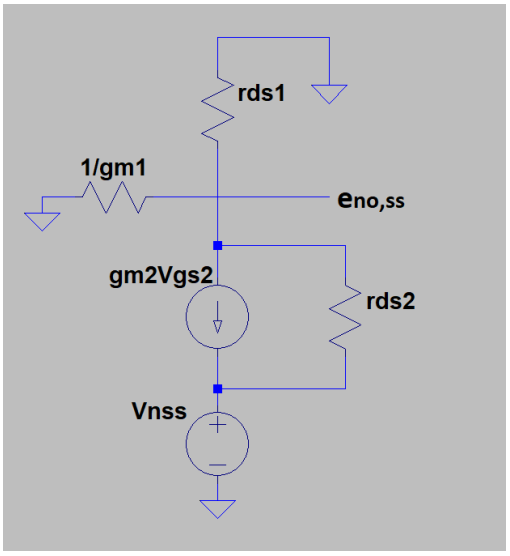

Fig. 4.8 Dual JFET - Output referred noise due to V_{nss} noise

By considering Q1 as active load and Q2 in common gate configuration,

$$Input\ impedance\ = \frac{1}{g_{m_2}}$$

$$Output\ impedance\ = r_{ds_2} || R_{load}$$

$$where\ R_{load} = r_{ds_1} || \frac{1}{g_{m_1}}$$

$$Gain\ = \left[\frac{g_m \times R_{load} + \frac{R_{load}}{r_{ds}}}{1+\frac{R_{load}}{r_{ds}}}\right]$$

$$Gain\ = \frac{g_{m_2} \times [\frac{1}{g_{m_1}} || r_{ds_1}] + \frac{[\frac{1}{g_{m_1}} || r_{ds_1}]}{r_{ds_2}}}{1+\frac{[\frac{1}{g_{m_1}} || r_{ds_1}]}{r_{ds_2}}}$$

$$= \frac{g_{m_2} \times [\frac{r_{ds_1}}{1+g_{m_1} \times r_{ds_1}}] + \frac{r_{ds_1}}{r_{ds_2}(1+g_{m_1} \times r_{ds_1})}}{1+\frac{r_{ds_1}}{r_{ds_2} \times (1+g_{m_1} \times r_{ds_1})}}$$

$$\therefore \quad e_{no,ss} = \frac{(1+g_{m_2} \times r_{ds_2}) \times r_{ds_1} \times V_{nss}}{r_{ds_1} + r_{ds_2} + g_{m_1} \times r_{ds_1} \times r_{ds_2}}$$

$$\therefore \quad \vec{e^2_{no,ss}} = \left[\frac{(1+g_{m_2} r_{rd_2}) r_{ds_1}}{(g_{m_1})(r_{ds_1})(r_{ds_2}) + r_{ds_1} + r_{ds_2}}\right]^2 \vec{V^2_{nss}}$$

4.1.4 Response of noise from channel noise of Q1 ($I_{n\_ch_1}$)

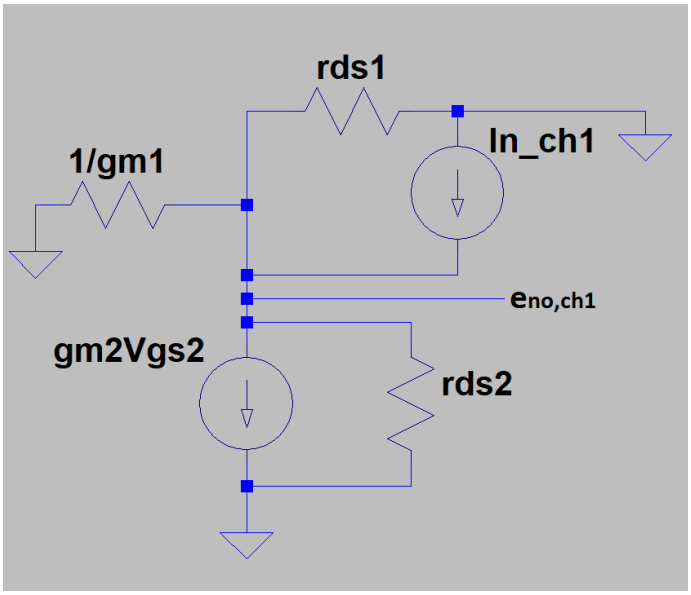

Fig. 4.9 Dual JFET - Output referred noise due to $I_{n\_ch_1}$ noise

By Ohm's Law:

$$\vec{e^2_{no,ch_1}} = \vec{I^2_{n\_ch_1}} (R_{op})^2$$

$$R_{op\ (output\ impedance)} = \left(\frac{1}{g_{m_1}} \parallel r_{ds_1} \parallel r_{ds_2}\right)$$

$$\therefore \quad \vec{e^2_{no,ch_1}} = \vec{I^2_{n\_ch_1}} \left(\frac{1}{g_{m_1}} \parallel r_{ds_1} \parallel r_{ds_2}\right)^2$$

$$\therefore \quad e^{2}_{no,ch_1}{}^{\rightarrow} = \left[\frac{r_{ds_2} \times r_{ds_1}}{(g_{m_1})(r_{ds_1})(r_{ds_2}) + r_{ds_1} + r_{ds_2}}\right]^2 I^{2}_{n\_ch_1}{}^{\rightarrow}$$

4.1.5 Response of noise from channel noise of Q2 ($I_{n\_ch_2}$)

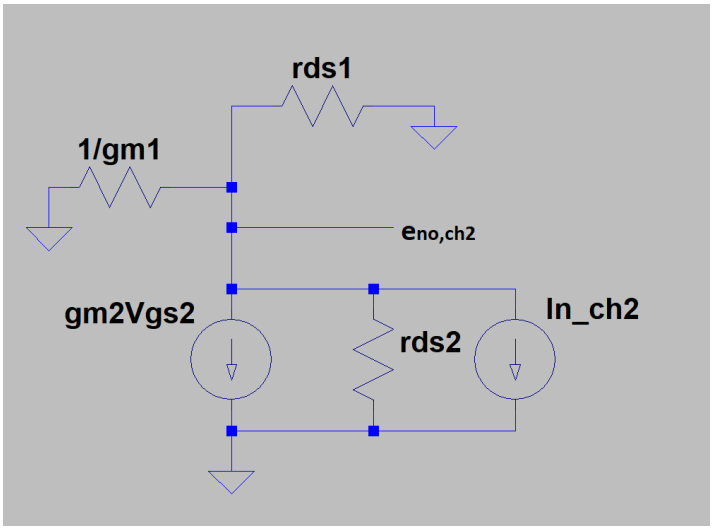

Fig. 4.10 Dual JFET - Output referred noise due to $I_{n\_ch_2}$ noise

By Ohm's Law:

$$e^2_{no,ch_2}\vec{} = I^2_{n\_ch_2}\vec{}(R_{op})^2$$

$$R_{op\ (output\ impedance)} = (\frac{1}{g_{m_1}} \parallel r_{ds_1} \parallel r_{ds_2})$$

$$\therefore \quad e^2_{no,ch_2}\vec{} = I^2_{n\_ch_2}\vec{}(\frac{1}{g_{m_1}} \parallel r_{ds_1} \parallel r_{ds_2})^2$$

$$e^2_{no,ch_2} = [\frac{r_{ds_2} \times r_{ds_1}}{(g_{m_1})(r_{ds_1})(r_{ds_2}) + r_{ds_1} + r_{ds_2}}]^2 I^2_{n\_ch_2}\vec{}$$

4.2 Output and Input Referred Voltage Noise Density

The output voltage noise density is given by:

$$\vec{e_{N,OUT}} = \sqrt{e^2_{no,dd}\,\vec{} + e^2_{no,gg}\,\vec{} + e^{2\,\vec{}}_{no,ch1} + e^2_{no,ch2}\,\vec{} + e^2_{no,ss}\,\vec{}}$$

The input referred voltage noise density can be found by dividing the individual response of output voltage noise density by square of gain of amplifier.

Thus, the input referred noise density is given by:

$$\vec{e_{N,IN}} = \sqrt{e^2_{ni,dd}\,\vec{} + e^2_{ni,gg}\,\vec{} + e^{2\,\vec{}}_{ni,ch1} + e^2_{ni,ch2}\,\vec{} + e^2_{ni,ss}\,\vec{}}$$

4.3 Simulation and verification of model with active load

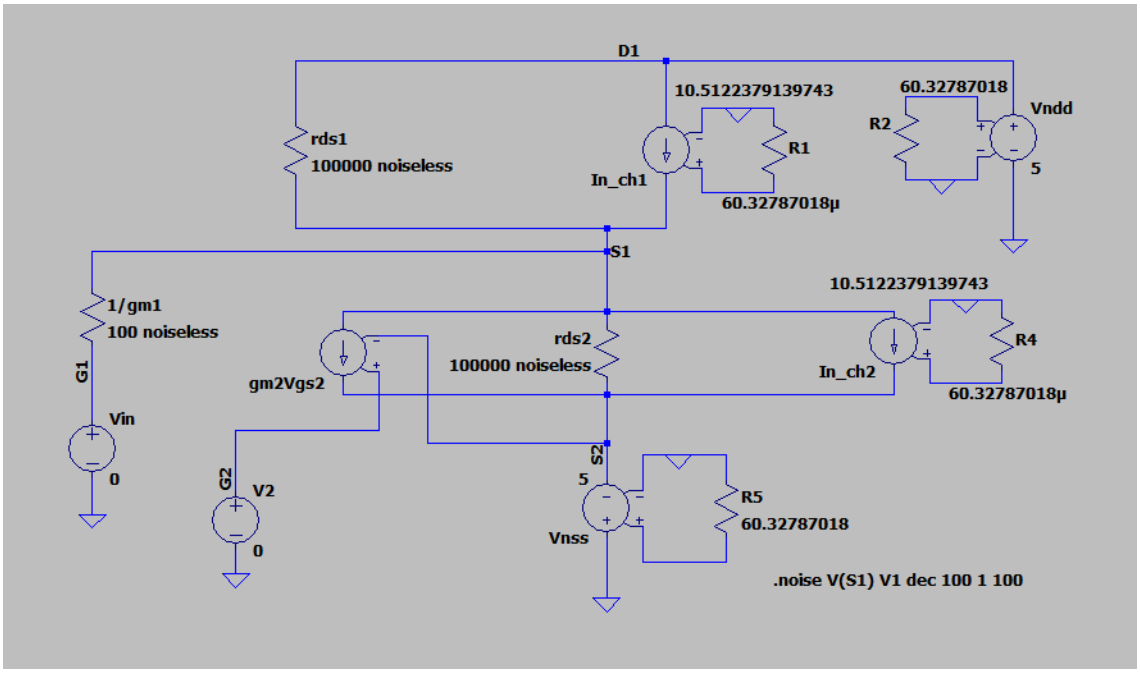

Fig. 4.11 LTSpice Schematic for Simulation of model with active load

As explained in Chapter 3.3, we used the same procedure to create the LTSpice® schematic for the small signal model of the complete pre-amplifier with the active load as seen in Fig. 4.11. We simulated the circuit for four different test cases as shown in Table 4.1 to Table 4.5.

4.4 Simulation observations for schematic with active load

Table 4.1 Simulation of dual JFET model (Test Case 1)

g_{m_1} = 10mS, g_{m_2} = 20mS, r_{ds_1} = 200kΩ, r_{ds_1} = 150kΩ				
V_{ndd} (nV/Hz½)	V_{nss} (nV/Hz½)	V_{ngg} (nV/Hz½)	Output Voltage Noise Density(nV/Hz½)	
			Analytical Model	Simulation
0	0	0	1.818	1.818
5	0	0	1.818	1.818
10	0	0	1.818	1.818
25	0	0	1.818	1.818
50	0	0	1.818	1.818
100	0	0	1.819	1.819
0	5	0	10.155	10.155
0	10	0	20.065	20.065
0	25	0	49.991	49.991
0	50	0	99.933	99.933
0	100	0	199.841	199.841
0	0	5	10.152	10.152
0	0	10	20.059	20.059
0	0	25	49.974	49.974
0	0	50	99.900	99.900
0	0	100	199.775	199.775

As seen from above table, for larger values of r_{ds_1} and r_{ds_2} ($r_{ds_1} and\, r_{ds_2} >> 1/g_{m_1} and\, 1/g_{m_2}$), the effect of noise from V_{ndd} is negligible, whereas the effect of V_{nss} and V_{ngg} is quite similar and very large compared to V_{ndd}.

Table 4.2 Simulation of dual JFET model (Test Case 2)

g_{m_1} = 1mS, g_{m_2} = 2mS, r_{ds_1} = 3kΩ, r_{ds_2} = 2kΩ				
V_{ndd} (nV/Hz½)	V_{nss} (nV/Hz½)	V_{ngg} (nV/Hz½)	Output Voltage Noise Density(nV/Hz½)	
			Analytical Model	Simulation
0	0	0	3.140	3.140
5	0	0	3.269	3.269
10	0	0	3.628	3.628
25	0	0	5.524	5.524
50	0	0	9.618	9.618
100	0	0	18.451	18.451

0	5	0	7.506	7.5067
0	10	0	13.993	13.993
0	25	0	34.235	34.235
0	50	0	68.254	68.254
0	100	0	136.399	136.399
0	0	5	6.294	6.294
0	0	10	11.352	11.352
0	0	25	27.452	27.452
0	0	50	54.6357	54.635
0	0	100	109.136	109.136

As seen from above table, for comparable values of r_{ds_1}, r_{ds_2}, $1/g_{m_1}$ and $1/g_{m_2}$, the effect of noise from V_{ndd} is relatively small but not negligible. But the effect of V_{nss} and V_{ngg} is quite similar and very large compared to V_{ndd}. Table 4.3, 4.4, 4.5 shows comparison between analytical model and simulation for some random values of the amplifier's parameters.

Table 4.3 Simulation of dual JFET model (Test Case 3)

V_{ndd}= 5nV/Hz½, V_{nss}= 0nV/Hz½, V_{ngg}= 0nV/Hz½					
gm1(mS)	gm2(mS)	rds1(kΩ)	rds2(kΩ)	Output Voltage Noise Density(nV/Hz½)	
				Model 1 (with 1/gm1)	Simulation (with gmVgs)
1	2	1	2	3.05	3.05
2	1	3	2	2.115	2.115
5	3	100	75	1.871	1.871
10	7	3	10	1.323	1.323

Table 4.4 Simulation of dual JFET model (Test Case 4)

V_{ndd}= 0nV/Hz½, V_{nss}= 5nV/Hz½, V_{ngg}= 0nV/Hz½					
gm1(mS)	gm2(mS)	rds1(kΩ)	rds2(kΩ)	Output Voltage Noise Density(nV/Hz½)	
				Model 1 (with 1/gm1)	Simulation (with gmVgs)
1	2	1	2	5.504	5.504
2	1	3	2	3.337	3.337
5	3	100	75	3.535	3.535
10	7	3	10	3.647	3.647

Table 4.5 Simulation of dual JFET model (Test Case 5)

V_{ndd}= 0nV/Hz½, V_{nss}= 0nV/Hz½, V_{ngg}= 5nV/Hz½					
gm1(mS)	gm2(mS)	rds1(kΩ)	rds2(kΩ)	Output Voltage Noise Density(nV/Hz½)	
				Model 1 (with 1/gm1)	Simulation (with gmVgs)
1	2	1	2	4.615	4.615
2	1	3	2	2.691	2.691
5	3	100	75	3.524	3.524
10	7	3	10	3.602	3.602

Conclusion

The very close agreement between the noise derived from the analytical model and SPICE simulation verified the correctness of our mathematical model. This analytical modeling and SPICE simulation shows us how various noises and noise sources may affect the output noise of a source follower amplifier with passive/active load. For a practical situation where drain to source channel resistance rds is much larger than $1/g_m$, noise from the power supply V_{ss} affects majorly on the output noise voltage of the JFET. Whereas, the effect of noise from the power supply V_{dd} is negligible. The noise from the power supply V_{gg} is not a concern as one can use a low pass RC circuit with a cut-off frequency less than 10Hz at the gate terminal and minimize the noise from V_{gg}. One can minimize the effect of noise from the supply V_{ss} by using better, high quality power supplies with low noise characteristics. The observation tables in Chapter 3.4 and Chapter 4.4 show exactly how each noise source contributes to the output voltage. Using this table will help designers to use correct apparatus and devices at the inputs of the JFET to effectively reduce the output noise.

As it can be observed, our simulation results match exactly with the values which we calculated. This brought us to the inference that our method for deriving the voltage densities satisfies the backend algorithm of the simulation software. Hence, the model can be used to develop an in-house noise calculator software. The model can be further utilised to optimize the noise performance of a source follower amplifier.

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