Bansilal Ramnath Agarwal Charitable Trust's

Vishwakarma Institute of Information Technology

(Department of Electronics and Telecommunication)

Internship Report

on

DESIGN AND SIMULATION OF JFET BASED LOW NOISE DC VOLTAGE SUPPLY FOR A SOURCE FOLLOWER CRYOGENIC PREAMPLIFIER

(ORGANISATION - TIFR, MUMBAI)

(DOMAIN - ANALOG CIRCUITS AND SYSTEMS)

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B. Tech E&TC

of

Savitribai Phule Pune University

(Formerly University of Pune)

Under supervision of

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Year 2020 - 2021

CERTIFICATE

This is to certify that internship work carried out at T.I.F.R., Mumbai in the eighth semester by,

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Our mentors

1. Prof. (Dr) Chandrashekhar Garde[1]
2. Prof. (Dr) Vandana Nanal[2]
3. Prof. (Dr) Shrikant Joshi[3]
4. Dr Ashif Reza[4#]

We would like to thank Prof. Chandrashekhar Garde from VIIT, Pune for giving us the opportunity to interact and connect us with great mentors from TIFR, Mumbai. Prof Garde's expertise in research, physics and cryogenics helped us understand our problem statement without any flaws and misconceptions. He mentored us for understanding the background of the project and motivated us to actively work on the project.

We thank Prof. Vandana Nanal from TIFR for giving us the great opportunity to work on the Neutrinoless double beta decay project.

We thank Prof. Shrikant Joshi (our final year project mentor) for interacting with us in every meeting and to solve all our queries related to the project. His expertise in core electronics helped us understand the fundamentals of analytical theorems, characteristics of microelectronics and power supply design processes. He helped us analyse our designs with utmost care.

Lastly, we thank our mentor Dr Ashif Reza from TIFR. His experience at TIFR and his direct involvement in the Neutrinoless double beta decay project helped us understand the problem statement, develop, and verify our designs through simulation. We thank him immensely to help us understand each aspect of designing and testing a low noise solution for a source follower amplifier.

Regards,
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Learnings and Achievements through the internship

This section highlights our experience, learnings, and achievements through this six-months internship programme at TIFR, Mumbai.

Interning at a research institute like TIFR is a task full of new learning experiences. This is a workspace which respects multiple opinions and sees them as a fundamental milestone leading towards a successful research. At TIFR, we realise the need to fully understand and frame the solution of a problem from multiple perspectives. It cultivates a mindset which never trusts a phenomenon without convincing enough scientific proof.

In this internship, we got to explore technology and infrastructure which we had not seen anywhere else. The Neutrinoless Double Beta Decay (NDBD) lab at TIFR is a fully equipped one with intelligently chosen devices.

While working on our project, we understood the importance of being a good researcher rather than having good information. Researching on available information, turning that into knowledge and then using this knowledge to develop proven technologies is what we learnt through this internship. Along with this, we realised that no information ever goes waste; from the smallest of meeting minutes to the longest research papers published by renowned scientists and professors in the past. This internship helped us to do a proper literature survey and taught us how to document our own work. This includes conducting a relevant and neat literature survey, writing useful minutes of meetings, maintaining logs of every task, communicating effectively with our mentors, and documenting our work collaboratively.

While these were philosophical learnings through our internship, we learnt numerous technical habits and tools too. The designing of a low noise amplifier was a multi-stage research consisting of theoretical design, simulation and analysis of the results. To understand how the amplifier operates at different bias points, we simulated and tabulated a very detailed spreadsheet full of useful data [6]. We then tabulated the effects of different input noises affecting the output noise. Using this data, we used our own analytical noise model of a JFET [5] to design filters and a low noise power supply for our preamplifier. After designing, troubleshooting and fine tuning was done to the schematic to provide accurate results. This resulted in a finalised schematic. PCB fabrication and testing will be done in near future.

During the course of our internship, we were able to visit TIFR campus once in January where we got first-hand experience of operating a dummy preamplifier circuit. This was the equipment for which we designed the low noise amplifier for. The research mindset which we picked up from this internship will be with us for a lifetime no matter where we choose to work in the future.

About NDBD Lab, TIFR

TIFR[5] is a National Centre of the Government of India, under the umbrella of the Department of Atomic Energy[6], as well as a deemed University awarding degrees for master's and doctoral programs. The Institute was founded in 1945 with support from the Sir Dorabji Tata Trust[7] under the vision of Dr. Homi Bhabha[8]. At TIFR, basic research in physics, chemistry, biology, mathematics, computer science and science education are carried out. Their main campus is in Mumbai, with centres at Pune, Bengaluru and Hyderabad.

Our internship was offered by Prof. Vandana Nanal[9] at the Department of Nuclear and Atomic Physics, TIFR[10]. Our internship was on a project called 'Search for Neutrinoless Double Beta Decay ($0\nu\beta\beta$)'[11]. $0\nu\beta\beta$ is a process which can tell us whether a neutrino is its own antiparticle or not. In other words, it will tell us whether the neutrino is a Dirac or a Majorana particle. This experiment will also provide the information on absolute effective mass of the neutrinos. The INdia-based TIN Detector (TIN.TIN) is a Sn cryogenic bolometer for the study of Neutrinoless Double Beta Decay ($0\nu\beta\beta$) in ^{124}Sn and is currently in the R&D stage at TIFR, Mumbai. It will be housed at the upcoming underground facility, India-based Neutrino Observatory (INO).

Fig. Inside NDBD lab[12]

[5] "Tata Institute of Fundamental Research." https://www.tifr.res.in/. Accessed 7 May. 2021.
[6] "Department of Atomic Energy." https://dae.gov.in/. Accessed 7 May. 2021.
[7] "About Sir Dorabji Tata - Tata Trusts." https://www.tatatrusts.org/about-tatatrusts/about-sir-dorabji-tata. Accessed 7 May. 2021.
[8] "Homi J. Bhabha - Wikipedia." https://en.wikipedia.org/wiki/Homi_J._Bhabha. Accessed 7 May. 2021.
[9] "tin.tin | Contact - Tata Institute of Fundamental Research." https://www.tifr.res.in/~tin.tin/contact/. Accessed 7 May. 2021.
[10] "TIFR | Department of Nuclear and Atomic Physics." https://www.tifr.res.in/~dnap/. Accessed 7 May. 2021.
[11] "tin.tin | Home." 29 Sept. 2020, https://www.tifr.res.in/~tin.tin/. Accessed 7 May. 2021.
[12] "tin.tin | Home." 29 Sept. 2020, https://www.tifr.res.in/~tin.tin/tin.tin/. Accessed 7 May. 2021.

Abstract

Objective

To design and simulate a low noise preamplifier requires a DC power supply with very low noise characteristics. Most of the commercially available general purpose DC power supplies have high voltage noise density (>10nV/√Hz), which is not good enough for the operation of a low noise preamplifier. In this internship, a DC supply with very low noise characteristics (<2nV/√Hz) needs to be designed for the source follower preamplifier [4] to be used in the NDBD project.

Methods

1. Simulate and tabulate data for G_m and R_{ds} of JFET at different bias points.
2. Simulate and tabulate voltage gain and output noise voltage densities at different bias points for a source follower amplifier with passive load. Compare these values to the theoretical values.
3. Simulate and tabulate voltage gain and output noise voltage densities at different bias points for a source follower amplifier with active load. Compare these values to the theoretical values.
4. Reduce output noise by using filters and designing V_{ss} power supply with low noise characteristics.

Results

1. First order low pass RC filter was included at the gate terminal of the preamplifier to reduce V_{gg} noise. This solution reduced the effect of gate noise on the output noise from 10nV√Hz to below 3nV/√Hz.
2. A low noise power supply was designed and simulated for supplying V_{ss} to the preamplifier. This solution reduced the effect of V_{ss} noise to 1.848nV/√Hz and 1.272nV/√Hz for negative and positive V_{ss} bias respectively at 1kHz.
3. The designed power supply would prove to be a very good alternative to get low noise operation on the bolometer detector.

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Chapter 6: Design and simulation of low noise DC supply

Chapter 1: Introduction

1.1 Background

A prototype tin cryogenic bolometer detector operating at 10 mK is being developed to study a phenomenon known as neutrinoless double-beta decay (NDBD) at TIFR, Mumbai [1]. To detect a very tiny change in temperature (~ few tens to hundreds of microKelvin) due to an incident radiation, a neutron transmutation doped (NTD) Germanium temperature sensor is used due to its very high sensitivity (dR/dT) at such a low temperature.

In order to detect a weak electrical signal from an NTD Ge sensor (typical sensor resistance ~ 500 Mohm), a low noise amplifier with a very high input impedance is required. Currently, the sensor signal is amplified using a commercial differential amplifier [2] kept at room temperature. To reduce the EMI pickups and to minimize the signal integration due to long transmission line connecting NTD Ge sensor at 10 mK to differential amplifier outside the cryostat, it is planned to mount a preamplification stage inside the cryogen free dilution refrigerator (CFDR) [3]. For this purpose, a high input impedance front-end source follower preamplifier is already designed and tested at 120 K [4]. The Source follower preamplifier with active load configuration offers almost unity voltage gain and very stable performance as compared to a conventional source follower with passive load.

To achieve a high precision measurement, the design of the front-end source follower amplifier needs to be further optimized to accomplish very low noise, high gain stability and very low drift performance. An analytical model [5] has already been derived to understand how noise from different components and DC power supply in a source follower amplifier affects the overall noise performance of the amplifier. Through this model, it was observed that noise from the power supply (V_{ss}) affects majorly on the output voltage noise of the JFET.

To reduce the output noise voltage density, power supplies (V_{gg} and V_{ss}) with very low noise characteristics are required. This internship report presents the design and simulation of a low noise DC supply and its effect on the noise performance of a source follower preamplifier.

1.2 Motivation

As discussed in Chapter 1.1, an analytical model has already been derived to understand the effects of noise from power supplies and different components on the output voltage noise of the amplifier. Conclusion of this model is that noise from power supply V_{ss} and V_{gg} affect the output noise voltage density to a great extent. For the NDBD project to work, it is crucial that this output noise be reduced as much as possible. We were hence motivated to do this internship where we would get a chance to design and simulate a low noise power supply and filters so that the output noise of the preamplifier gets reduced as much as possible.

Chapter 2: Literature Survey

2.1 Noise modelling of source follower amplifier

To design a low noise amplifier for our application, a noise model of a source follower amplifier is used to figure out the output referred noise voltage depending on the different inputs of the amplifier. For this, we referred to our own noise model [5] which we developed before this internship.

2.2 Noise model of amplifier with passive load

The analytical model included two circuit designs. This chapter discusses the noise model for a source follower amplifier with passive load.

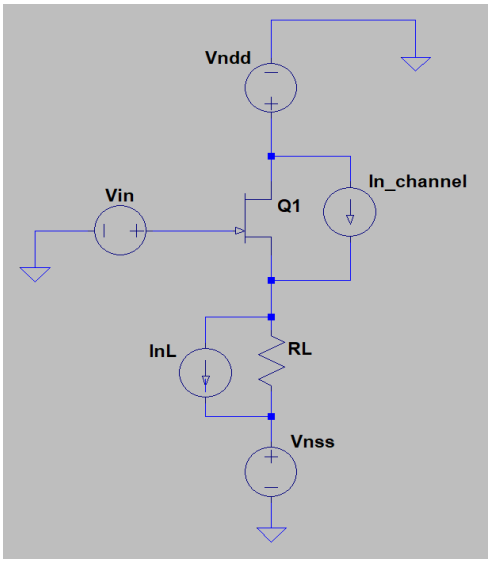

Fig. 2.1(a) Source follower amplifier with passive load with simplified noise sources

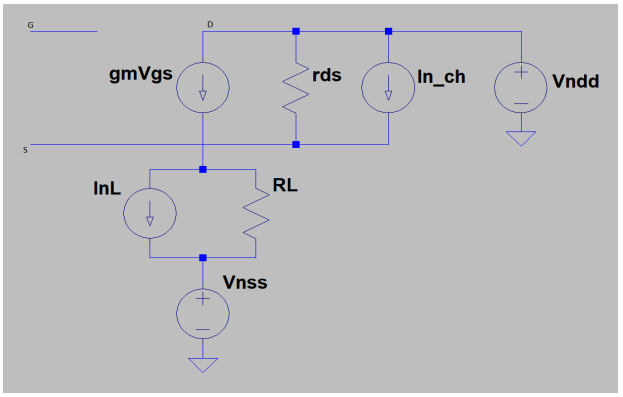

Fig. 2.1(b) Small signal model of a source follower amplifier with passive load

Formulae generated by the analytical model are as follows. We will use these formulae to theoretically calculate the output noise added due to each individual noise sources of the amplifier..

Noise Source	**Response of a noise source**
Channel noise	$\vec{e^2_{no,channel}} = \vec{I^2_{n,channel}} \left(\frac{R_{eq}}{1+g_m R_{eq}}\right)^2$ $where\ R_{eq} = r_{ds} \| R_L$

Load resistor	$\overrightarrow{e^2_{no,L}} = \frac{4k_BT}{R_L}\left(\frac{R_{eq}}{1+g_m R_{eq}}\right)^2$
Power supply V_{nss}	$\overrightarrow{e^2_{no,ss}} = \left[\frac{1/gm \| rds}{(R_L+(1/gm \| rds)}\right]^2 \overrightarrow{V^2_{nss}}$
Power supply noise V_{ndd}	$\overrightarrow{e^2_{no,dd}} = \left[\frac{R_L \| 1/gm}{(R_L \| 1/gm)+rds}\right]^2 \overrightarrow{V^2_{ndd}}$

Table 2.1 Response of noise sources in passive load preamplifier

2.3 Noise model of amplifier with active load

We shall now discuss the noise model for a source follower amplifier with active load.

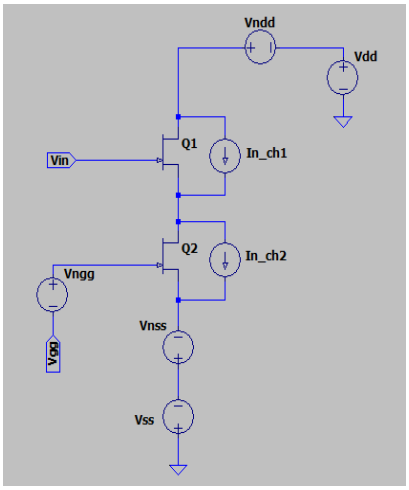

Fig. 2.2(a) Source follower amplifier with active load with simplified noise sources

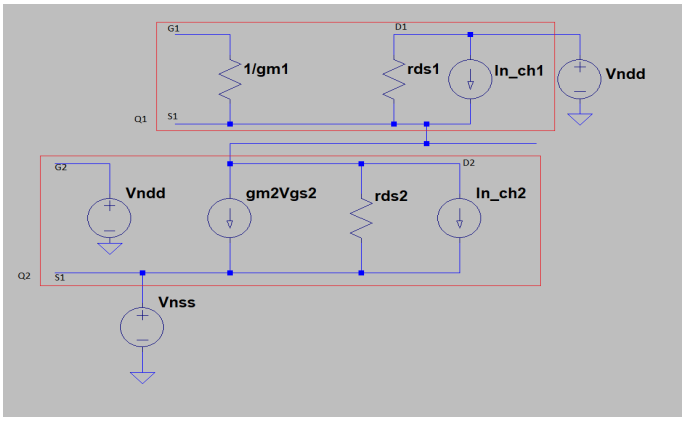

Fig. 2.2(b) Small signal model of a source follower amplifier with active load

Formulae generated by the analytical model are as follows. We will use these formulae to theoretically calculate the output noise added due to each individual noise sources of the amplifier..

Noise source	**Response of noise source**
Power supply V_{ndd}	$\overrightarrow{e^2_{no,dd}} = \left[\frac{(r_{ds_2})}{(g_{m_1})(r_{ds_1})(r_{ds_2})+r_{ds_1}+r_{ds_2}}\right]^2 \overrightarrow{V^2_{ndd}}$

Power supply V_{ngg}	$e_{no,gg}^{2} \rightarrow = \left[\frac{g_{m_2} r_{ds_1} r_{ds_2}}{(g_{m_1})(r_{ds_1})(r_{ds_2}) + r_{ds_1} + r_{ds_2}}\right]^2 V_{ngg}^{2} \rightarrow$
Power supply V_{nss}	$e_{no,ss}^{2} \rightarrow = \left[\frac{(1+g_{m_2} r_{rd_2}) r_{ds_1}}{(g_{m_1})(r_{ds_1})(r_{ds_2}) + r_{ds_1} + r_{ds_2}}\right]^2 V_{nss}^{2} \rightarrow$
Channel noise of Q1 ($I_{n\_ch_1}$)	$e_{no,ch_1}^{2} \rightarrow = \left[\frac{r_{ds_2} \times r_{ds_1}}{(g_{m_1})(r_{ds_1})(r_{ds_2}) + r_{ds_1} + r_{ds_2}}\right]^2 I_{n\_ch_1}^{2} \rightarrow$
Channel noise of Q2 ($I_{n\_ch_2}$)	$e_{no,ch_2}^{2} = \left[\frac{r_{ds_2} \times r_{ds_1}}{(g_{m_1})(r_{ds_1})(r_{ds_2}) + r_{ds_1} + r_{ds_2}}\right]^2 I_{n\_ch_2}^{2} \rightarrow$

Table 2.2 Response of noise sources in active load preamplifier

2.4 Inference

From the contents of this literature survey, we can further decide how to reduce the noise of the preamplifier. In this case, we can conclude that the noise from V_{gg} and V_{ss} are the most significant factors to govern the output noise voltage density. Hence reducing the noises from V_{ss} and V_{gg} can be a solution to reduce output noise. In the coming chapters, we shall discuss how to reduce the noises from these two sources in detail.

Chapter 3: Prerequisites - Tabulating g_m and r_{ds}

3.1 Need to tabulate g_m and r_{ds}

Values of g_m and r_{ds} vary with different biasing conditions. These values are very crucial for theoretical calculations for various parameters in an amplifier. We will need the values of g_m and r_{ds} at different bias points to calculate the gain and the output noise voltage density by using the analytical model [Refer Chapter 2].

3.2 Simulation schematic for g_m and r_{ds} calculations

Following are the simulation schematics used to tabulate the values of g_m and r_{ds}.

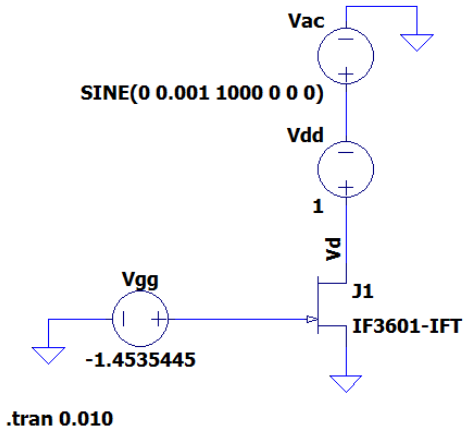

Fig. 3(a) Simulation for r_{ds} calculation

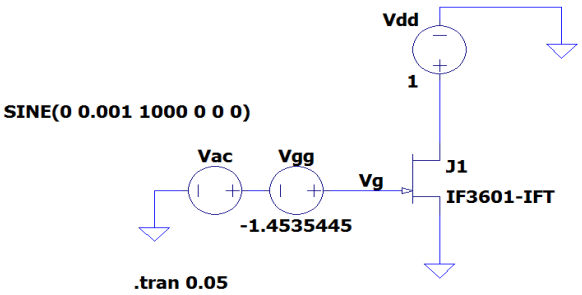

Fig. 3(b) Simulation for g_m calculation

Two tables can be seen below. In Table 3(a), g_m and r_{ds} is tabulated with variation in I_d and in Table 3(b), the same is tabulated with variation in V_{ds}.

For tabulating values of r_{ds}, V_{dd} was superimposed with an AC signal and the change in I_d was noted for the change in V_{ds} in both Table 3(a) and Table 3(b). Peak-to-peak values were measured. The slope of the drain characteristics i.e, I_d vs V_{ds} graph is equal to $\frac{1}{r_{ds}}$. So, r_{ds} can be calculated as, $r_{ds} = \frac{\Delta V_{ds}}{\Delta I_d}$.

On the other hand, for tabulating values of g_m, V_{gg} was superimposed with an AC signal. The change in I_d was noted for the change in V_{gs} in both the tables. g_m can be calculated using transfer characteristics of a JFET. With peak-to-peak values and with the formula, $g_m = \frac{\Delta I_d}{\Delta V_{gs}}$, we can now tabulate all values of g_m.

Table 1: Vds=1V			
Vgs	Id (mA)	gm (mS)	rds (kOhm)
-1.467	0.50	30.16	299.34
-1.454	1.00	41.93	278.13
-1.443	1.50	51.18	266.77
-1.434	2.00	58.95	245.43
-1.426	2.50	65.69	238.61
-1.419	3.00	71.98	220.89

Table 3(a) G_m and R_{ds} for varying I_d

Table 2: Id=1mA			
Vgs	Vds(V)	gm (mS)	rds (kOhm)
-1.45	0.10	42.407	242.504
-1.45	0.20	42.422	249.025
-1.45	0.30	42.419	251.115
-1.45	0.40	42.429	257.730
-1.45	0.50	42.367	261.600
-1.45	1.00	42.423	280.408
-1.45	1.50	42.421	297.042
-1.45	2.00	42.426	321.309
-1.45	2.50	42.438	332.745
-1.45	3.00	42.374	346.856

Table 3(b) G_m and R_{ds} for varying V_{ds}

3.3 Inference

From Table 3(a), it is observed that for a constant V_{ds}, the value of g_m increases with increase in drain current I_d. The value of g_m is increased from 30.16mS to 71.98mS for increase in drain current from 0.5mA to 3mA. The value of r_{ds} is decreased from 299.34kΩ to 220.89kΩ for increase in drain current from 0.5mA to 3mA.

From Table 3(b), it is observed that, for a constant I_d the value of r_{ds} increases with increase in V_{ds} . The value of r_{ds} increases from 242.5kΩ to 346.8kΩ for increase in V_{ds} from 0.1V to 3.0V. There is no significant variation in the value of g_m. It is almost constant at 42.4mS.

The values obtained from Table 3(a) and Table 3(b) will be used in further chapters, to select a proper operating point for biasing the source follower amplifier and thereby verifying the gain and output voltage noise density with the analytical model.

Chapter 4: Simulating source follower with passive load

4.1 Preamplifier with noiseless power supplies

This step was to check the voltage gain and the output noise voltage density of the JFET by assuming completely noiseless power supplies. This is to tabulate the noises from the I_{n_ch} and R_L. In Table 4.1, the simulation results have been compared with the analytical model for voltage gain and output noise voltage density.

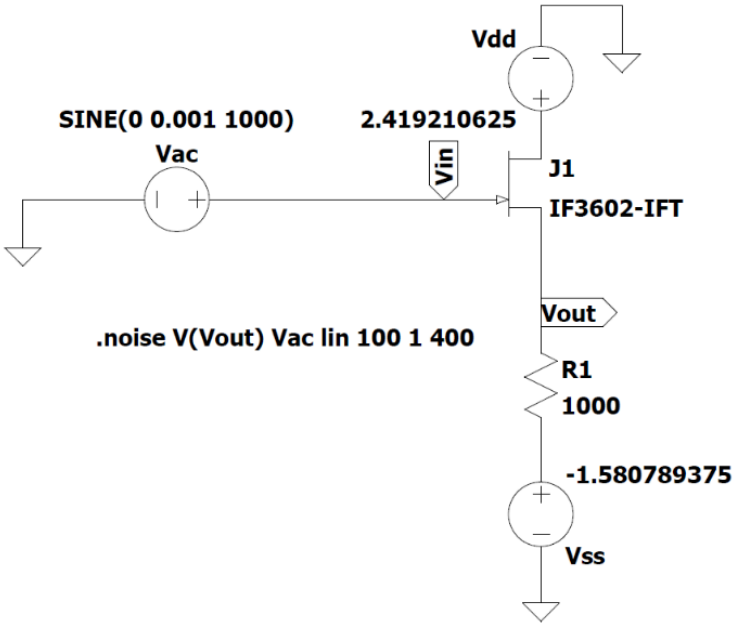

Fig. 4.1 Preamplifier with passive load with noiseless power supplies

Table 4.1 Gain and output noise for passive load preamplifier with noiseless power supplies

Id (mA)	Vds (V)	Vdd (V)	Vss (V)	Theoretical Gain (Av)	Simulated Gain (Av)	Theoretical Noise Density (RL & channel) (nV/Hz^1/2)	Simulated Noise Density (RL & channel) (nV/Hz^1/2)
Table 1							
0.50	1.00	2.467	0.967	0.968	0.968	0.600	0.600
1.00	1.00	2.454	0.454	0.977	0.977	0.507	0.508
1.50	1.00	2.443	-0.057	0.981	0.981	0.462	0.461
2.00	1.00	2.434	-0.566	0.983	0.983	0.431	0.430
2.50	1.00	2.426	-1.074	0.985	0.985	0.409	0.407
3.00	1.00	2.419	-1.581	0.986	0.986	0.390	0.390
Table 2							
1.00	0.10	1.554	0.454	0.977	0.977	0.507	0.508
1.00	0.20	1.654	0.454	0.977	0.977	0.507	0.508
1.00	0.30	1.754	0.454	0.977	0.977	0.507	0.508
1.00	0.40	1.854	0.454	0.977	0.977	0.507	0.508
1.00	0.50	1.954	0.454	0.977	0.977	0.508	0.508
1.00	1.00	2.454	0.454	0.977	0.977	0.507	0.508
1.00	1.50	2.954	0.454	0.977	0.977	0.507	0.507
1.00	2.00	3.454	0.454	0.977	0.977	0.507	0.507
1.00	2.50	3.954	0.454	0.977	0.977	0.507	0.507
1.00	3.00	4.454	0.454	0.977	0.977	0.508	0.507

As I_d increases, the output noise decreases. However, change in V_{ds} does not affect the output noise. The output noise here is the noise due to $I_{n\_channel}$ and R_L (load).

4.2 Amplifier with noisy power supplies

In this step, I_d and V_{ds} are kept constant but power supply noises have been added. In Table 4.2, two sub-tables have been included which show how noise from V_{dd} and V_{ss} independently affect the output noise voltage density. The following Fig. 4.2 is the schematic used for simulation in LTSpice[13] simulation tool.

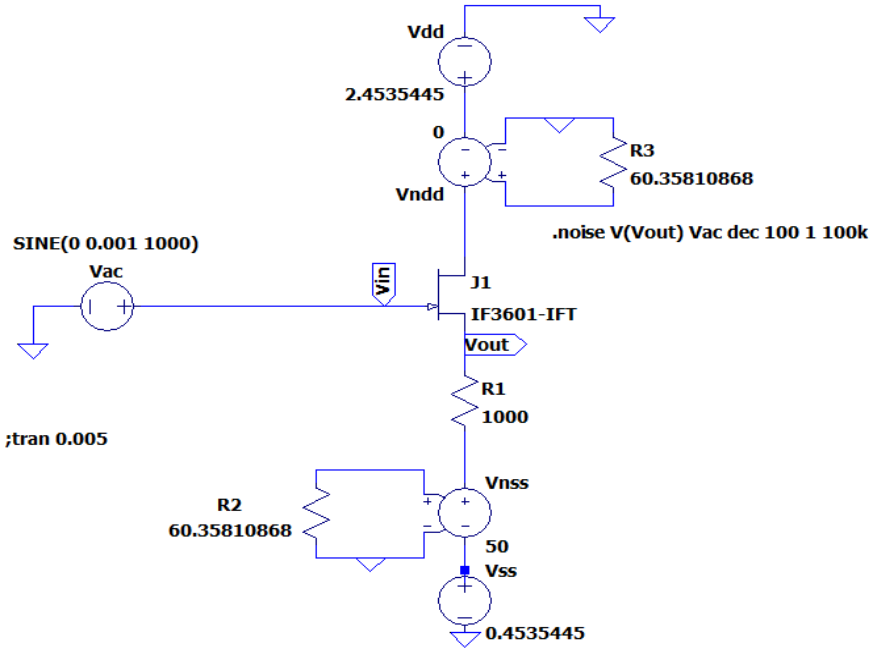

Fig. 4.2 Preamplifier with passive load with noisy power supplies

[13] "LTspice Simulator | Analog Devices." 17 Sept. 2017, https://www.analog.com/en/design-center/design-tools-and-calculators/ltspice-simulator.html. Accessed 7 May. 2021.

Table 4.2 Output noise for passive load preamplifier with noisy power supplies

Id (mA)	Vds (V)	Vndd (nV/Hz^1/2)	Vnss (nV/Hz^1/2)	Simulated Noise Density (All) (nV/Hz^1/2)	Theoretical Noise Density (All) (nV/Hz^1/2)
Table 1					
1.00	1.00	0	0	0.505	0.510
1.00	1.00	5	0	0.505	0.510
1.00	1.00	10	0	0.505	0.510
1.00	1.00	15	0	0.505	0.510
1.00	1.00	20	0	0.505	0.510
1.00	1.00	25	0	0.505	0.510
1.00	1.00	30	0	0.505	0.510
1.00	1.00	35	0	0.505	0.510
1.00	1.00	40	0	0.505	0.510
1.00	1.00	45	0	0.505	0.510
1.00	1.00	50	0	0.505	0.510
Table 2					
1.00	1.00	0	0	0.505	0.510
1.00	1.00	0	5	0.518	0.523
1.00	1.00	0	10	0.554	0.561
1.00	1.00	0	15	0.610	0.618
1.00	1.00	0	20	0.681	0.691
1.00	1.00	0	25	0.762	0.774
1.00	1.00	0	30	0.852	0.865
1.00	1.00	0	35	0.946	0.962
1.00	1.00	0	40	1.044	1.062
1.00	1.00	0	45	1.145	1.166
1.00	1.00	0	50	1.249	1.271
Table 3					
1.00	1.00	0	0	0.506	0.510
1.00	1.00	5	5	0.518	0.523
1.00	1.00	10	10	0.555	0.561
1.00	1.00	15	15	0.611	0.618
1.00	1.00	20	20	0.681	0.691
1.00	1.00	25	25	0.763	0.774
1.00	1.00	30	30	0.851	0.865
1.00	1.00	35	35	0.946	0.962
1.00	1.00	40	40	1.044	1.062
1.00	1.00	45	45	1.145	1.166
1.00	1.00	50	50	1.248	1.272

As noise from V_{dd} supply increases, output noise does not vary significantly. However, as noise from V_{ss} supply increases, output noise varies much more significantly.

4.3 Inference

This chapter helps us verify that the mathematical model is accurate and can provide us the same results as the simulation tool. Note that this circuit is not the circuit which we

will be using on the actual project owing to the higher power consumption due to the passive load. Refer Chapter 5 to see the simulation of the preamplifier with active load.

Additionally, the data in Table 4.1 and Table 4.2 will be used to see how V_{dd} and V_{ss} can affect output noise at various bias points. When we design our low noise solution, we shall use this table to check if our solution is reducing the output noise properly at all bias points.

Chapter 5: Simulating source follower with active load

5.1 Preamplifier with noiseless power supplies

Similar to Chapter 4.1, this step was to check the voltage gain and the output noise voltage density of the JFET by assuming completely noiseless power supplies. V_{ds1} and V_{ds2} are varied to provide different bias points. This is to tabulate the noises from the I_{n_ch1} and I_{n_ch2}. In Table 4.2, the simulation results have been compared with the analytical model for voltage gain and output noise voltage density.

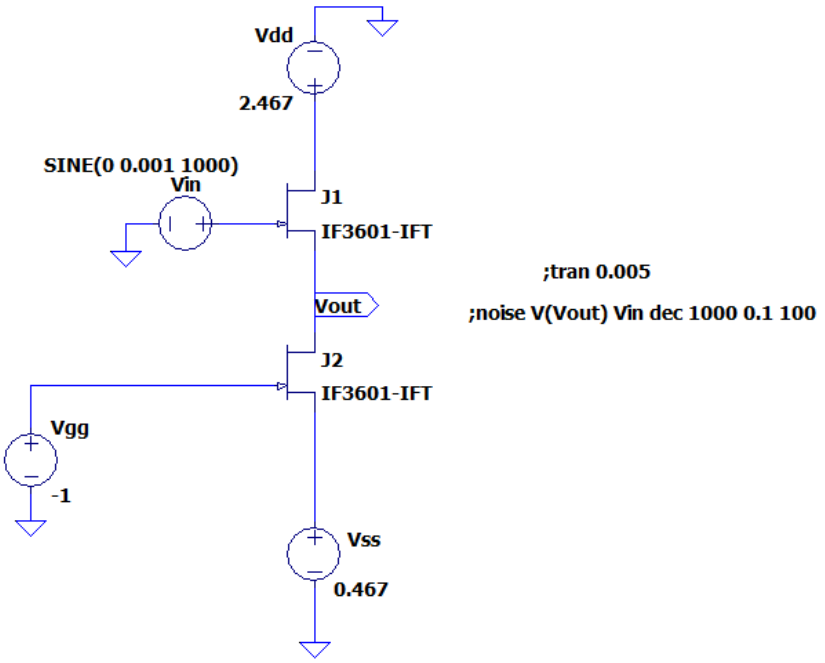

Fig. 5.1 Preamplifier with active load with noiseless power supplies

Table 5.1 Gain and output noise for active load preamplifier with noiseless power supplies

Id (mA)	Vds1 (V)	Vds2 (V)	Vgg (V)	Vdd (V)	Vss (V)	Theoretical Gain (Av)	Simulated Gain (Av)	Simulated Noise Density (nV/Hz^1/2)	Theoretical Noise Density (nV/Hz^1/2)
Table 1									
0.50	1.00	1.00	-1.00	2.467	0.467	0.9998	0.9958	0.853	0.856
1.00	1.00	1.00	-1.00	2.454	0.454	0.9998	0.9962	0.719	0.722
1.50	1.00	1.00	-1.00	2.443	0.443	0.9999	0.9962	0.650	0.657
2.00	1.00	1.00	-1.00	2.434	0.434	0.9999	0.9963	0.606	0.612
2.50	1.00	1.00	-1.00	2.426	0.426	0.9999	0.9962	0.574	0.580
3.00	1.00	1.00	-1.00	2.419	0.419	0.9999	0.9963	0.548	0.554
Table 2									
1.00	0.10	0.10	-0.10	1.554	1.354	0.9998	0.9969	0.719	0.722
1.00	0.20	0.20	-0.20	1.654	1.254	0.9998	0.9970	0.719	0.722
1.00	0.30	0.30	-0.30	1.754	1.154	0.9998	0.9969	0.719	0.722
1.00	0.40	0.40	-0.40	1.854	1.054	0.9998	0.9969	0.719	0.722
1.00	0.50	0.50	-0.50	1.954	0.954	0.9998	0.9970	0.719	0.722
1.00	1.00	1.00	-1.00	2.454	0.454	0.9998	0.9969	0.719	0.722
1.00	1.50	1.50	-1.50	2.954	-0.046	0.9998	0.9981	0.719	0.722
1.00	2.00	2.00	-2.00	3.454	-0.546	0.9999	0.9981	0.719	0.722
1.00	2.50	2.50	-2.50	3.954	-1.046	0.9999	0.9981	0.718	0.722
1.00	3.00	3.00	-3.00	4.454	-1.546	0.9999	0.9981	0.718	0.722

As I_d increases, the output noise decreases. However, change in V_{ds} does not impact the output noise. The output noise here is the noise coming from $I_{n\_channel1}$ and $I_{n\_channel2}$.

5.2 Amplifier with noisy power supplies without RC filter

In this step, I_d and V_{ds} for both JFETs are kept constant but power supply noises have been added. In Table 5.2, two sub-tables have been included which show how noise from V_{dd} and V_{ss} independently affect the output noise voltage density. The following Fig. 5.2 is the schematic used for simulation in LTSpice[14] simulation tool.

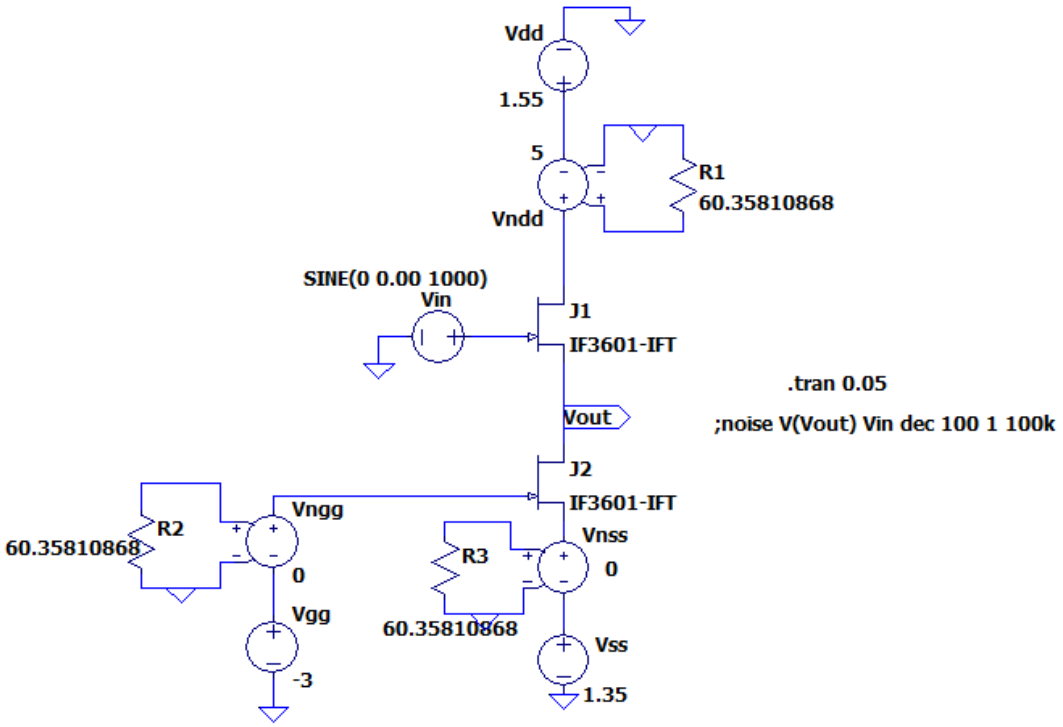

Fig. 5.2 Preamplifier with active load with noisy power supplies without RC filter

[14] "LTspice Simulator | Analog Devices." 17 Sept. 2017, https://www.analog.com/en/design-center/design-tools-and-calculators/ltspice-simulator.html. Accessed 7 May. 2021.

Table 5.2 Output noise for active load preamplifier with noisy power supplies

Vndd (nV/Hz^1/2)	Vnss (nV/Hz^1/2)	Vngg (nV/Hz^1/2)	Simulated Noise Density (nV/Hz^1/2)	Theoretical Noise Density (nV/Hz^1/2)
Table 1				
0	0	0	0.719	0.722
5	0	0	0.719	0.722
10	0	0	0.719	0.722
15	0	0	0.719	0.722
20	0	0	0.719	0.722
25	0	0	0.719	0.722
30	0	0	0.719	0.722
35	0	0	0.719	0.722
40	0	0	0.719	0.722
45	0	0	0.719	0.722
50	0	0	0.719	0.722
Table 2				
0	0	0	0.719	0.722
0	5	0	5.053	5.051
0	10	0	10.028	10.025
0	15	0	15.021	15.016
0	20	0	20.017	20.011
0	25	0	25.016	25.008
0	30	0	30.015	30.006
0	35	0	35.015	35.004
0	40	0	40.016	40.003
0	45	0	45.016	45.002
0	50	0	50.016	50.001
Table 3				
0	0	0	0.719	0.722
0	0	5	5.052	5.051
0	0	10	10.028	10.024
0	0	15	15.020	15.015
0	0	20	20.017	20.010
0	0	25	25.015	25.006
0	0	30	30.015	30.004
0	0	35	35.014	35.002
0	0	40	40.015	40.000
0	0	45	45.015	44.998
0	0	50	50.015	49.997
Table 4				
0	0	0	0.719	0.722
5	5	5	7.109	7.107
10	10	10	14.163	14.159
15	15	15	21.230	21.223
20	20	20	28.300	28.290
25	25	25	35.370	35.358
30	30	30	42.442	42.427
35	35	35	49.513	49.496
40	40	40	56.585	56.566
45	45	45	63.657	63.636
50	50	50	70.730	70.705

Noise from V_{ss} and V_{gg} affect the output noise most significantly. However, noise from V_{dd} makes no significant impact on output noise.

5.3 Inference

This chapter plots the output noise of a preamplifier with active load at different bias points. This preamplifier also contains noise response from V_{gg}. Using these tables as a benchmark, we would be able to check if our low noise solution reduces all noises at all bias points.

Using the data from Table 5.2, we will now be working on our solution for reducing input noises from V_{ss} and V_{gg} inputs of the preamplifier.

Chapter 6: Design and simulation of low noise DC supply

6.1 Reducing noise from V_{gg}

As observed in Table 5.2, the output noise voltage density is majorly affected by noise from V_{gg} and noise from V_{ss} power supplies. In this chapter, we will try to reduce the noise from the V_{gg} power supply using a RC filter. Refer Fig. 6.1 This will reduce the output noise contributed by V_{gg}. The chosen low-pass RC filter has a cut-off frequency of 0.02Hz.

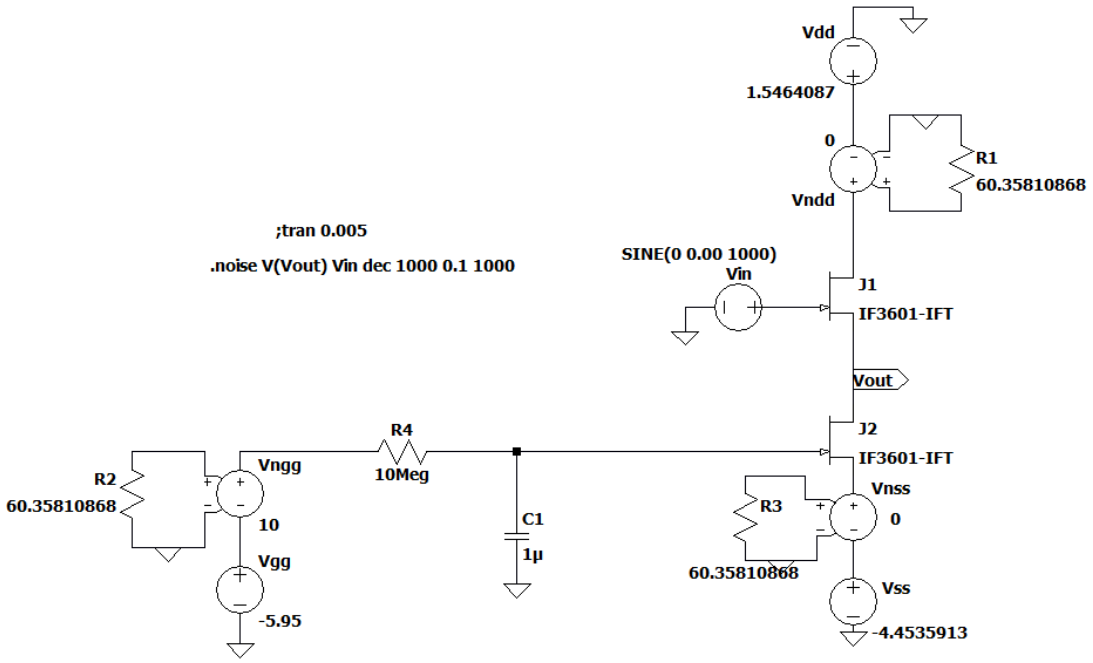

Fig. 6.1 Preamplifier with active load with noisy power supplies with RC filter

Refer Fig 6.2(a) and Fig 6.2(b) to compare the difference in output noise voltage density. Fig 6.2(a) shows the noise density without the above solution to reduce V_{gg} noise and Fig 6.2(b) shows the noise density after the filter was implemented. This noise density due to V_{gg} is simulated with a noise source V_{ngg} of 10nV/√Hz and noise sources V_{nss} and V_{ndd} are set to zero.

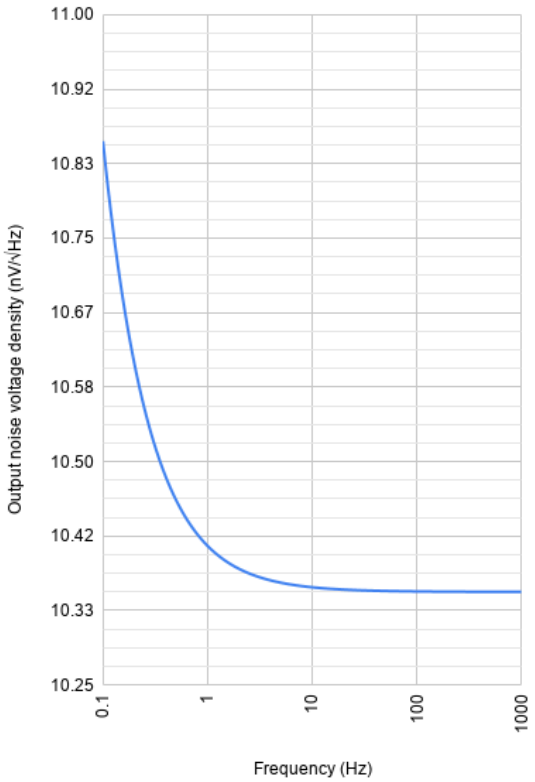

Fig 6.2(a) Output noise voltage density for active load preamplifier with noise power supplies without RC filter at Gate terminal

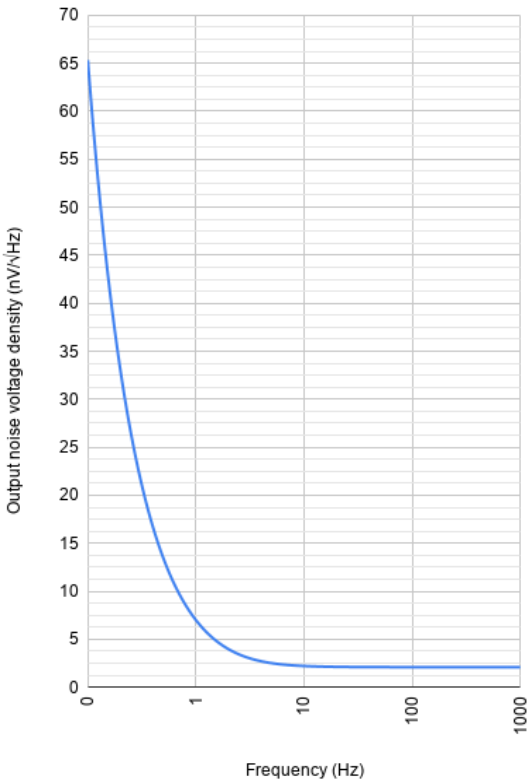

Fig 6.2(b) Output noise voltage density for active load preamplifier with noisy power supplies with RC filter at Gate terminal

As observed in Fig 6.2(a) and Fig 6.2(b), there is a very significant drop in output noise after using the RC filter at the Gate terminal. Without using the RC filter, the output noise voltage density flattens at 75Hz and is around 10.35nV/√Hz. After using the RC filter, this noise is settled below 3nV/√Hz after 3Hz. Hence, the problem of noise affected by the gate power supply is solved.

6.2 Reducing noise from V_{ss}

The noise from V_{ss} terminal affects greatly on the output noise as suggested by our noise model studied in Chapter 2. To reduce the noise of the V_{ss} power supply, using a filter is not a wise idea as the passive components in the filter cause a lot of power dissipation. So, we went with another design approach.

6.2.1 Design approach

Our noise model can tell us that the power supply V_{gg} and V_{ss} mainly affects the output noise of the amplifier.. Also, we figured out how to reduce the noise from V_{gg} in Chapter 6.1. We used this information to design a power supply which used another source follower JFET amplifier with a passive load (henceforth referred to as PSA or Power Supply Amplifier). We incorporated an RC filter at its gate terminal and grounded the V_{ss} terminal so that there is no noise coming from both these terminals. By varying V_{dd} and V_{gg} of the PSA, we were able to generate a low noise DC output. This output can now be connected to our original preamplifier's V_{ss} terminal. To avoid loading effects and to isolate the two circuits, we also used an Op-Amp based on LT1128/1028.

As the original preamplifier should support all bias points as simulated in Chapter 4 and Chapter 5, the V_{ss} power supply generated by the PSA should be able to support negative as well as positive supply capability. But without a V_{ss} supply on our PSA, we would not be able to create a negative output. Hence, two circuits were developed: one for negative and one for positive supply. The difference between these two was the Op-Amp configuration used to invert/non-invert the PSA output.

6.2.2 Circuit design for positive PSA

Here, the output of PSA is given to V_{ss2} through a simple buffer with unity gain. Refer Fig. 6.2.2 for circuit diagram.

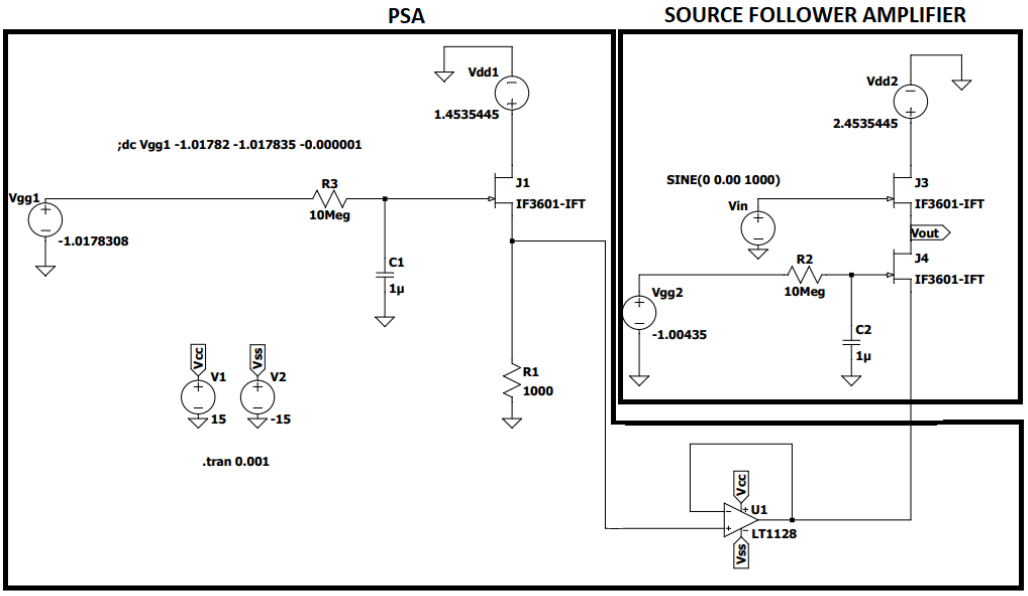

Fig. 6.2.2 Circuit diagram for positive PSA

Test results of positive PSA:

- Using LT1128 as buffer: Gain: 0.999117
- Without considering power supply noises: Output Noise density at 1kHz: **1.2717694nV/√Hz**
- After considering 20nV/√Hz for each supply: Output noise density at 1kHz: **1.2718214nV/√Hz**

Table 6.2.2(a) Output noise test results of preamplifier for positive PSA

Frequency (Hz)	Output Noise Density (nV/Hz^1/2)	Frequency (Hz)	Output Noise Density (nV/Hz^1/2)
0.1	92.1721	10	1.6972
0.2	46.6578	20	1.4253
0.3	31.5362	30	1.3596
0.4	23.5267	40	1.3301
0.5	18.8778	50	1.3151
0.6	15.9250	60	1.3065
0.7	13.7413	70	1.3004
0.8	11.9320	80	1.2956
0.9	10.7685	90	1.2927
1	9.6050	100	1.2898
2	5.0298	200	1.2795
3	3.5767	300	1.2765
4	2.8357	400	1.2750
5	2.4258	500	1.2742
6	2.1791	600	1.2737
7	2.0040	700	1.2733
8	1.8636	800	1.2730
9	1.7804	900	1.2728
10	1.6972	1000	1.2726

The above table shows the output noise density as observed at the output of the preamplifier at varying frequencies for positive V_{ss} biasing through PSA.

Table 6.2.2(b) Comparison table for noise results of preamplifier for positive PSA

Amplifier Output Noise Density (nV/Hz^1/2)			
Frequency	With noiseless power supply and Vss supplied directly	With noisy power supply and Vss supplied directly	With noisy power supply and PSA
0.1	3.375	28.491	92.172
1	1.266	28.319	9.605
10	0.791	28.301	1.697
100	0.726	28.300	1.290
1000	0.719	28.300	1.273

This table shows the comparison of the amplifier's output noise voltage densities at different frequencies and for different configurations. The output noise voltage densities were observed with the following configurations: V_{ss} supplied directly with noiseless supplies, V_{ss} supplied directly with noisy power supplies and finally with the noisy power supply and PSA. In case of noisy power supplies, we have supplied 20nV/√Hz noise voltage.

For frequency of 1kHz, noise density in case 1 is 0.719nV/√Hz. In case 2, it is about 28 nV/√Hz and finally with the designed PSA, it is 1.273nV/√Hz. For lower frequencies, we see an increase in output noise density.

Hence, the design for positive PSA ensures that the output noise varies on a miniscule level even after a huge change in V_{ss} noise.

6.2.3 Circuit design for negative PSA

Here, the output of PSA is given to V_{ss2} through an inverting configuration Op-Amp with unity gain. In order to avoid loading effect at V_{ss} while also maintaining very low noise characteristics, low pass RC filters were used in the Op-Amp configuration at the input and the feedback circuit (R_s, C4, R_f and C3). Refer Fig. 6.2.3 for circuit diagram.

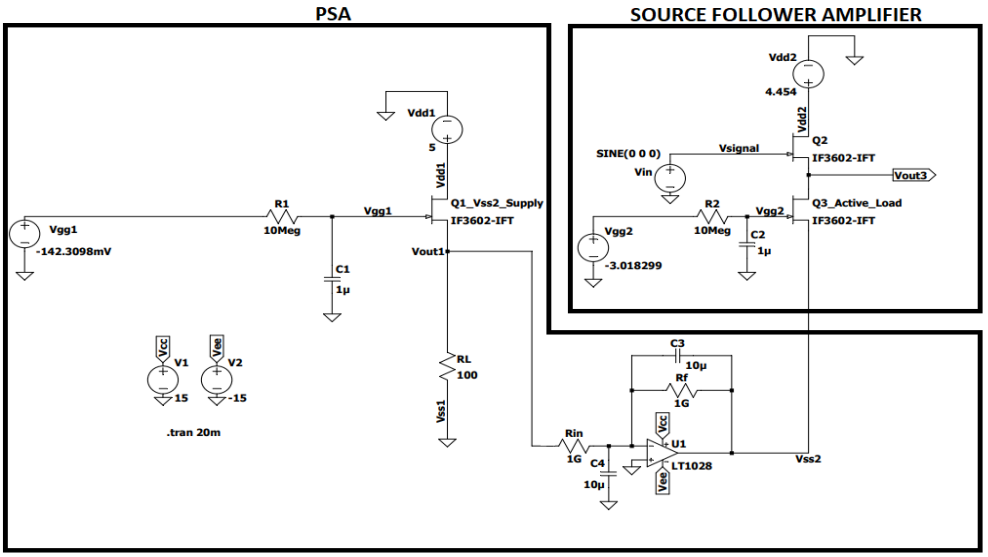

Fig. 6.2.3 Circuit diagram for negative PSA

Test results of negative PSA:

- Using LT1028 as inverting OpAmp: Gain of preamplifier: 0.9860077
- Without considering power supply noises: Output noise density at 1kHz: **1.8476816nV/√Hz**
- After considering 20nV/√Hz for each supply: Output noise density at 1kHz: **1.8476817nV/√Hz**

Fig. 6.2.3(a) Output noise test results of preamplifier for positive PSA

Frequency (Hz)	Output Noise Density (nV/Hz^1/2)	Frequency (Hz)	Output Noise Density (nV/Hz^1/2)
0.1	20384.9940	10	20.9034
0.2	7214.8892	20	7.7595
0.3	3999.7050	30	4.6609
0.4	2554.0983	40	3.3525
0.5	1826.9298	50	2.7601
0.6	1414.2030	60	2.4652
0.7	1128.8112	70	2.2801
0.8	904.5280	80	2.1469
0.9	775.1784	90	2.0841
1	645.8288	100	2.0212
2	229.0200	200	1.8827
3	127.2023	300	1.8627
4	81.4019	400	1.8554
5	58.3530	500	1.8522
6	45.2666	600	1.8506
7	36.2169	700	1.8495
8	29.1045	800	1.8486
9	25.0040	900	1.8481
10	20.9034	1000	1.8477

The above table shows the output noise density as observed at the output of the preamplifier at varying frequencies for negative V_{ss} biasing through PSA.

Hence, the design for negative PSA ensures that the output noise varies on a miniscule level even after a huge change in V_{ss} noise.

Table 6.2.3(b) Comparison table for noise results of preamplifier for negative PSA

Amplifier Output Noise Density (nV/Hz^1/2)			
Frequency	With noiseless power supply and Vss supplied directly	With noisy power supply and Vss supplied directly	With noisy power supply and PSA
0.1	3.371	28.489	20384.994
1	1.265	28.317	645.829
10	0.790	28.300	20.903
100	0.726	28.298	2.021
1000	0.719	28.298	1.848

This table shows the comparison of the amplifier's output noise voltage densities at different frequencies and for different configurations. In case of noisy power supplies, we have supplied 20nV/√Hz noise voltage.

For frequency of 1kHz, noise density in the case 1 is 0.719nV/√Hz. In case 2, it is about 28 nV/√Hz and finally with the designed PSA, it is 1.273nV/√Hz. For lower frequencies, we see an increase in output noise density.

This makes a good proof of concept that at least the power supply noises are not affecting the output noise voltage density

6.3 Inference

From Chapter 6.1, the noise from V_{gg} and its impact made on the output noise voltage density is reduced by implementing an RC filter at the gate terminal of the preamplifier.

From Chapter 6.2, the noise from V_{ss} and its impact made on the output noise voltage density is reduced by implementing a PSA (Power Supply Amplifier) circuit to generate a low noise power supply which can be used to power V_{ss} on the original preamplifier. This PSA is divided into two different sub-circuits based on the bias point we need our preamplifier to run at. For positive V_{ss2}, we have a buffer-based PSA and for a negative V_{ss2}, we have an inverting configuration based PSA.

Conclusion

A DC power supply with very low noise characteristics (<2nV/√Hz) was designed for the source follower preamplifier [4] to be used in the NDBD project [1]. Most of the commercially available general purpose DC power supplies have high voltage noise density (>10nV/√Hz), which is not good enough for the operation of the low noise preamplifier. Hence, this power supply would prove to be a very good alternative to get low noise operation on the bolometer detector.

According to the analytical noise model of a source follower preamplifier, noise from V_{gg} and V_{ss} power supplies are the major source of output noise voltage density. To reduce this, a low pass RC filter was designed to reduce the effect of V_{gg} noise on the output noise. This solution reduced the effect of gate noise on the output noise from 10nV√Hz to below 3nV/√Hz. To reduce the noise from V_{ss}, a low noise power supply was designed and simulated. Simulated results show that the output noise density of the preamplifier was reduced to 1.848nV/√Hz and 1.272nV/√Hz for negative and positive V_{ss} bias respectively at 1kHz. Simulated results show that this output noise voltage density remains constant for varying input noise from 0V/√Hz to 50nV/√Hz.

This setup will be able to operate at 120K, which can be used in series with the RTD sensor placed at 10mK in the dilution refrigerator at the NDBD lab, TIFR.

The internship at TIFR has given us plenty of experiences in terms of design approach and documentation. Our data was documented in tables which were made on Google Sheets[15] to improve collaborative work experience and to include version control in our project work [6]. Maintaining a proper log of our multiple changes, readings and findings on our Trello[16] board helped us a lot. In the end, we were able to complete all the theoretical design processes which were required by TIFR for designing a preamplifier with very low noise characteristics.

[15] "Google Sheets: Sign-in." https://docs.google.com/spreadsheets/. Accessed 7 May. 2021.
[16] "Trello." https://trello.com/en-GB. Accessed 7 May. 2021.

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