Kaipeng Wang

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EDUCATION

University of Electronic Science and Technology of China(UESTC), Chengdu, Sichuan Province 2022.9~Present
Bachelor program in Integrated Circuits and Integrated Systems
GPA: 3.99/4.00
Average Score: 91.32
Interests: Data converters ; Analog and mixed-signal CMOS integrated circuits; RF Transceiver
Course work: Signals and Systems (98), Circuit Analysis and Electronic Circuits(98), Pinciple of Communication(93)

WORK EXPERIENCE

Research Assistant, *UESTC*, Chengdu, China 2023.6~Present

Supervisor: Prof. Jiaxin Liu (https://scholar.google.com.hk/citations?user=CE7PYu4AAAAJ&hl=zh-CN)

Research Focus: Analog and mixed-signal circuits, with emphasize on analog-to-digital converters(ADCs)

Details: Under the supervision of Prof. Jiaxin Liu, I am exposed to the state-of-the-art ADC designs,including ZOOM ADC,noise-shaping SAR ADC and high speed SAR ADC. I learned the full procedure of ADC design, from MATLAB simulation, pre-layout simulation, layout drawing, post-layout simulation to chip testing.

PROJECT EXPERIENCE

A 28nm SAR ADC with improved kT/C noise cancellation(tapeout), *Research Assistant* Chengdu, Sichuan Province 2024.4~2024.9

- Chip Performance: SNDR ≥ 75 dB, BW=100MHz, Power ≤ 1.56mW
- Description: I conducted this ADC research. As there is an inherent linearity threat in the typical kT/C noise cancellation architecture, in this chip, a novel kT/C noise cancellation architecture was used to deal with the linearity problem.This technique eliminates the frequency limitation of the input signal and enhances the signal-to-noise ratio (SNR), increasing the signal frequency from 20 MHz to 100 MHz. To reduce the DAC switching power,a Detect-and-Skip operation was implemented in this chip.

A Current Reference in 0.18μm CMOS (pre-layout simulation), *course project* *Chengdu, Sichuan Province* 2024.9~2024.10

- Performance: Temperature Coefficient ≤ 29.1 ppm/℃, Line Sensitivity ≤ 0.43%/V, Establishment Time ≤ 0.92us
  PSRR of Voltage Reference: 85.5dB@dc,-55.8dB@1kHz
- Description: I conducted this project. The design incorporates key elements like current mirrors, start-up circuits, and operational trans-conductance amplifiers (OTA), ensuring high precision, low temperature coefficient, and effective power supply rejection.

Electronics Design in Communication field (skills training), *student member* Chengdu, Sichuan Province 2023.4~Present

- Work: High efficiency circuit boards design and debug of prototype machines; implementation of circuit boards for modulation and demodulation; PCB design under high-frequency (DDS, PLL, etc.).
- Projects: Wireless transmission system modeling; development of multi-channel adaptive wireless receivers; implementation of signal recovery and demodulation devices.
- Awards: Won awards in the National Undergraduate Electronics Design Contest,which is widely known as TI CUP, in the communication field in both 2023 and 2024, achieving the highest regional score in Sichuan in 2024.

PUBLICATIONS

- Gu, Y., **Wang, K.**, Yi, T., Chen, X., Yang, S. and Liu, J. (2024), An improved kT/C noise cancellation technique with presampling for high-speed SAR ADCs. Electron. Lett.

AWARDS AND SCHOLARSHIPS

FIRST PRIZE SCHOLARSHIP(top 10%), UESTC *2022~2023*
SECOND PRIZE SCHOLARSHIP(top 15%), UESTC *2023~2024*