Transistors

COMP311 Connor McMahon

Announcements

- Homework 0 due tomorrow
- Lab 0 released tomorrow, due next Thursday

Arithmetic vs Logical Shifting

sizeof(int) = 4 bytes

```c
unsigned int x3 = (unsigned int) -5;
printf("x3 >> 1 = 0x%x\n", x3 >> 1);
```

Arithmetic vs Logical Shifting

sizeof(int) = 4 bytes

```c
unsigned int x3 = (unsigned int) -5;
printf("x3 >> 1 = 0x%x\n", x3 >> 1);
```

This is a 32-bit number because its type is unsigned int

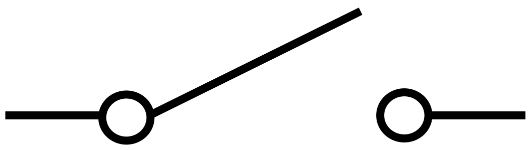
-5 in binary is $1...1011_2$

$1...1011_2$ >> 1 = $0111...1101_2$ = 0x7FFFFFFD

A logical shift was performed because this number is an **unsigned** int

Transistors are like switches

Off

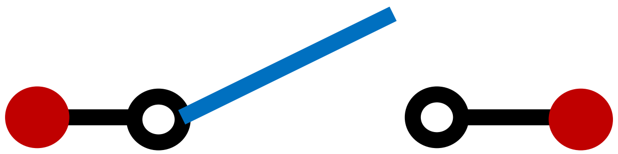


On

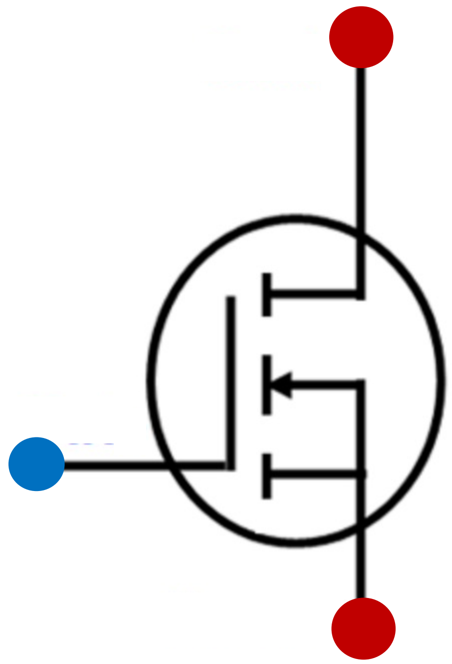
Switches are controlled by physical contact

Transistors are controlled by a **voltage**

Transistor Symbol

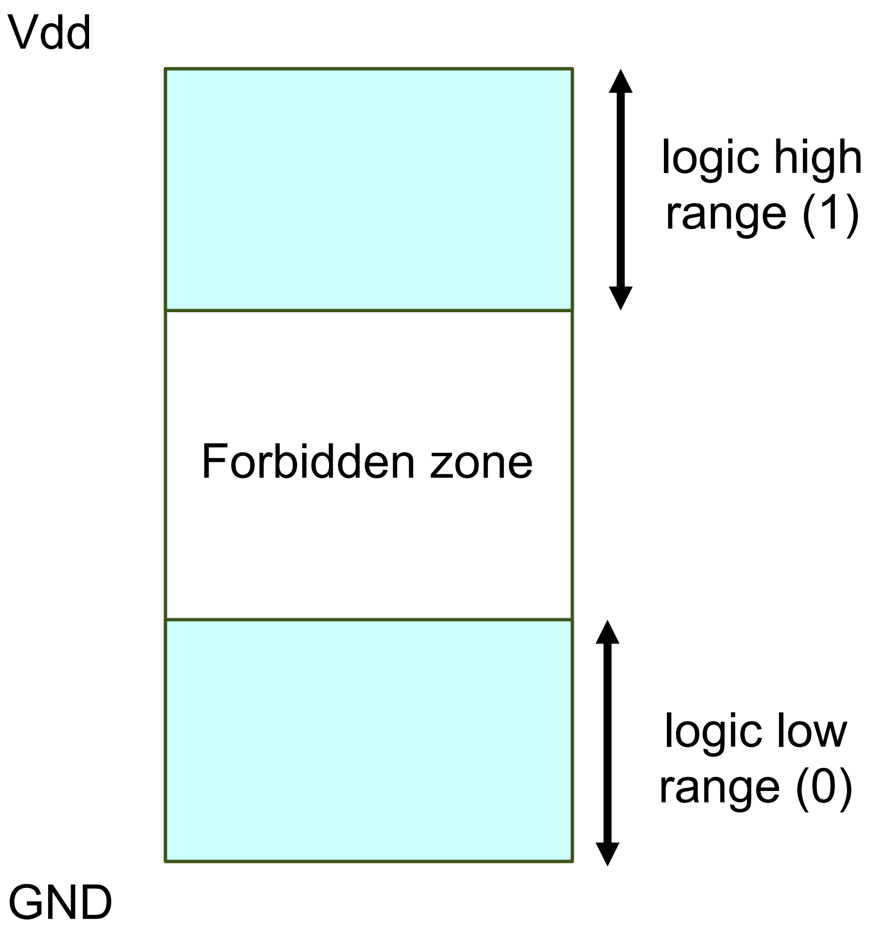


Switch



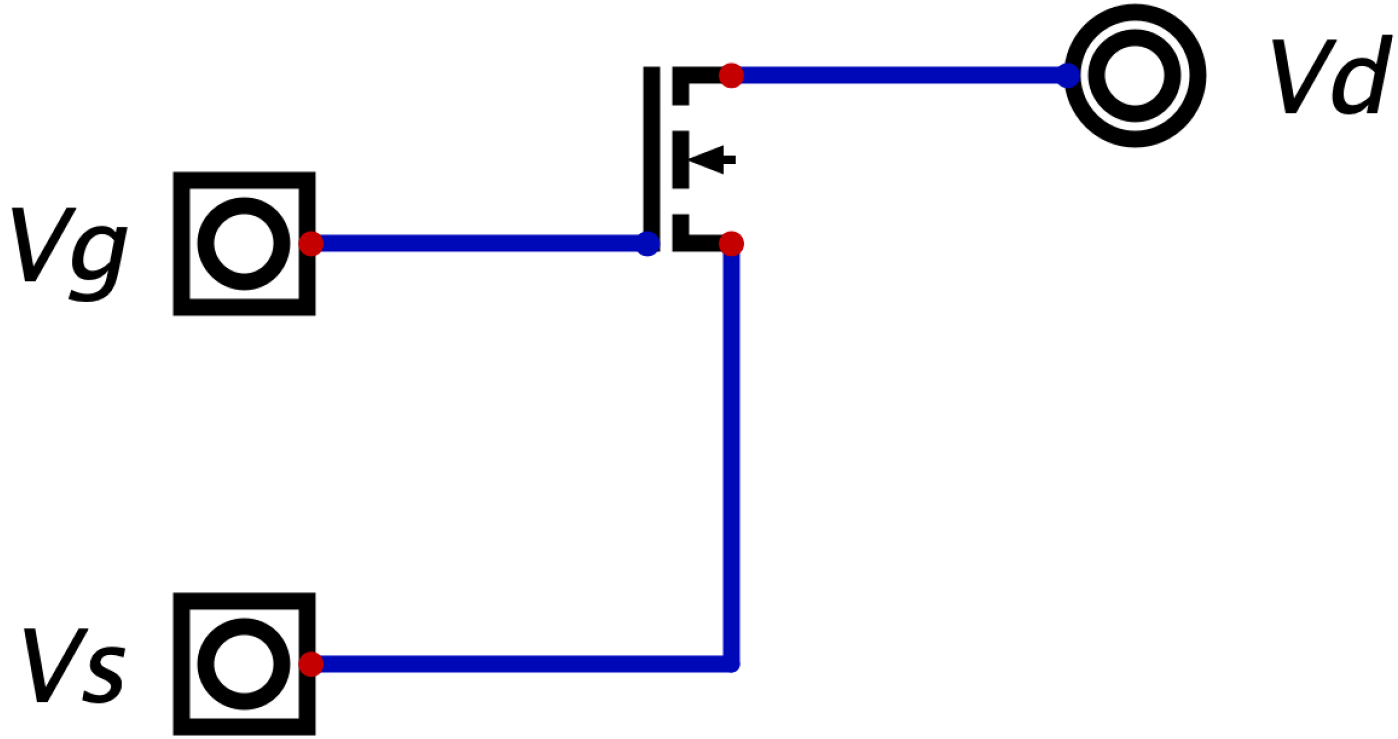
Transistor
(n-channel MOSFET)

Logic Levels



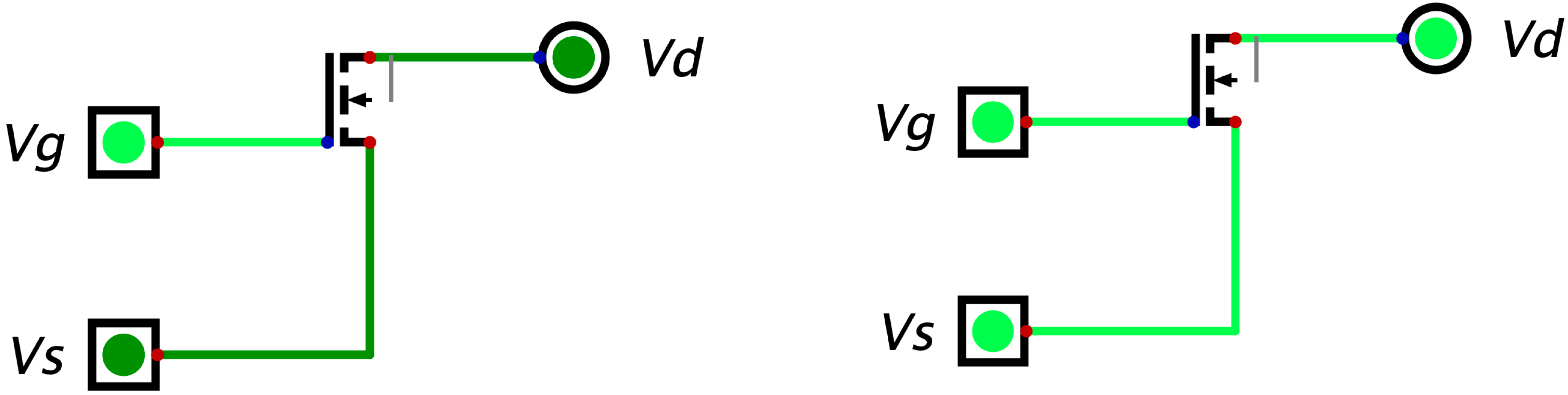
The exact voltage ranges are determined by the characteristics of the transistor

NMOS Transistor



NMOS Transistor in “on” state

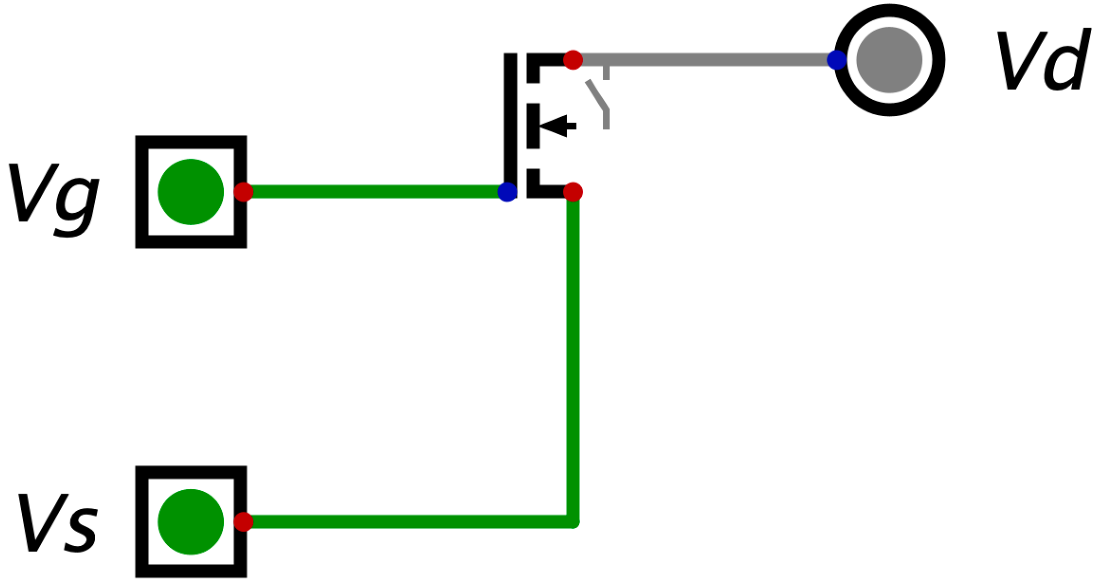
Dark green = Logic 0
Light green = Logic 1

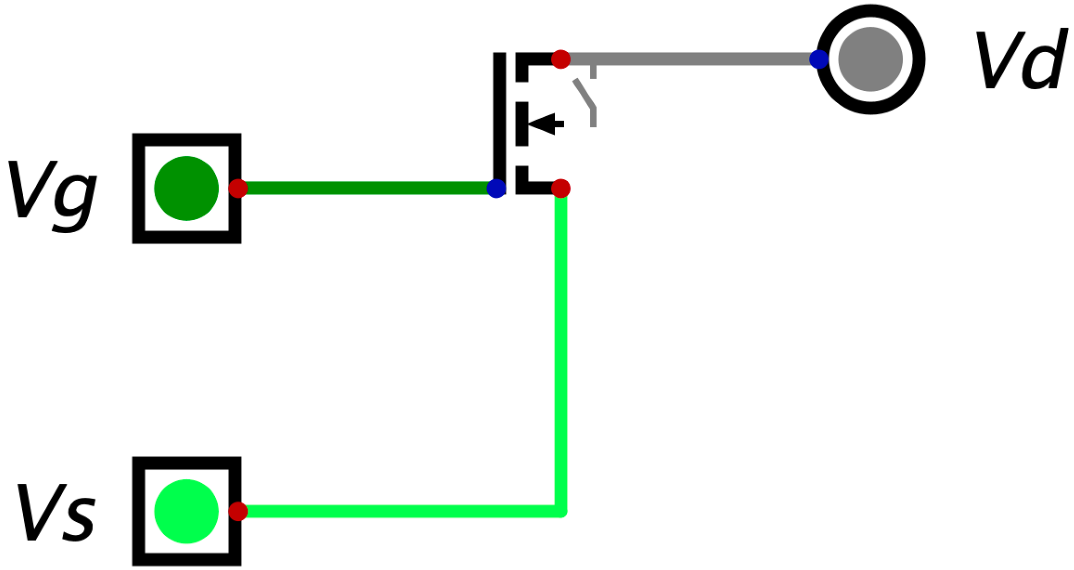


Current **can** flow between the source and drain terminals because **Vg is high**

NMOS Transistor in “off” state

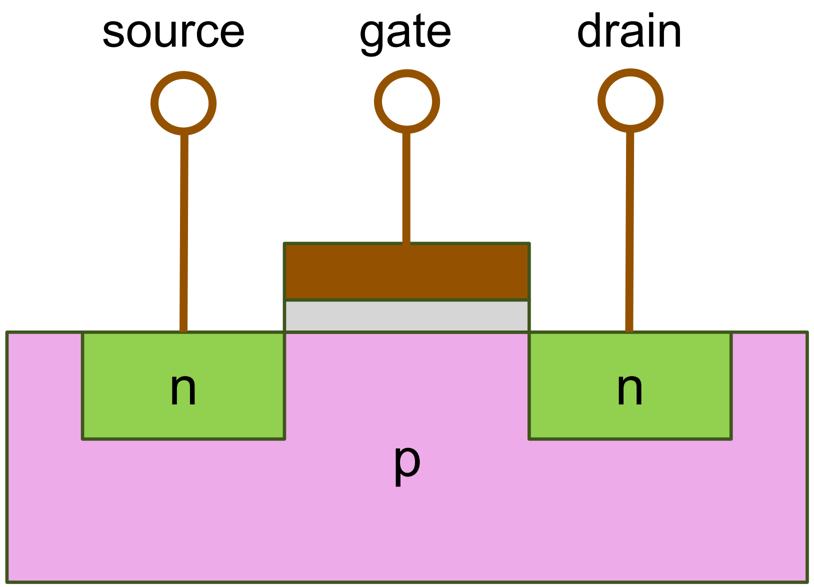
Dark green = Logic 0
Light green = Logic 1



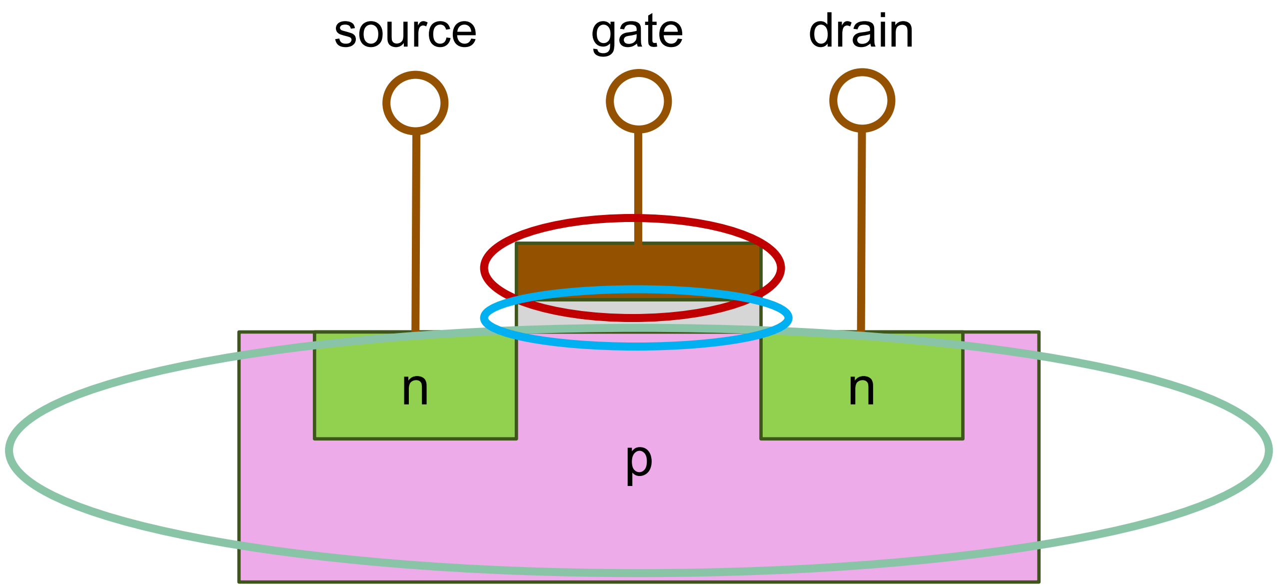


Current **cannot** flow between the source and drain terminals because **Vg is low**

n-channel Metal-Oxide-Semiconductor-Field-Effect Transistor (MOSFET)



n-channel Metal-Oxide-Semiconductor-Field-Effect Transistor (MOSFET)



Metal

material with high electrical conductivity

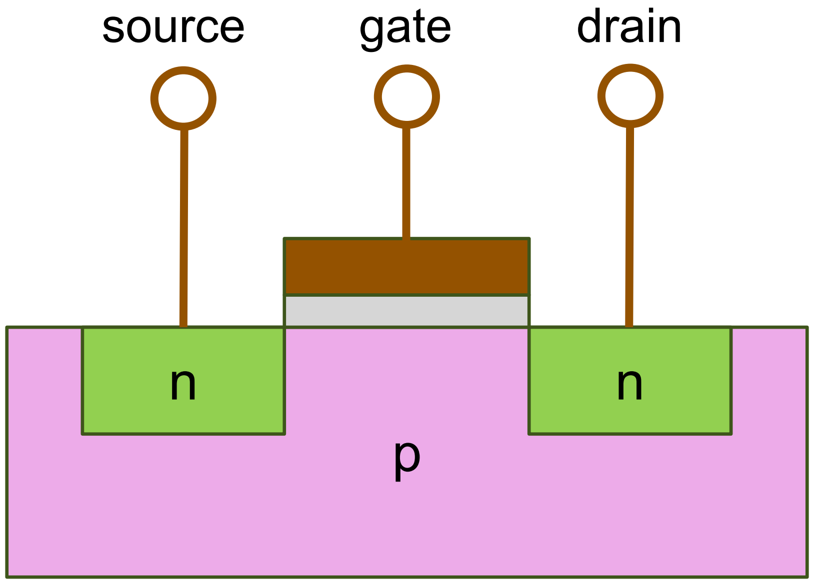
Oxide

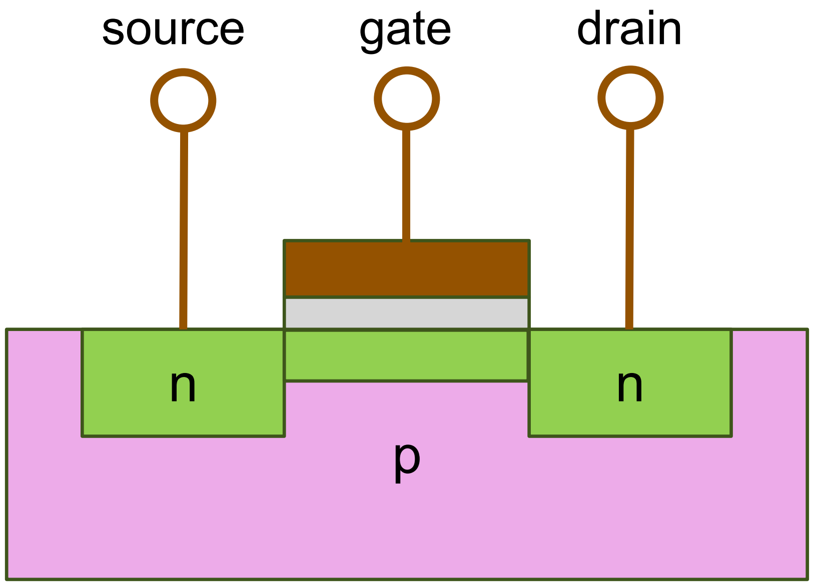
insulates the semiconductor from the metal layer, forming a capacitor structure

Semiconductor

a material with an electrical conductivity between an insulator and conductor

n-channel MOSFET (nMOS)

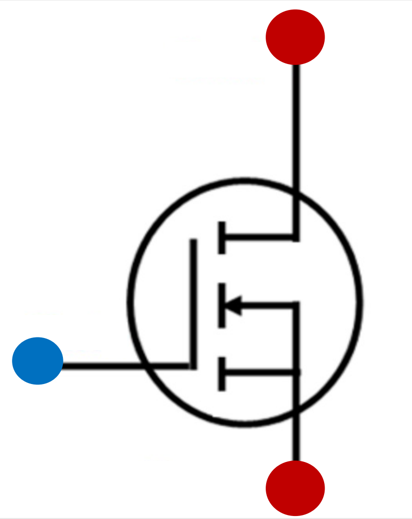




Vg (gate voltage) = logic low
current cannot flow between source and drain

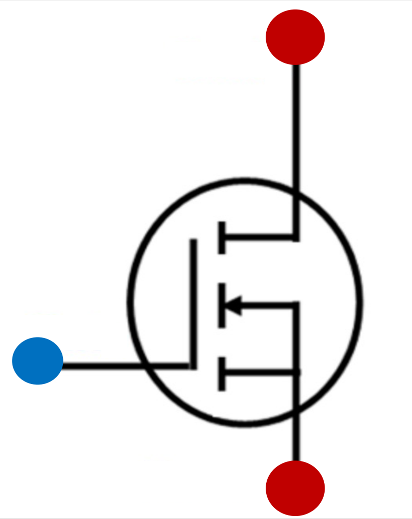
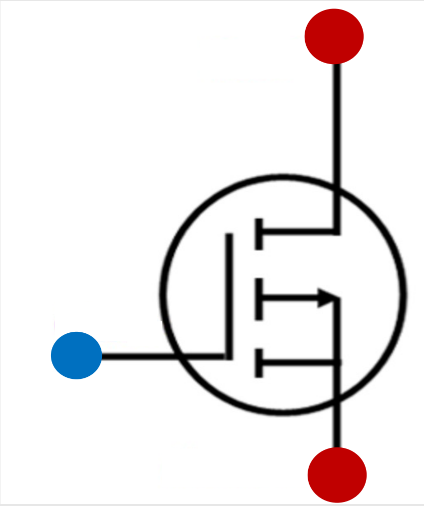
Vg (gate voltage) = logic high
current can flow between source and drain

Two Types of Transistors

	nMOS	pMOS
		
Behaves as an open switch when	Vg is low	
Behaves as a closed switch when	Vg is high	

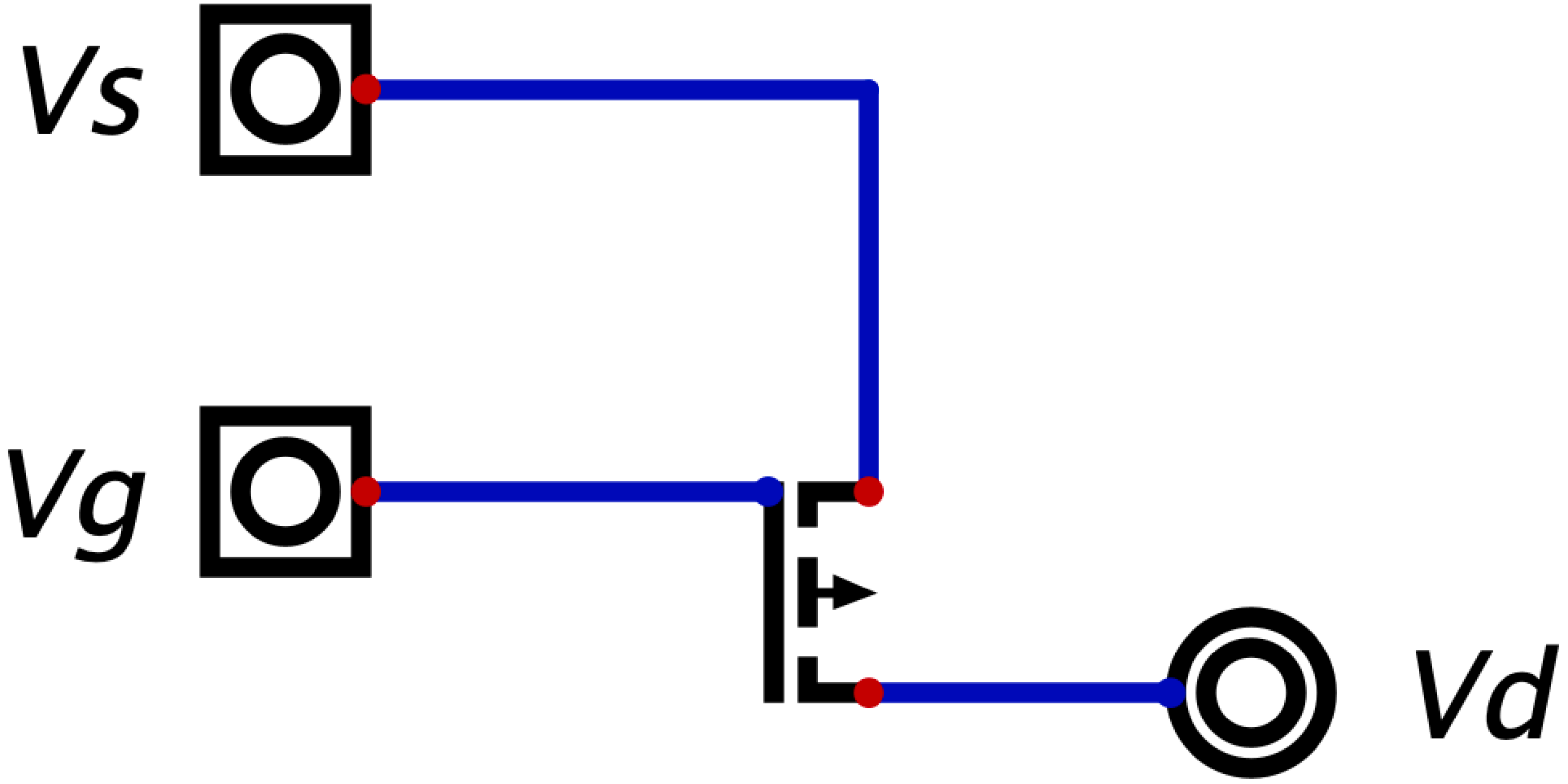
Vg is the gate voltage (voltage on the blue terminal)

Two Types of Transistors

	nMOS	pMOS
		
Behaves as an open switch when	Vg is low	Vg is high
Behaves as a closed switch when	Vg is high	Vg is low

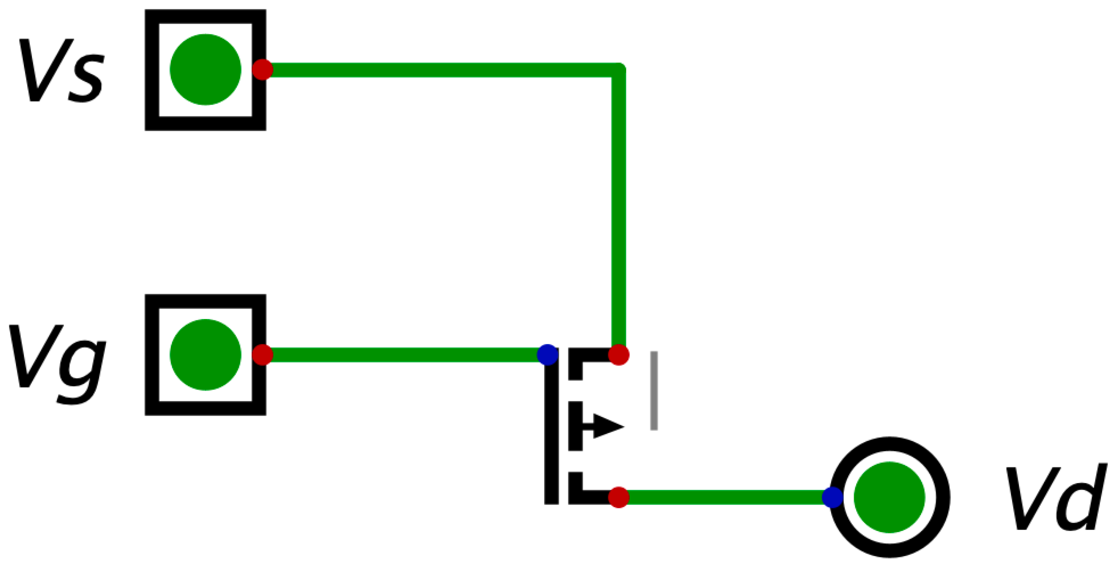
Vg is the voltage on the blue terminal

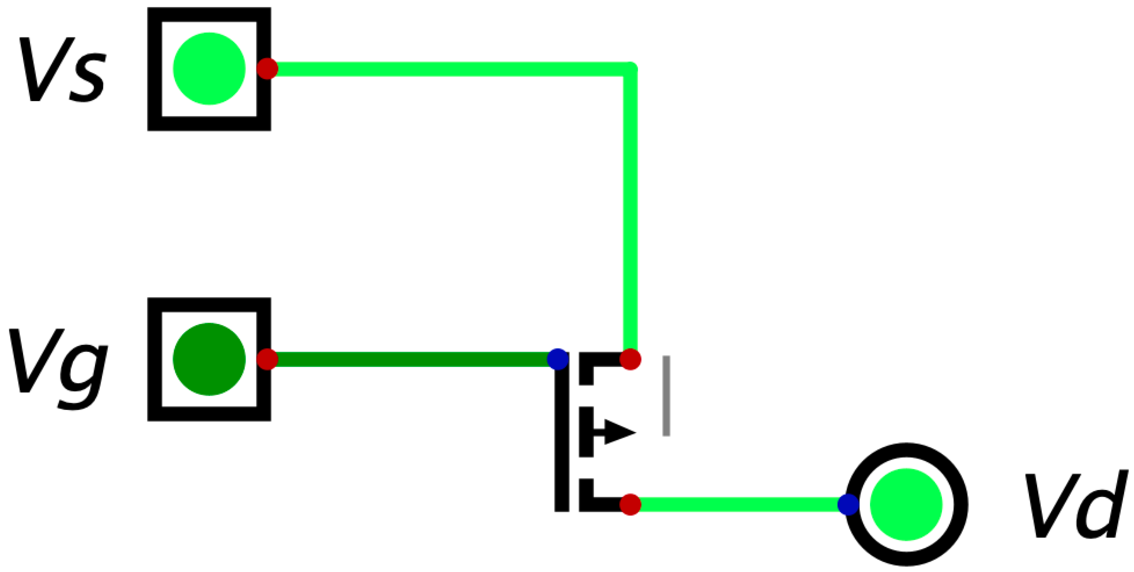
PMOS Transistor



PMOS Transistor in “on” state

Dark green = Logic 0
Light green = Logic 1

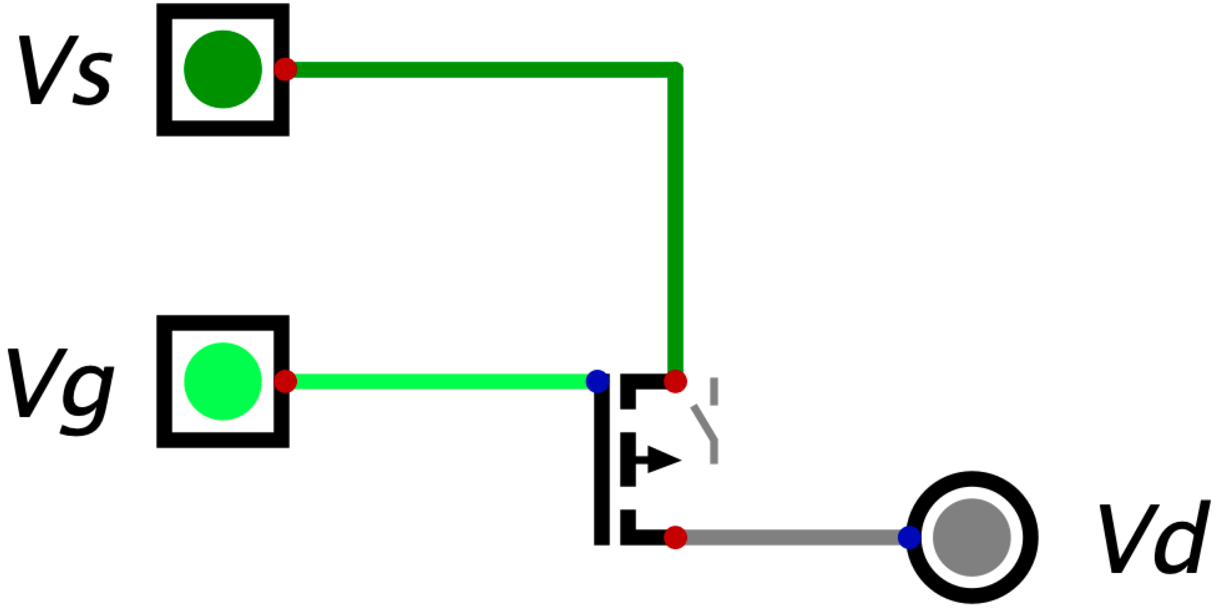


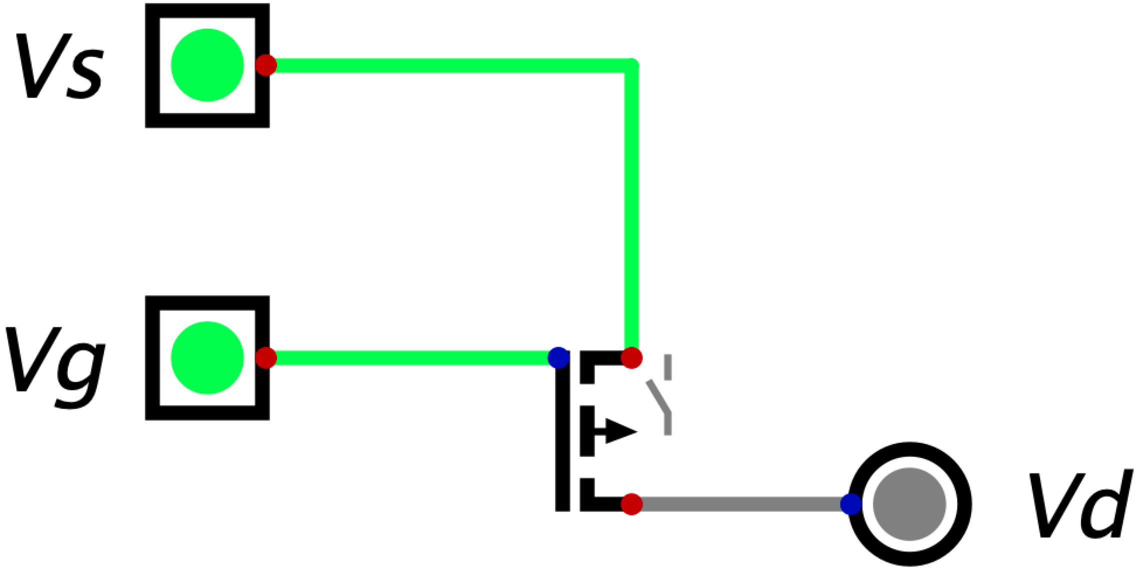


Current **can** flow between the source and drain terminals because **Vg is low**

PMOS Transistor in “off” state

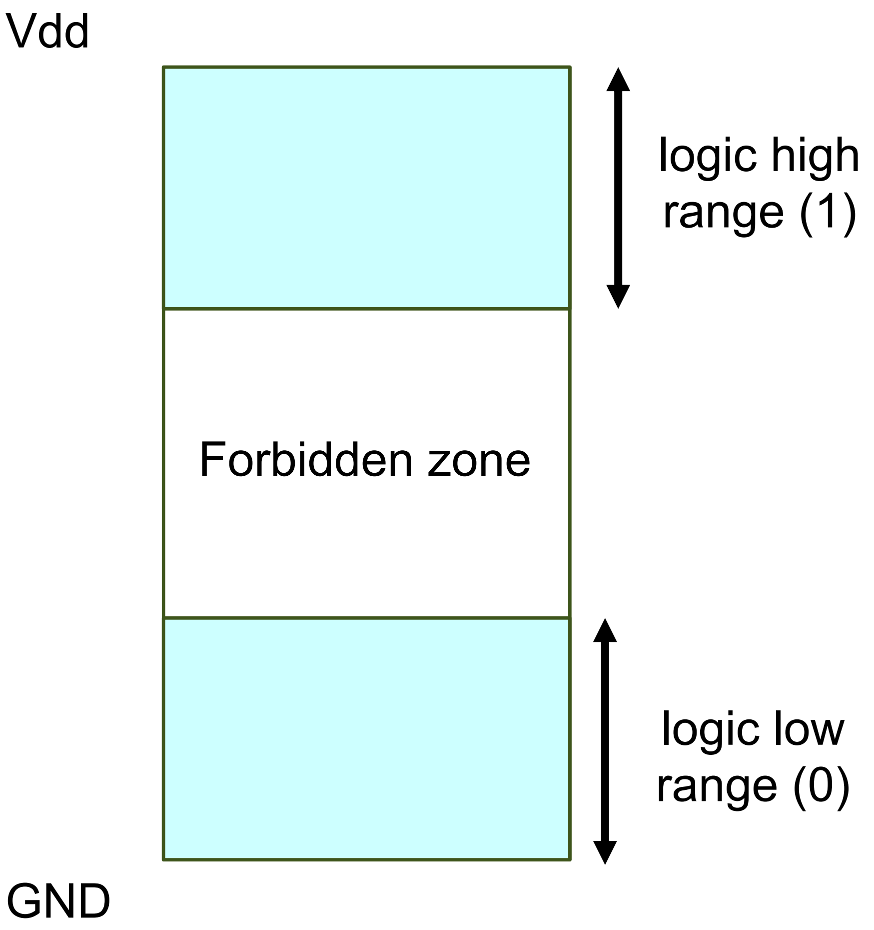
Dark green = Logic 0
Light green = Logic 1





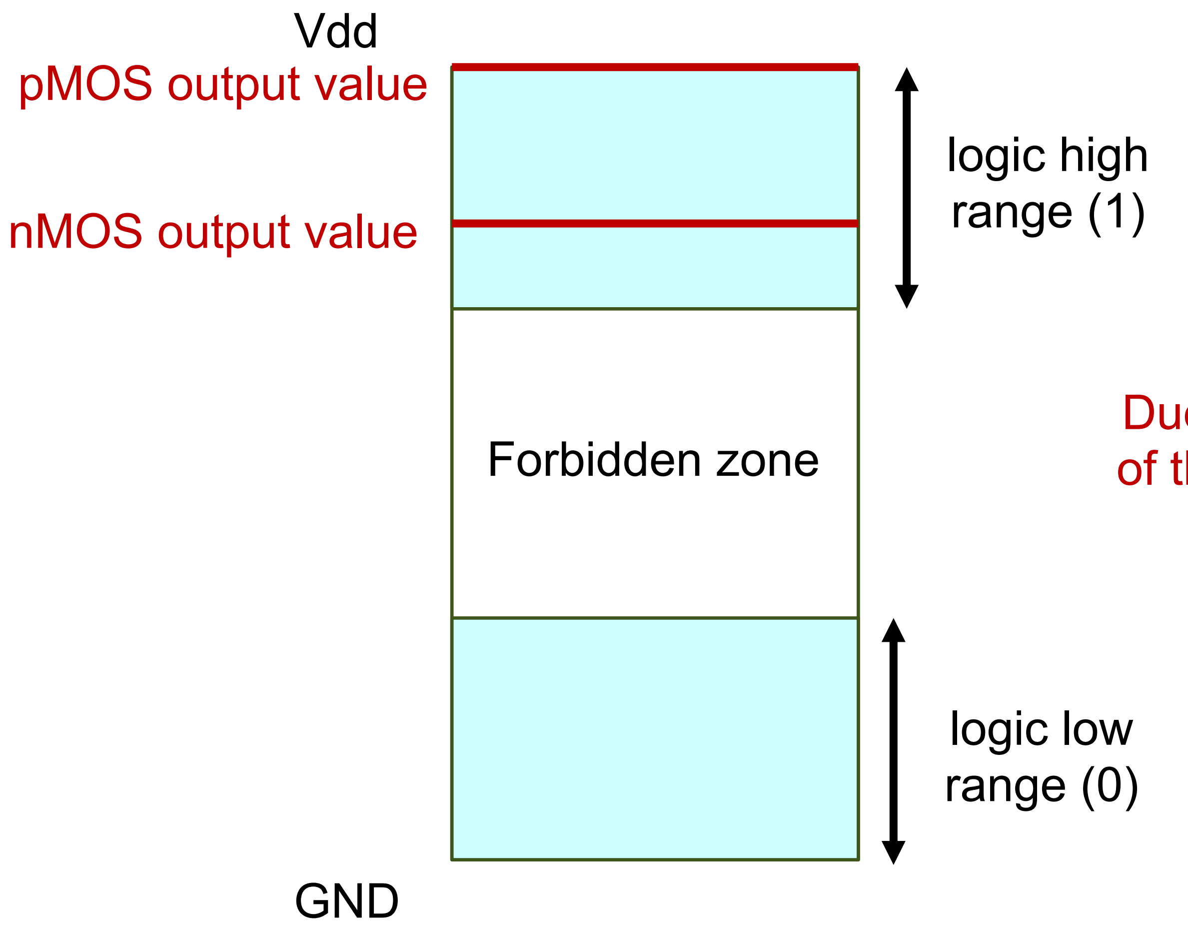
Current **cannot** flow between the source and drain terminals because **Vg is high**

Recall: Logic Levels



The exact voltage ranges are determined by the characteristics of the transistor

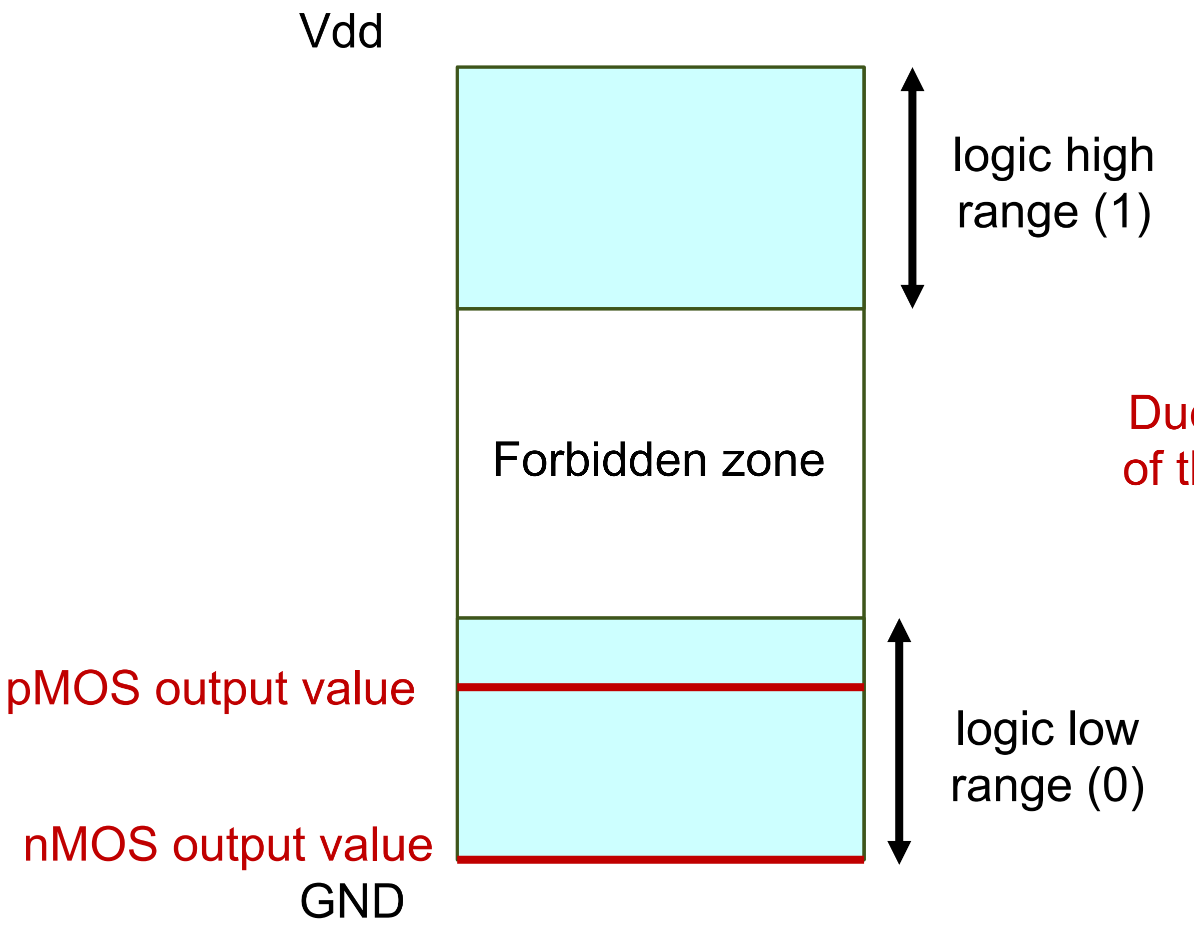
Comparing Logic High Outputs



Due to the physical characteristics of the nMOS transistor, it outputs a voltage lower than Vdd

The exact voltage ranges are determined by the characteristics of the transistor

Comparing Logic Low Outputs

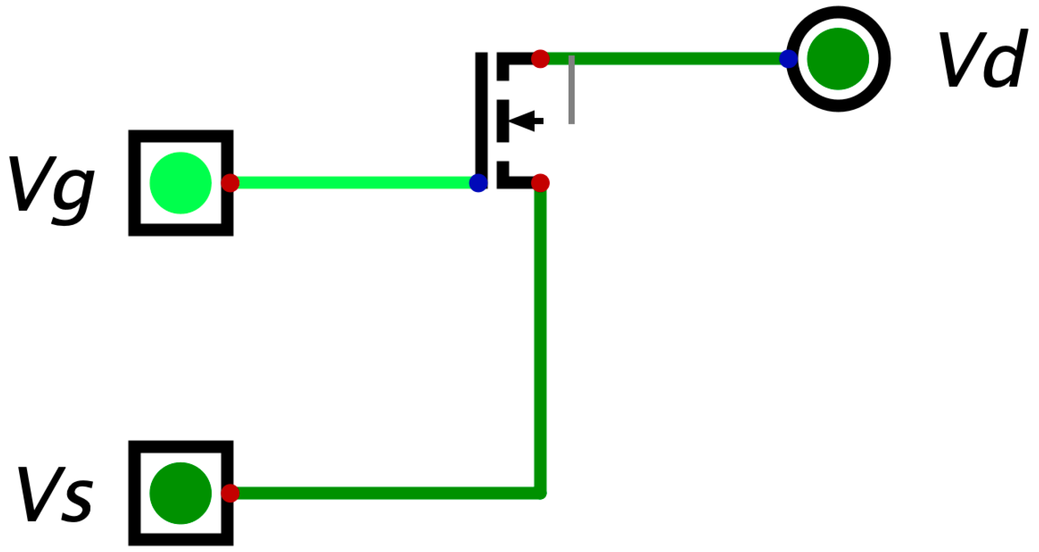


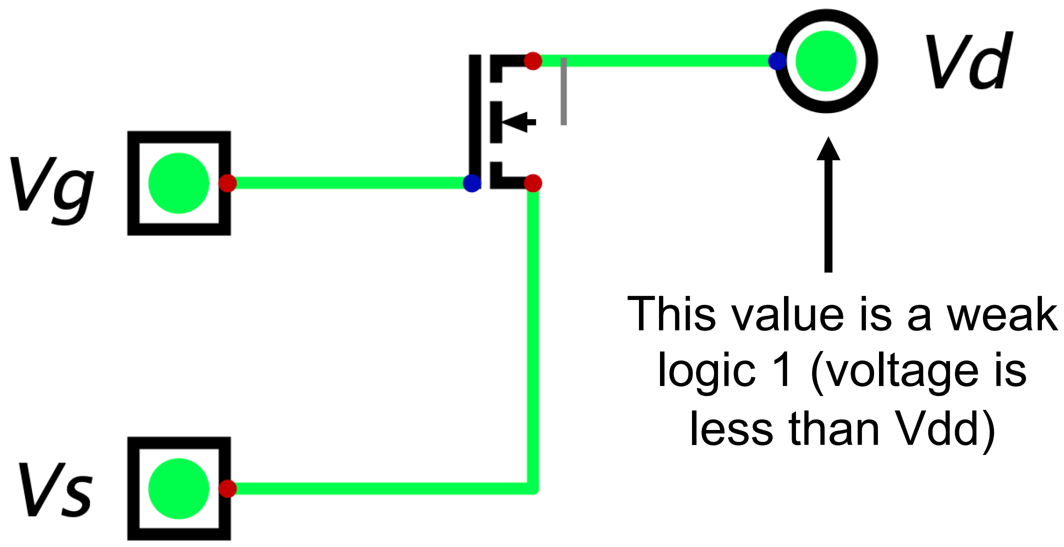
Due to the physical characteristics of the pMOS transistor, it outputs a voltage higher than ground

The exact voltage ranges are determined by the characteristics of the transistor

NMOS Transistor in “on” state

Dark green = Logic 0
Light green = Logic 1

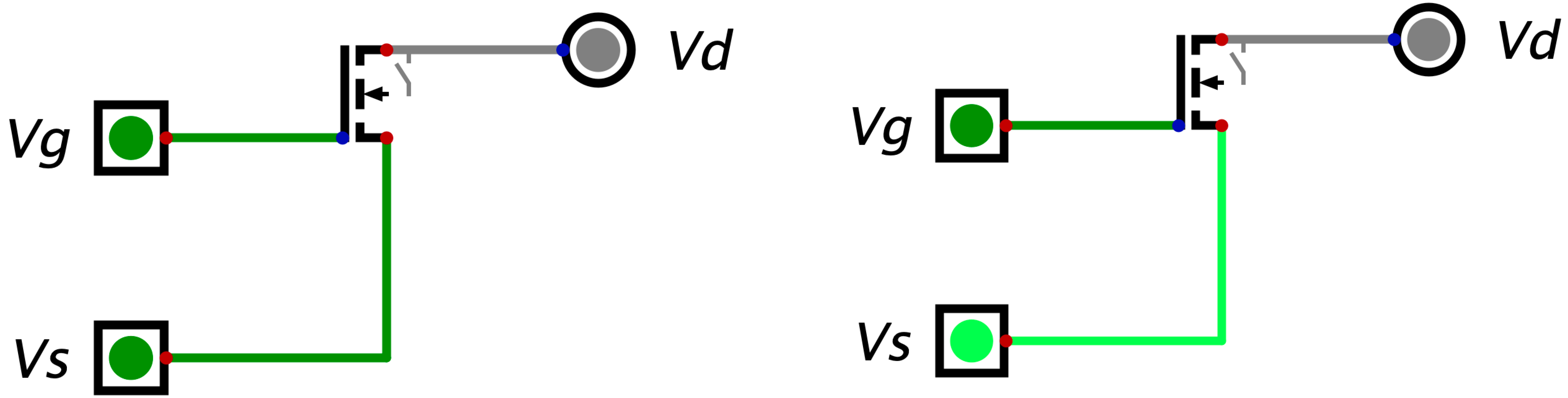




Current **can** flow between the source and drain terminals because **Vg is high**

NMOS Transistor in “off” state

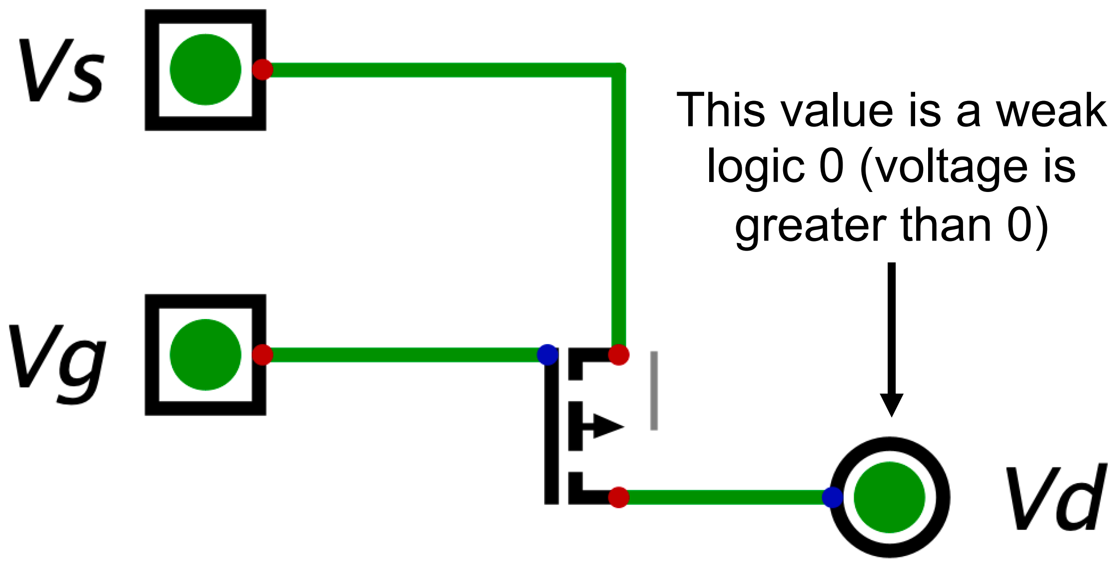
Dark green = Logic 0
Light green = Logic 1

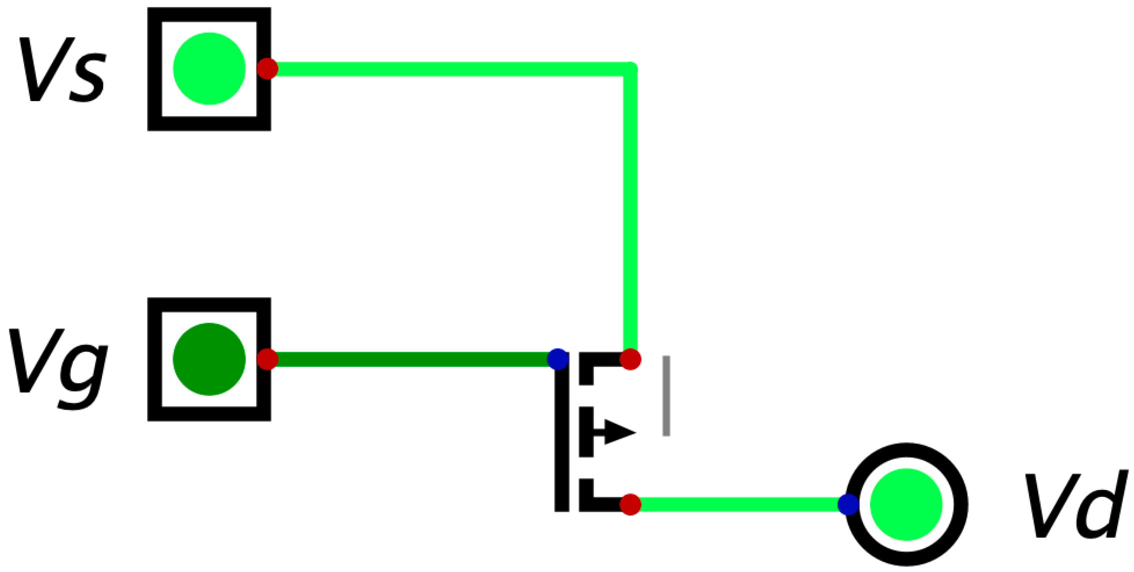


Current **cannot** flow between the source and drain terminals because **Vg is low**

PMOS Transistor in “on” state

Dark green = Logic 0
Light green = Logic 1





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PMOS Transistor in “off” state

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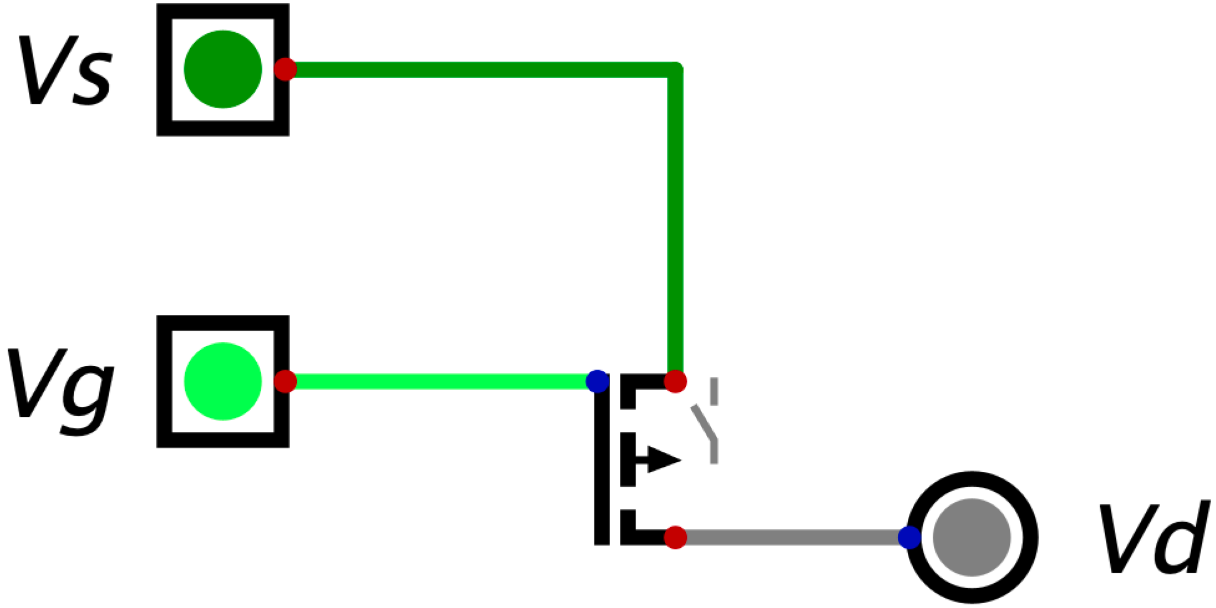
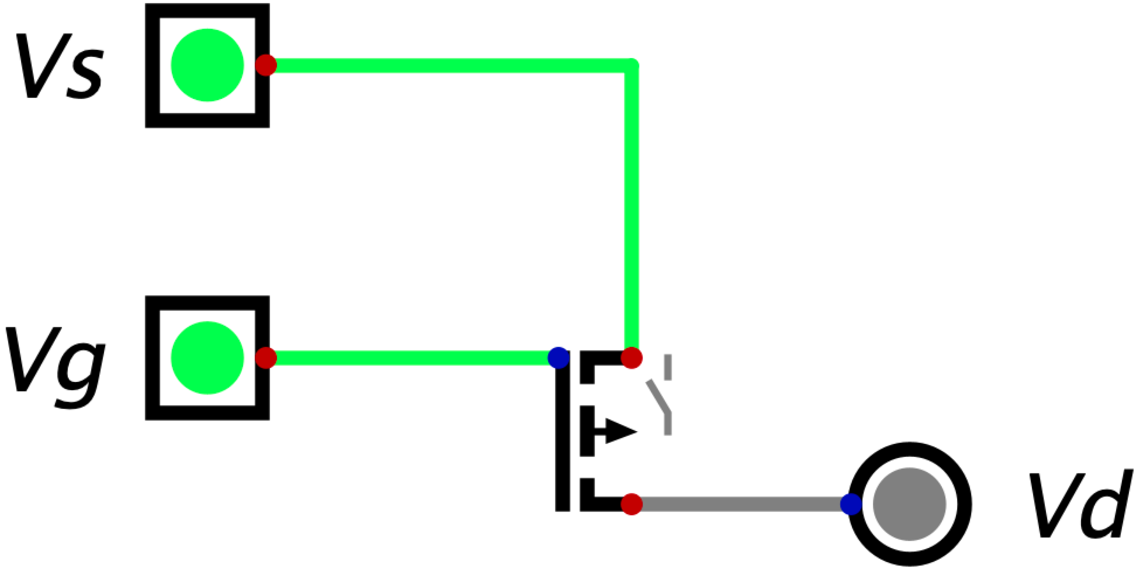




Current **cannot** flow between the source and drain terminals because **Vg is high**

nMOS vs pMOS

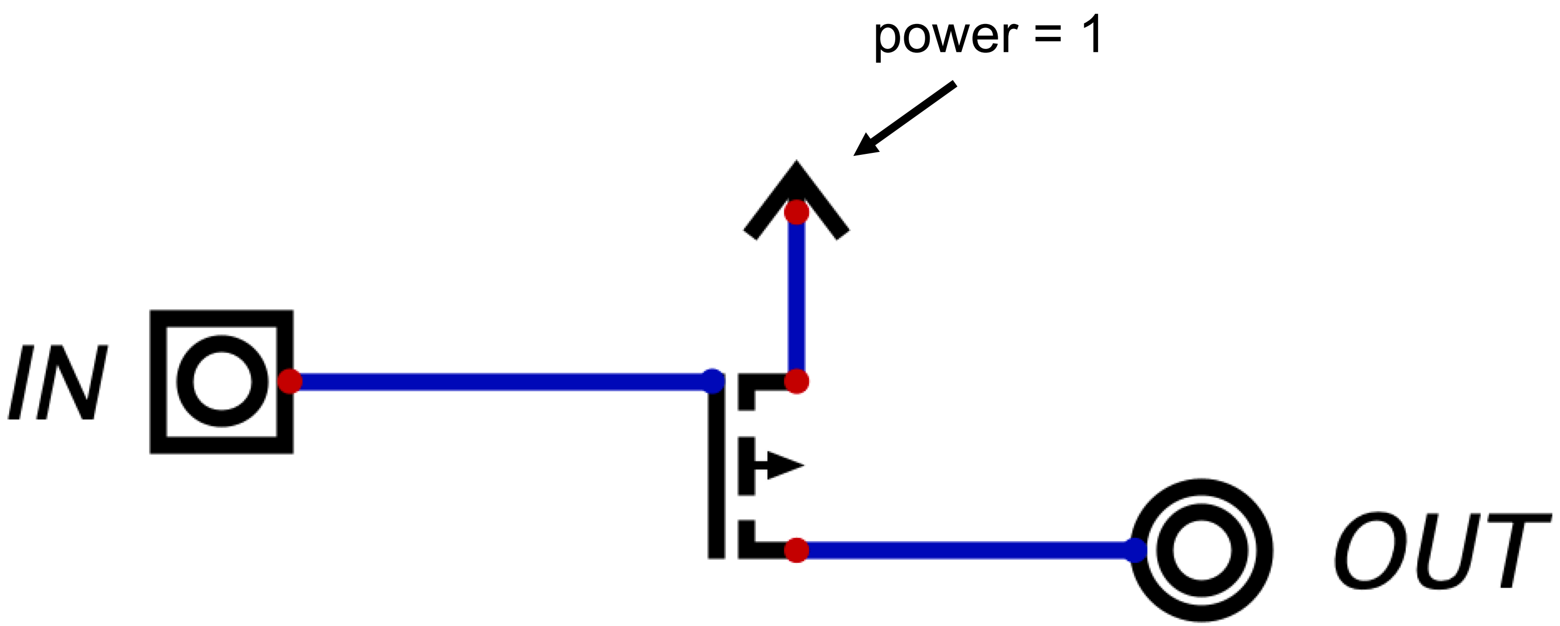
Characteristic	nMOS	pMOS
Vg = 1	on	off
Vg = 0	off	on
Which signal is passed well	low	high
Symbol	arrow facing in	arrow facing out

Designing An Inverter

- I want to design a circuit that takes as an input a one-bit value and outputs the complement of that number.
    - Input = 0, Output = 1
    - Input = 1, Output = 0
- I want to avoid having weak outputs.

Designing An Inverter

We will use a PMOS transistor to drive the output when the input is 0.



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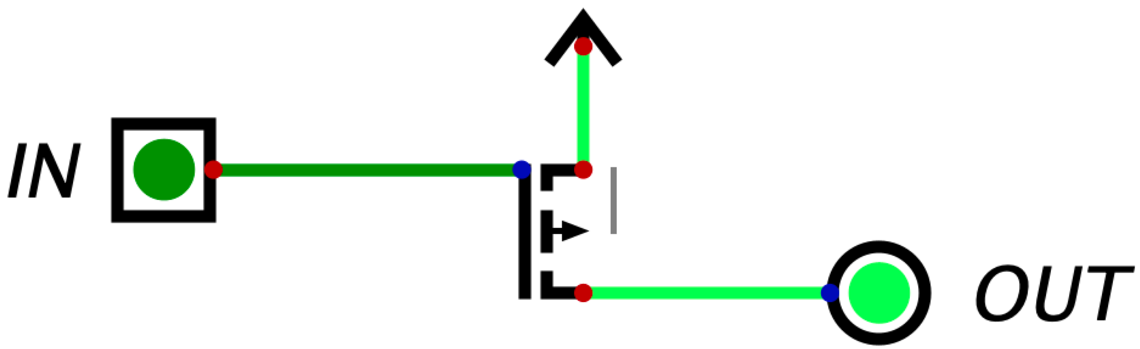
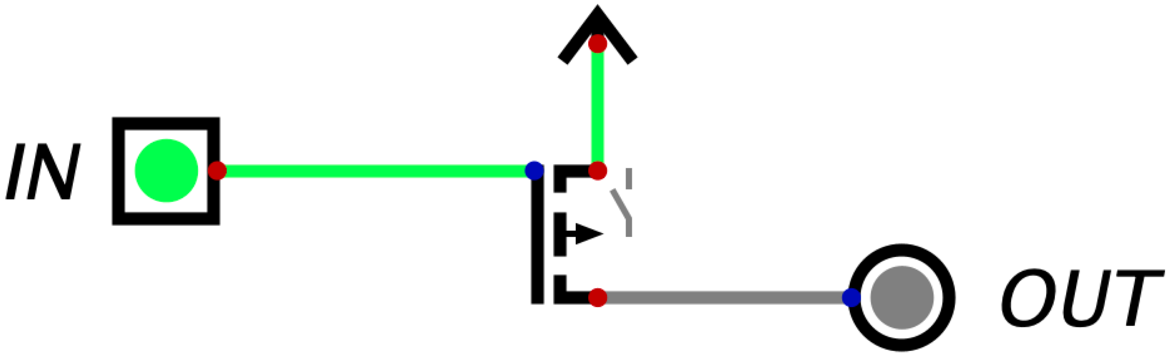


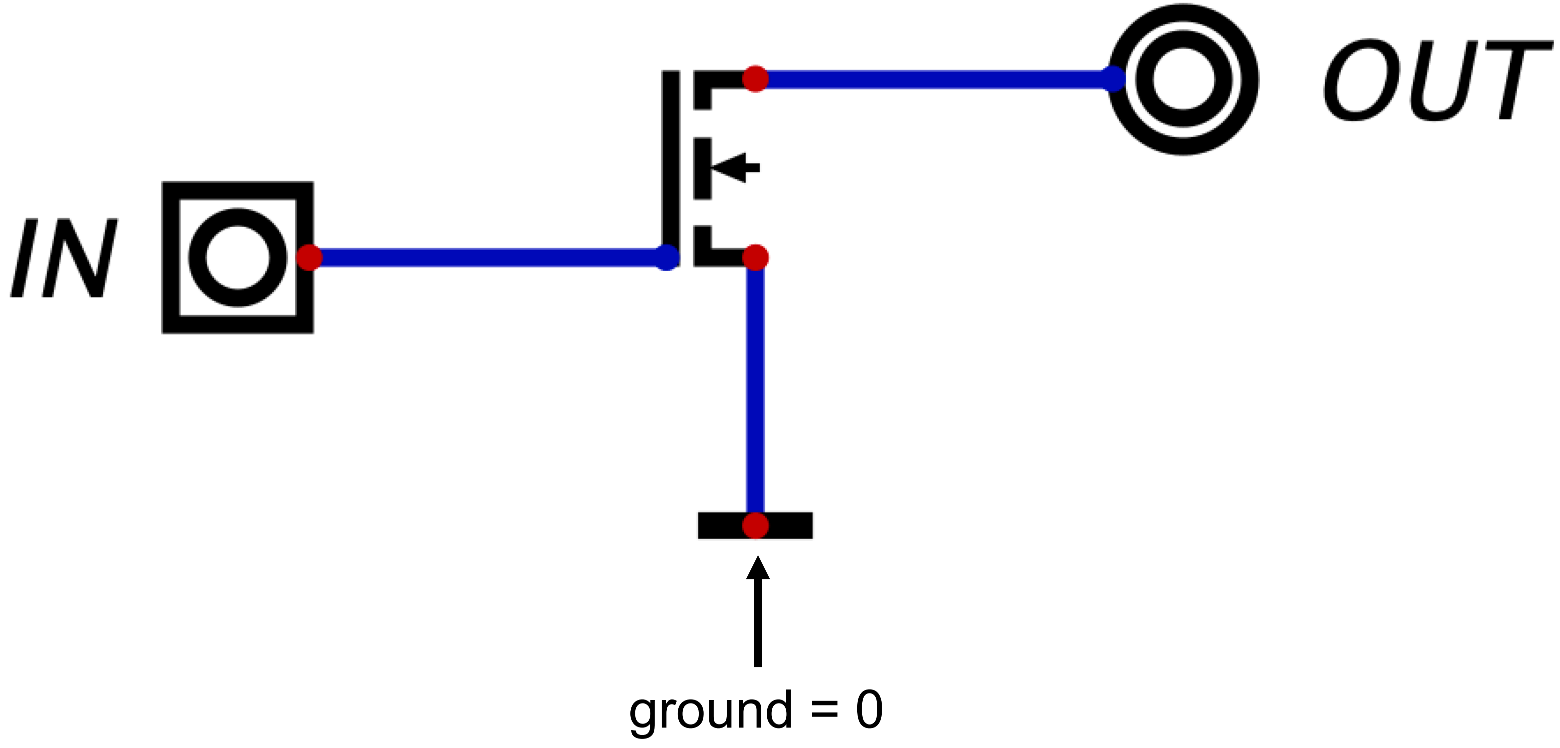
When the input is 0, the output is 1



When the input is 1, the output is not connected

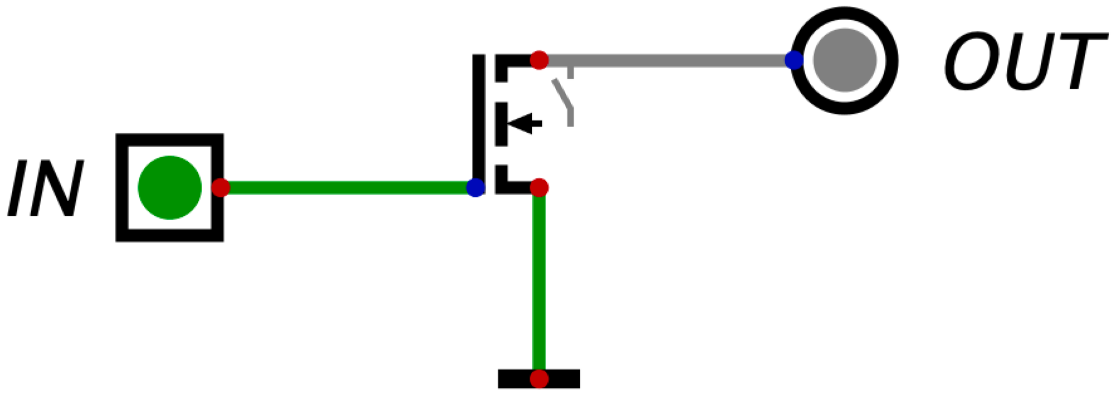
Designing An Inverter

We will use an NMOS transistor to drive the output when the input is 1.

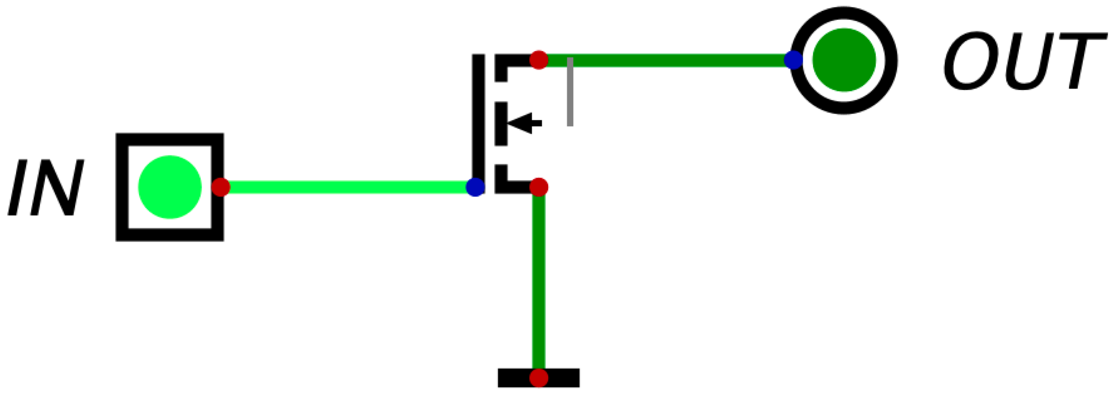


Designing An Inverter

We will use an NMOS transistor to drive the output when the input is 1.



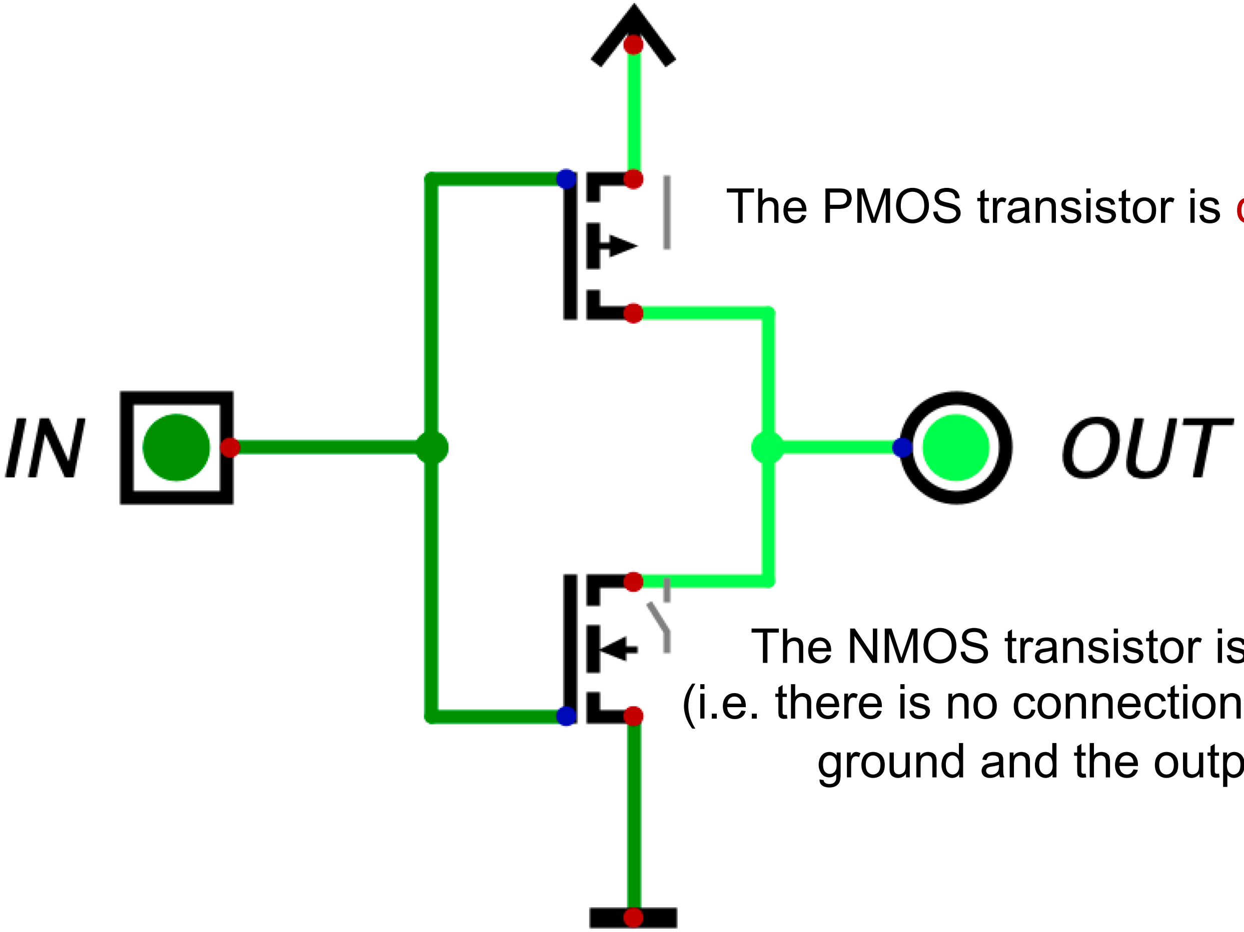
When the input is 0, the output is not connected



When the input is 1, the output is 0

CMOS (Complementary Metal Oxide Semiconductor) Inverter

When the input is 0, power is connected to the output

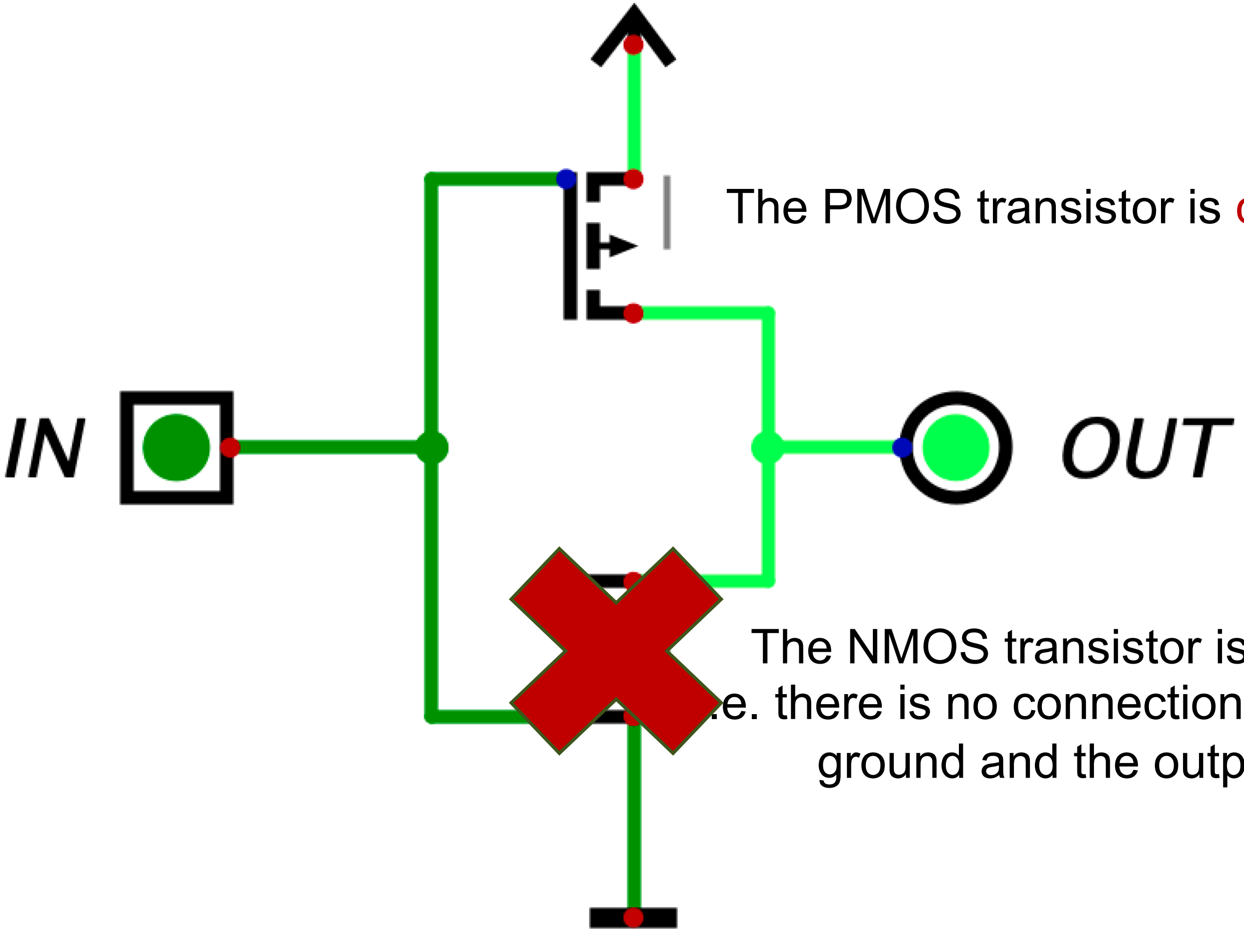


The PMOS transistor is closed

The NMOS transistor is open
(i.e. there is no connection between ground and the output)

CMOS Inverter

When the input is 0, power is connected to the output

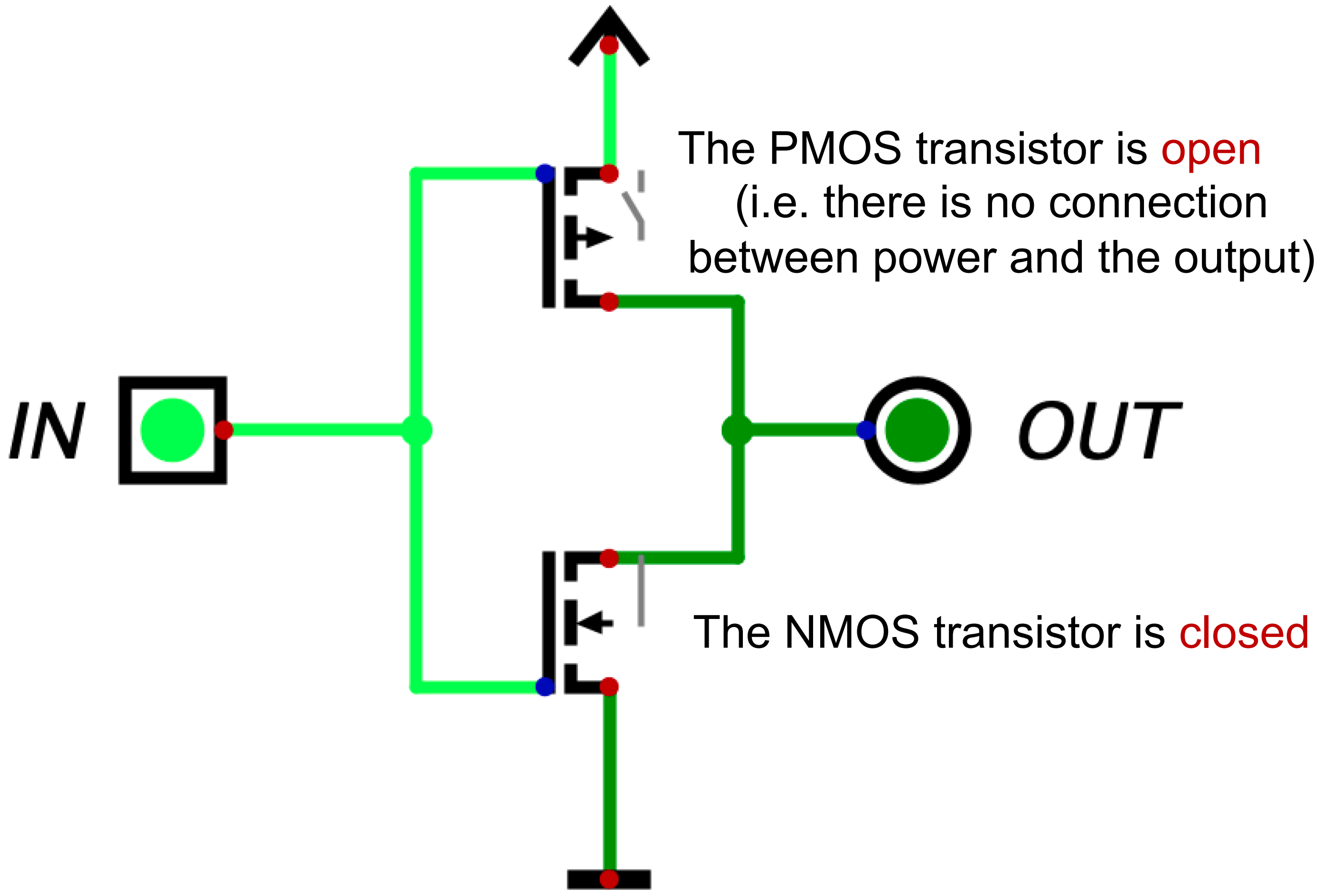


The PMOS transistor is closed

The NMOS transistor is open
.e. there is no connection between
ground and the output)

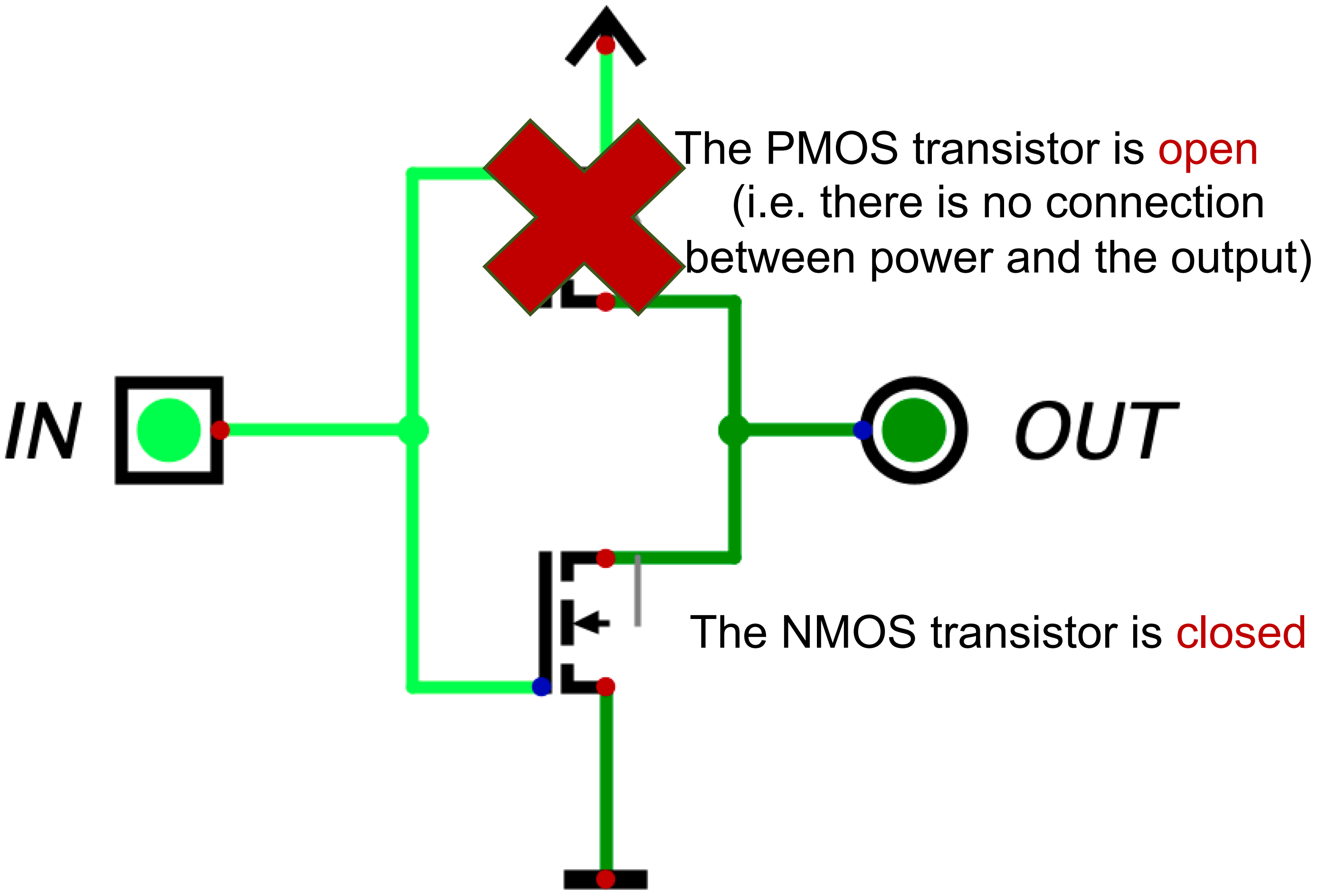
CMOS Inverter

When the input is 1, ground is connected to the output

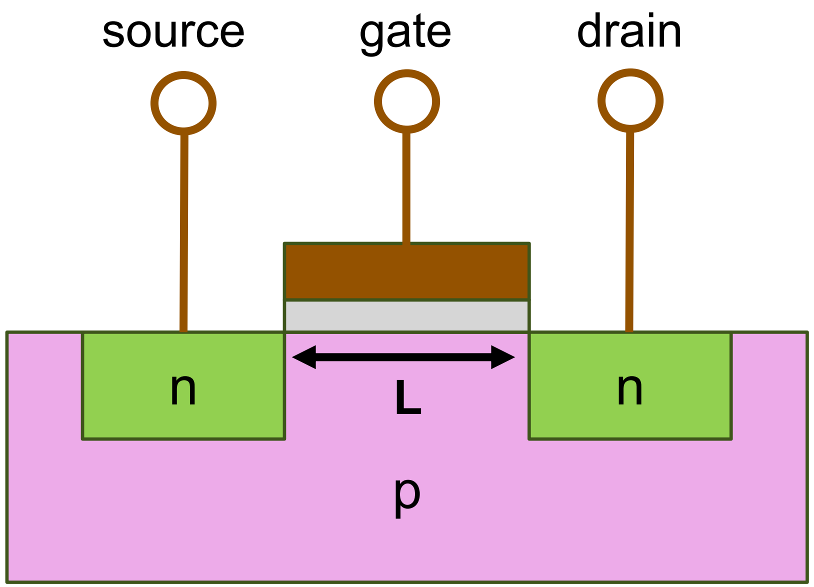


CMOS Inverter

When the input is 1, ground is connected to the output

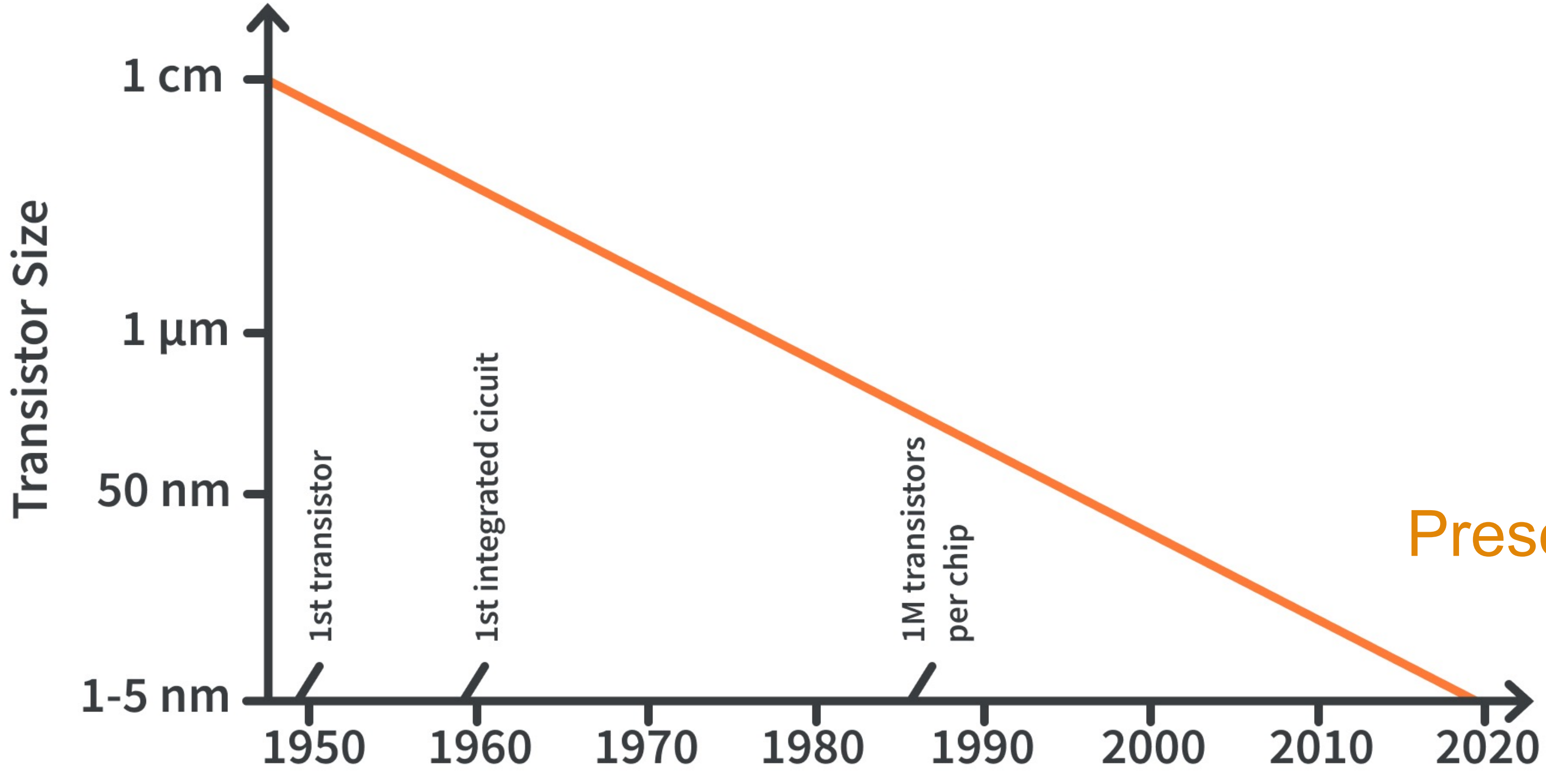


n-channel Metal-Oxide-Semiconductor-Field-Effect Transistor (MOSFET)



L = length of the channel

Transistor Size

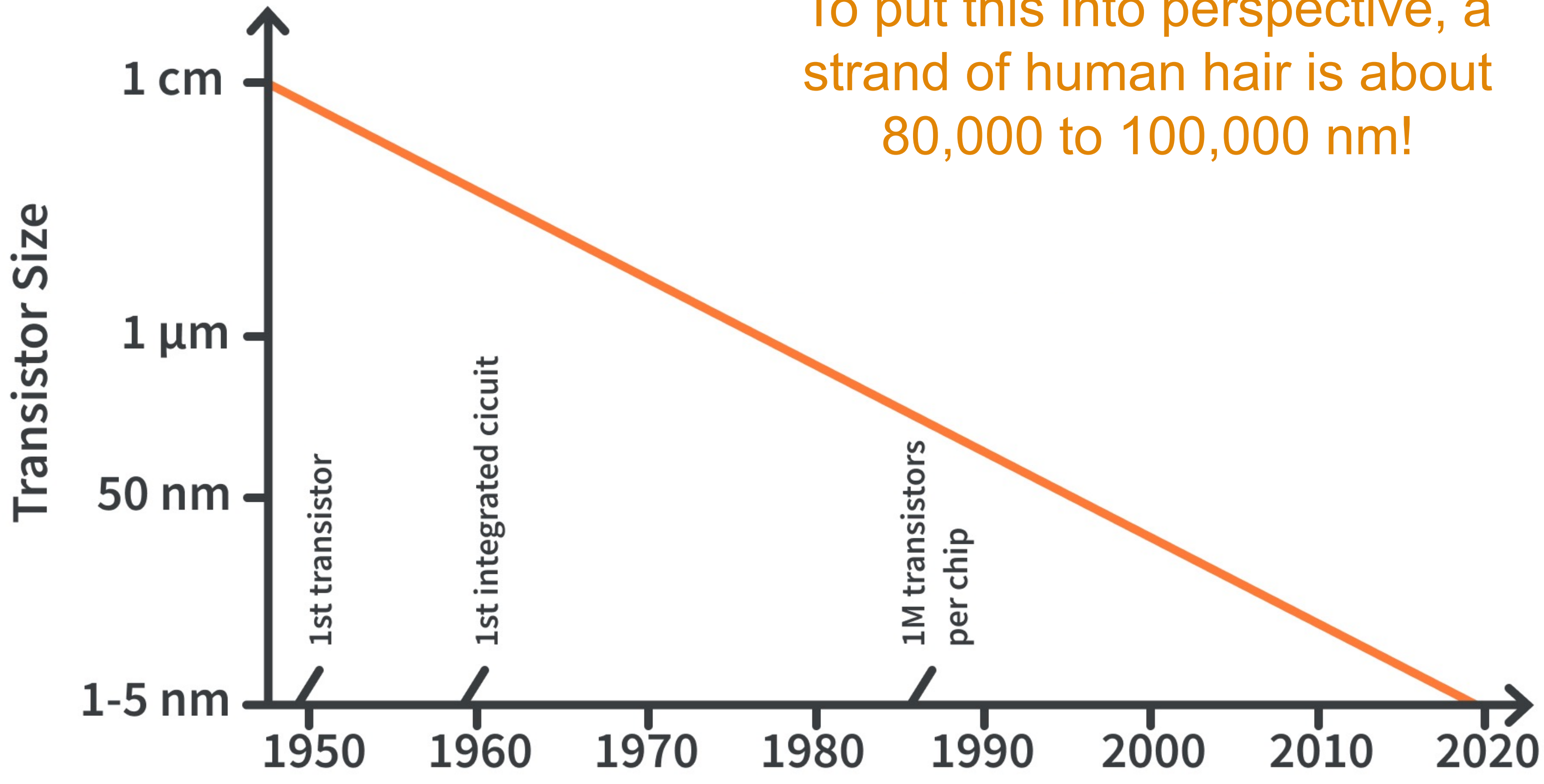


Present day technology: 5nm

Transistor Size

Present day technology: 5nm

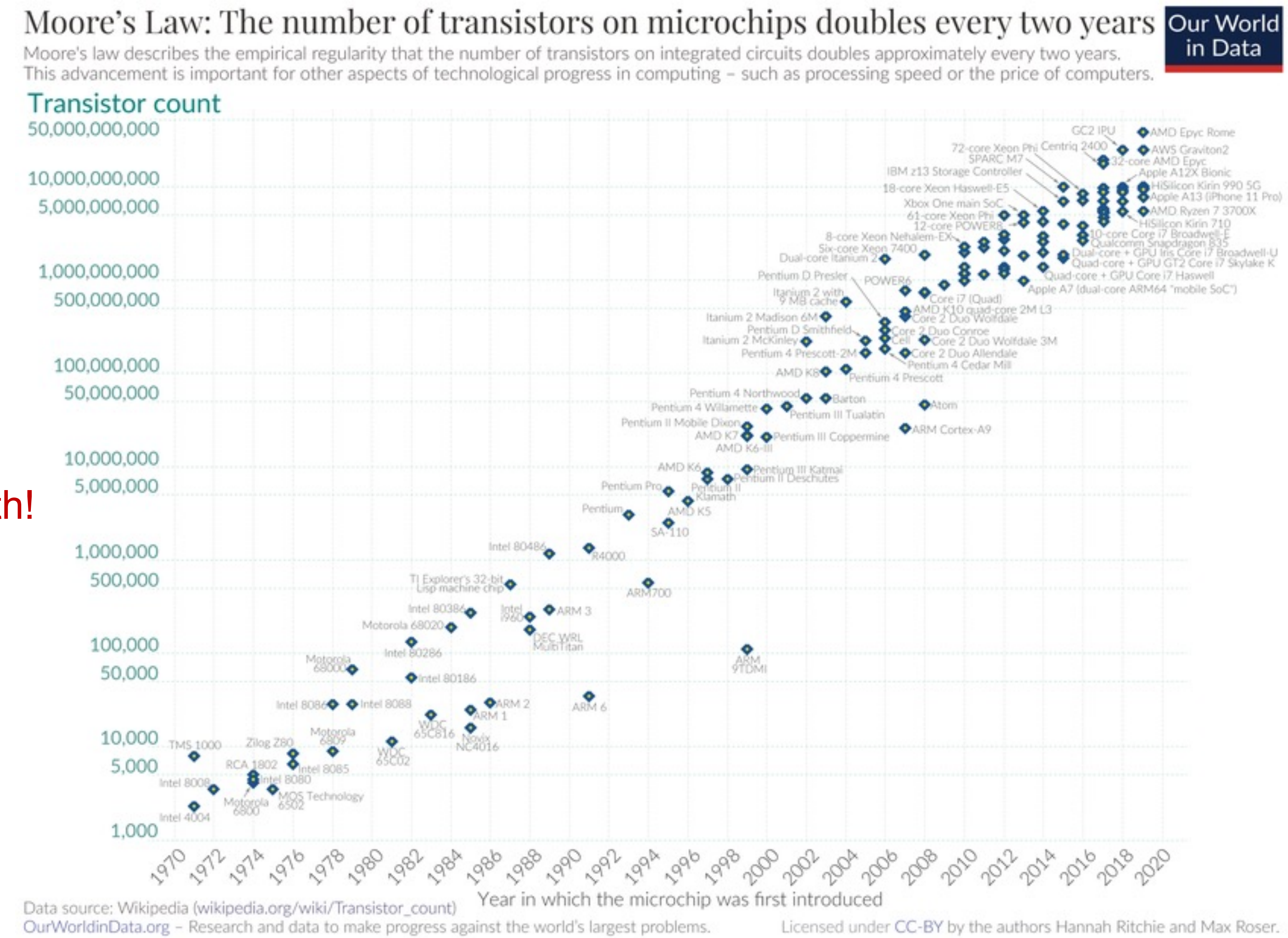
To put this into perspective, a strand of human hair is about 80,000 to 100,000 nm!



As transistor size decreases, speed increases

Moore’s Law

Exponential growth!



Logic Gates

Inverter/Not Gate

Symbol

Truth Table

A	Y
0	
1	

Equation

Inverter/Not Gate

Symbol

Truth Table

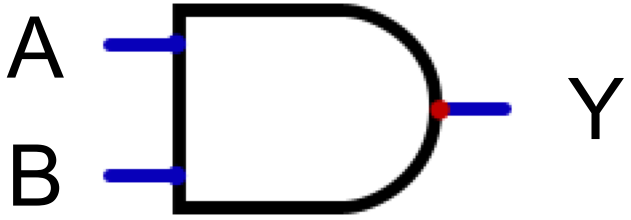
A	Y
0	1
1	0

Equation

$$Y = \overline{A}$$

AND Gate

Symbol



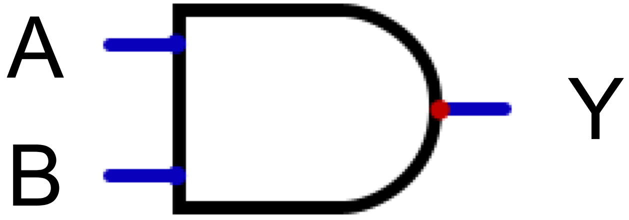
Truth Table

A	B	Y
0	0	
0	1	
1	0	
1	1	

Equation

AND Gate

Symbol



Truth Table

A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

Equation

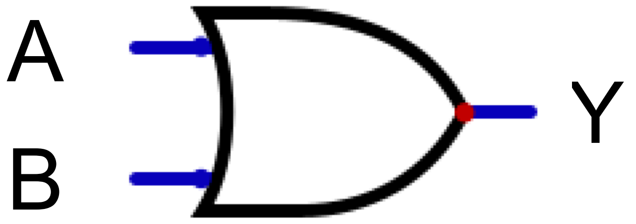
$$Y = A \text{ x } B$$

or

$$Y = AB$$

OR Gate

Symbol



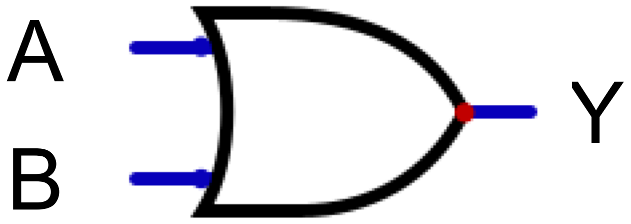
Truth Table

A	B	Y
0	0	
0	1	
1	0	
1	1	

Equation

OR Gate

Symbol



Truth Table

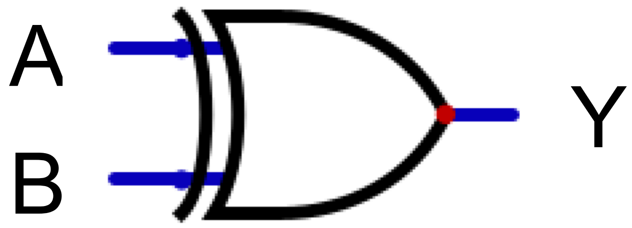
A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

Equation

$$Y = A + B$$

XOR Gate

Symbol



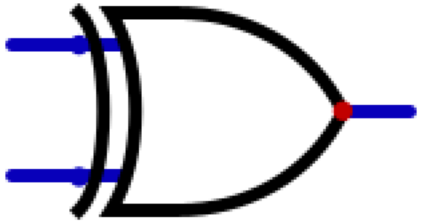
Truth Table

A	B	Y
0	0	
0	1	
1	0	
1	1	

Equation

XOR Gate

Symbol



Truth Table

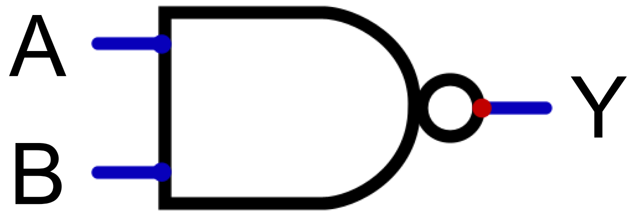
A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

Equation

$$Y = A \oplus B$$

NAND

Symbol



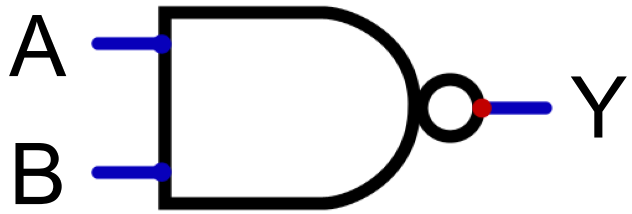
Truth Table

A	B	Y
0	0	
0	1	
1	0	
1	1	

Equation

NAND

Symbol



Truth Table

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

Equation

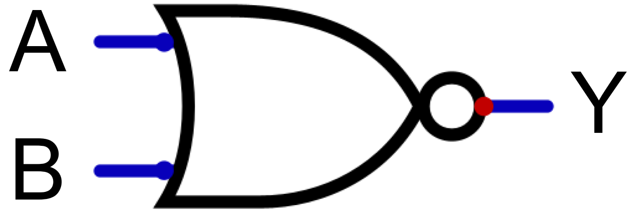
$$\mathrm{Y} = \overline{A\ x\ B}$$

or

$$Y = \overline{AB}$$

NOR

Symbol



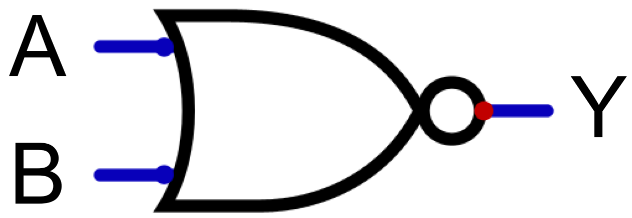
Truth Table

A	B	Y
0	0	
0	1	
1	0	
1	1	

Equation

NOR

Symbol



Truth Table

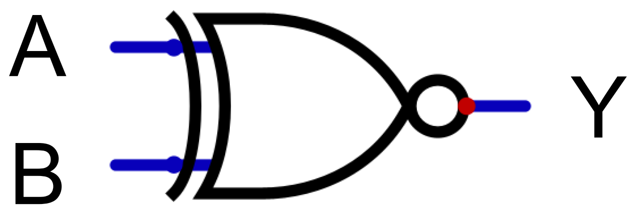
A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

Equation

$$Y = \overline{A + B}$$

XNOR Gate

Symbol



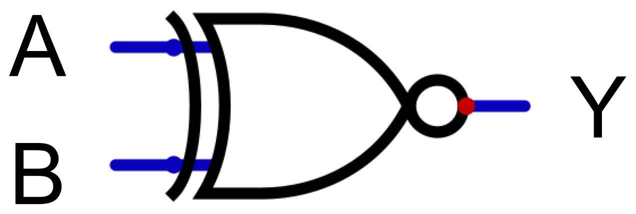
Truth Table

A	B	Y
0	0	
0	1	
1	0	
1	1	

Equation

XNOR Gate

Symbol



Truth Table

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	1

Equation

$$Y = \overline{A \oplus B}$$