Digital Logic

COMP311 Connor McMahon

Announcements

- Lab 0 due tomorrow
- Homework 1 released tomorrow, due next Thursday

Minimizing Transistor Count

Transistor Count

Gate	Number of Transistors
NOT	2
AND	6
OR	6
NAND	4
NOR	4
XOR	12
XNOR	12

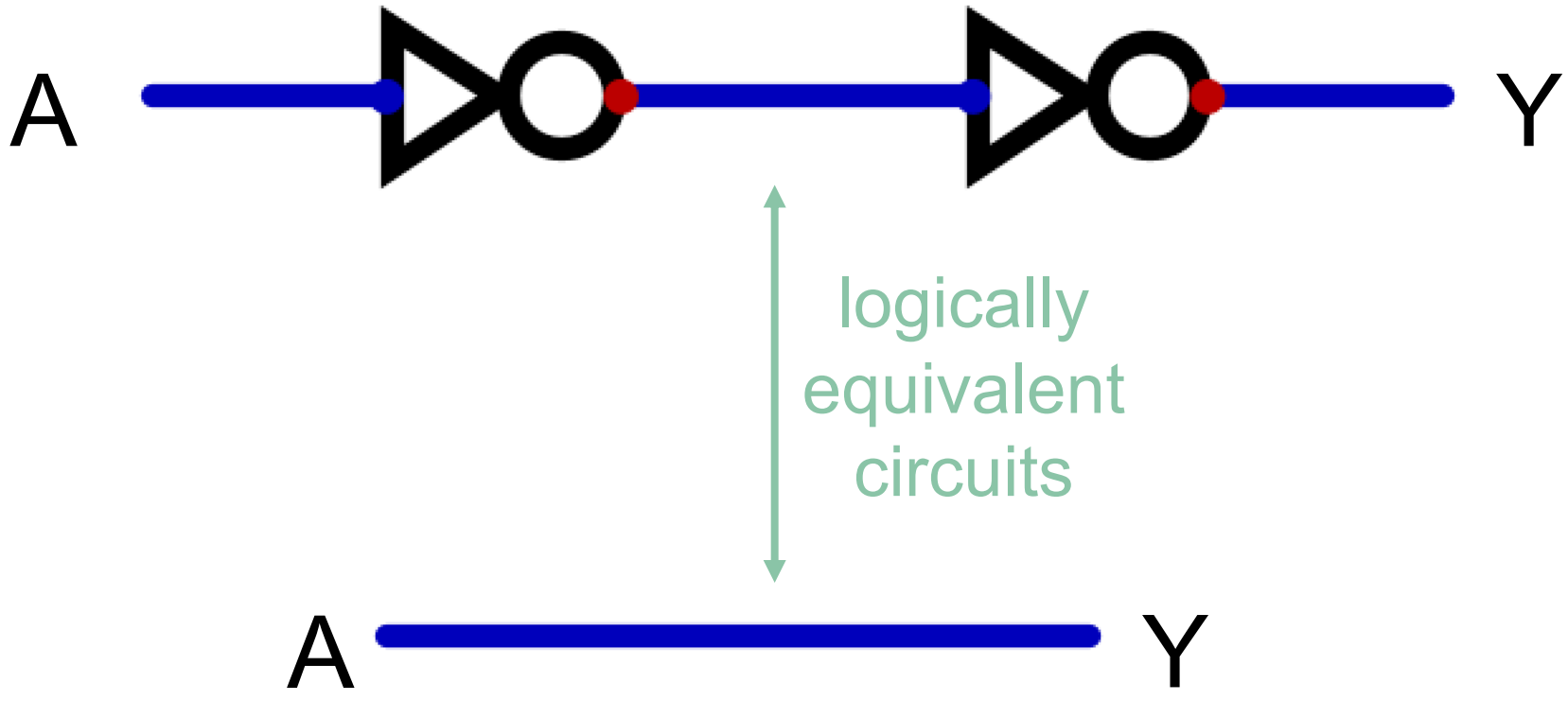
Minimizing Transistor Count

- Reduces
  - Delay from input to output
  - The area of the circuit
  - Power consumption
  - The cost of the circuit

Logically Equivalent Circuits

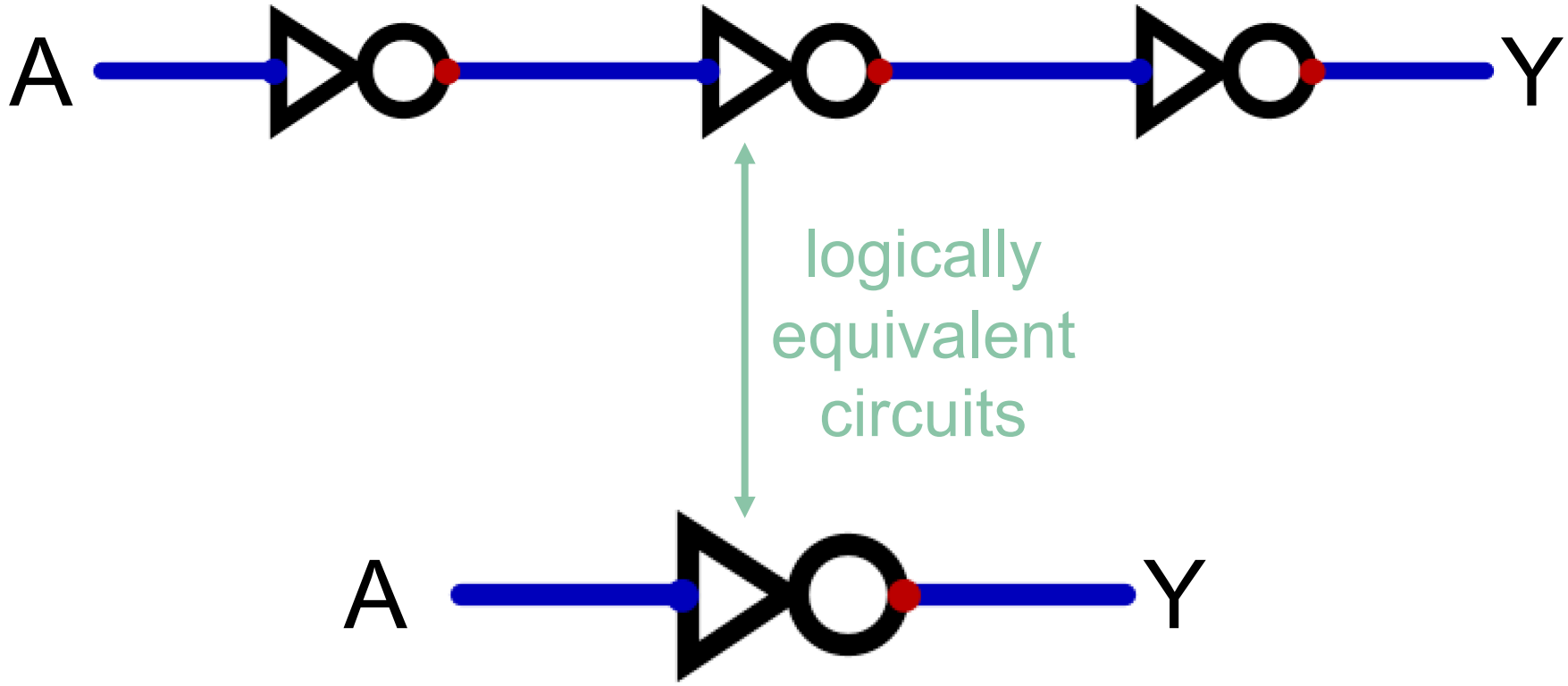
- For any input, they will produce the same output
- In other words, their truth tables are equivalent

Inverters



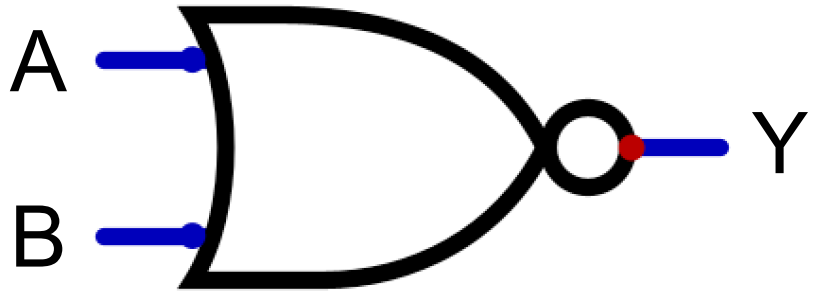
Any even number of inverters chained together is logically equivalent to having no inverters

Inverters

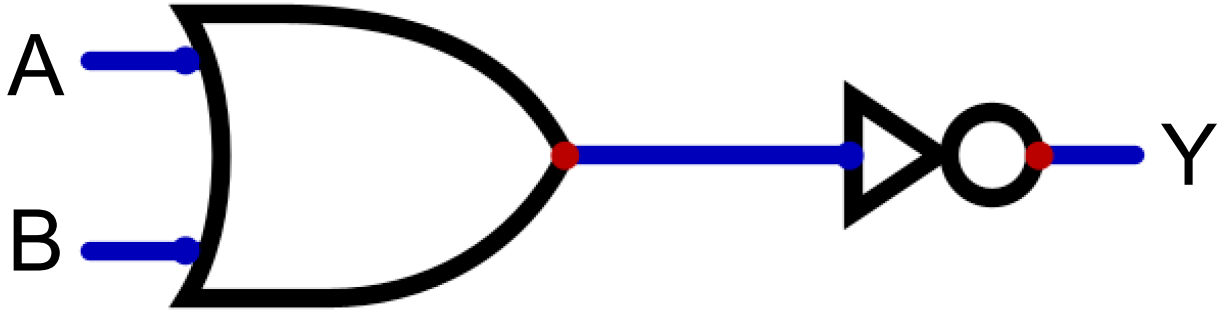


Any odd number of inverters chained together is logically equivalent to having one inverter

Bubble is Logically Equivalent to Inverter

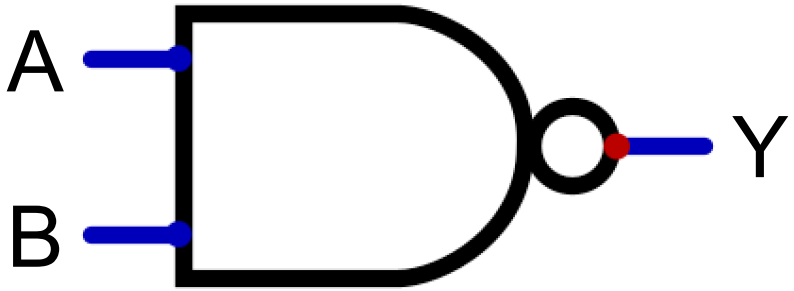


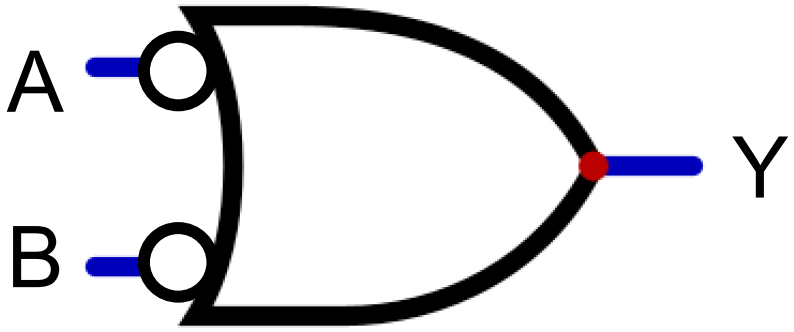
4 transistors



8 transistors

NAND

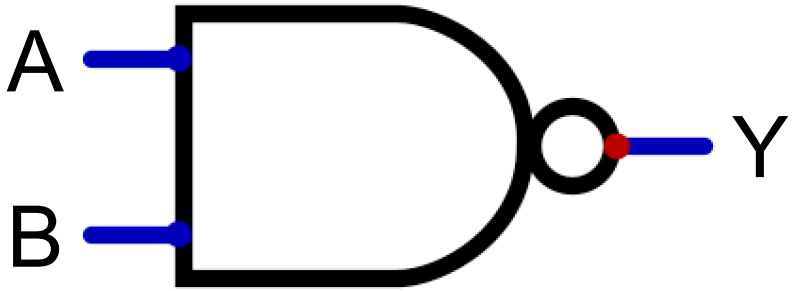


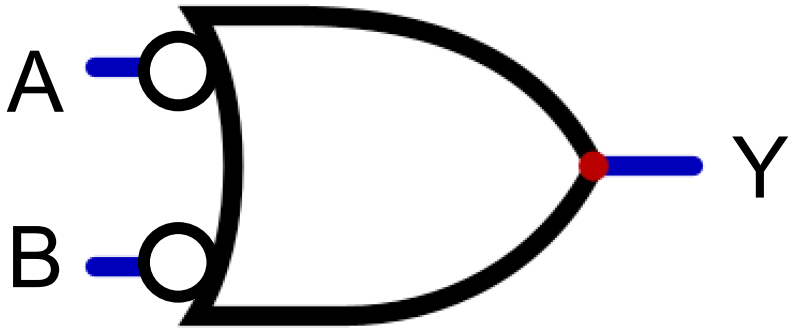


A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

A	B	Y
0	0	
0	1	
1	0	
1	1	

NAND

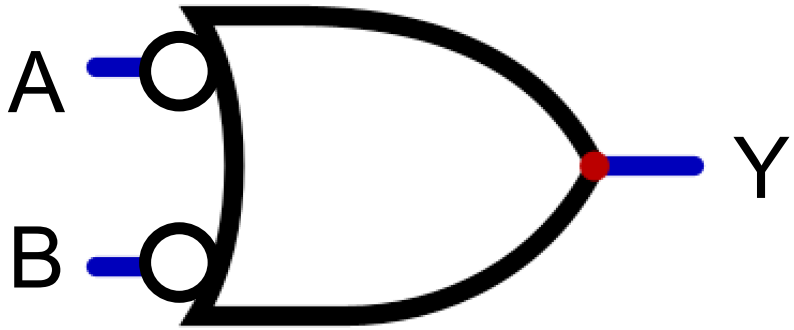




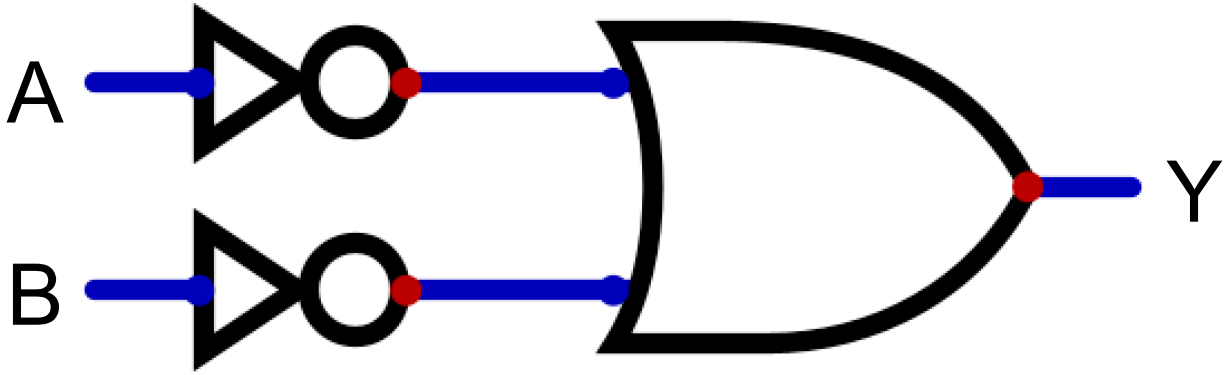
A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

Bubble is Logically Equivalent to Inverter

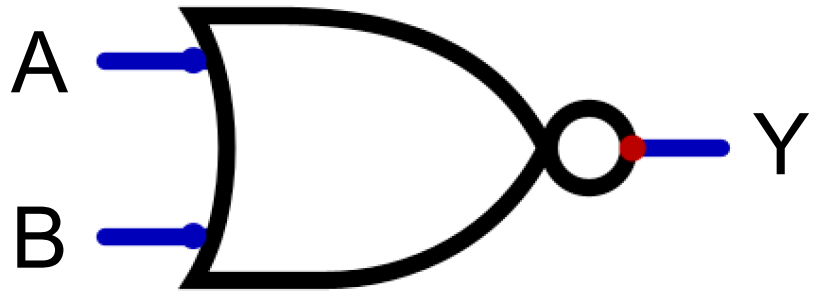


4 transistors

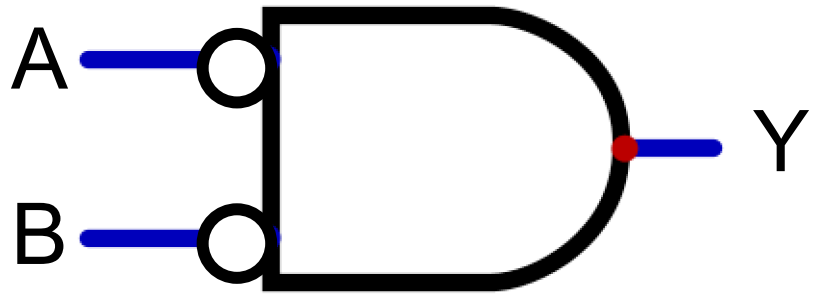


10 transistors

NOR

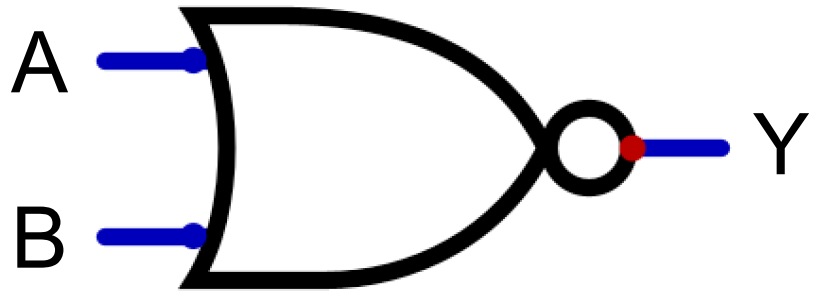


A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

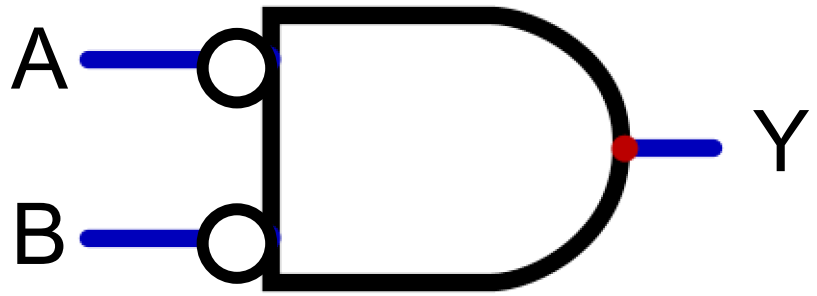


A	B	Y
0	0	
0	1	
1	0	
1	1	

NOR



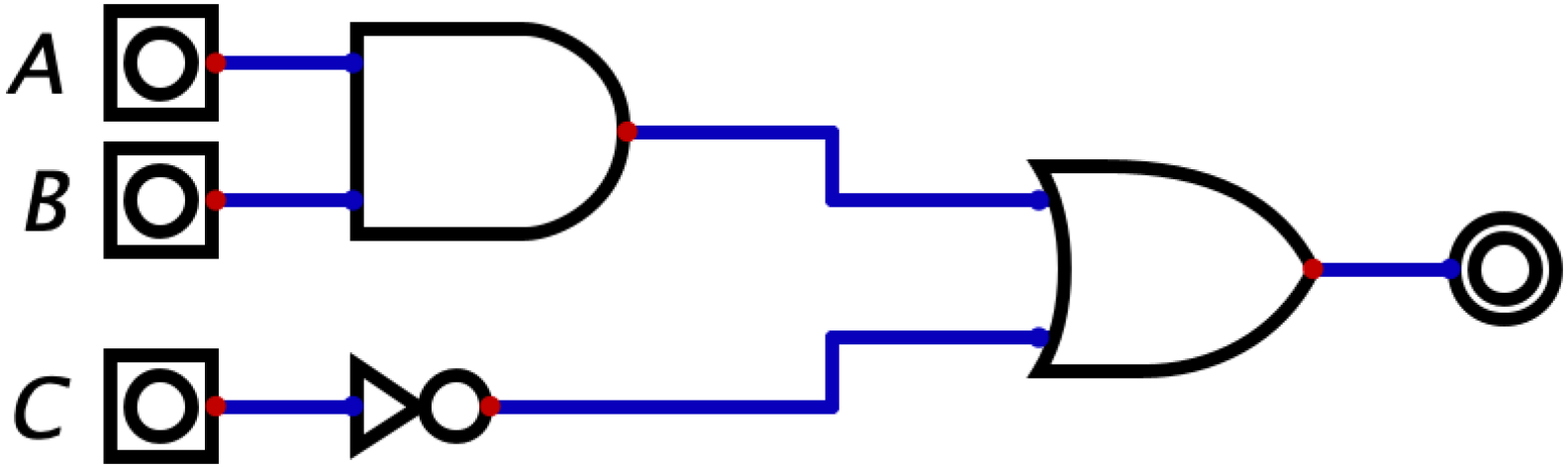
A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0



A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

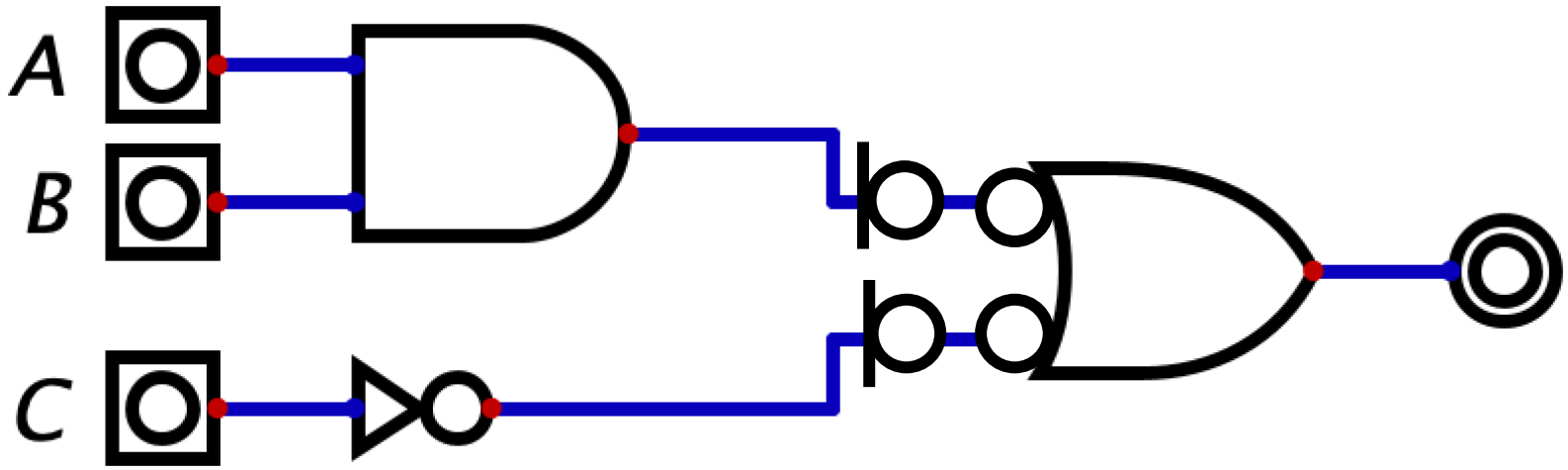
Ex1: Minimizing Transistor Count

Minimize the number of transistors in this circuit by implementing it using only NAND gates and inverters.

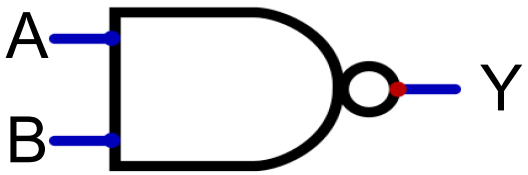


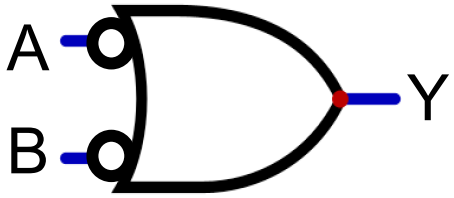
NAND gates:

Ex1: Minimizing Transistor Count



NAND gates:





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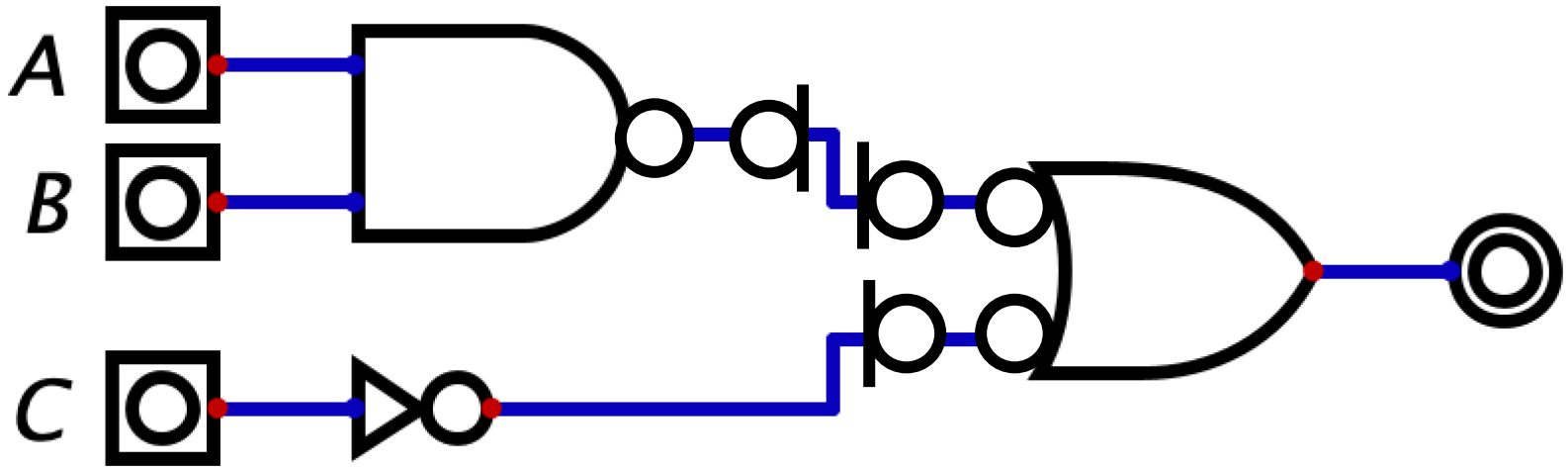
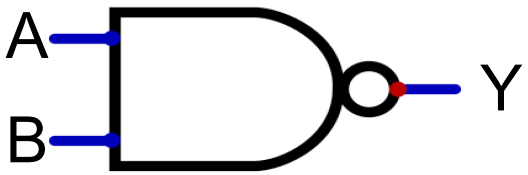
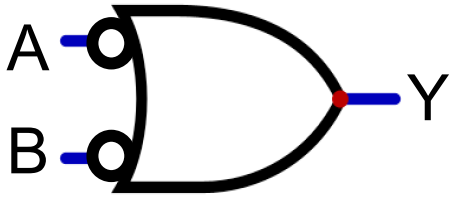


NAND gates:





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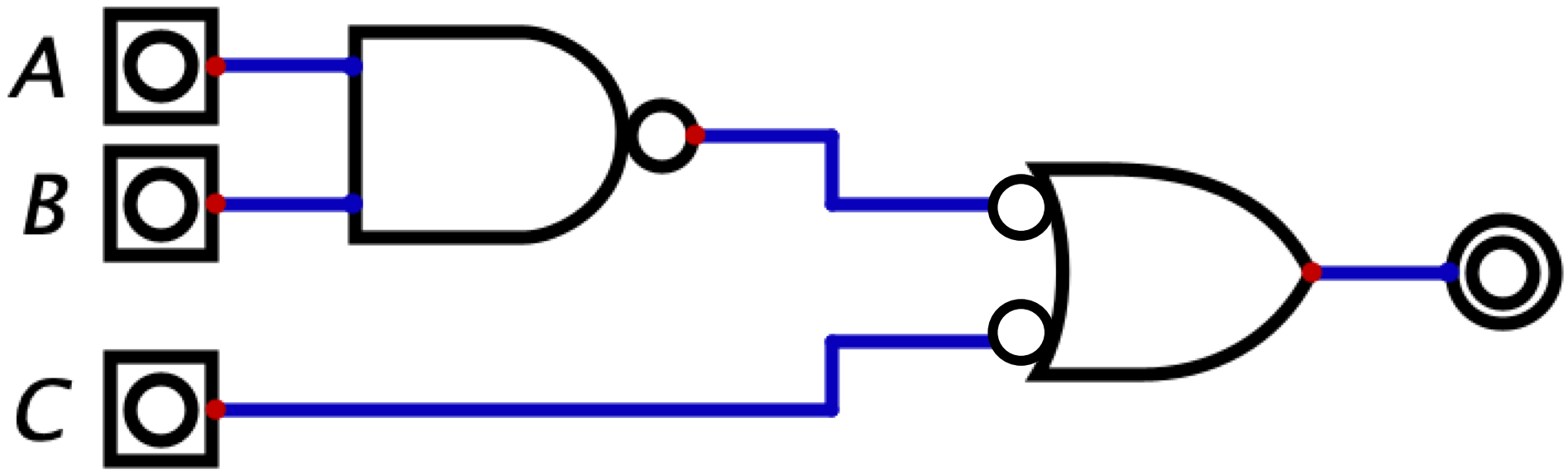
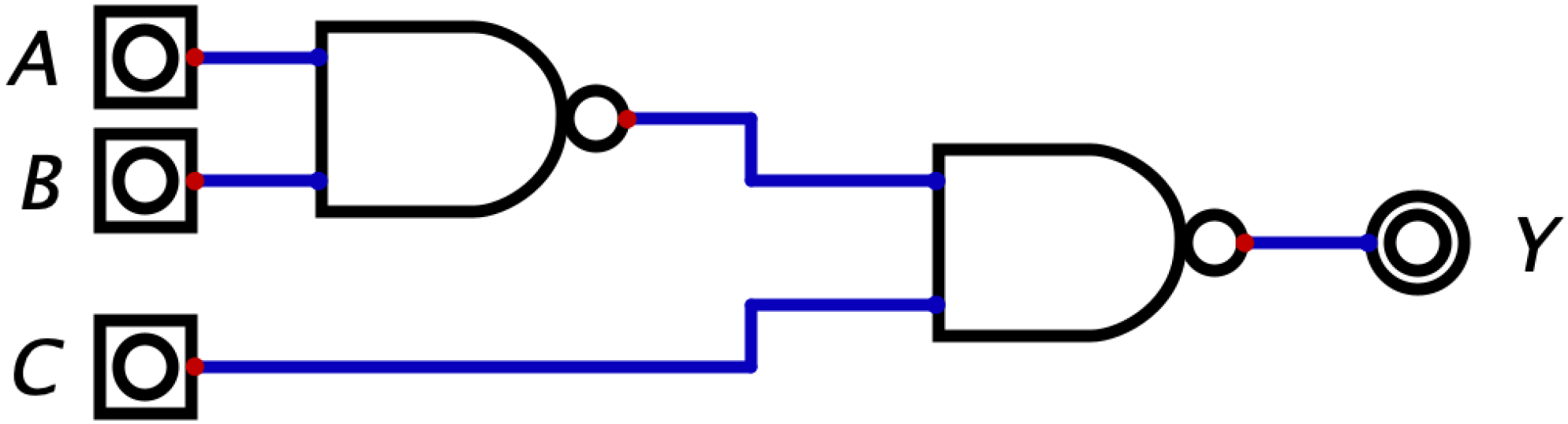


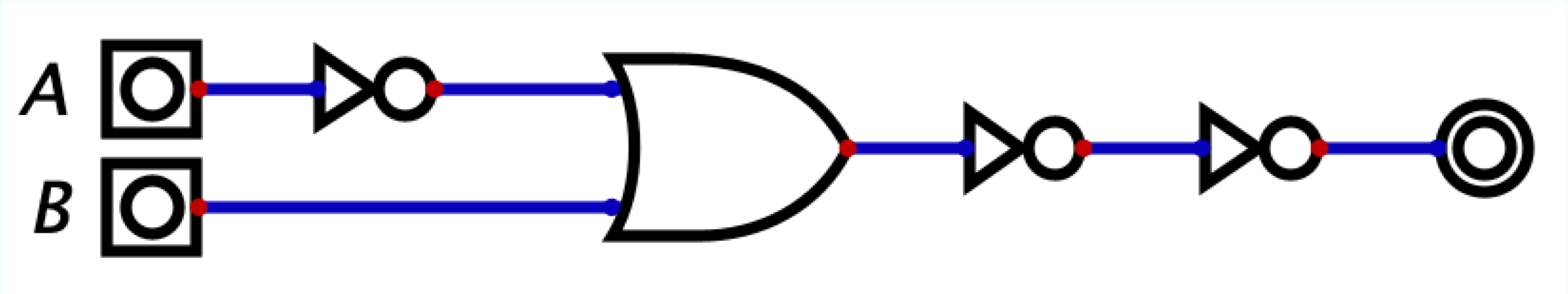
Ex1: Minimizing Transistor Count



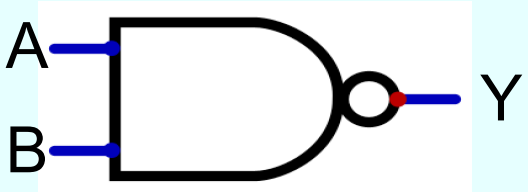
Original Transistor Count: 14
Final Transistor Count: 8

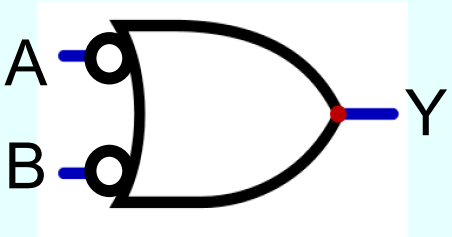
Minimizing Transistor Count

Minimize the number of transistors in this circuit by implementing it using only NAND gates and inverters. Compare the number of transistors in the original circuit and the new circuit.

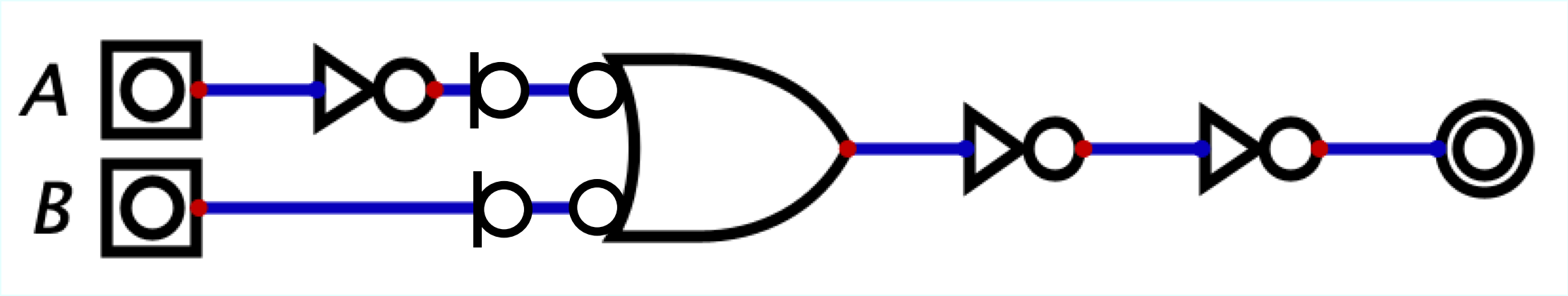


NAND gates:

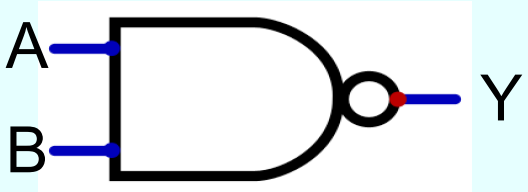


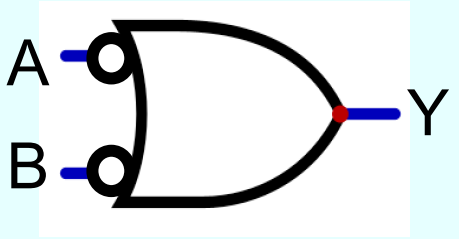


Minimizing Transistor Count

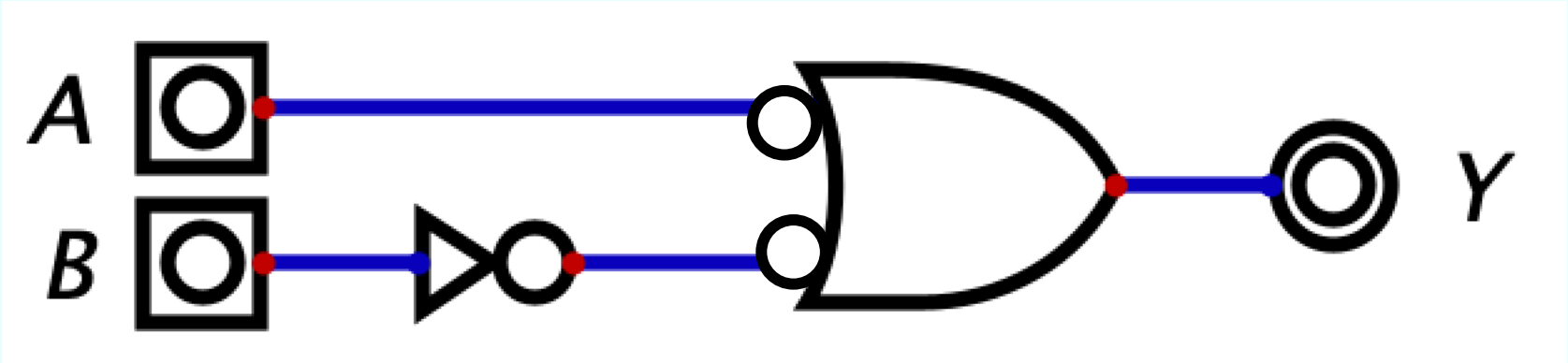


NAND gates:

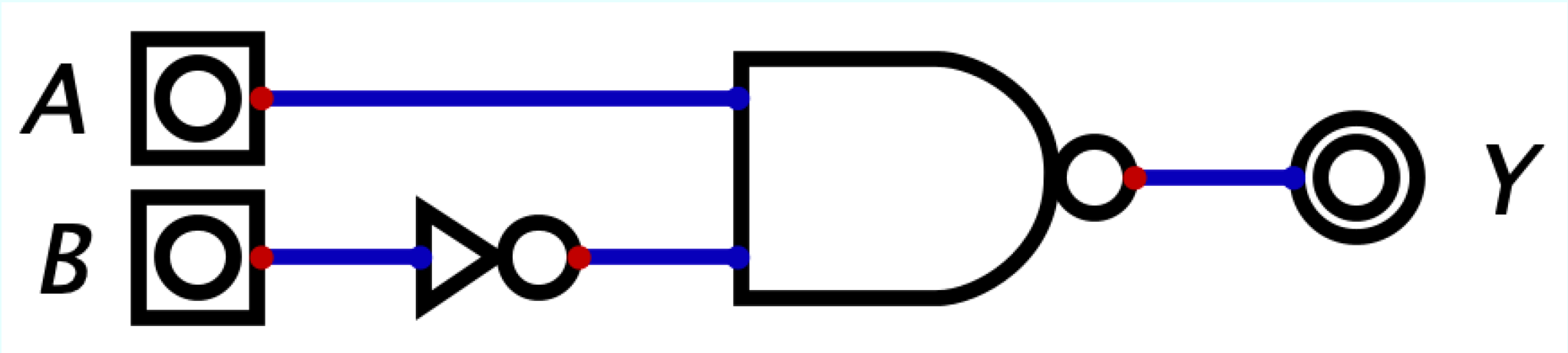




Minimizing Transistor Count



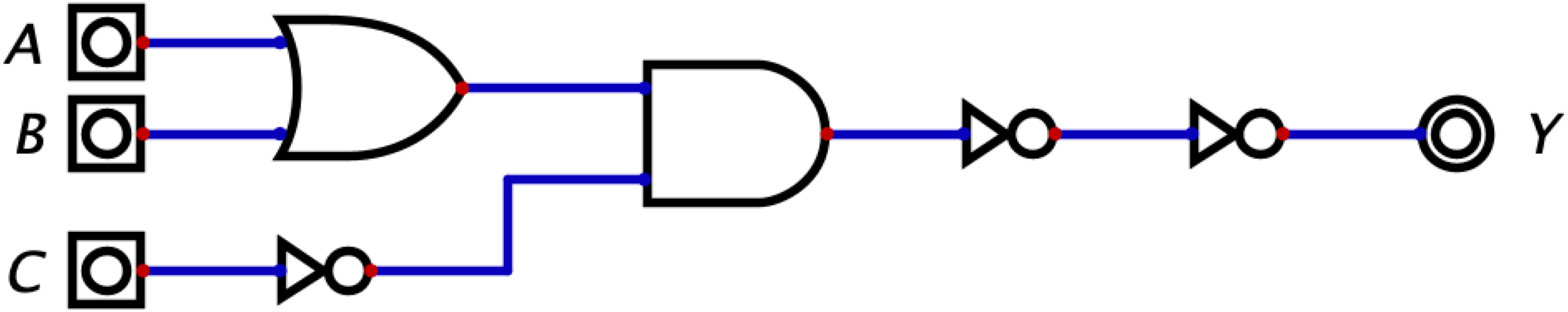
Minimizing Transistor Count



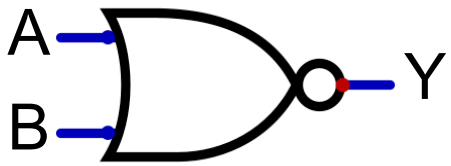
Original Transistor Count: 12
Final Transistor Count: 6

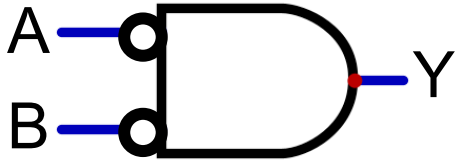
Ex2: Minimizing Transistor Count

Minimize the number of transistors in this circuit by implementing it using only NOR gates and inverters.

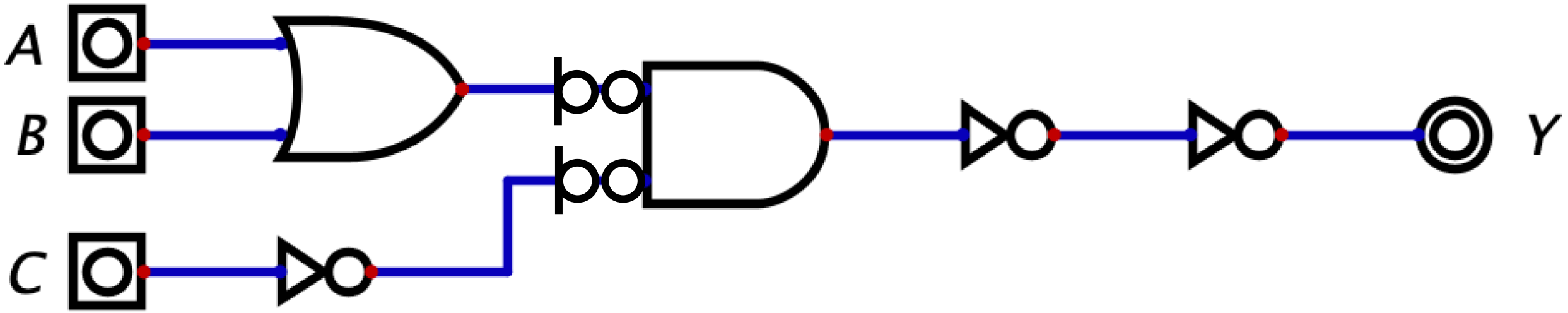


NOR gates:

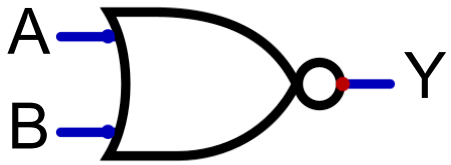


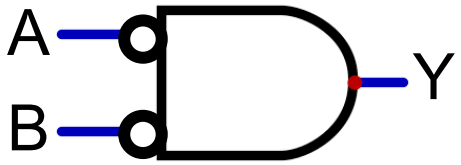


Ex2: Minimizing Transistor Count

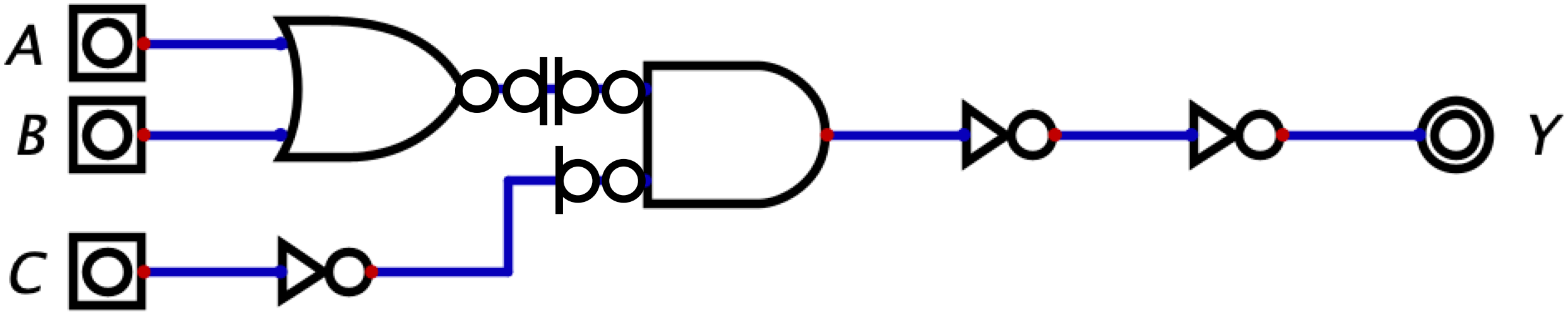


NOR gates:

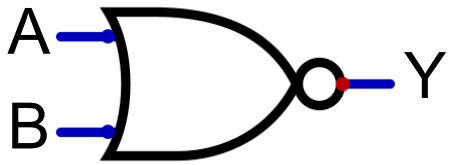


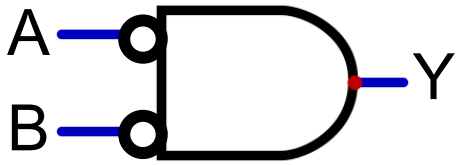


Ex2: Minimizing Transistor Count



NOR gates:





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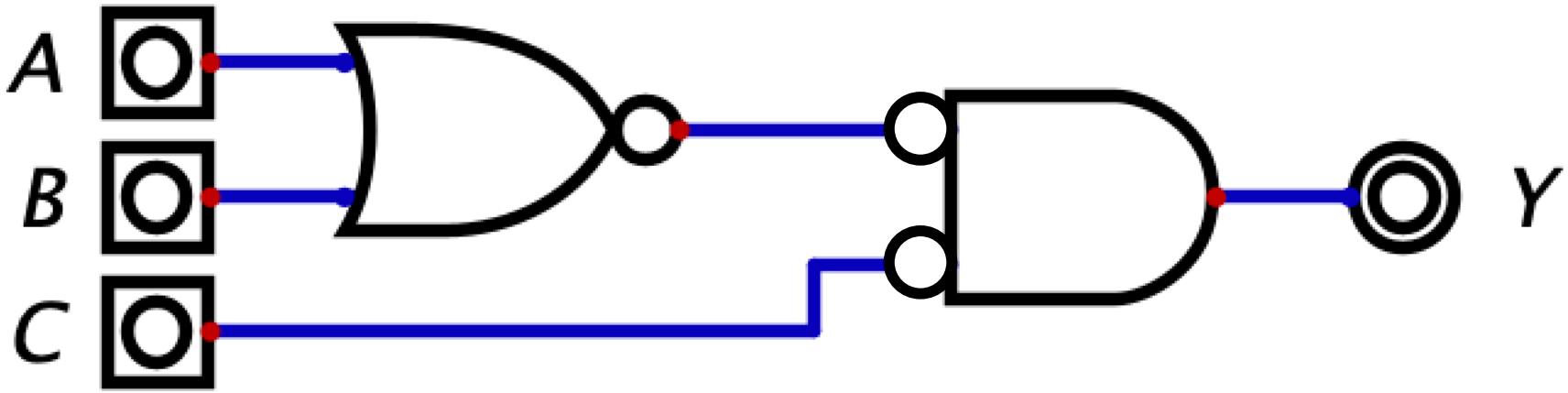
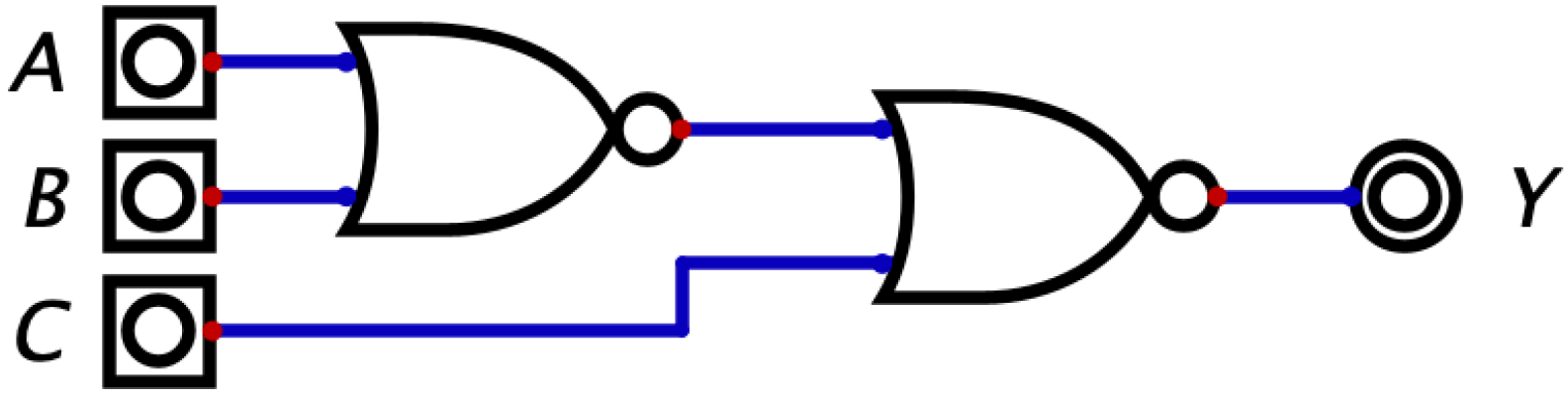


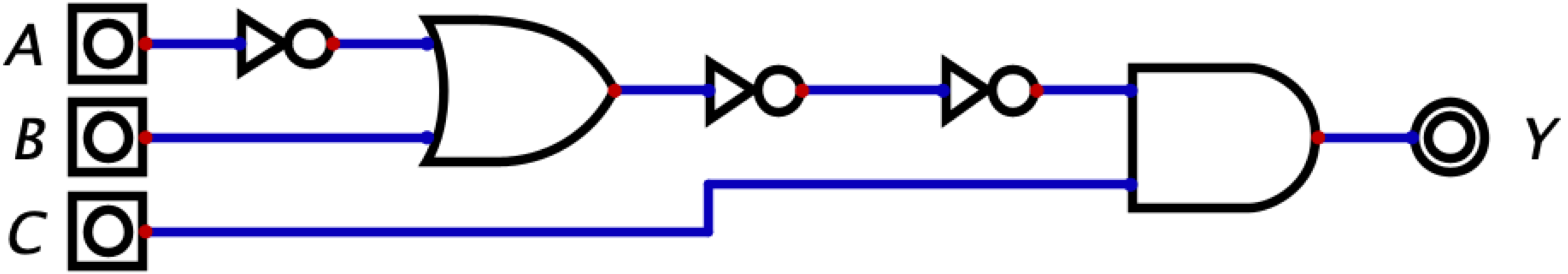
Ex2: Minimizing Transistor Count



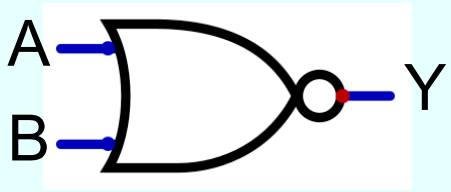
Original Transistor Count: 18
Final Transistor Count: 8

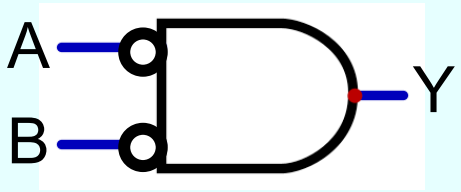
Minimizing Transistor Count

Minimize the number of transistors in this circuit by implementing it using only NOR gates and inverters. Compare the number of transistors in the original circuit and the new circuit.

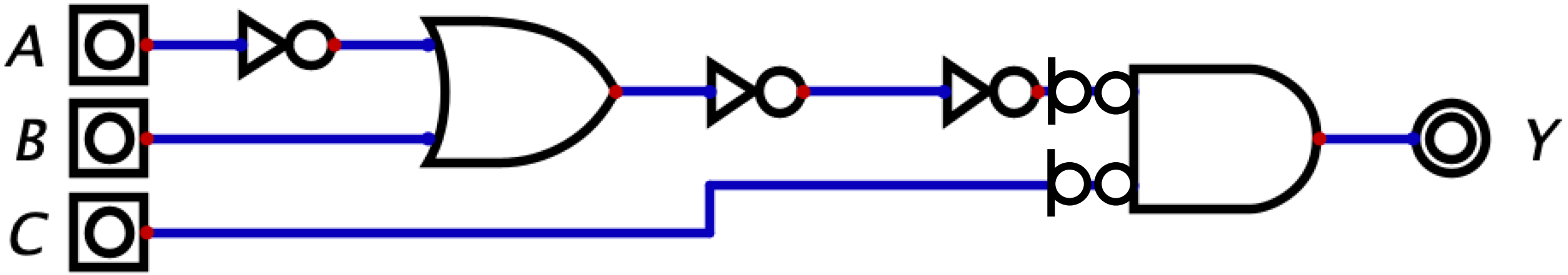


NOR gates:

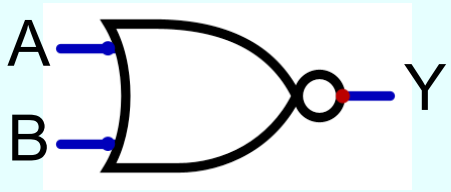


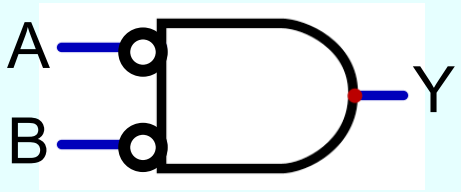


Minimizing Transistor Count

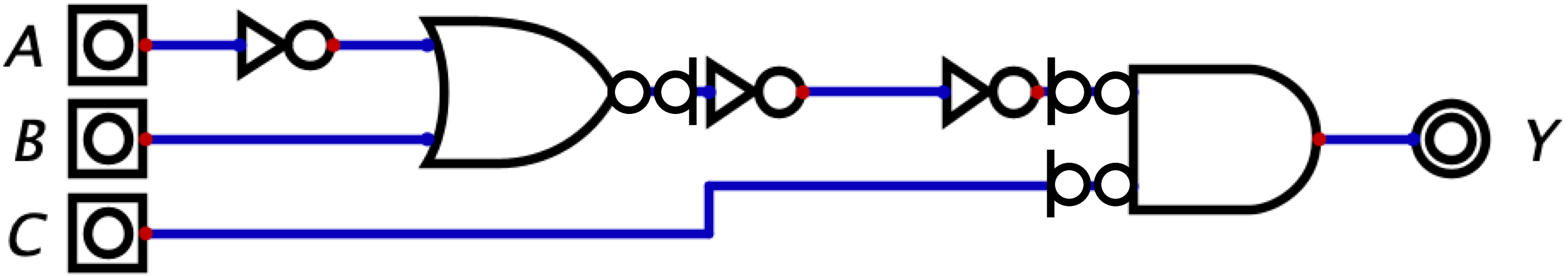


NOR gates:

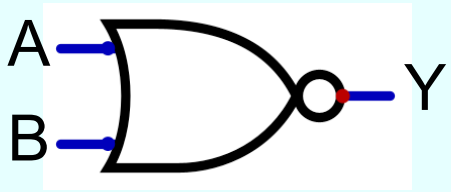


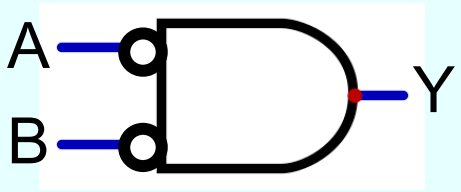


Minimizing Transistor Count

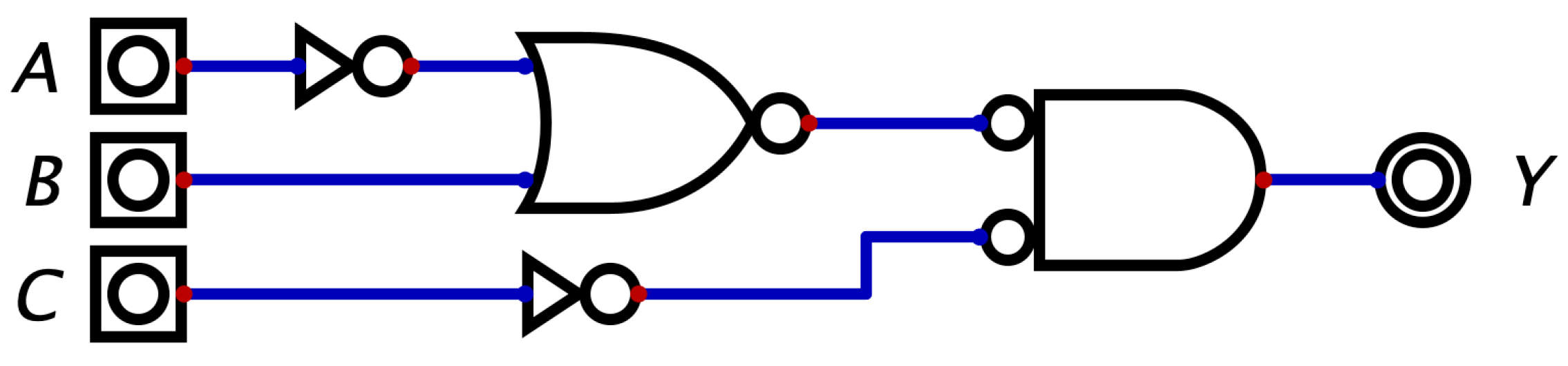


NOR gates:

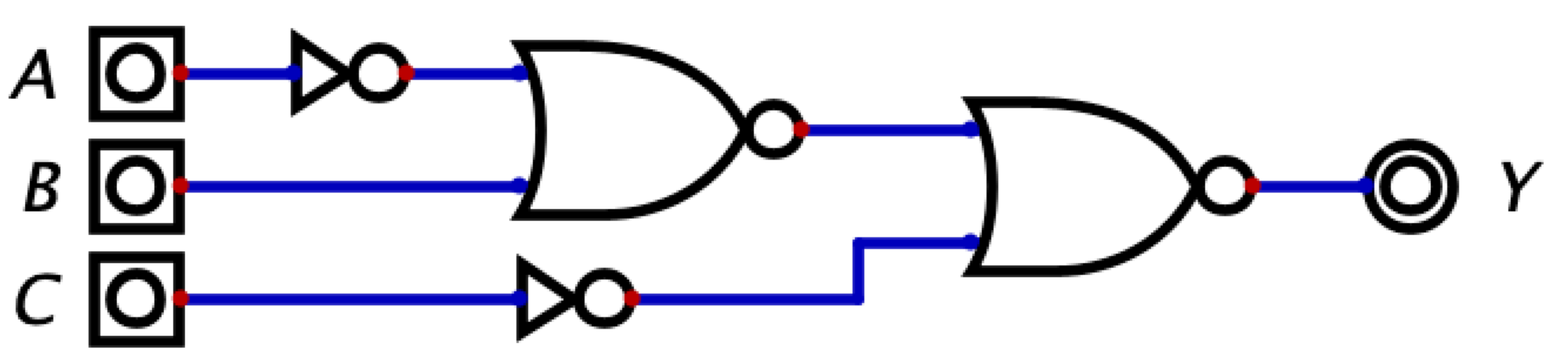




Minimizing Transistor Count



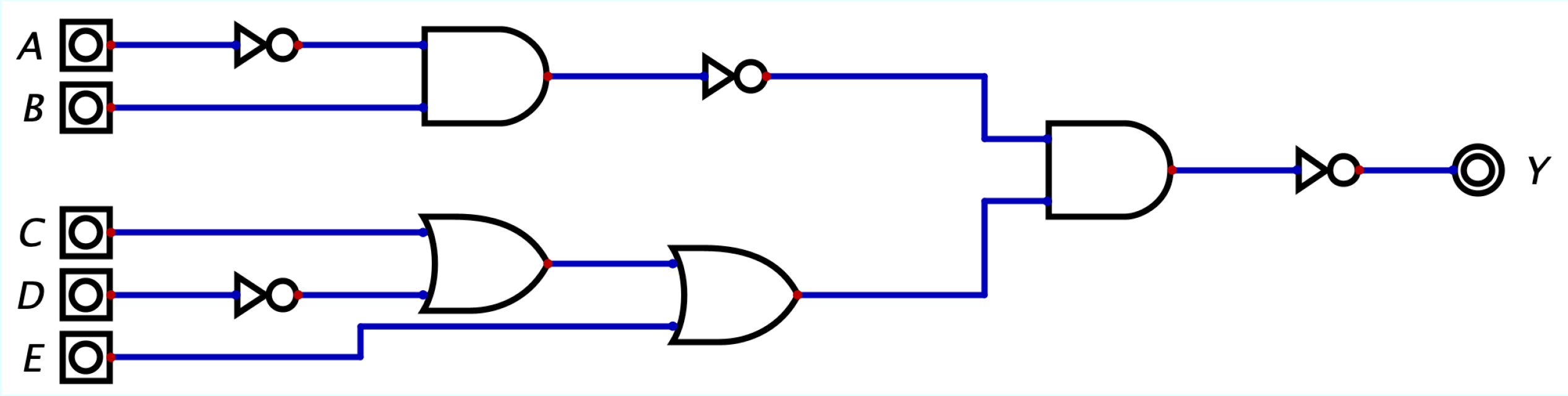
Minimizing Transistor Count



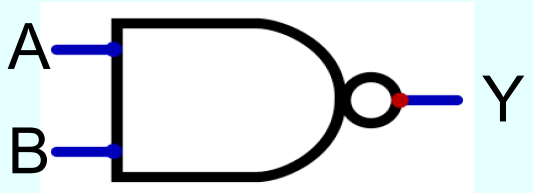
Original Transistor Count: 18
Final Transistor Count: 12

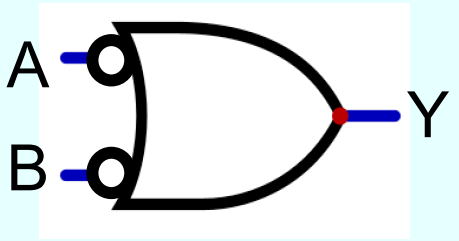
Minimizing Transistor Count

Minimize the number of transistors in this circuit by implementing it using only NAND gates and inverters. Compare the number of transistors in the original circuit and the new circuit.



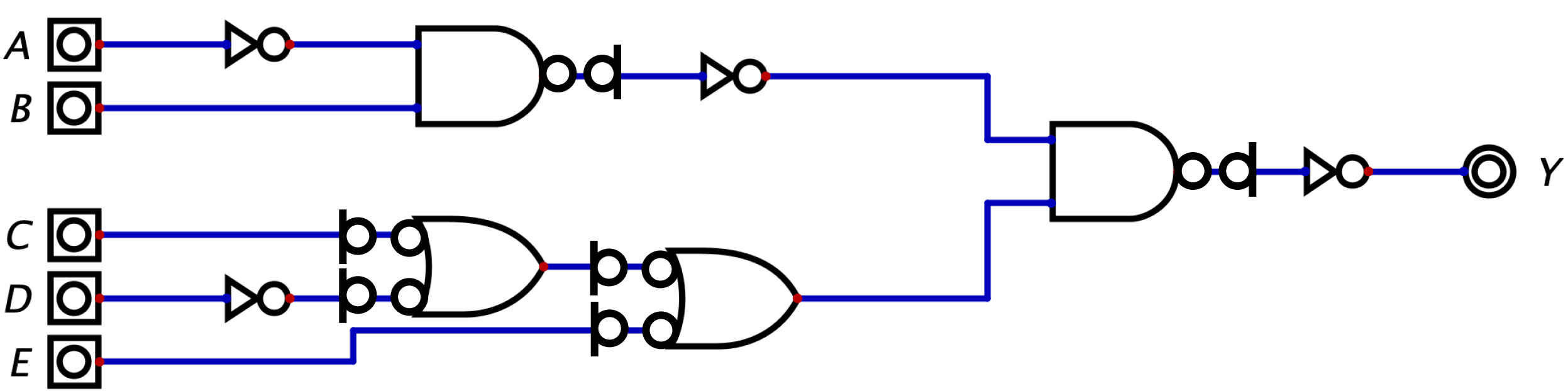
NAND gates:



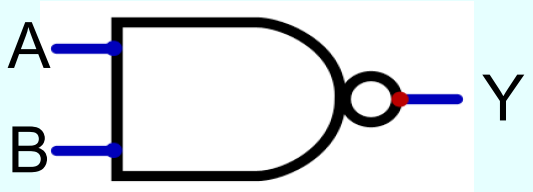


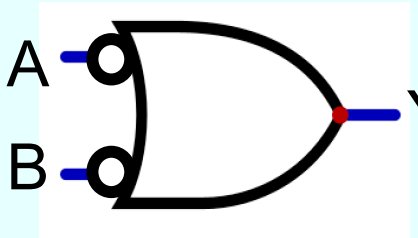
Minimizing Transistor Count

Minimize the number of transistors in this circuit by implementing it using only NAND gates and inverters. Compare the number of transistors in the original circuit and the new circuit.



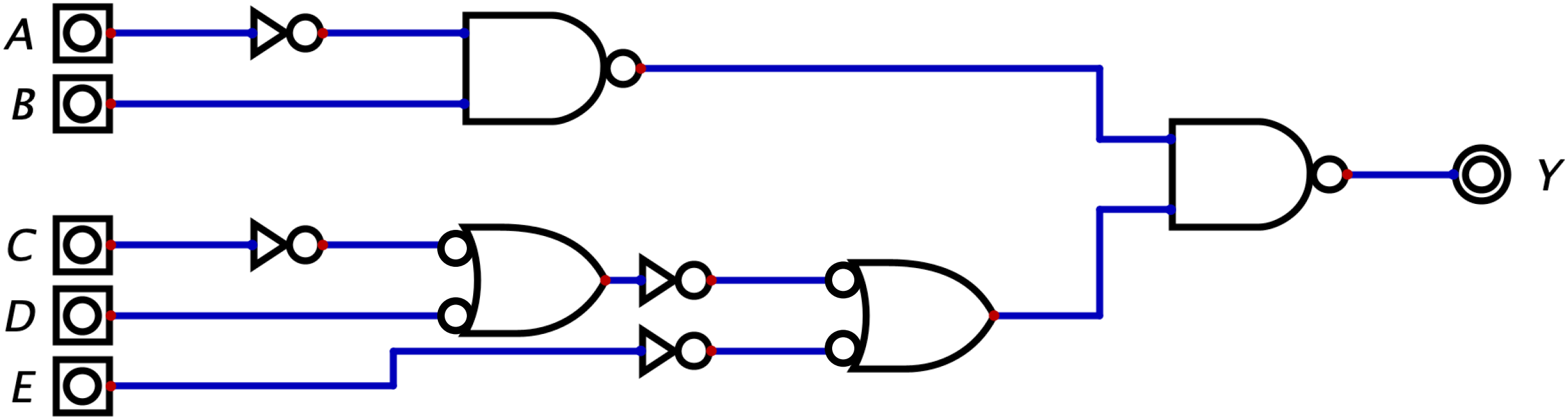
NAND gates:



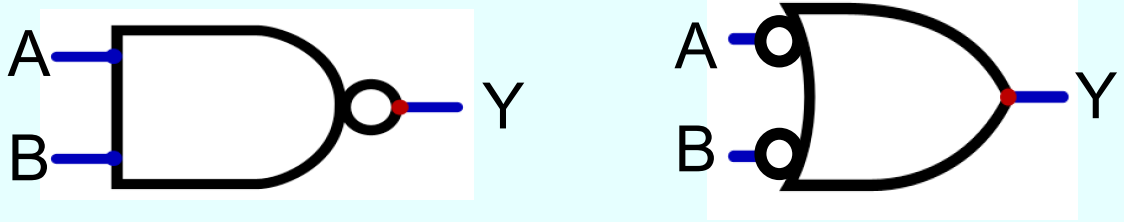


Minimizing Transistor Count

Minimize the number of transistors in this circuit by implementing it using only NAND gates and inverters. Compare the number of transistors in the original circuit and the new circuit.

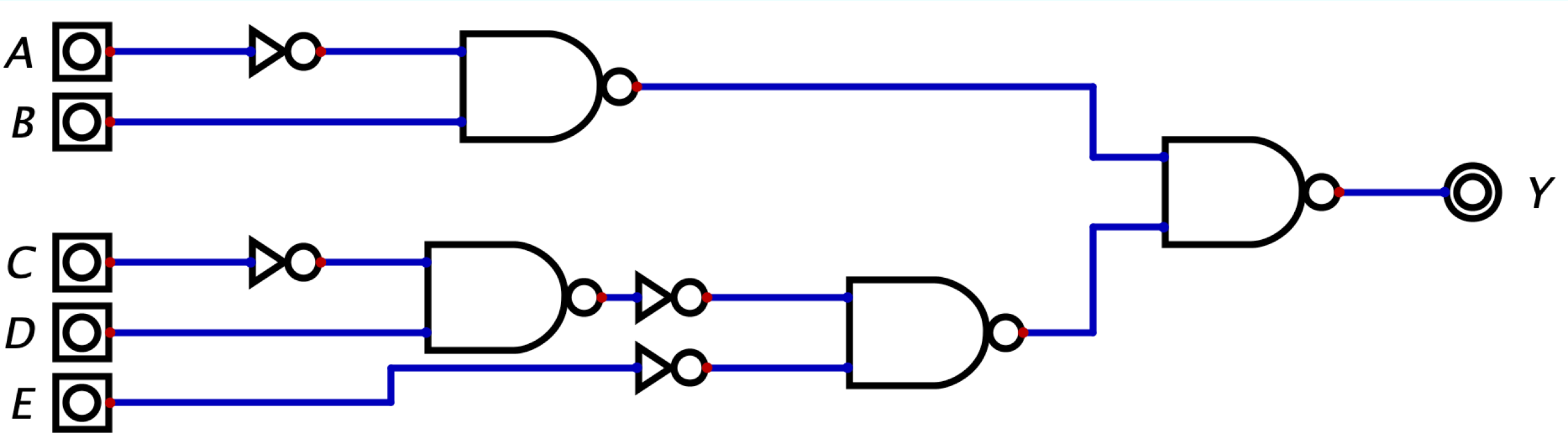


NAND gates:



Minimizing Transistor Count

Minimize the number of transistors in this circuit by implementing it using only NAND gates and inverters. Compare the number of transistors in the original circuit and the new circuit.

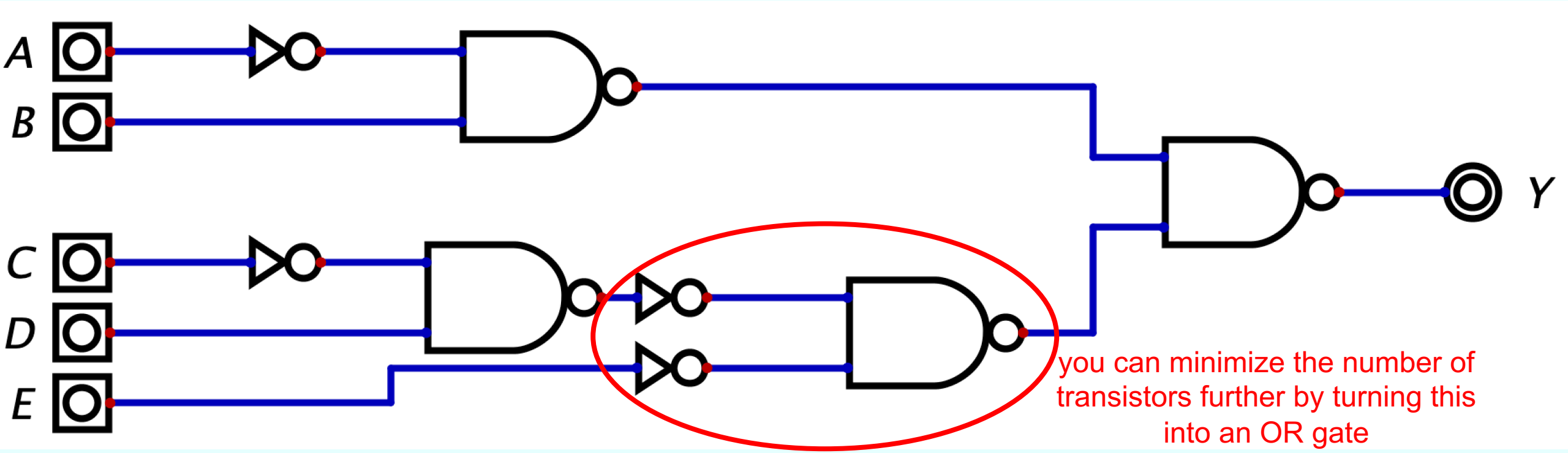


Original Transistor Count: 32

Final Transistor Count: 24

Minimizing Transistor Count

Minimize the number of transistors in this circuit by implementing it using only NAND gates and inverters. Compare the number of transistors in the original circuit and the new circuit.

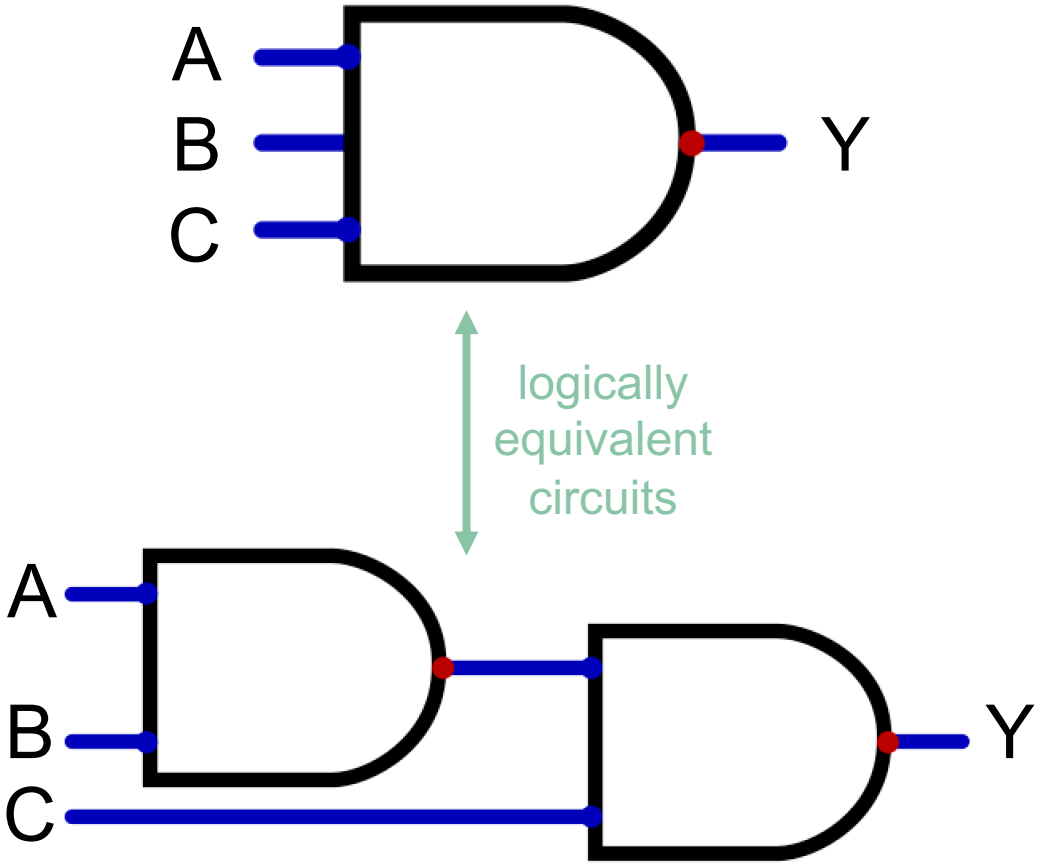


Original Transistor Count: 32

Final Transistor Count: 24

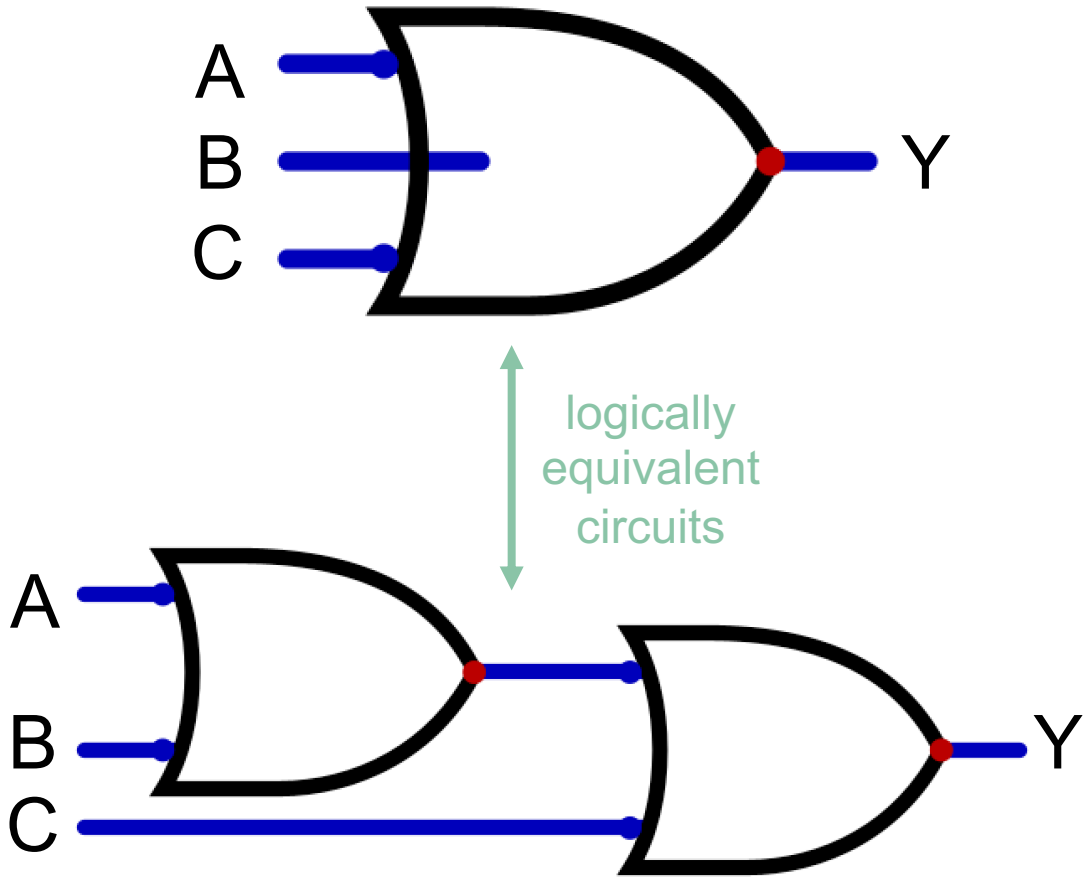
Gates with more than 2 inputs

3-input AND



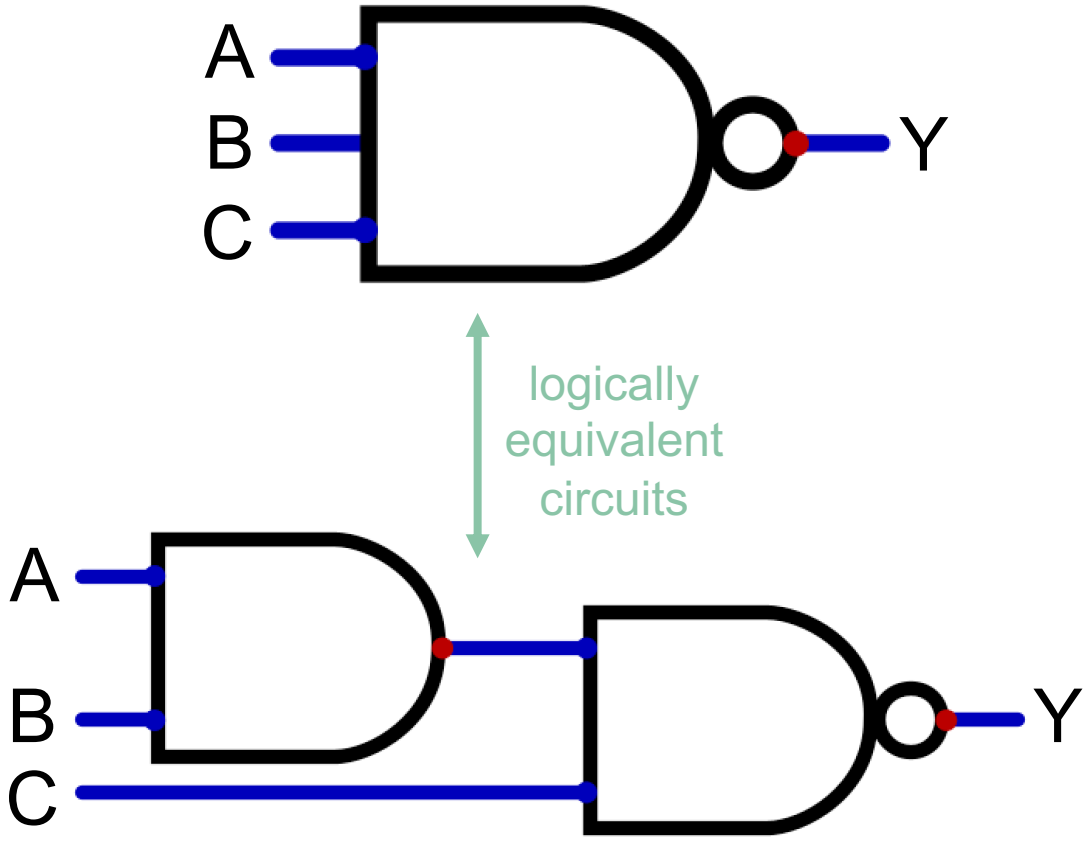
A	B	C	Y
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	1

3-input OR



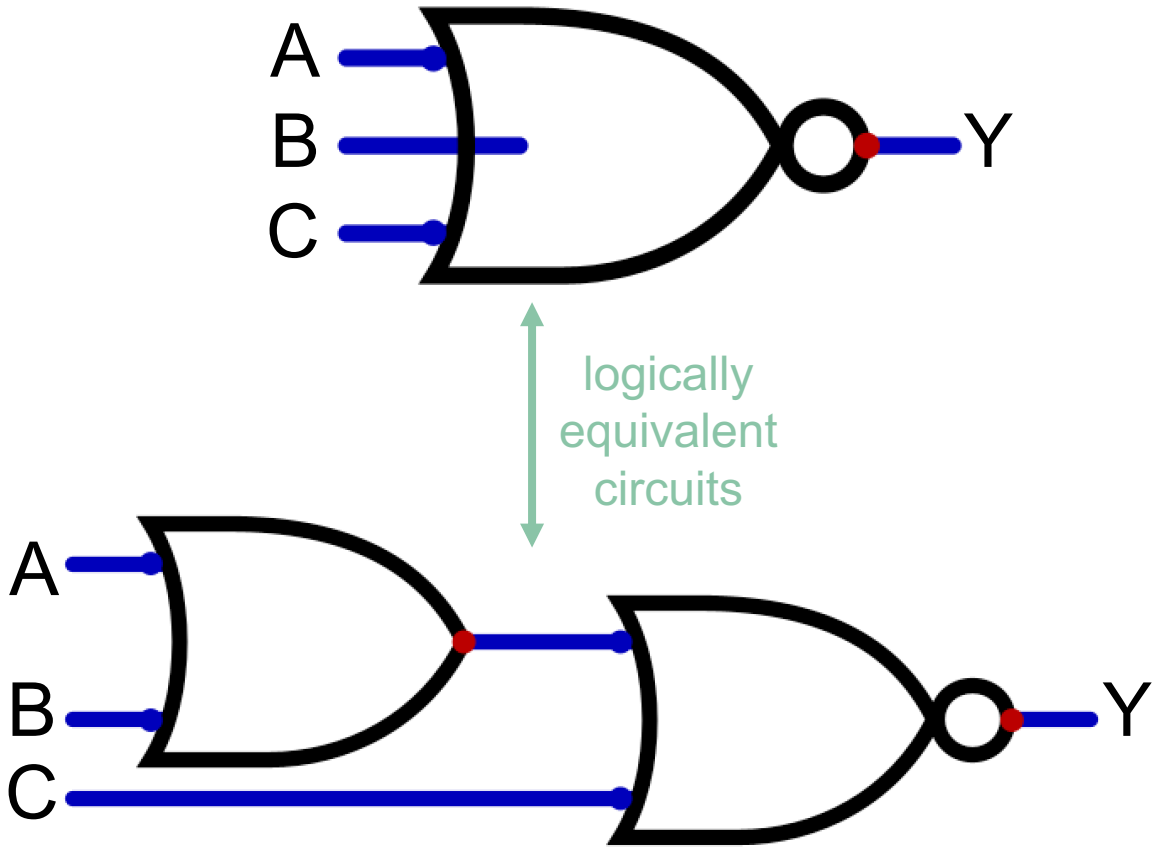
A	B	C	Y
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	1

3-input NAND



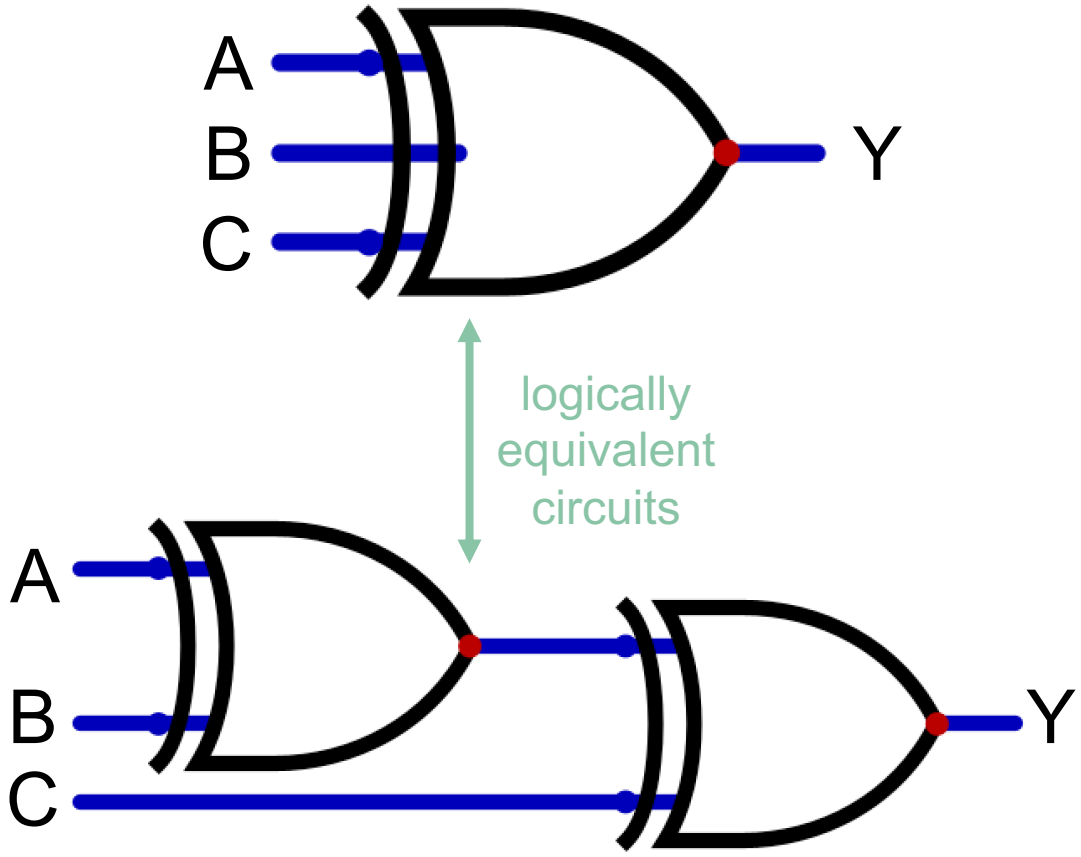
A	B	C	Y
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

3-input NOR



A	B	C	Y
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	0

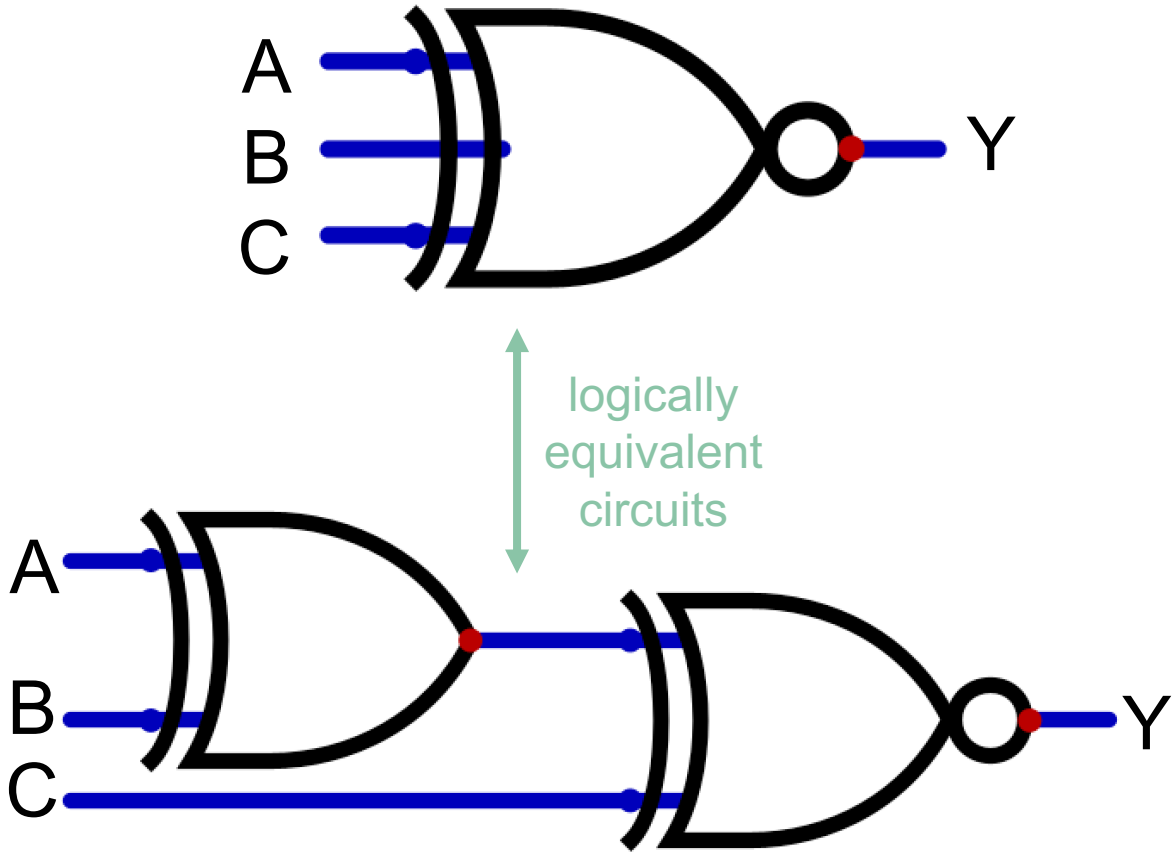
3-input XOR



A	B	C	Y
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

For any number of inputs, the output is 1 when an odd number of inputs is 1

3-input XNOR



A	B	C	Y
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	0