Exp-2: Learning VHDL through Combinational Circuit Design

## Objectives:

The objectives of this laboratory are:

1. Learn the basic programming style of VHDL module and VHDL TestBench
2. Design a Full-Adder using three types of Architecture of VHDL
3. Design a 4-bit Parallel Adder.

## Required circuits diagrams



Fig 1. Logic Diagram of Half-adder



Fig 2. Logic Diagram of Full-adder



Fig 3. Logic Diagram of 4-bit parallel-adder