Exp-3: Learning VHDL through Sequential Circuit Design

## Objectives:

The objectives of this laboratory are:

1. Design a JK Flip-flop T Flip-flop and D Flip-flop in VHDL
2. Design a 4-bit register and a 4-bit counter in VHDL
3. Design a 4-bit shift-register in VHDL

## Required diagrams

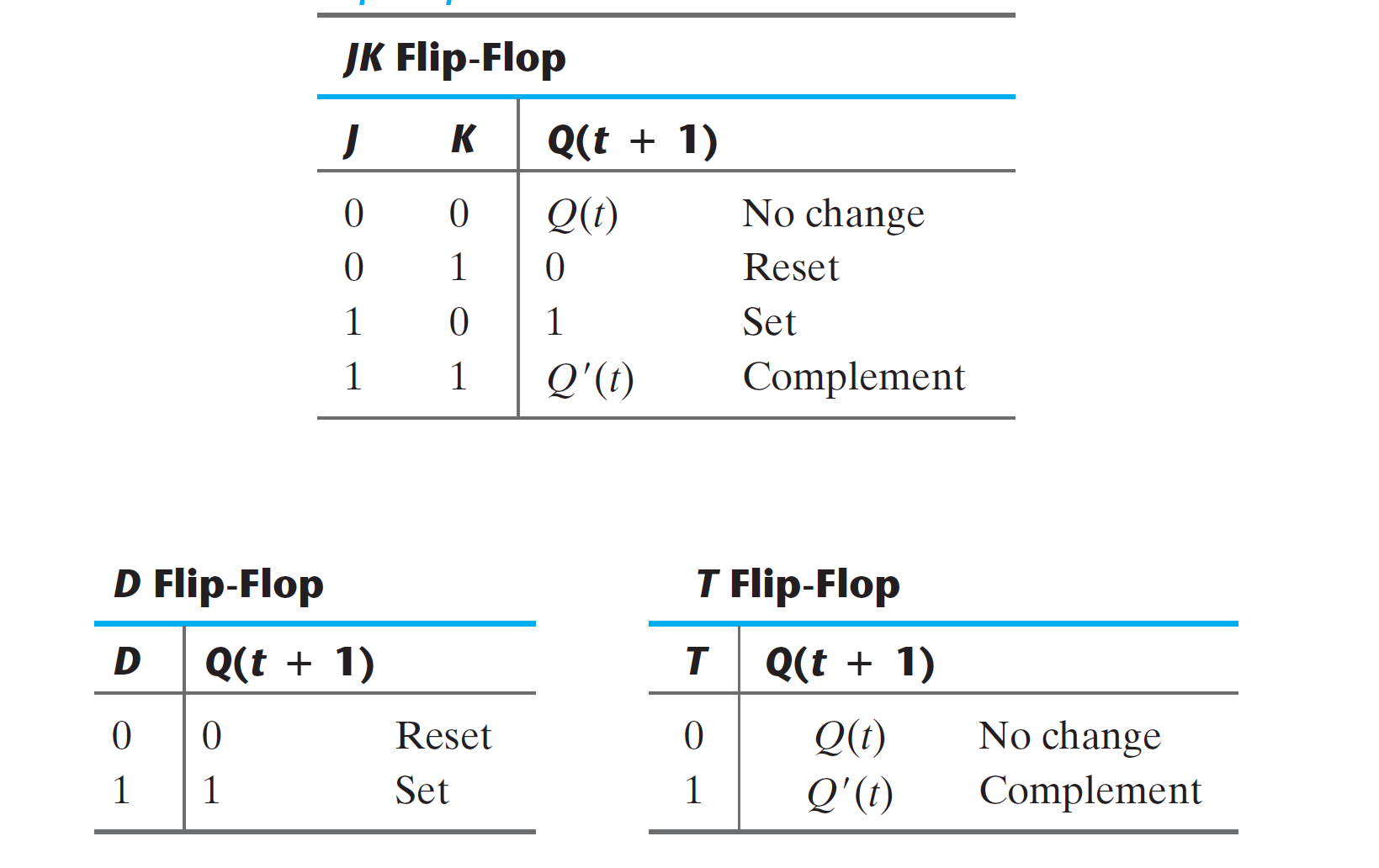


Fig. 1 Characteristic Tables of FFs

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Fig 2. Logic Diagram of a 4-bit register