

MAVEN SILICON

RISC-V RV32I RTL Design using Verilog HDL

VLSI Design Internship Project Report

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Faculty name: Sushmita Nayak

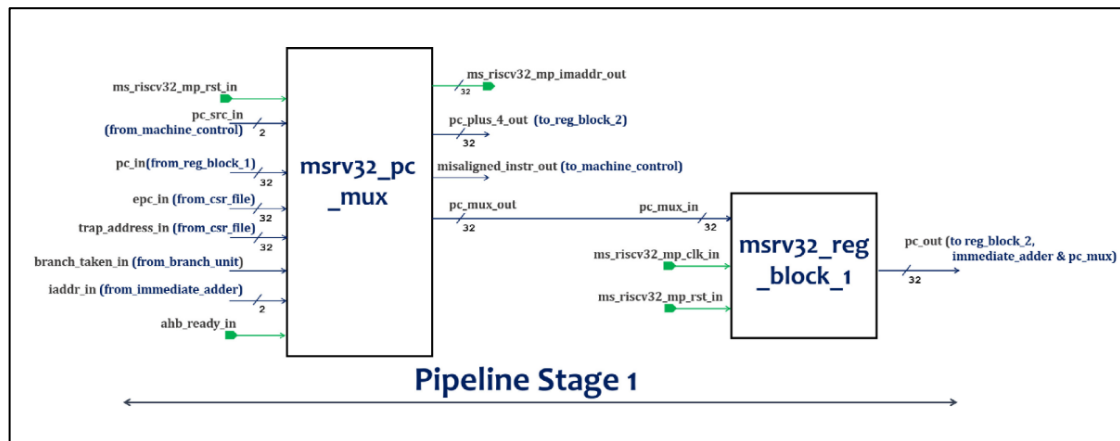
11-2-2023

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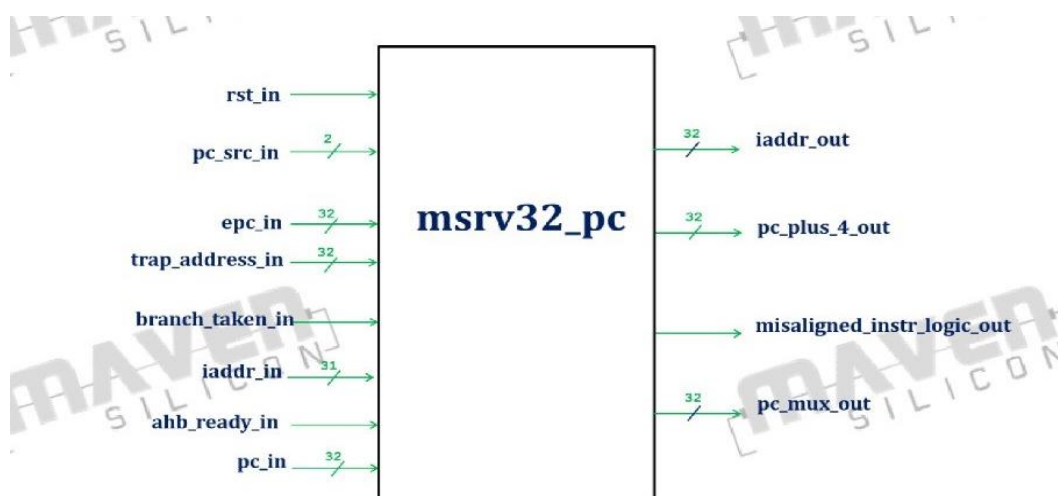
Three stages of pipelining with the subblocks and its synthesis diagram and waveform:

Pipelining stage 01:

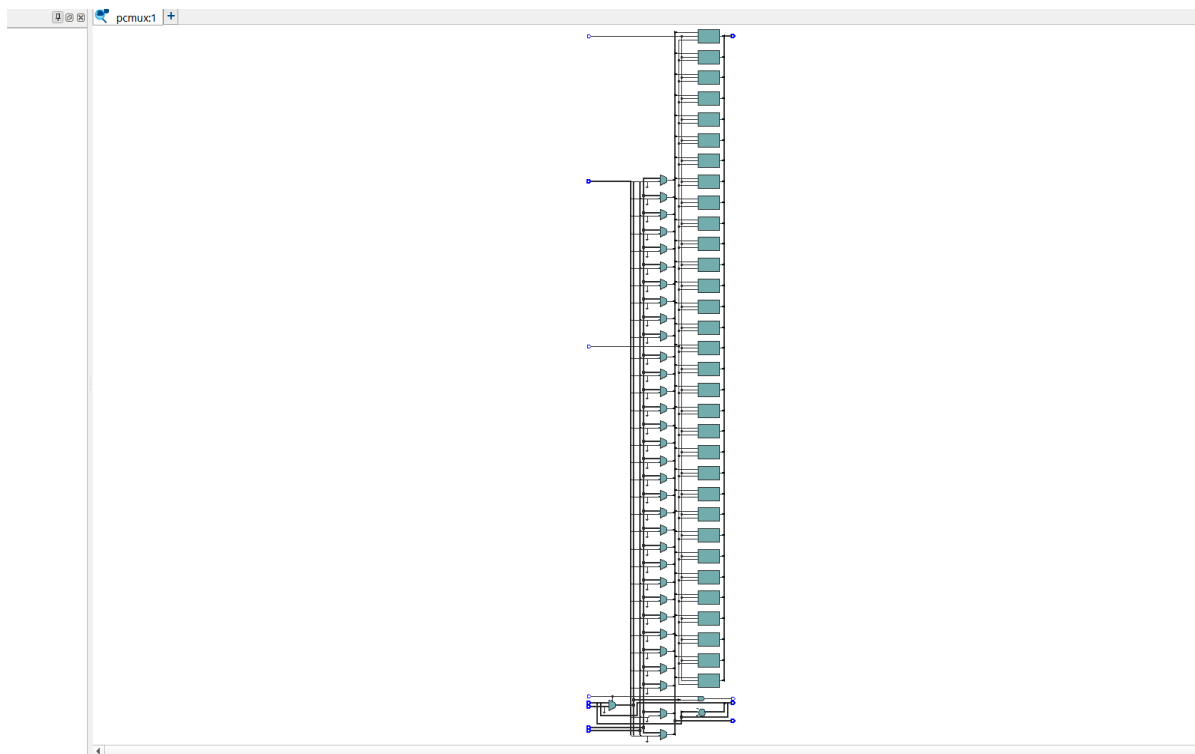


1) PC MUX:

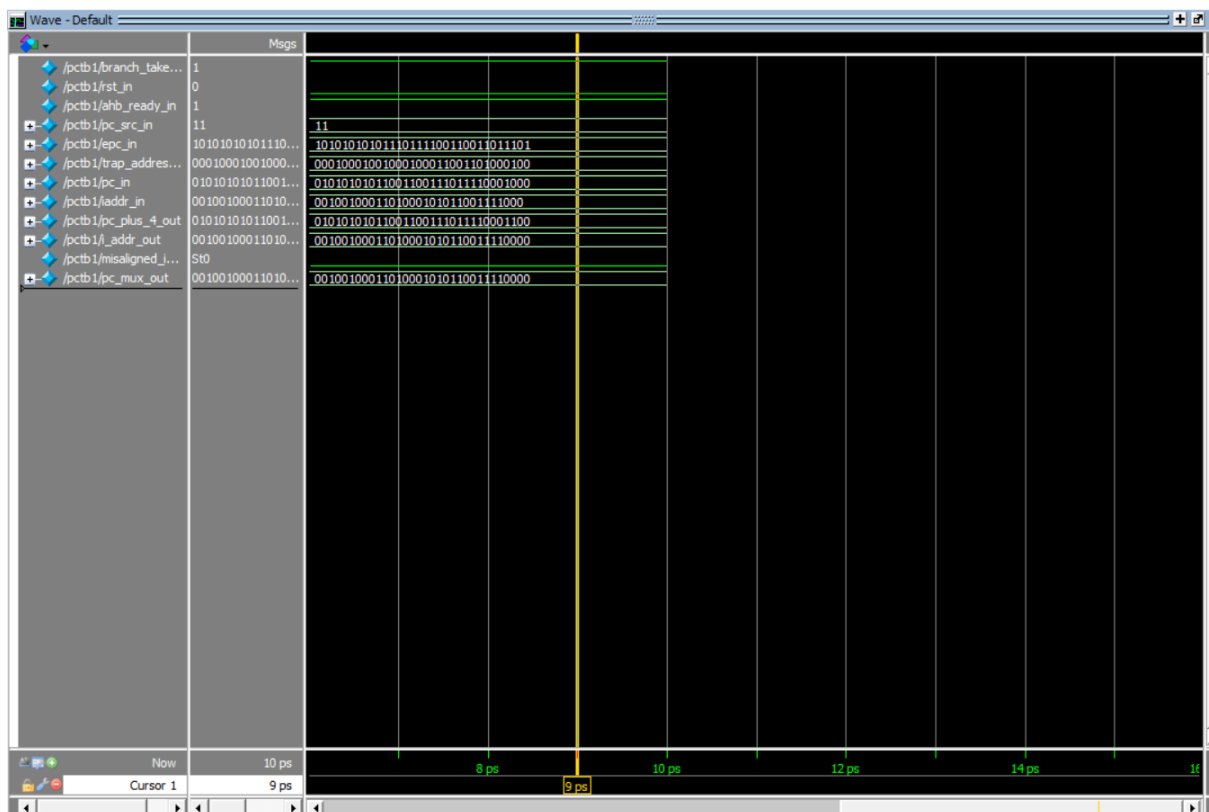
Block diagram:



Synthesis diagram:

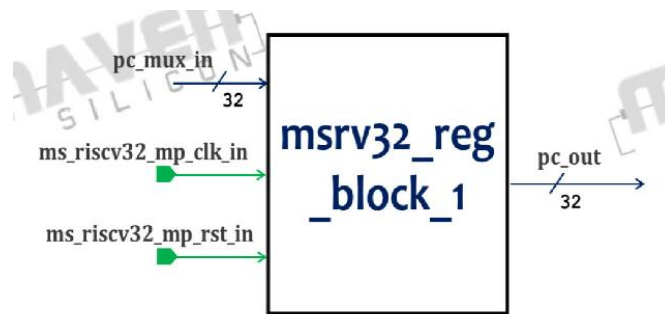


Waveform:

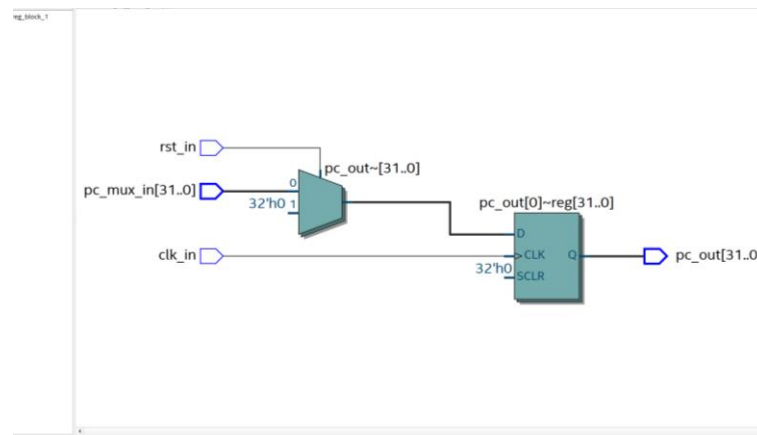


2) Register Block one:

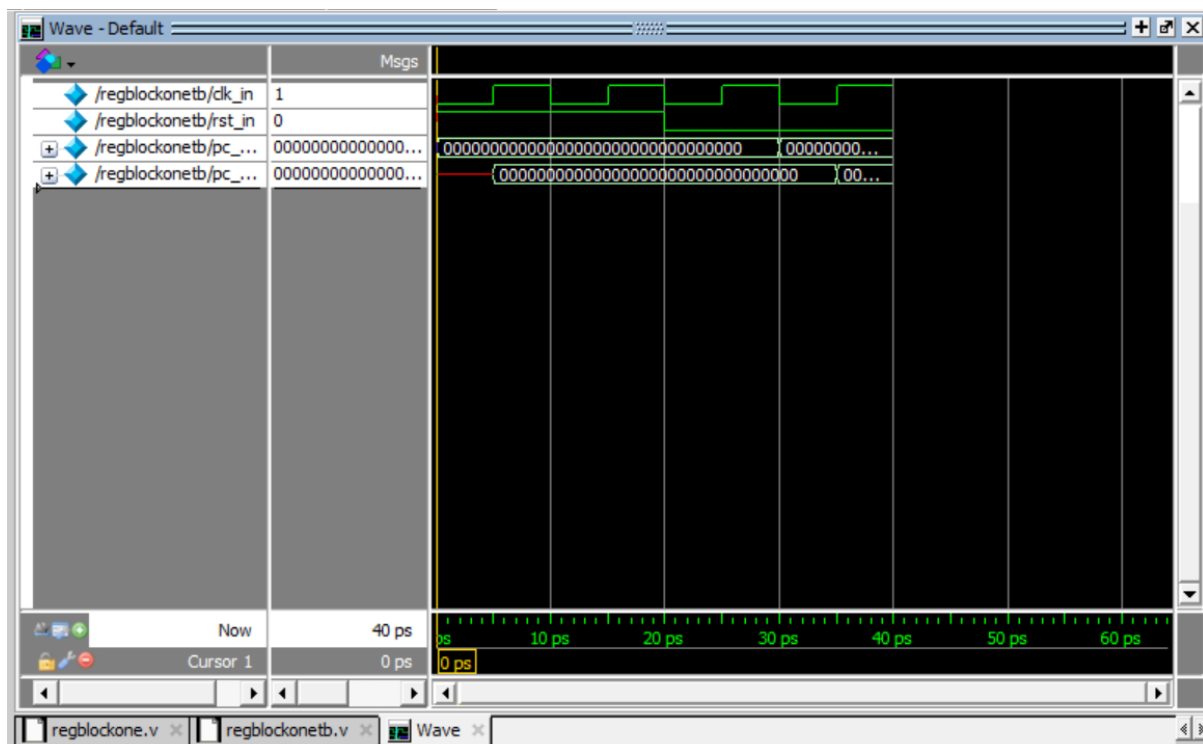
Block diagram:



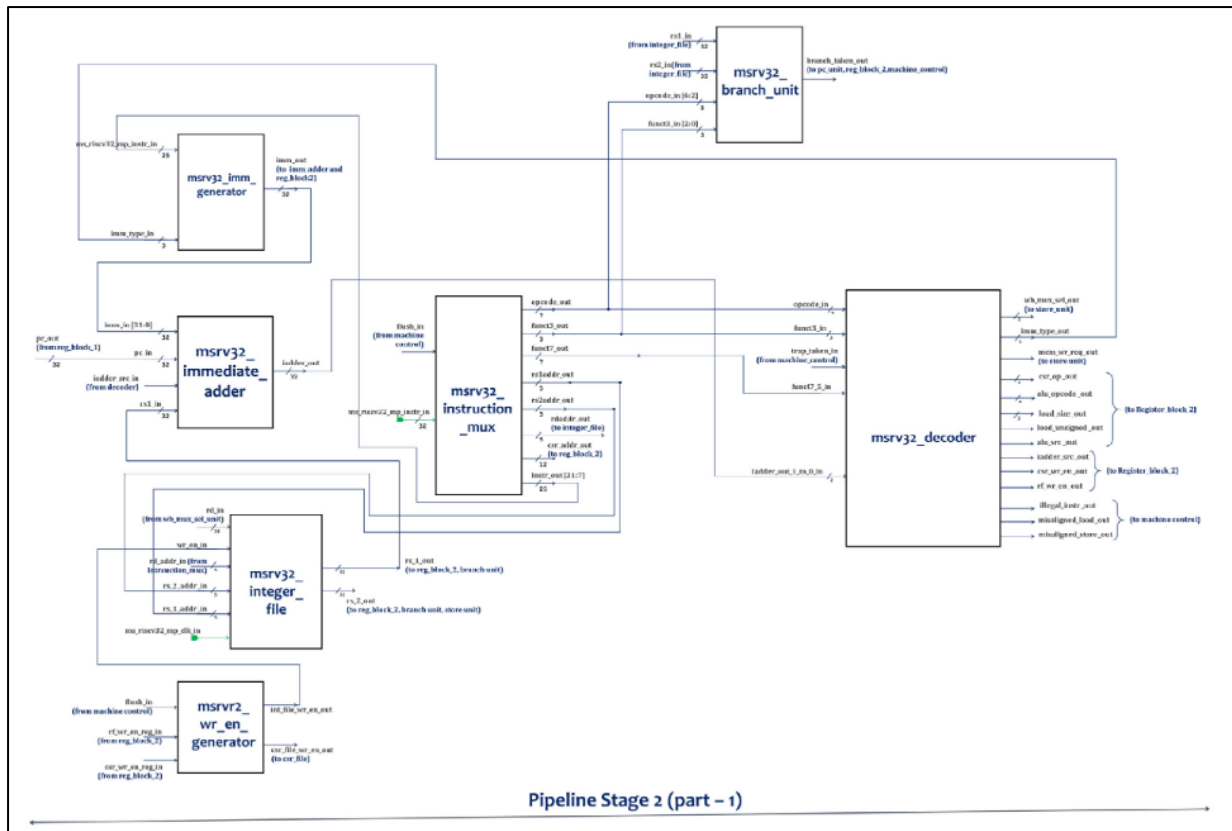
Synthesis diagram:



Waveform:

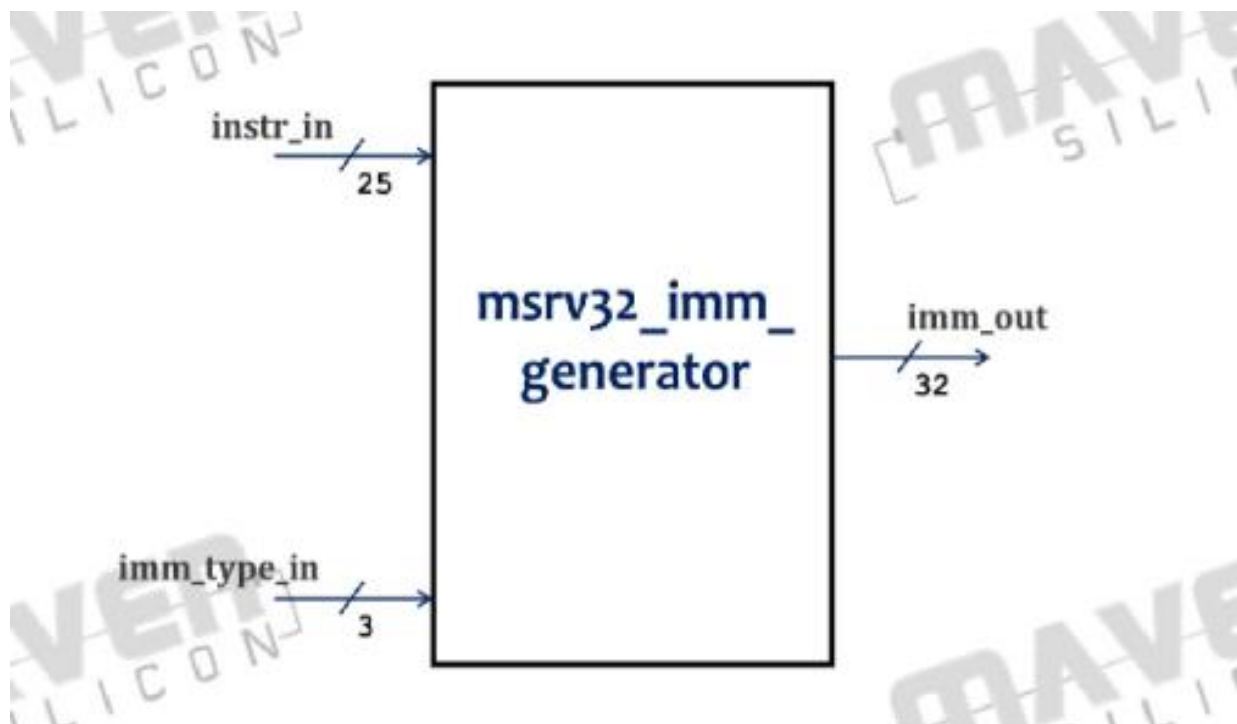


Pipelining stage 02: Part one

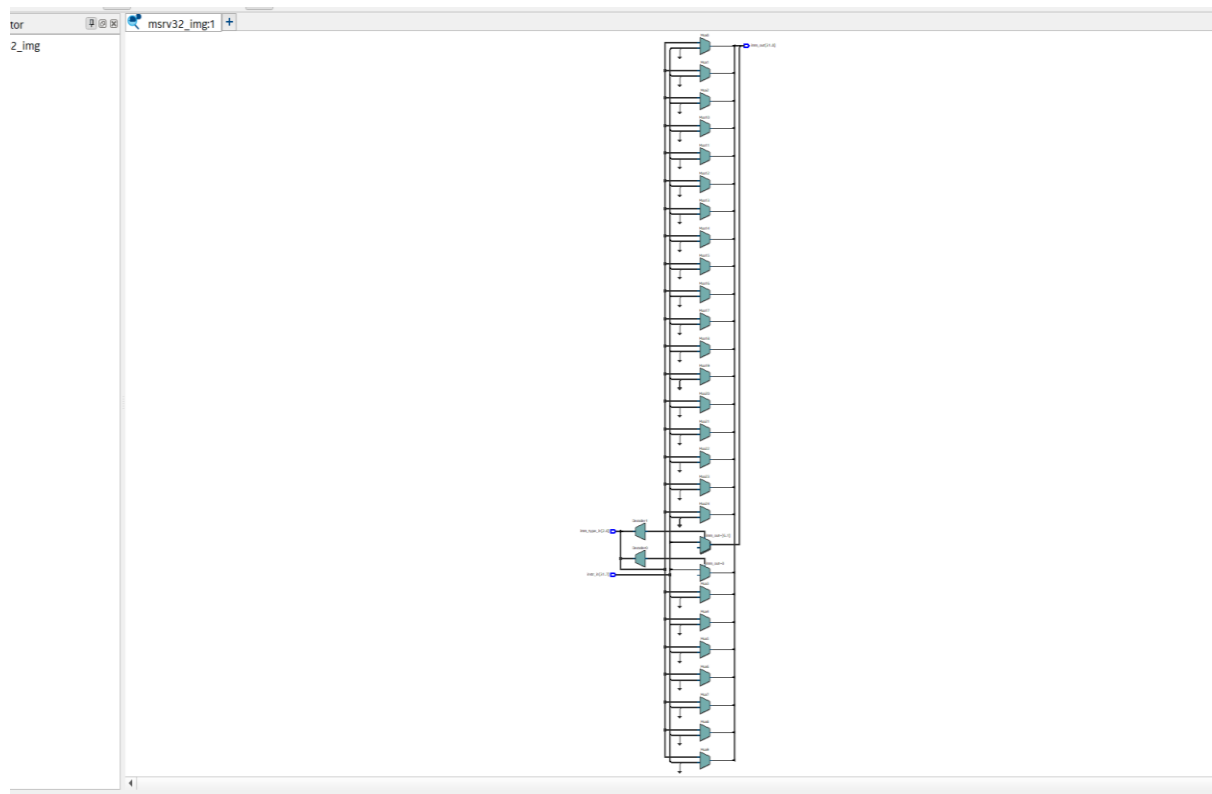


1) Immediate generator:

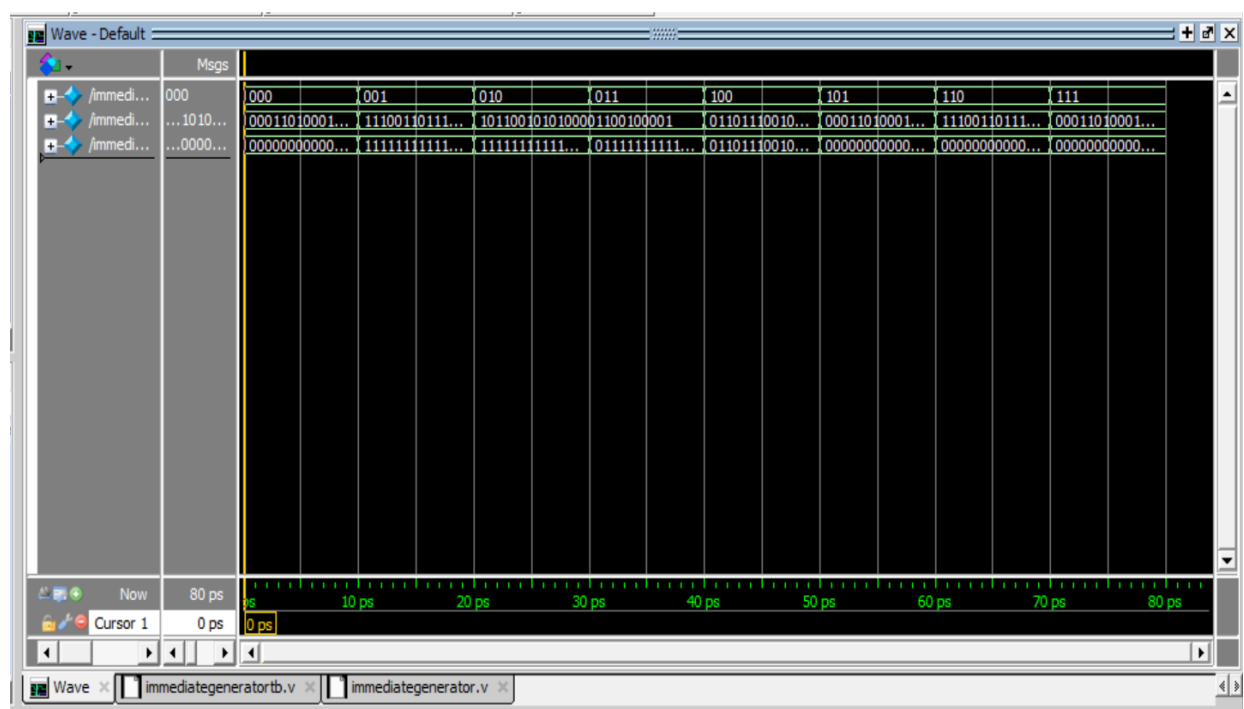
Block diagram:



Synthesis diagram:

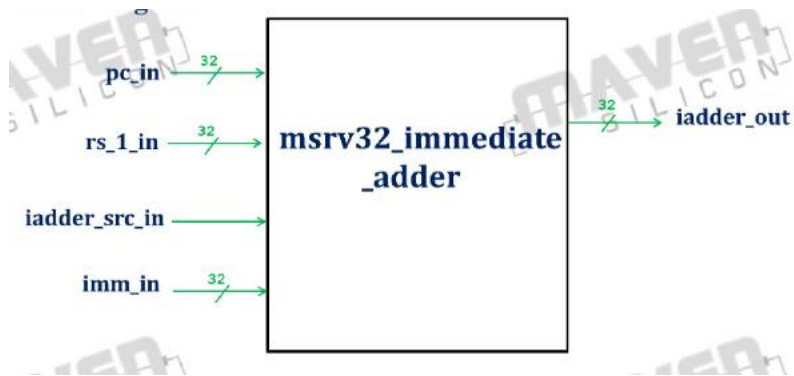


Waveform:

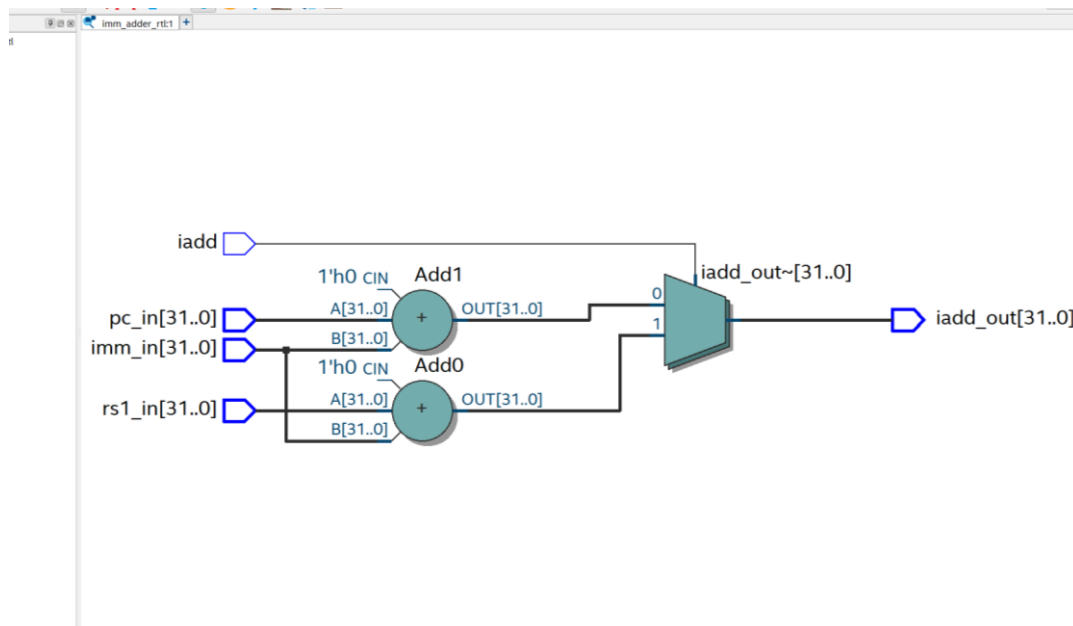


2) Immediate adder:

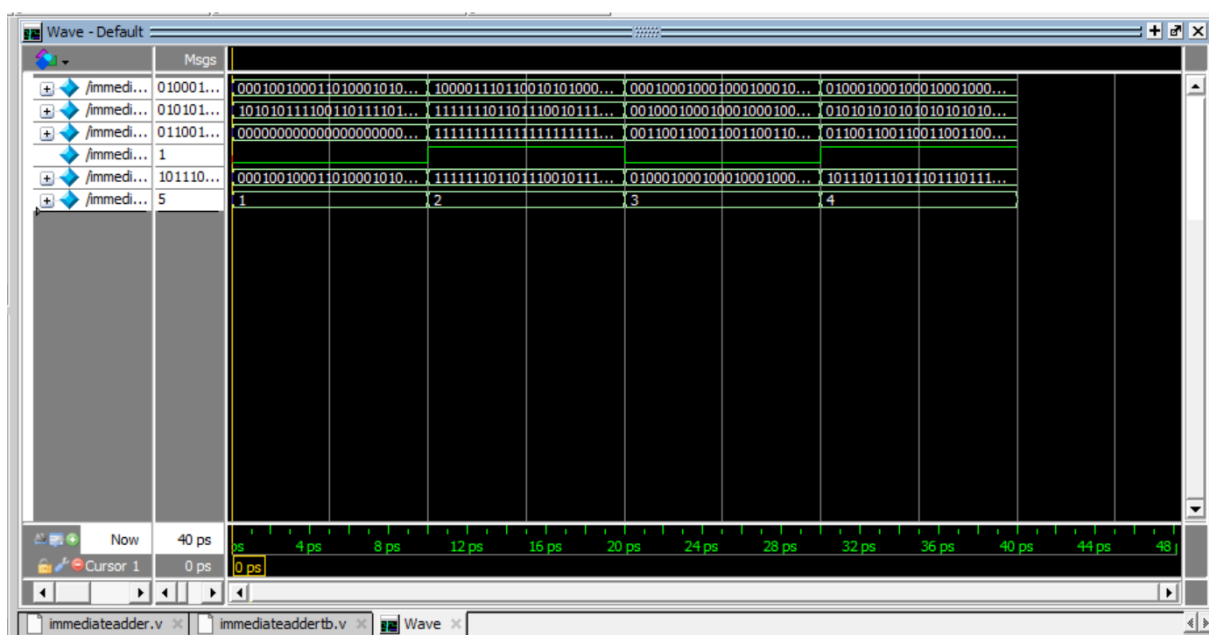
Block diagram:



Synthesis diagram:

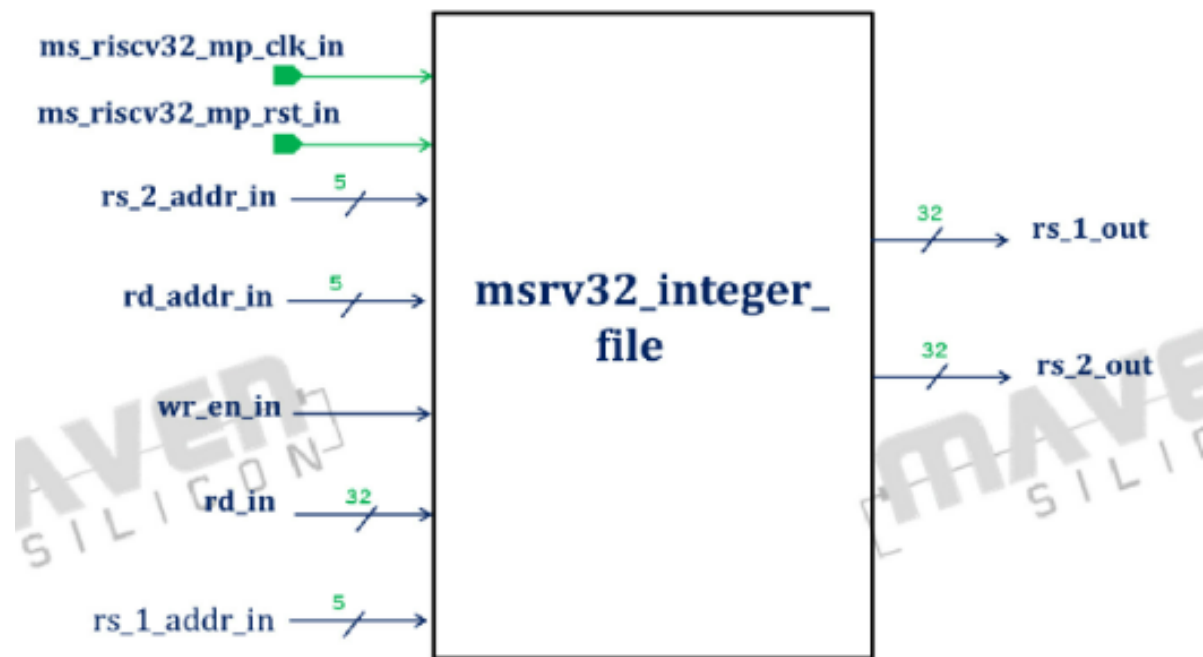


Waveform:

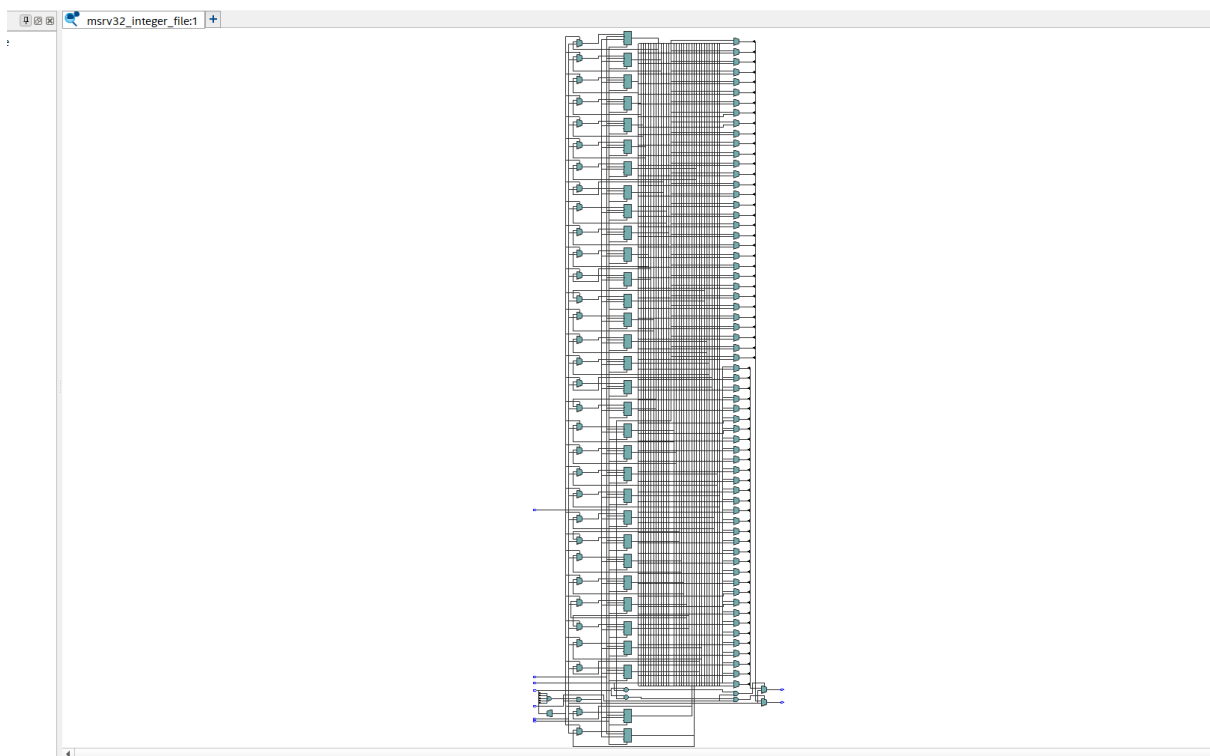


3) Integer file:

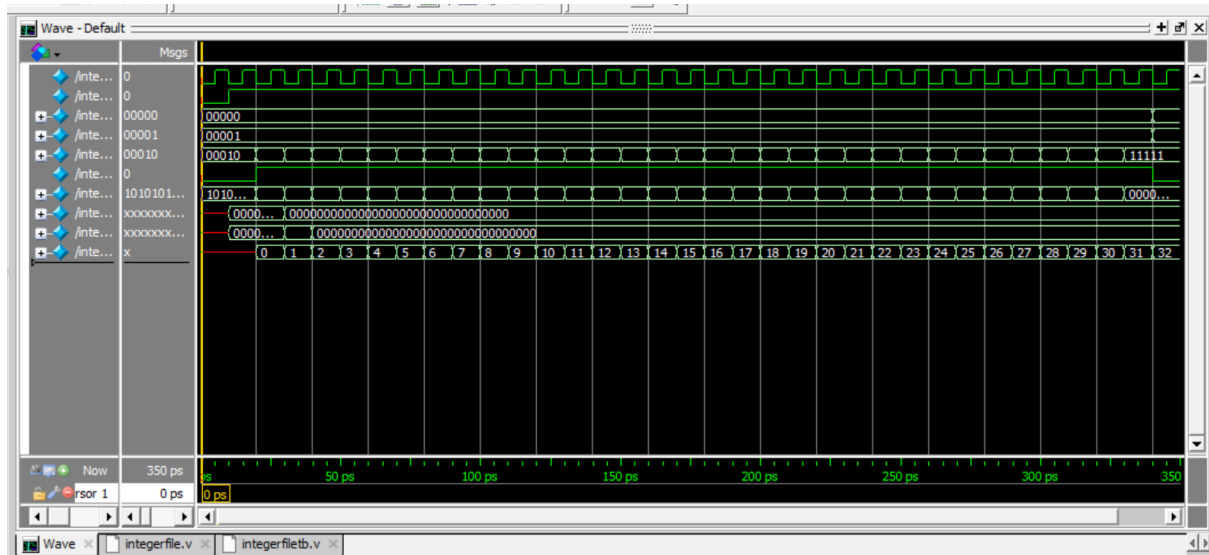
Block diagram:



Synthesis diagram:

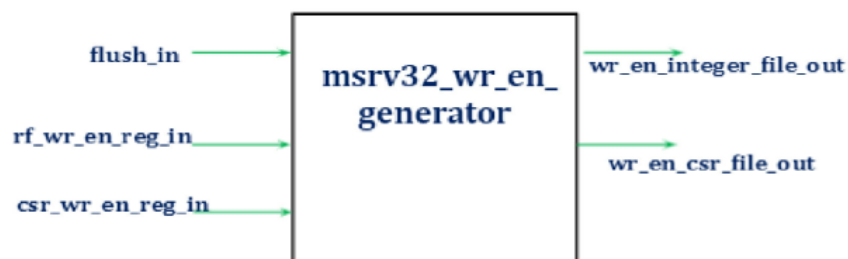


Waveform:

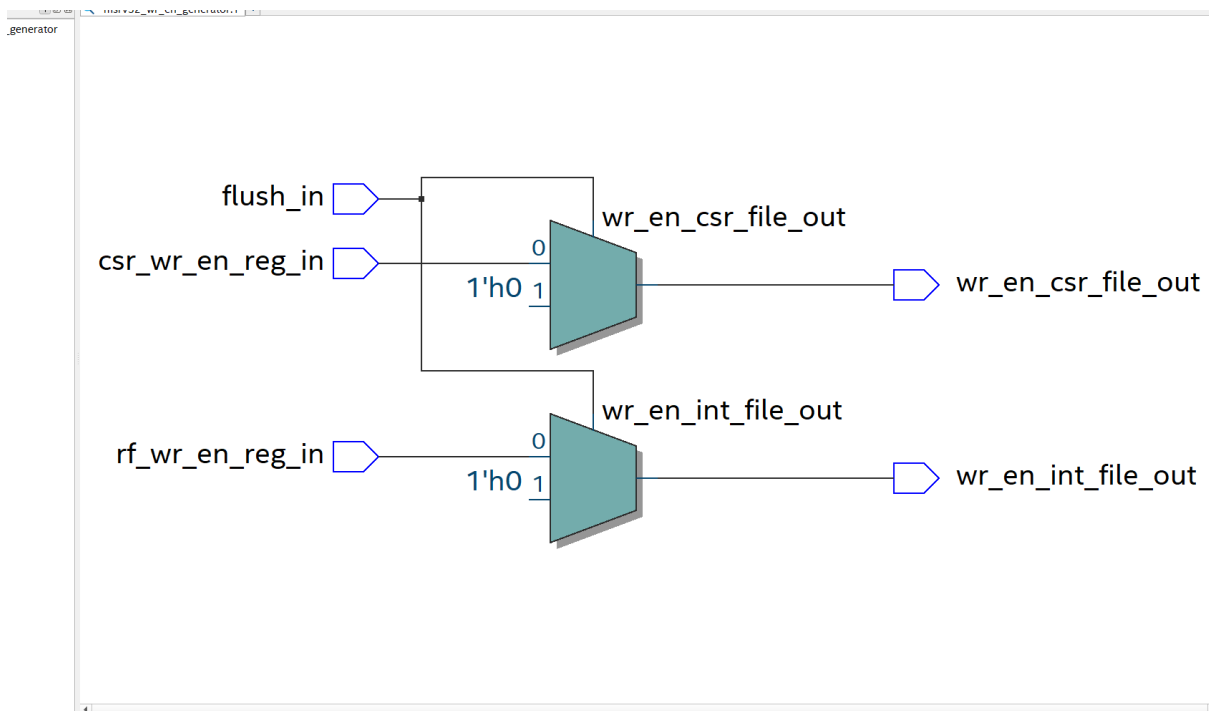


4) Write enable generator:

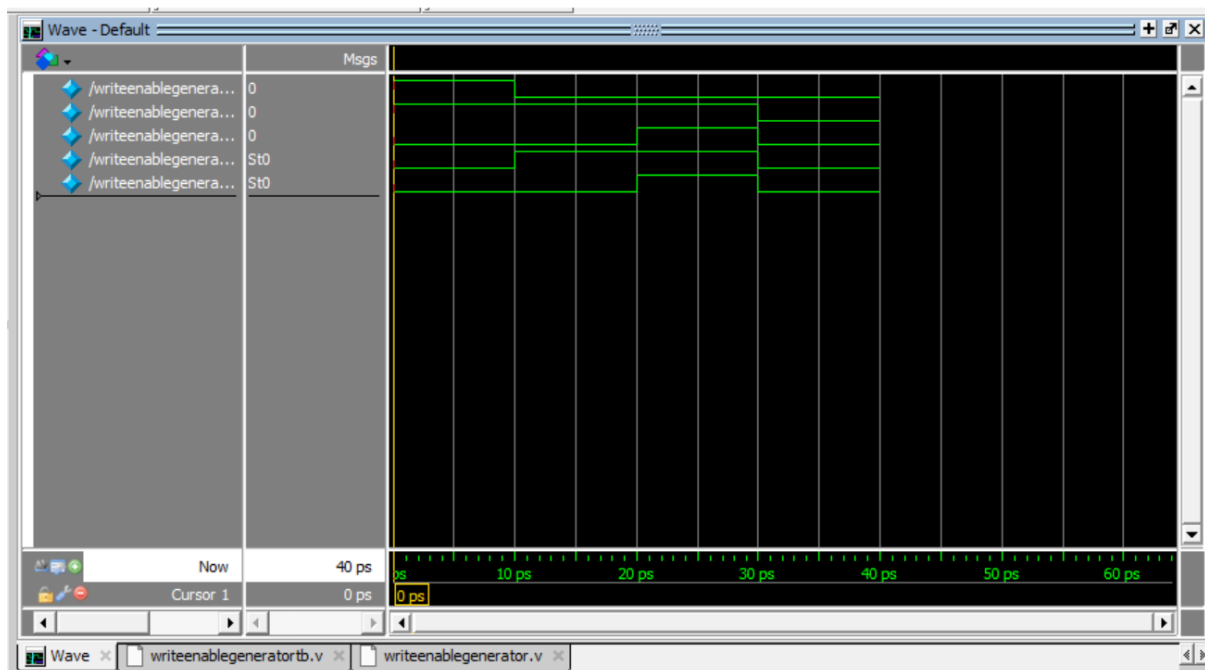
Block diagram:



Synthesis diagram:

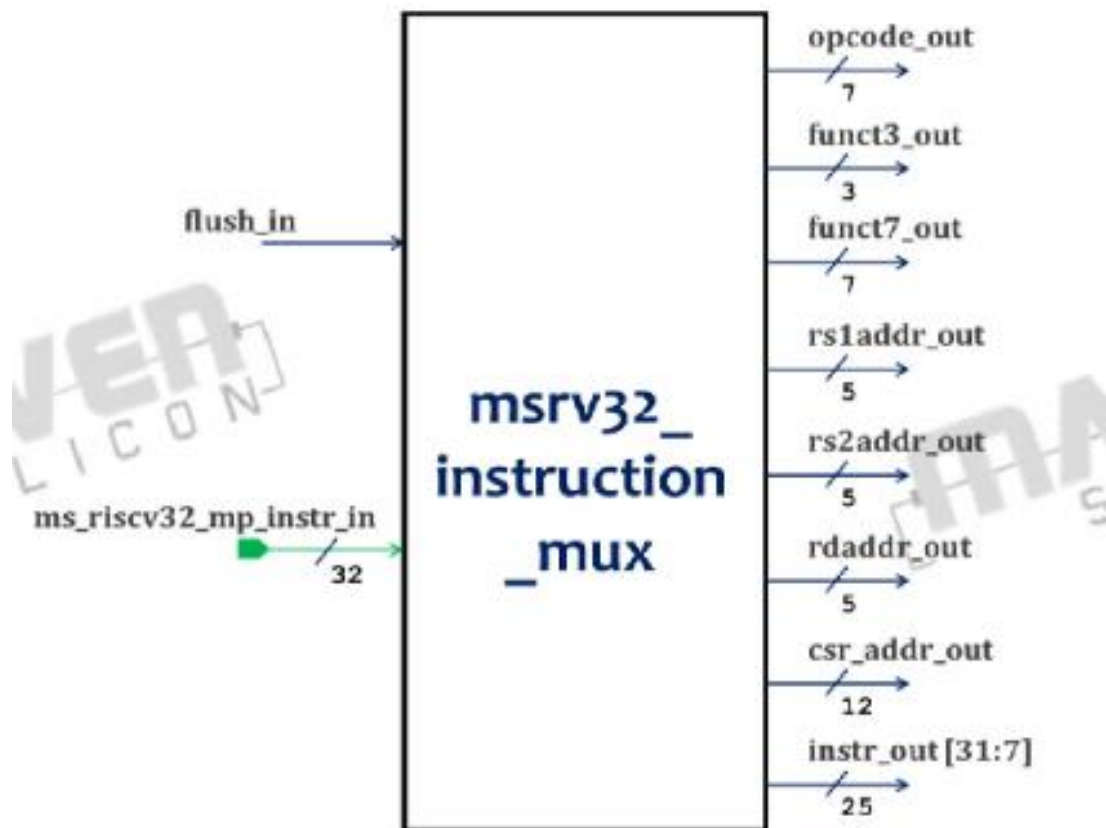


Waveform:

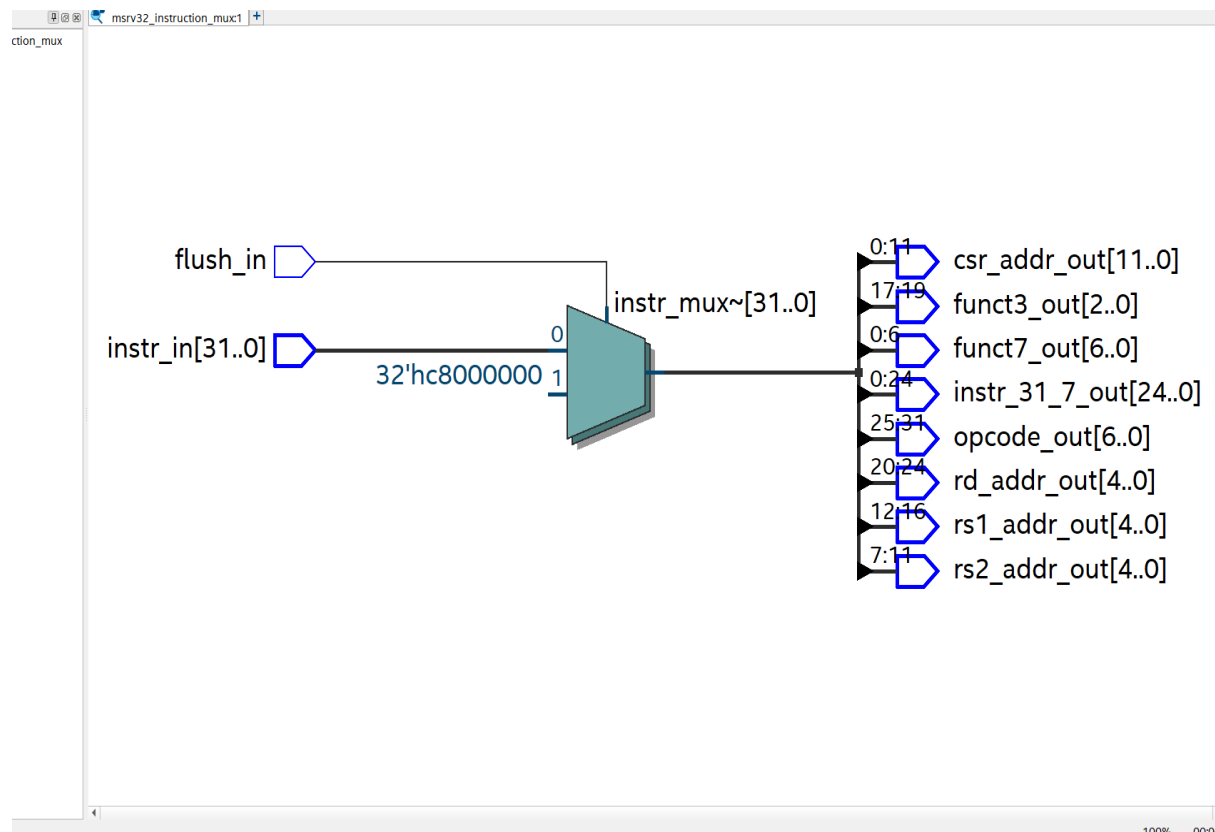


5) Instruction MUX:

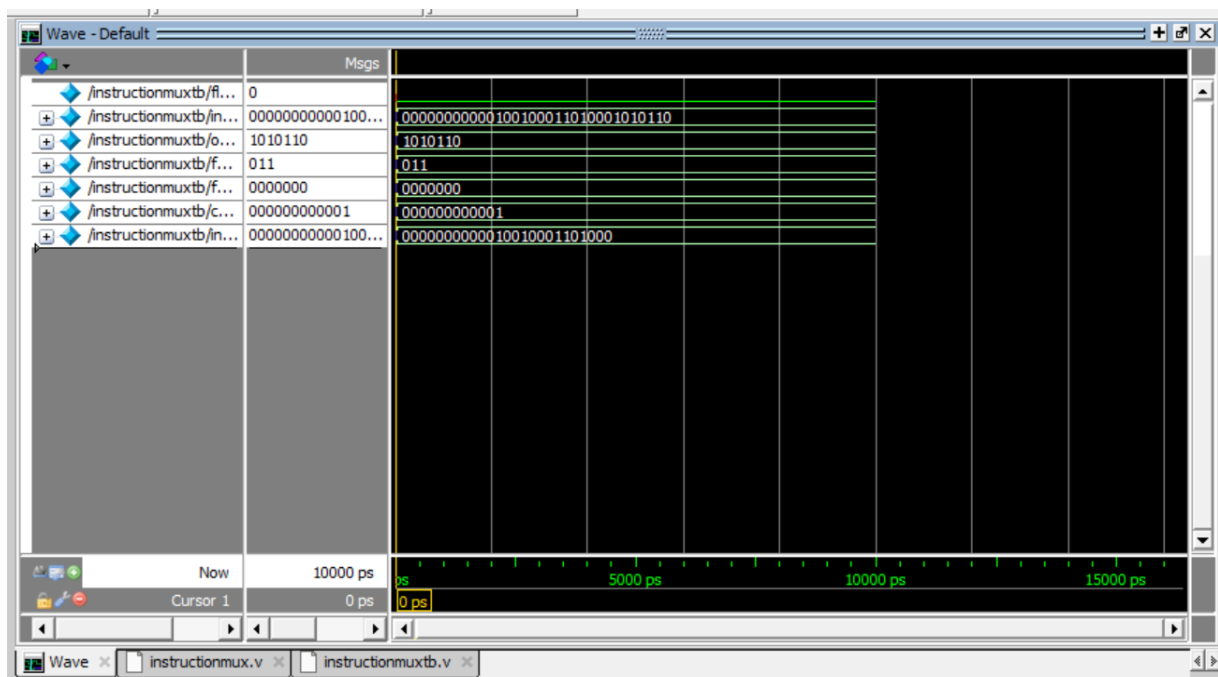
Block diagram:



Synthesis diagram:

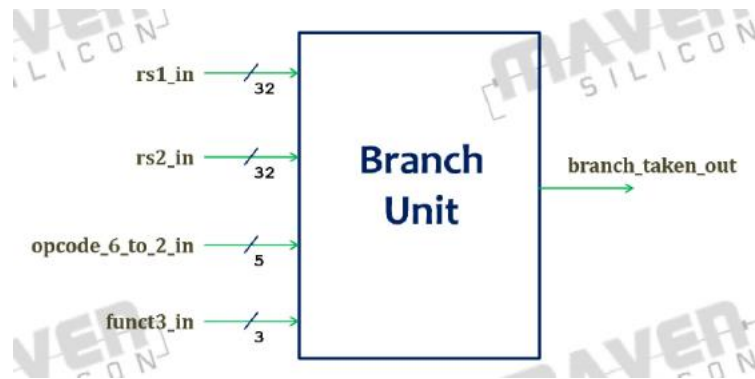


Waveform:

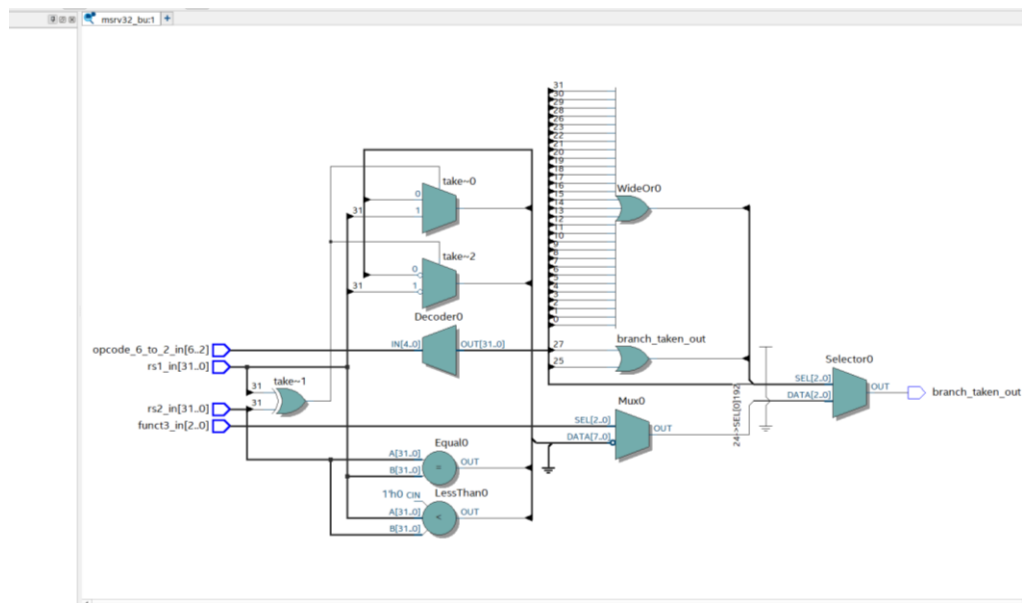


6) Branch unit:

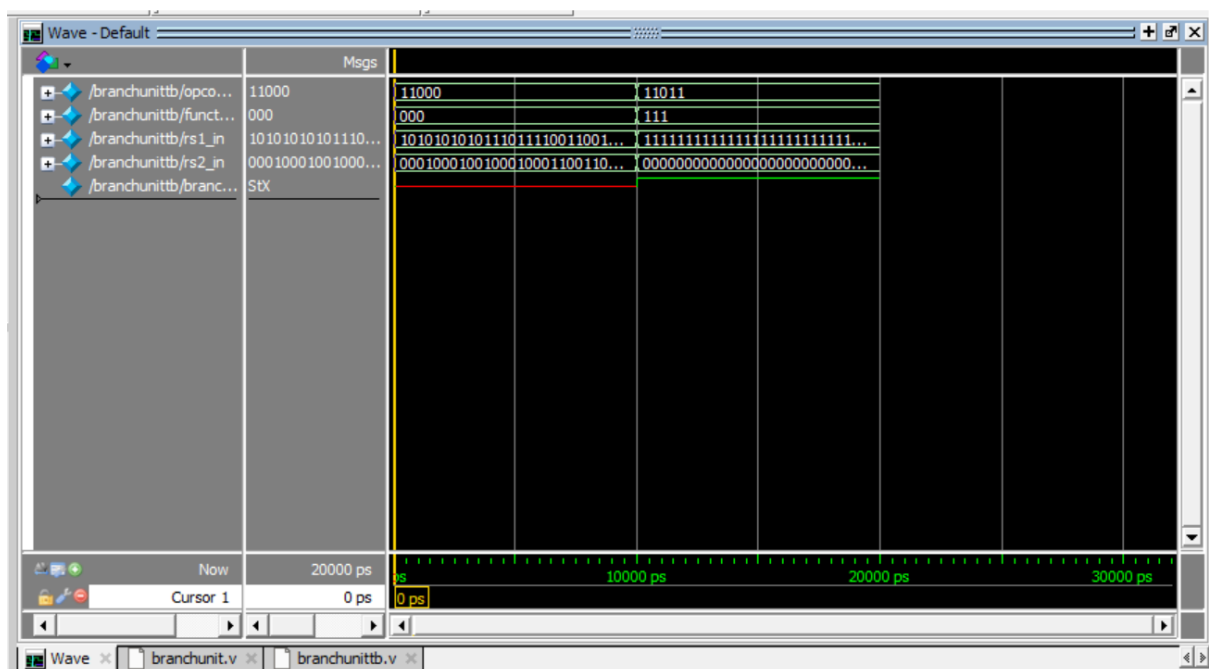
Block diagram:



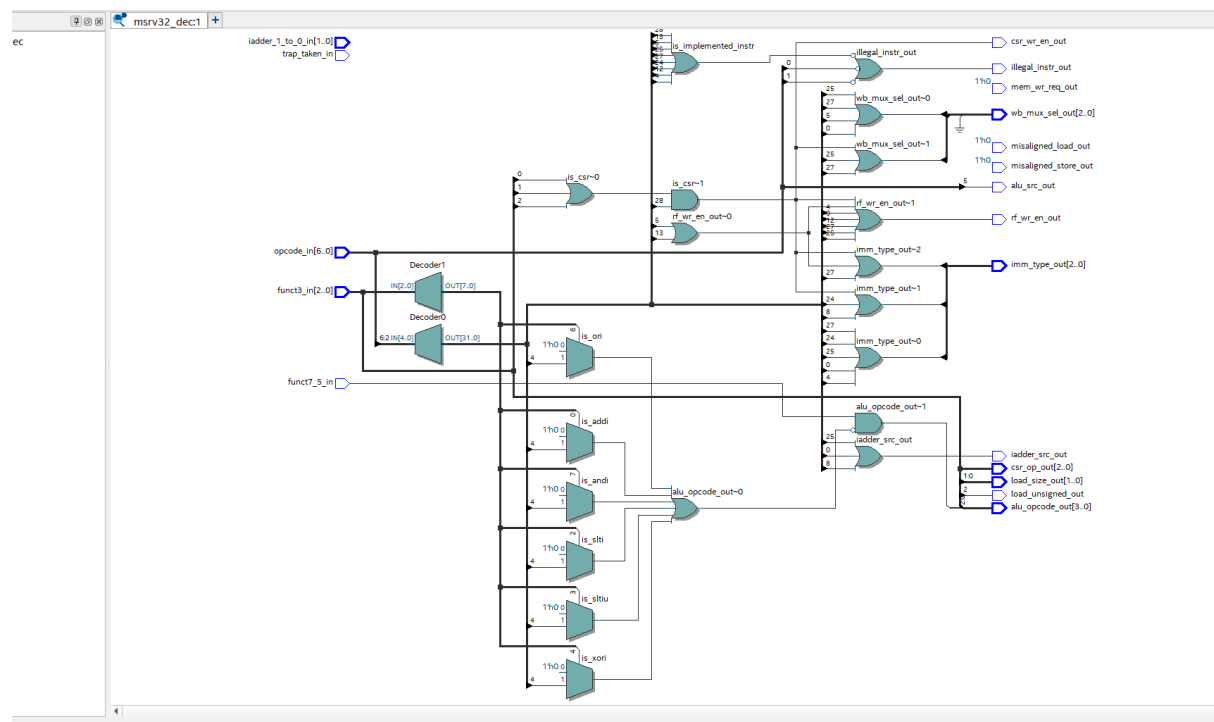
Synthesis diagram:



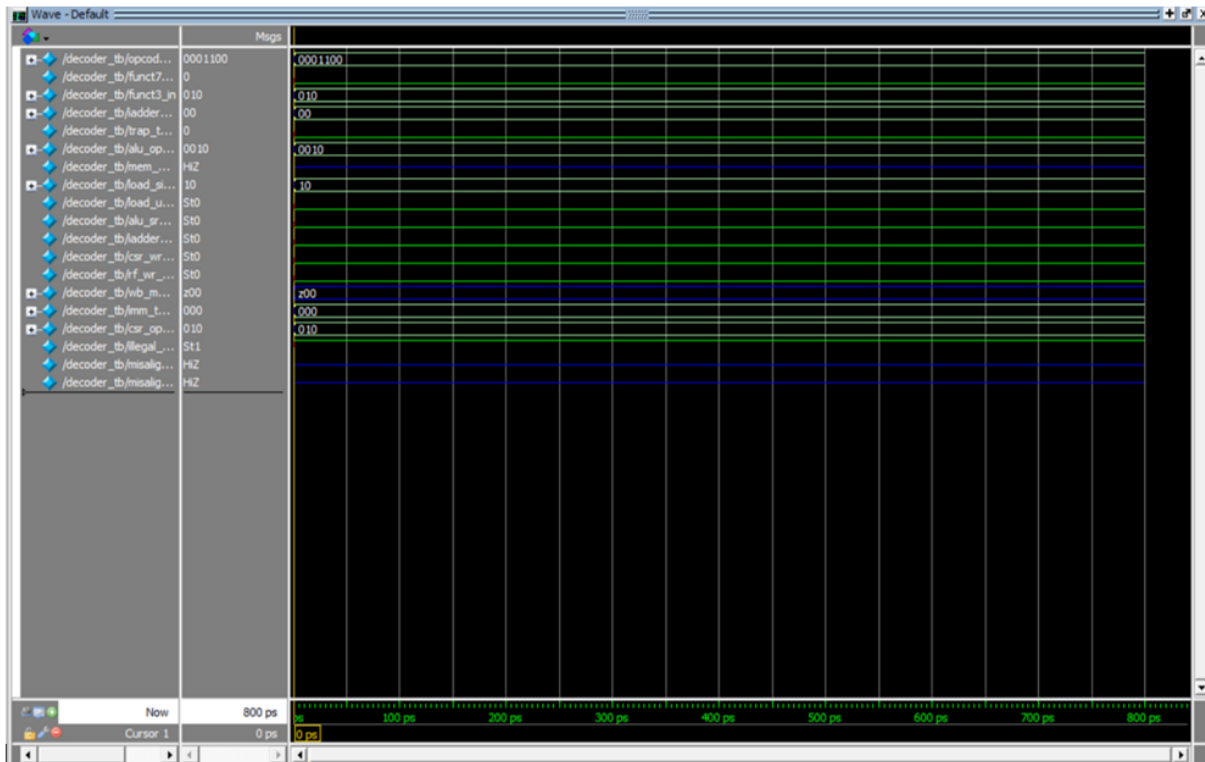
Waveform:



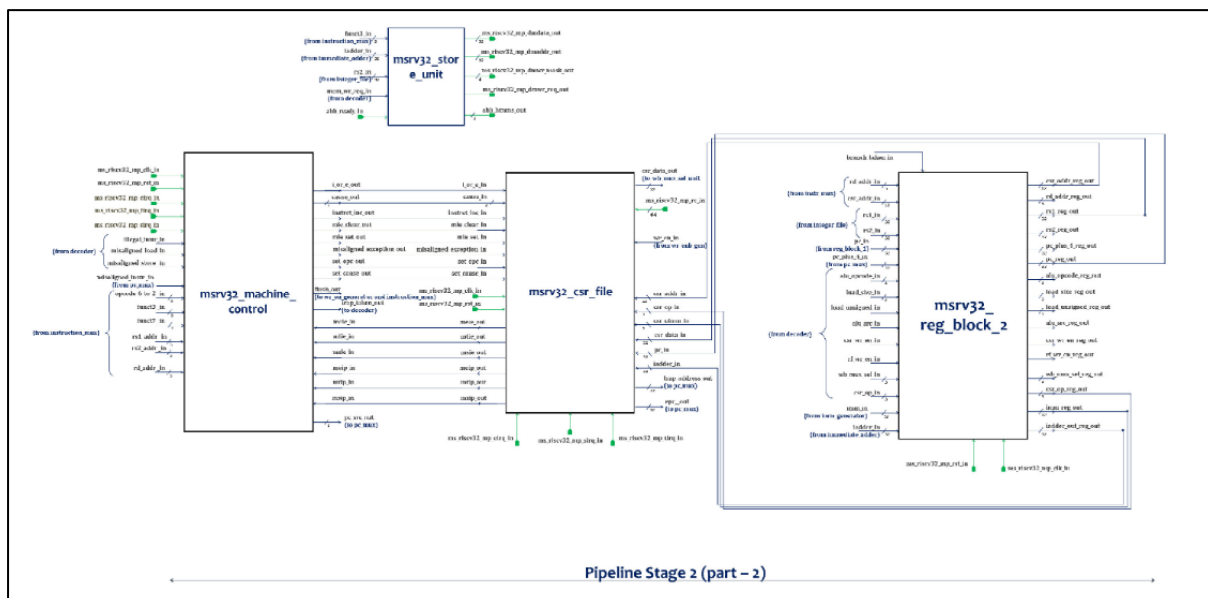
Block diagram:



Waveform:

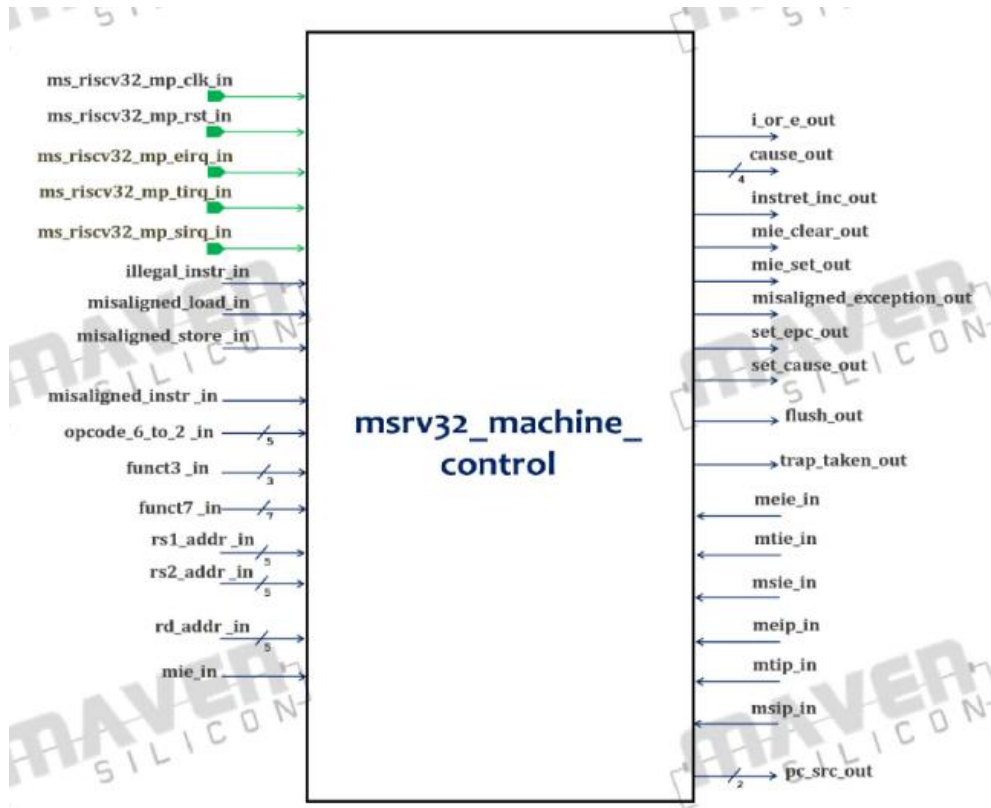


Pipelining stage 02: Part two



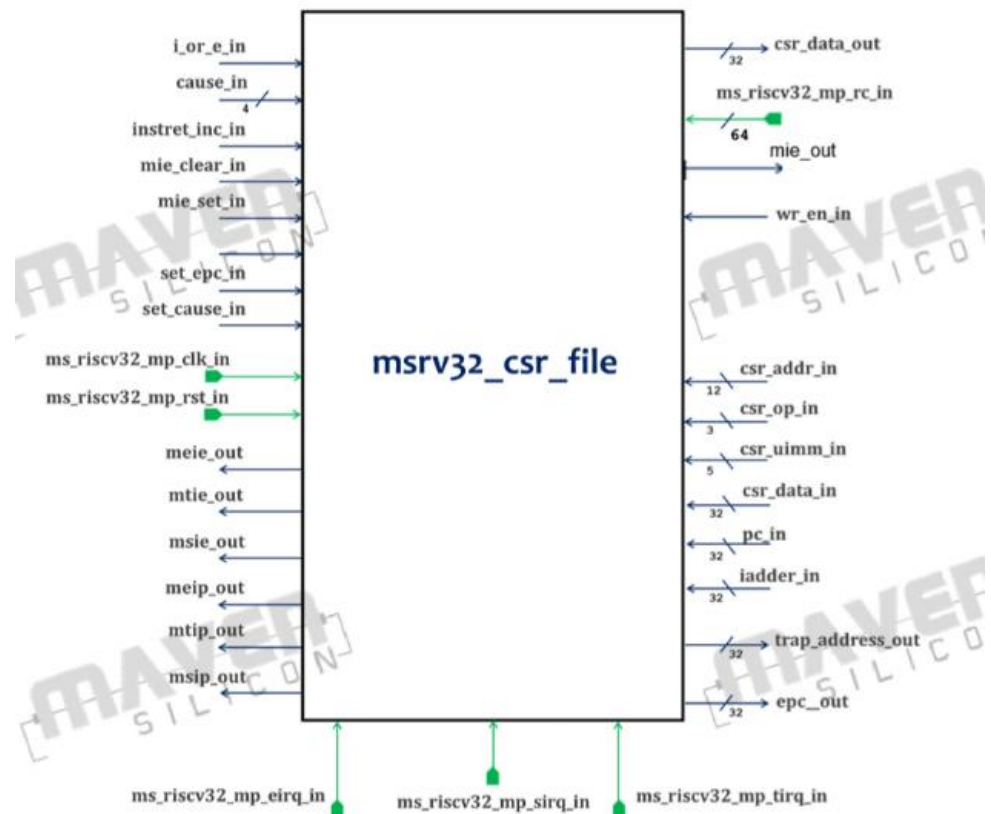
1) Machine control:

Block diagram:



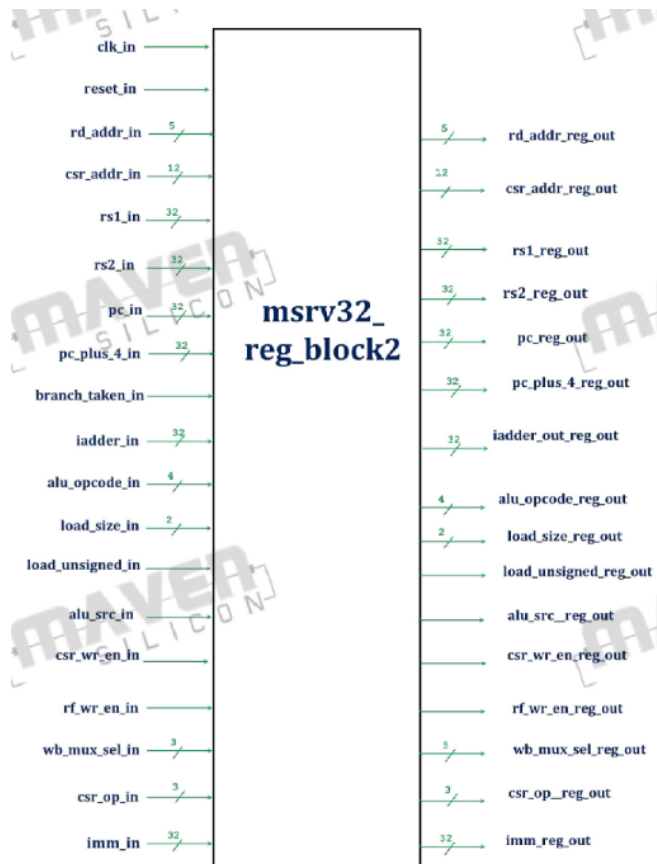
2) CSR file:

Block diagram:



3) Register block two:

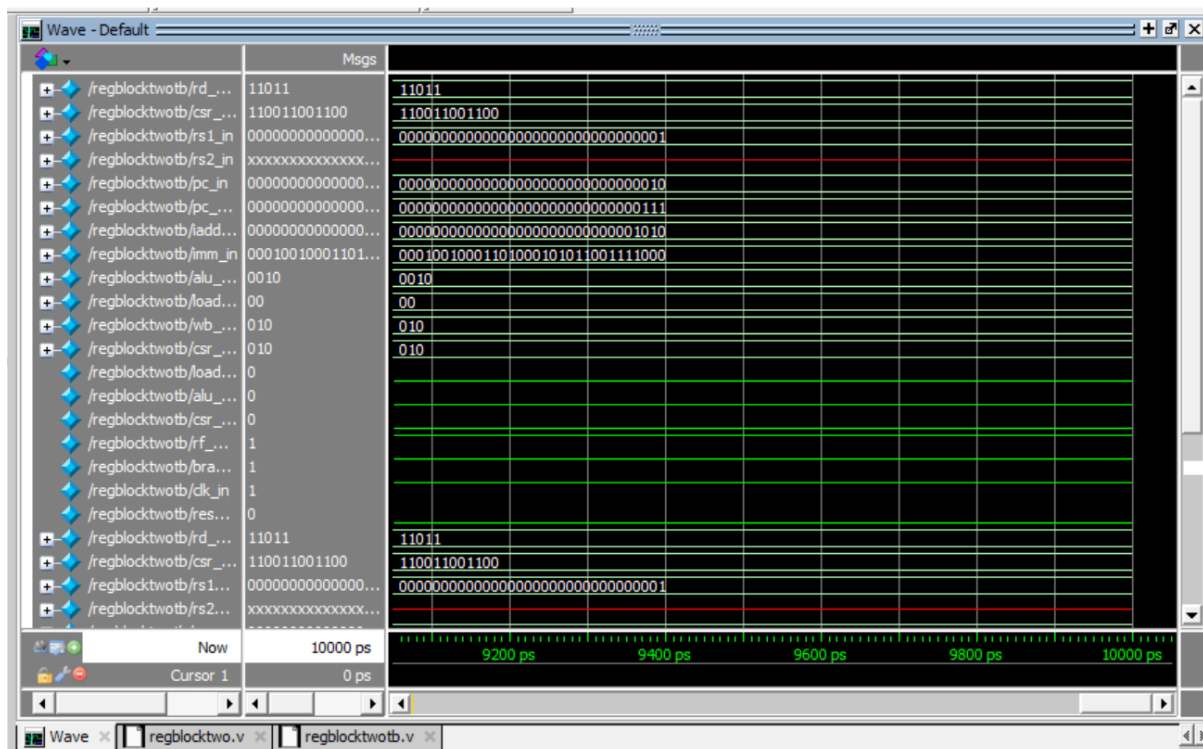
Block diagram:



Synthesis diagram:

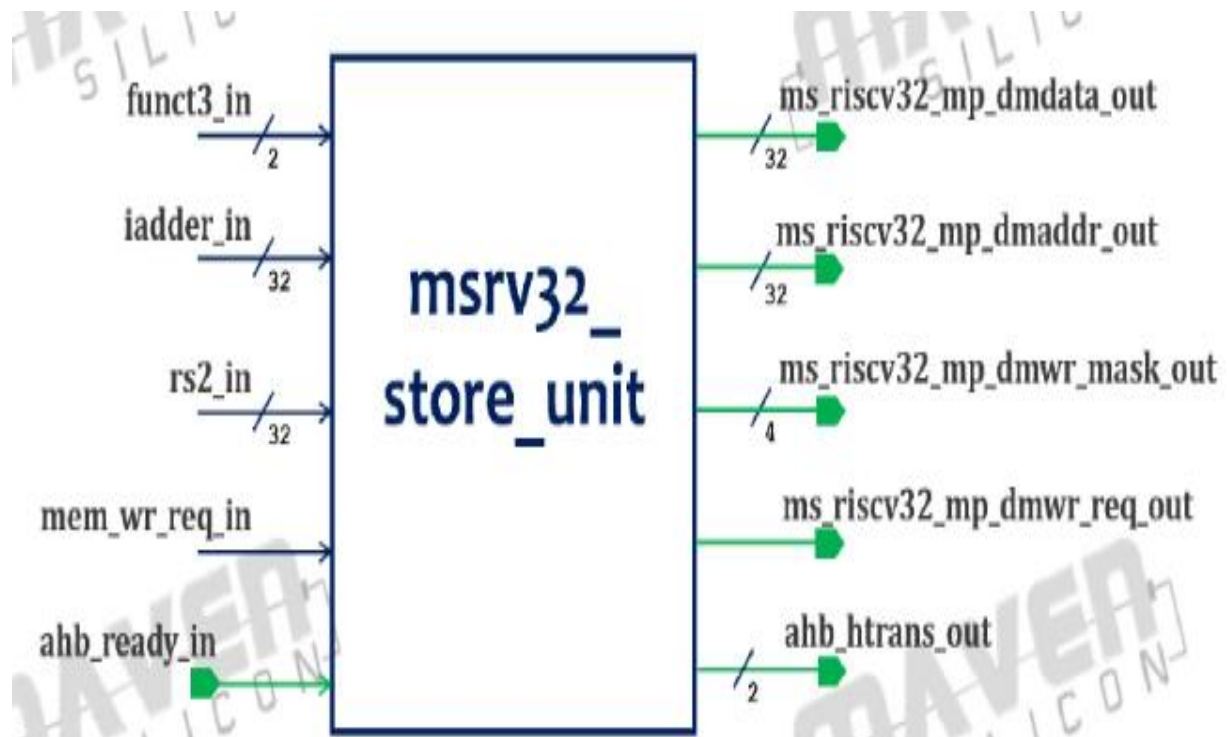


Waveform:

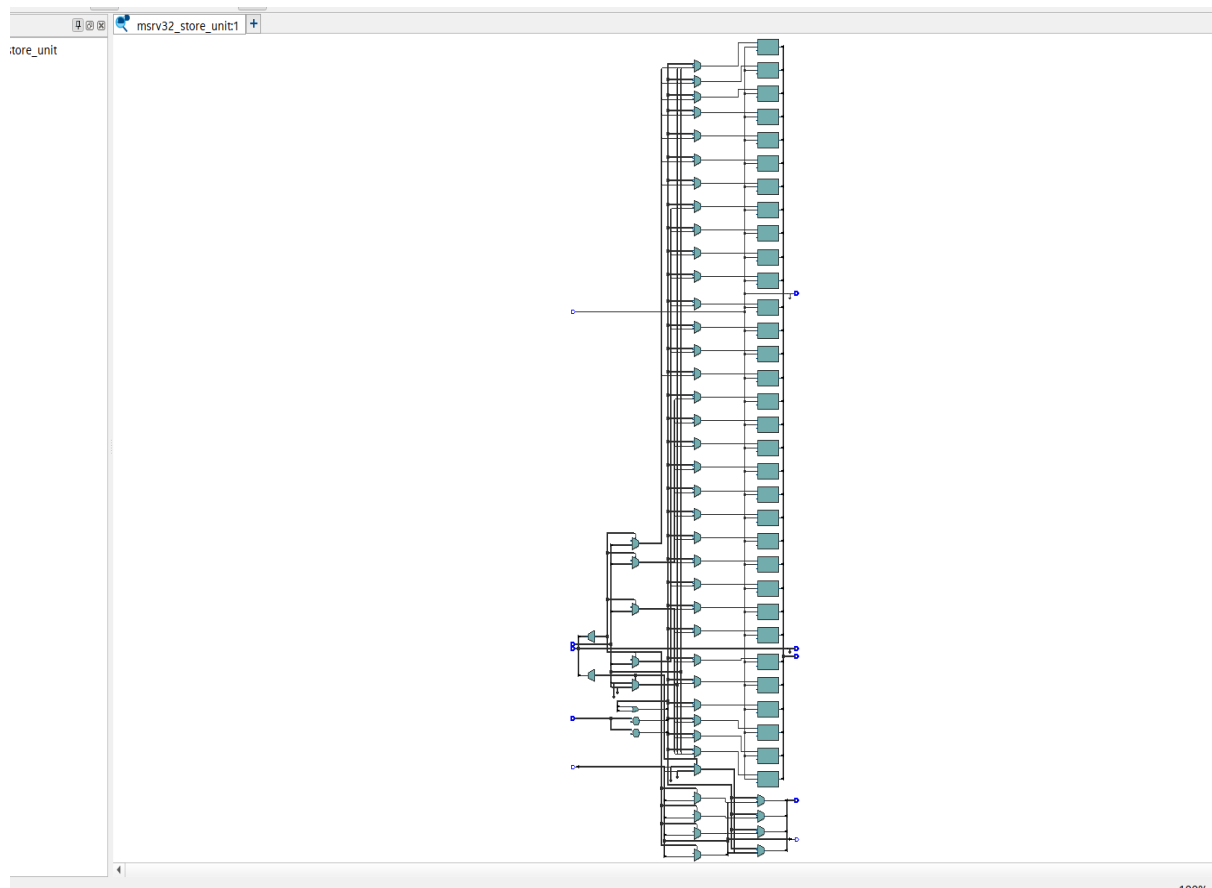


4) Store unit:

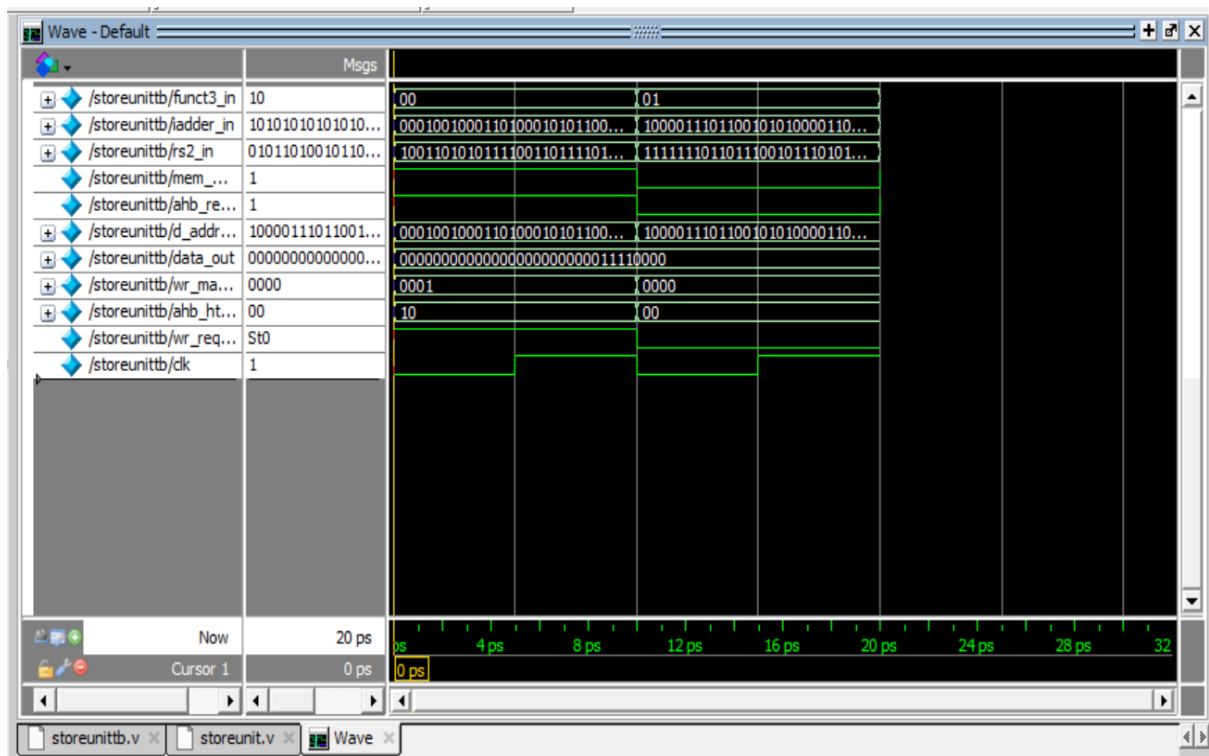
Block diagram:



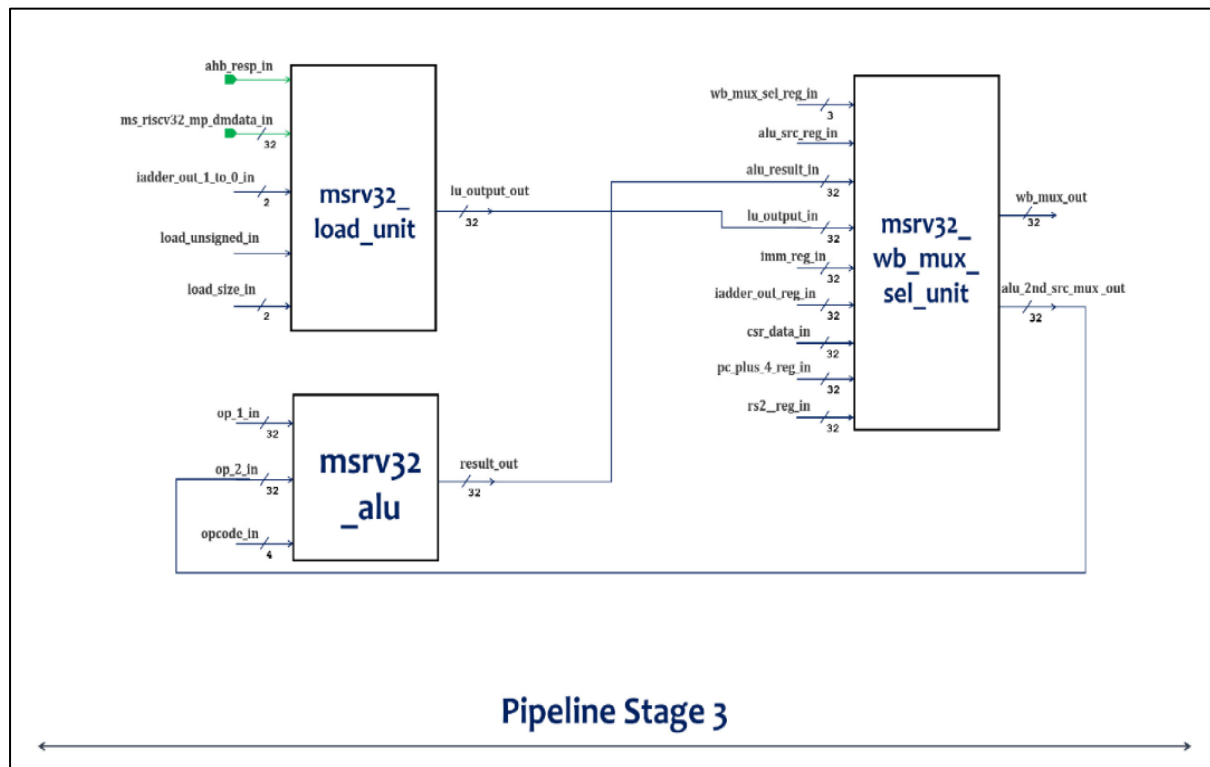
Synthesis diagram:



Waveform:

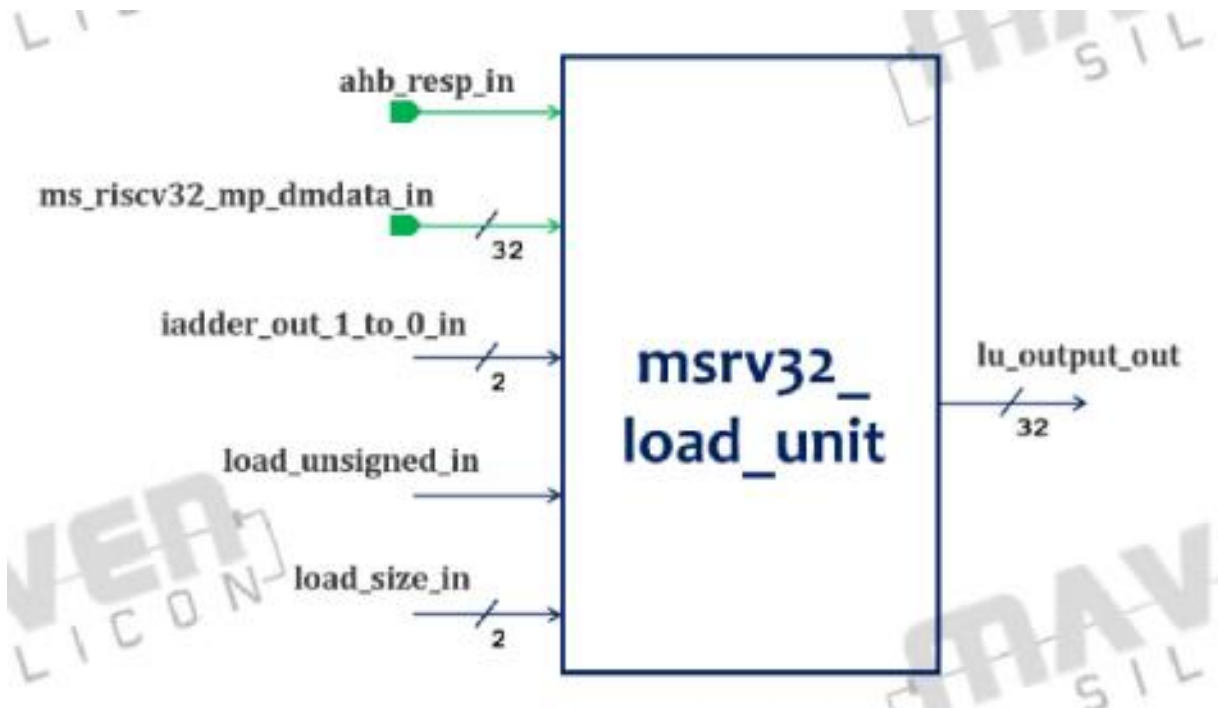


Pipelining stage 03:

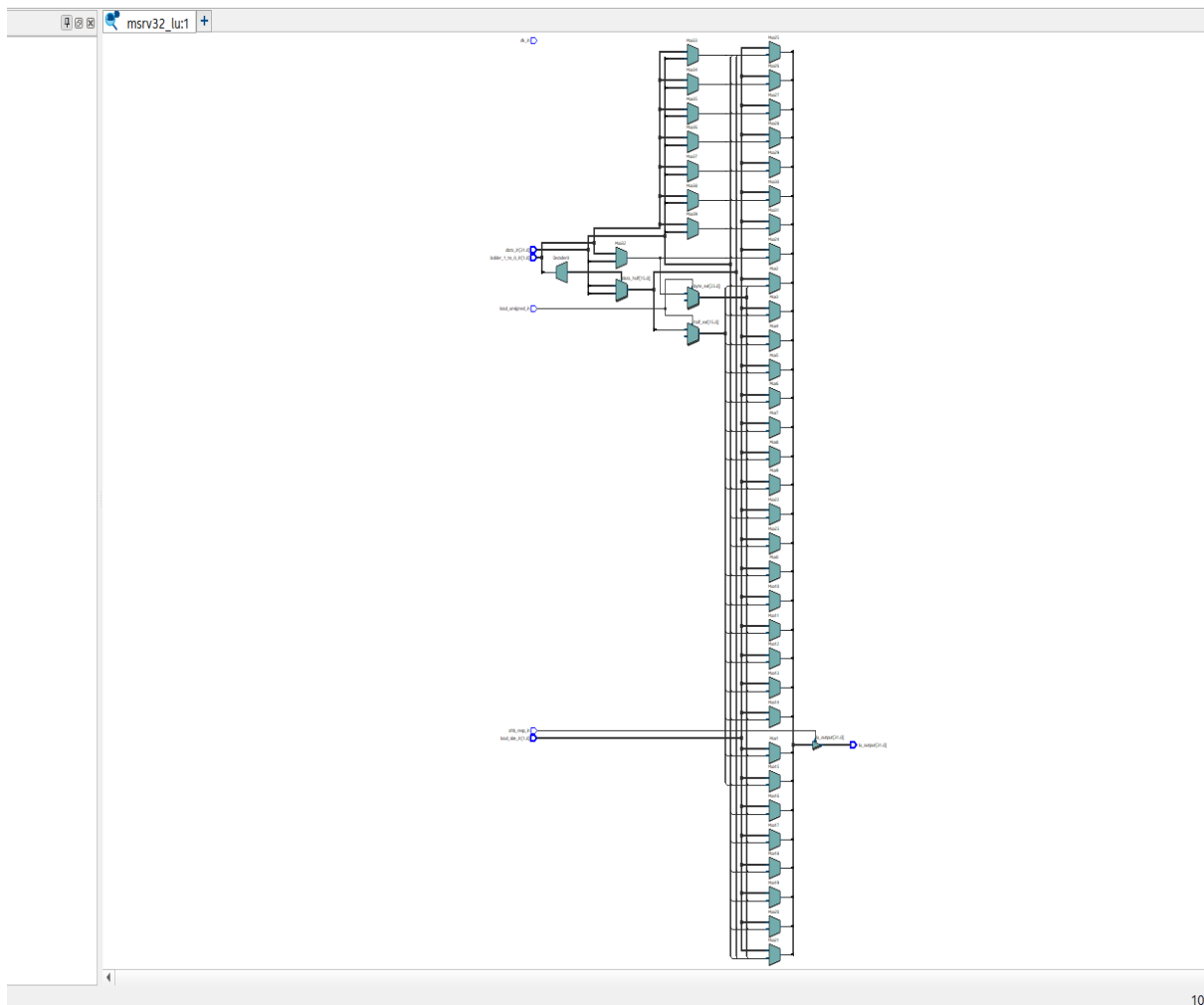


1) Load unit:

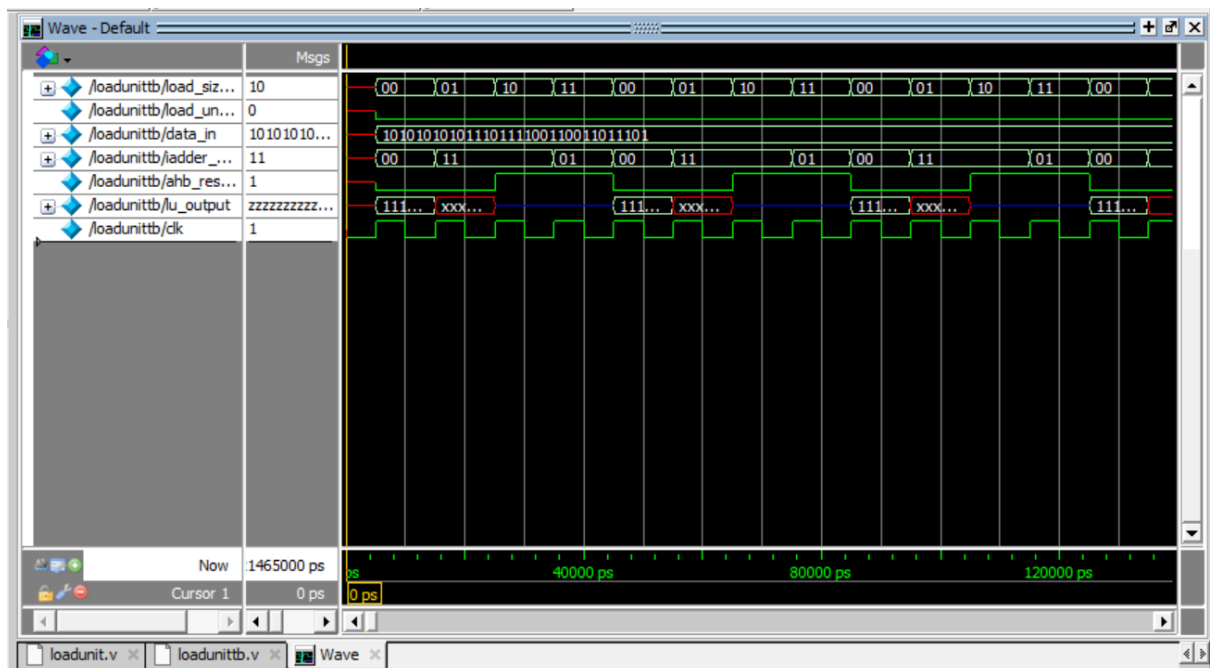
Block diagram:



Synthesis diagram:

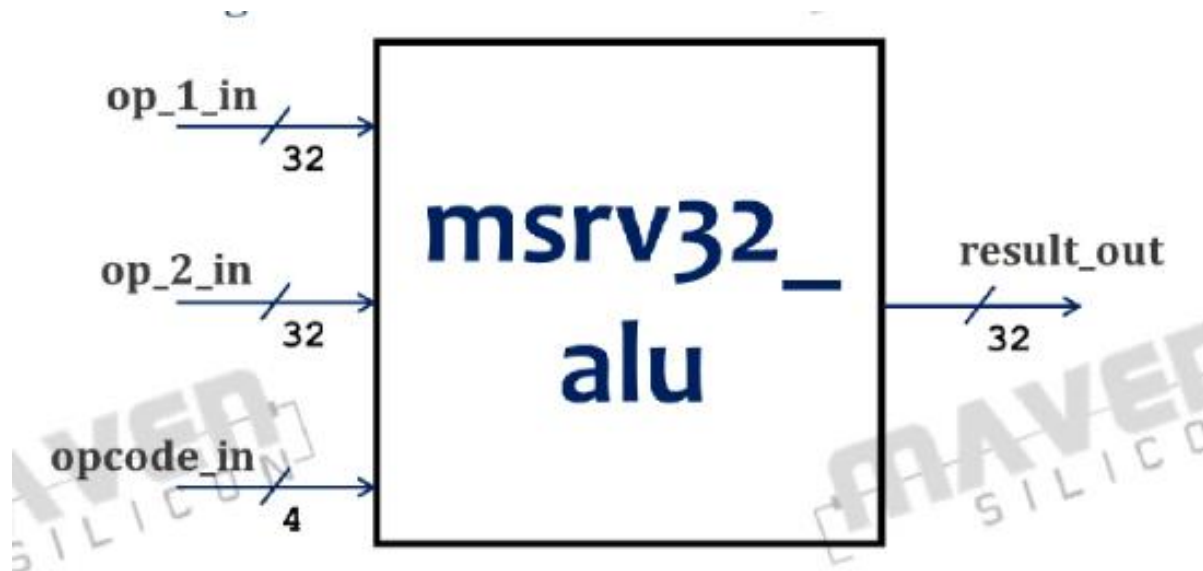


Waveform:

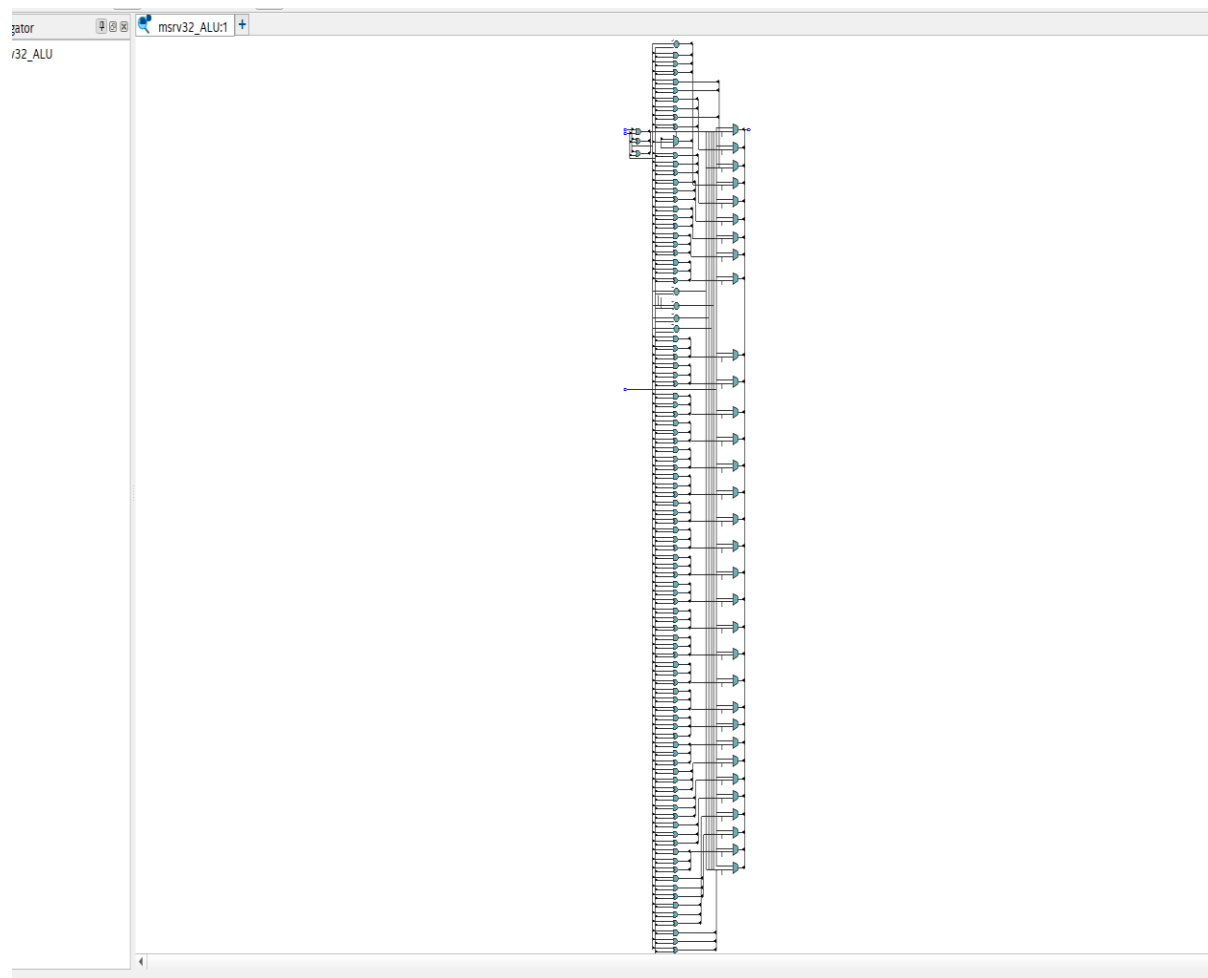


2) ALU:

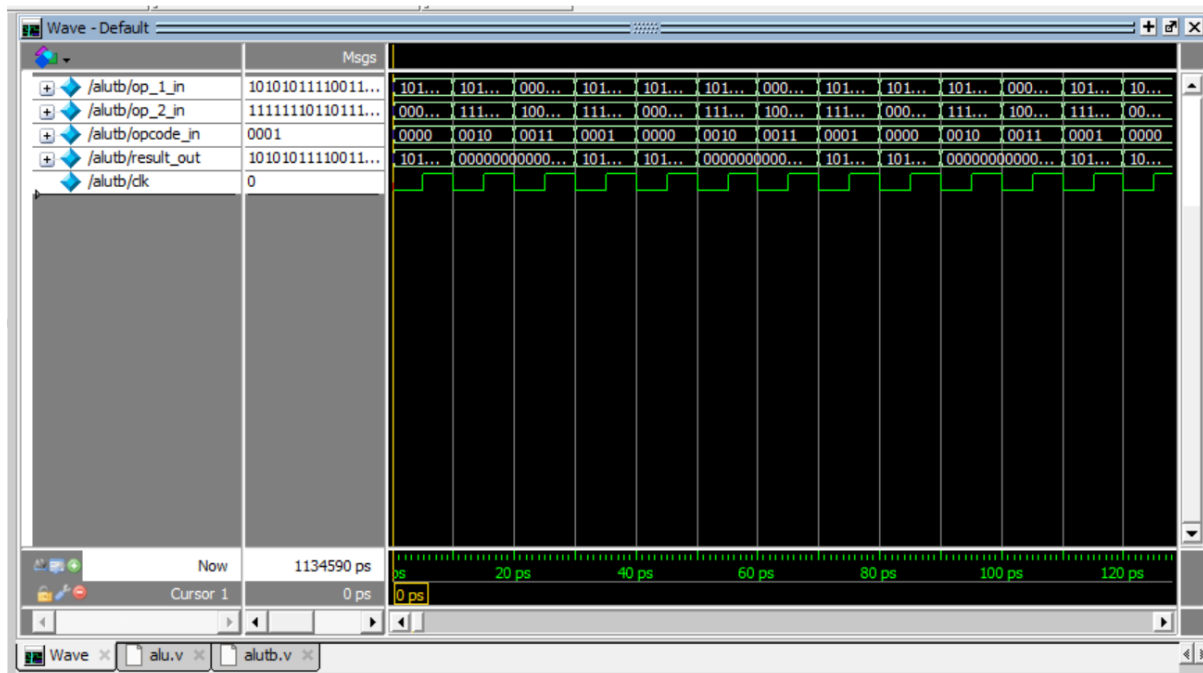
Block diagram:



Synthesis diagram:

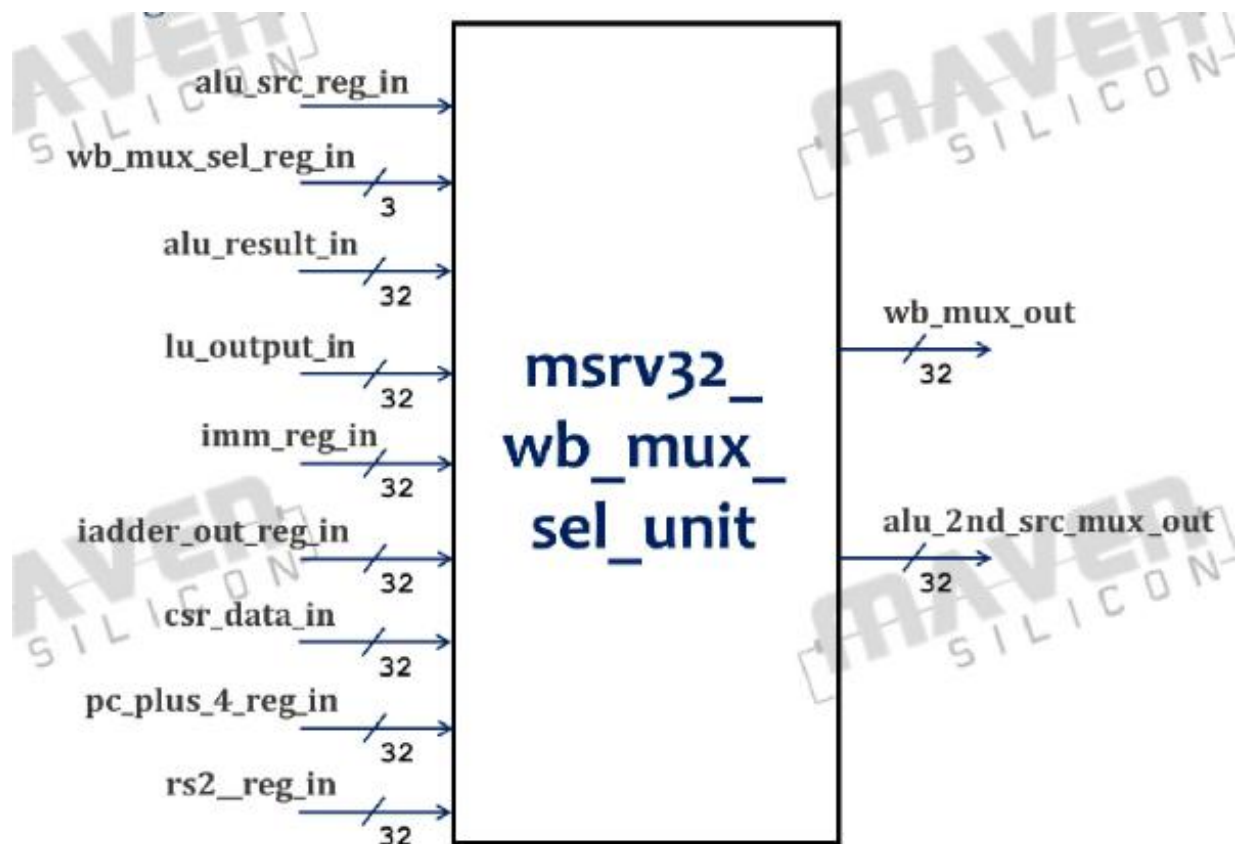


Waveform:

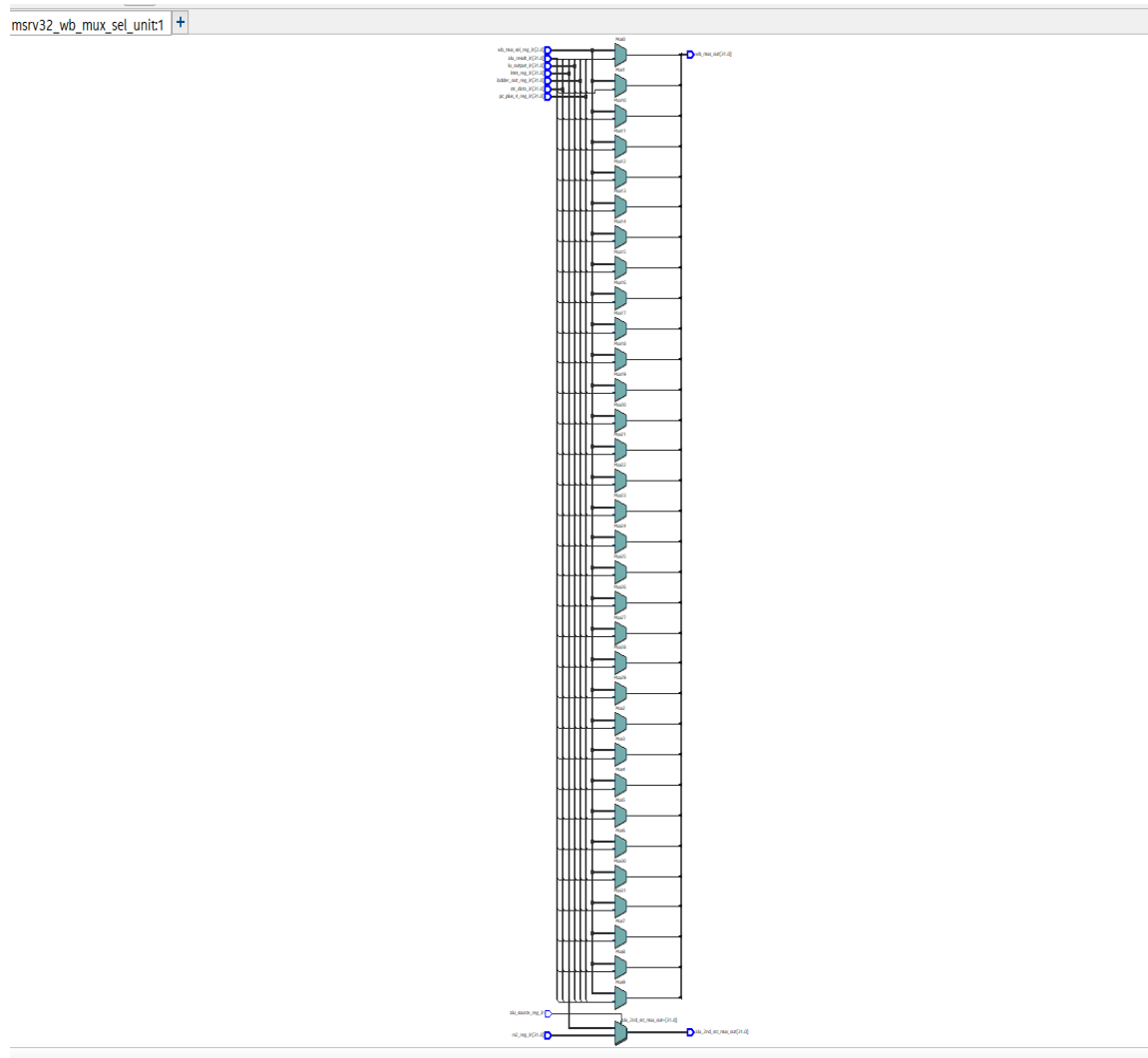


3) WB MUX selection unit:

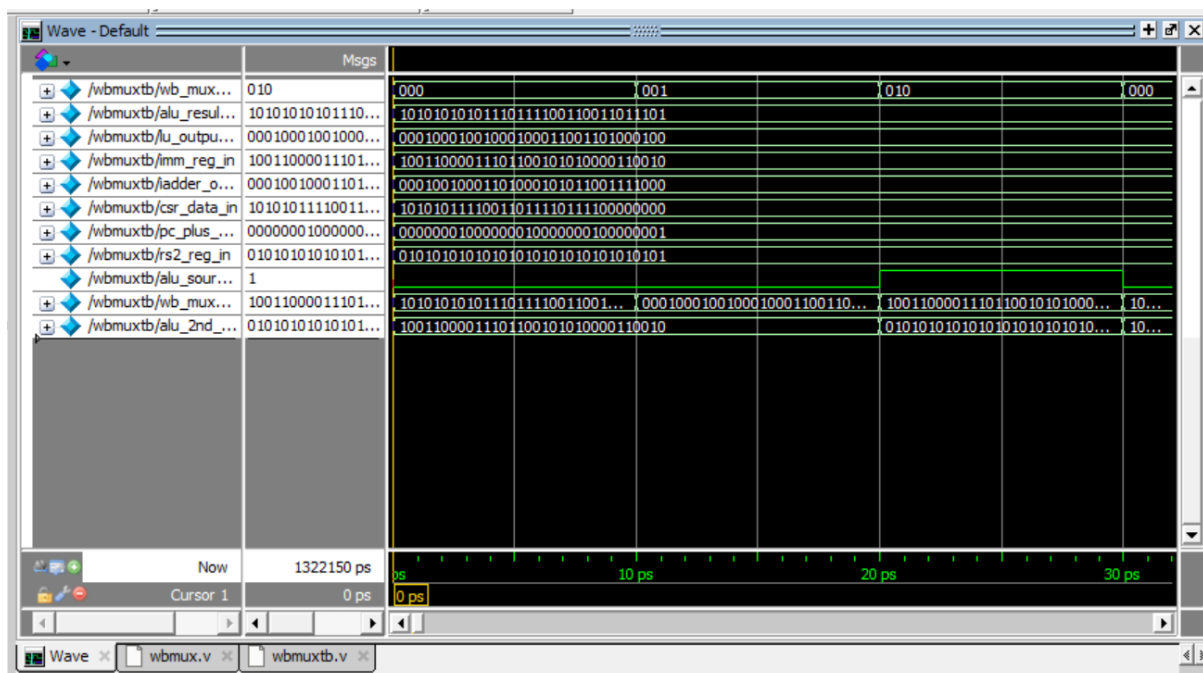
Block diagram:



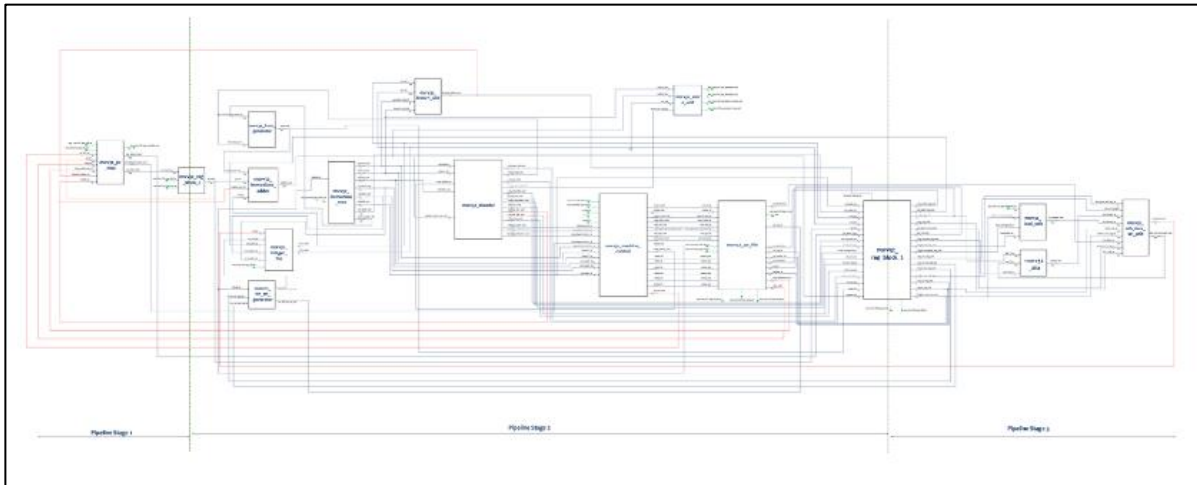
Synthesis diagram:



Waveform:



TOP module block diagram:



UVM testbench result and final output:

```
AChattopadhyay@mavenserver-RH3:~/RISC_V_Encrypted_TB/risc/Source_code/sim
Terminal Sessions View X server Tools Games Settings Macros Help
Session Servers Tools Games Sessions View Split MultiExec Tunneling Packages Settings Help
Quick connect...
# sltu is done successfully
# SLTU Command Working Perfectly
# the following list of command are working fine
# {"ADD", "SUB", "XOR", "OR", "AND", "SLL", "SRL", "SRA", "SLT", "SLTU"}
# and test result is
#
# -----
# 8888888b. d8888 .d8888b. .d8888b.
# 888 Y88b d88888 d88P Y88b d88P Y88b
# 888 888 d88P888 Y88b. Y88b.
# 888 d88P d88P 888 *Y888b. *Y888b.
# 88888888P* d88P 888 *Y88b. *Y88b.
# 888 d88P 888 *888 *888
# 888 d888888888 Y88b d88P Y88b d88P
# 888 d88P 888 *Y8888P* *Y8888P*
#
# ----- NOP or NO_INSTRUCTION -----
# UVM INFO verilog_src/uvvm-1.1d/src/base/uvvm_objection.svh(1267) @ 1000091500: reporter [TEST_DONE] 'run' phase is ready to proceed to the 'extract' phase
# --- UVM Report Summary ---
#
# ** Report counts by severity
# UVM INFO :60008
# UVM_WARNING : 1
# UVM_ERROR : 0
# UVM_FATAL : 0
# ** Report counts by id
# [IN AGENT TOP] 1
# [Questa UVM] 2
# [RNTST] 1
# [TEST_DONE] 1
# [UVMTOP] 1
# [r_type_sequence] 10000
# [uvvm_sequence_base] 1
#
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```