



# **Qualcomm RB3 Gen 2 Development Kit Guide**

80-70018-251 AB

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# Contents

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<b>1</b>	<b>Introduction</b>	<b>3</b>
<b>2</b>	<b>Hardware overview</b>	<b>4</b>
2.1	Status LEDs and buttons . . . . .	8
2.2	Mainboard and interposer connectors . . . . .	9
2.3	Vision mezzanine . . . . .	10
2.4	Sensors . . . . .	13
2.5	Ethernet . . . . .	15
2.6	Mainboard RF antennas . . . . .	16
2.7	Next steps . . . . .	17
<b>3</b>	<b>Power up and power cycle</b>	<b>18</b>
3.1	Power up . . . . .	18
3.2	Power cycle . . . . .	19
<b>4</b>	<b>Force RB3 into emergency download mode</b>	<b>20</b>
<b>5</b>	<b>References</b>	<b>22</b>
5.1	Low-speed and high-speed expansion connectors . . . . .	22
5.2	DIP switches . . . . .	35
5.3	Thermal testing and results . . . . .	47
5.4	Connect a custom camera sensor . . . . .	58
5.5	Reference designs and related documents . . . . .	64
5.6	Acronyms and terms . . . . .	65
<b>6</b>	<b>Development regulatory notice</b>	<b>66</b>

# 1 Introduction

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The Qualcomm Dragonwing™ RB3 Gen 2 Development Kit accelerates the creation of devices for enterprise, industrial, and professional service applications. It simplifies the training and development of machine learning applications. A variety of expansion boards, SDKs, and development tools are available for prototyping and evaluations.

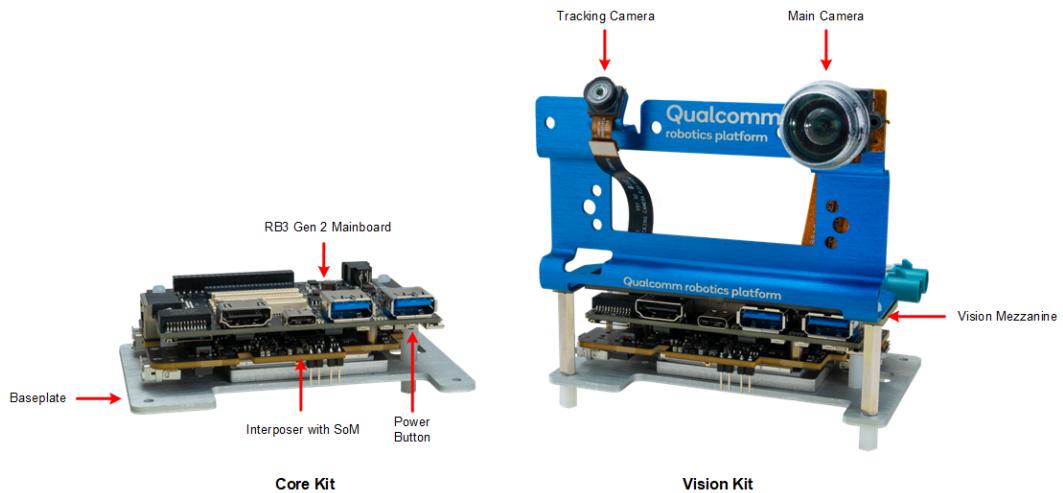
The following video explains the architecture, features, and capabilities of the RB3 Gen 2 Development Kit.



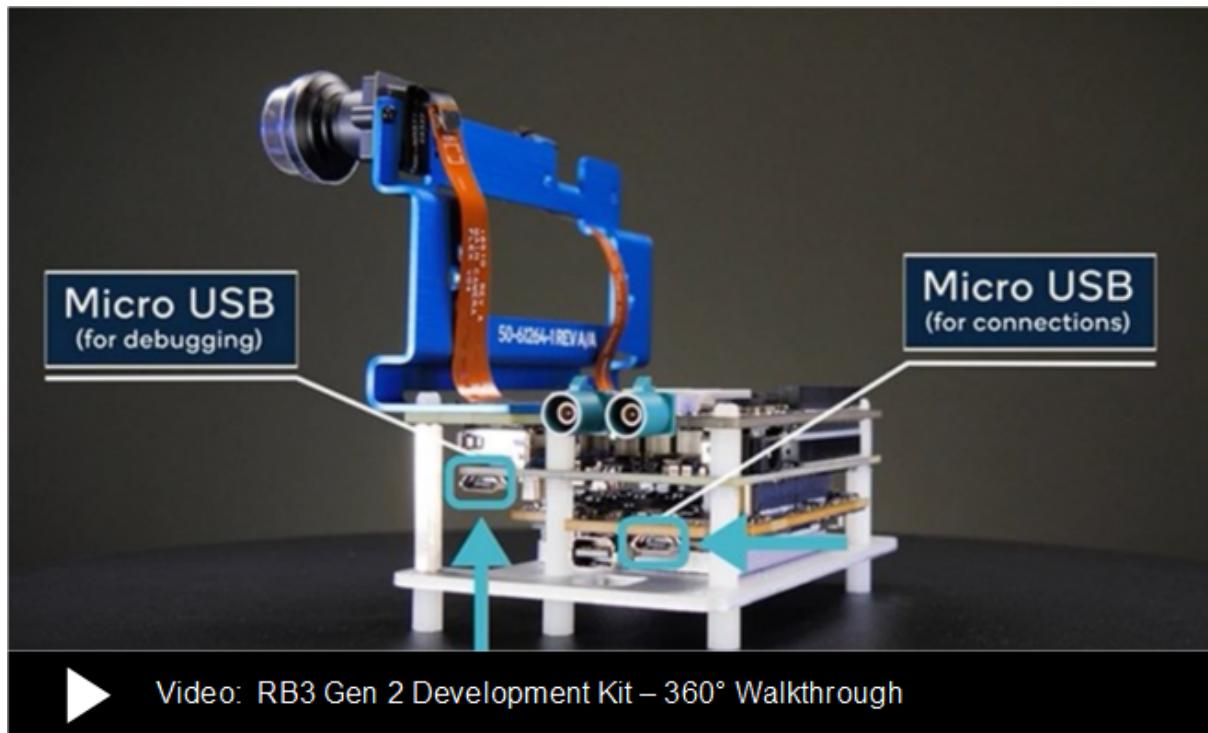
## 2 Hardware overview

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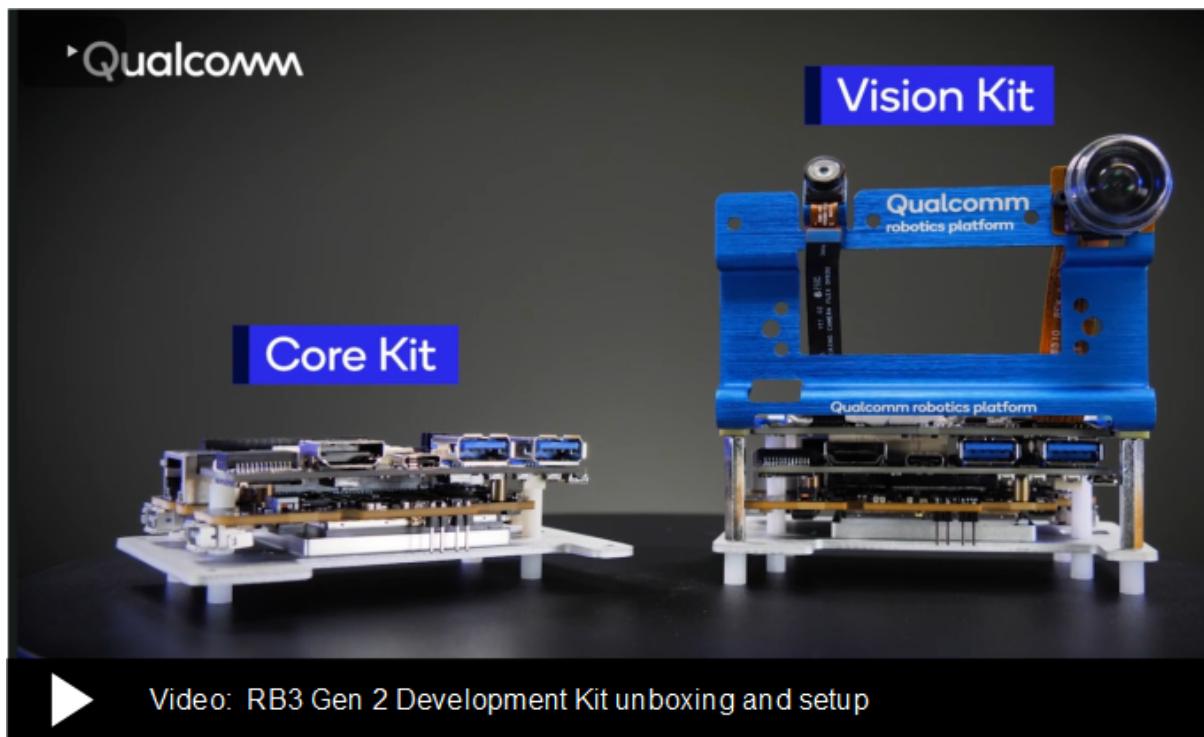
The Qualcomm RB3 Gen 2 Development Kit is available as a Core Kit and a Vision Kit. Both kits feature a system-on-module (SoM) that integrates a Qualcomm system-on-chip (SoC). The SoM is mounted to an interposer that's connected to the mainboard using a 500-pin connector. The mainboard includes many connectors to support a variety of different peripheral interfaces and stackable mezzanine cards. The Vision Kit includes everything in the Core Kit plus the Qualcomm Vision mezzanine board, a high-resolution main camera, and a low-resolution tracking camera.



The following video shows the architecture of the RB3 Gen 2 Development Kit hardware and the location of the interfaces, buttons, LEDs, DIP switches, and connectors.



The following video shows the unboxing and setup of the RB3 Gen 2 Development Kit. It also shows running a sample app on the kit.



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**Note:** The RB3 Gen 2 Vision Kit includes cameras with protective lens covers. Remove these covers before using the kit.

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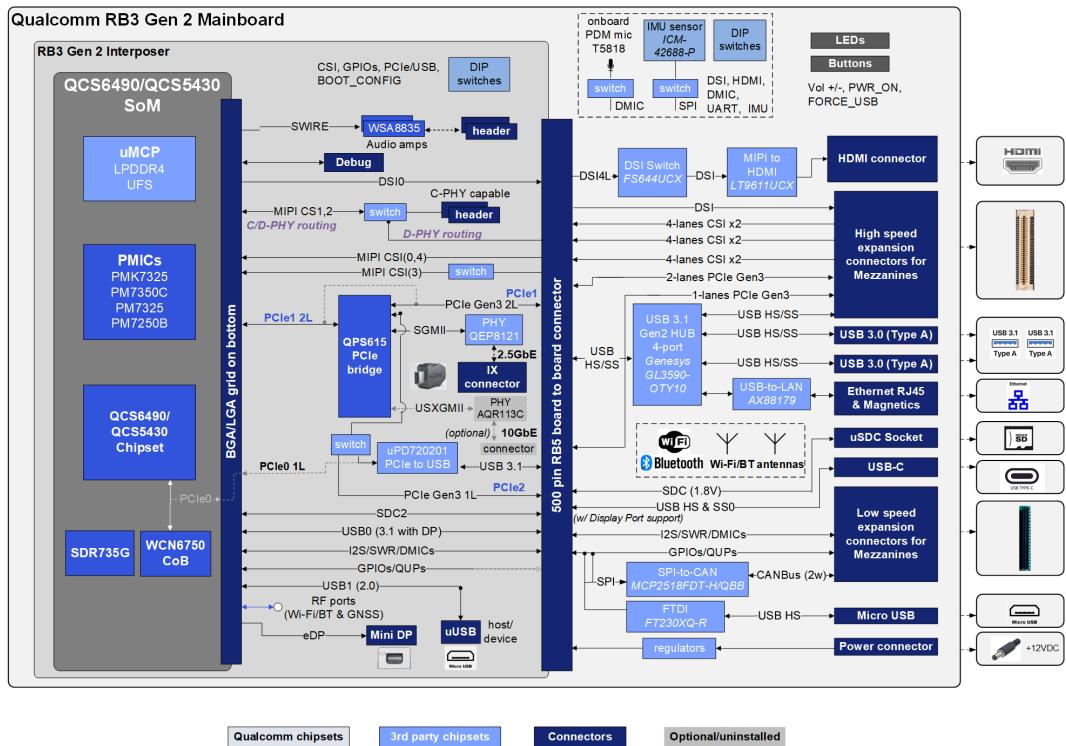
### Kit components

Core Kit	Vision Kit
<ul style="list-style-type: none"><li>• Qualcomm RB3 Gen 2 mainboard</li><li>• Interposer with SoM</li><li>• Power supply (12 V)</li><li>• USB-A to USB-C cable</li><li>• Two speakers</li><li>• Pick tool to help access DIP switches</li></ul>	<ul style="list-style-type: none"><li>• Qualcomm RB3 Gen 2 Core Kit</li><li>• Qualcomm Vision mezzanine board</li><li>• IMX577 camera</li><li>• OV9282 tracking camera</li></ul>

### Mainboard and interposer block diagram

The following block diagram shows the RB3 Gen 2 mainboard and interposer. Connectors are shown in dark blue. Some connectors are on the interposer board and some on the mainboard. Knowing the placement of these connectors is useful in configuring and debugging them easily and

effectively.



Mainboard and interposer block diagram

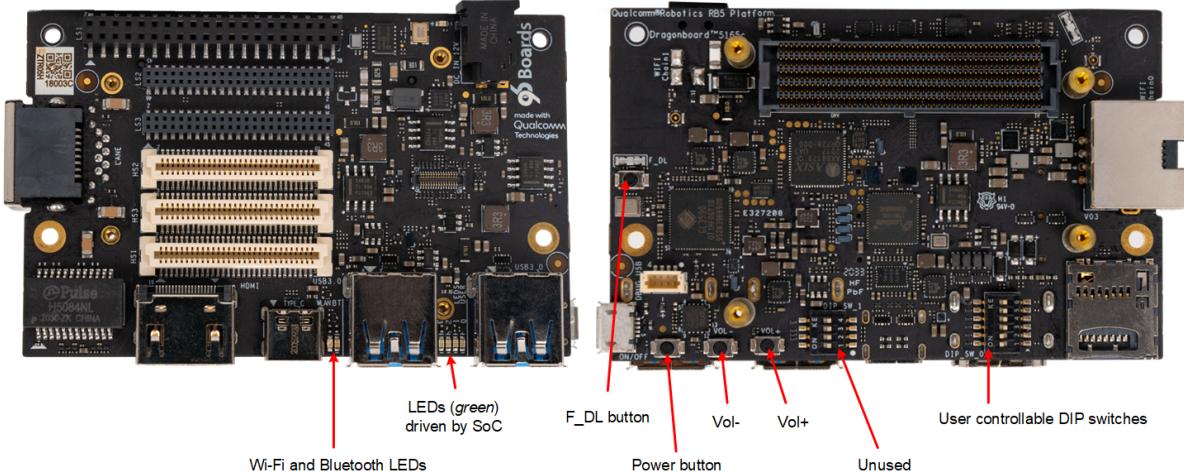
### Hardware features in RB3 Gen 2 Dev Kit

Feature	Component name	Interface	Details
DSI to HDMI bridge	Lontium LT9611UCX	HDMI Type-A connector	4K at 30-Hz HDMI support with I2S audio
USB hub	Genesys GL3590	2x USB Type-A connectors	USB 3.1 Gen2 10 Gb 4-port hub controller
USB to LAN	ASIX AX88179	RJ45 connector	USB 3.0 Gb to 1 Gb Ethernet controller
Audio amplifiers (2)	Qualcomm WSA8835	Header pins (2) on interposer	Class-D SoundWire audio amplifier
CAN bus controller	Microchip MCP2518FD	Pins on LS1 connector	External CAN-FD controller with SPI
Sensor	TDK ICM-42688-P	Sensor on mainboard	3-axis gyroscope and 3-axis accelerometer
On-board digital microphone	TDK T5818	Microphone on mainboard	PDM digital MEMS microphone

Feature	Component name	Interface	Details
USB host/Device port	USB Type-C	Type C connector	USB Type-C with display port (direct connect to processor)
Input power	DC power input	Barrel jack connector	+12-V from wall supply
microSD storage	microSD card	microSD card tray	microSD card tray
WLAN/Bluetooth antenna	Antenna0	Printed antenna on mainboard	2.4 GHz/5 GHz printed antenna
WLAN/Bluetooth antenna	Antenna1	Printed antenna on mainboard	2.4 GHz/5 GHz printed antenna
Debug UART	FTDI UART to USB converter	microUSB connector	Connector with FTDI USB to UART converter
DP display	DP display output	Micro DisplayPort connector (on interposer)	Display only, not including touch or backlight control
GNSS	SDR735G chipset	RF connector for external antenna on interposer	GNSS/GPS support
USB 2.0	USB1 port from SoC	Micro USB connector on interposer	Additional USB port for host/ device mode
Second Ethernet port	From QPS615 PCIe expander	IX Ethernet connector on interposer	2.5 GbE from PCIe
Third Ethernet port	From QPS615 PCIe expander	IX Ethernet connector on interposer	10 GbE from PCIe (not installed by default, special order)
Camera port 1	From chipset	30-pin flex connector	Support for C/D-PHY camera
Camera port 2	From chipset	30-pin flex connector	Support for C/D-PHY camera

## 2.1 Status LEDs and buttons

The following figure shows the LEDs and buttons on the RB3 Gen 2 mainboard.



[L] Top view of mainboard LEDs and buttons, [R] bottom view

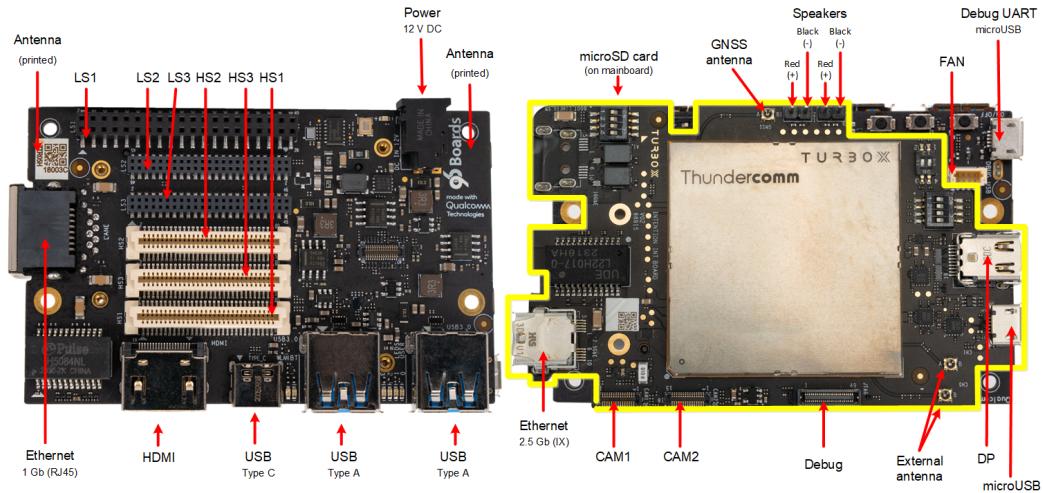
The following LED colors indicate different statuses:

- Yellow LED is for Wi-Fi status.
- Blue LED is for Bluetooth status.

The F\_DL button is used for emergency boot. In addition to volume control, Vol- is also used to reset the device.

## 2.2 Mainboard and interposer connectors

The following figures show the location of the different connectors on the mainboard and interposer. The image at left shows the connectors from the top view of the mainboard. The image at right shows the connectors from the bottom view of the interposer board (outlined in yellow) attached to the mainboard. The bottom view is shown with the baseplate removed.



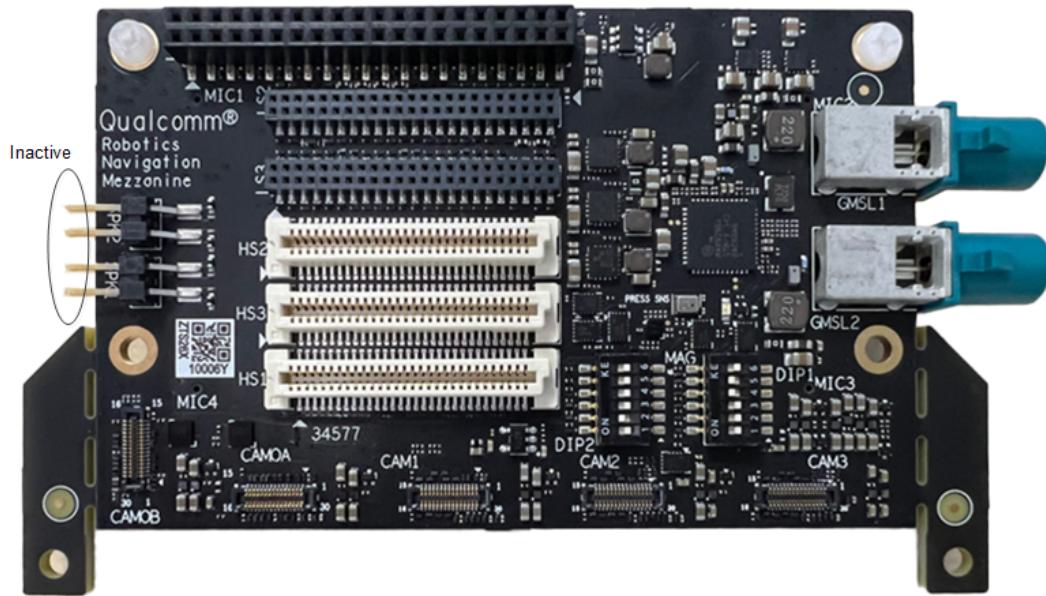
[L] Connectors on top view of mainboard, [R] bottom view of interposer (in yellow) and mainboard

Low-speed connectors (LS1, LS2, LS3) and high-speed connectors (HS1, HS2, HS3) provide various functionalities including UART, SPI, camera CSI, interrupt signals, DC power, and additional GPIOs.

See [low-speed and high-speed expansion connectors](#) for details.

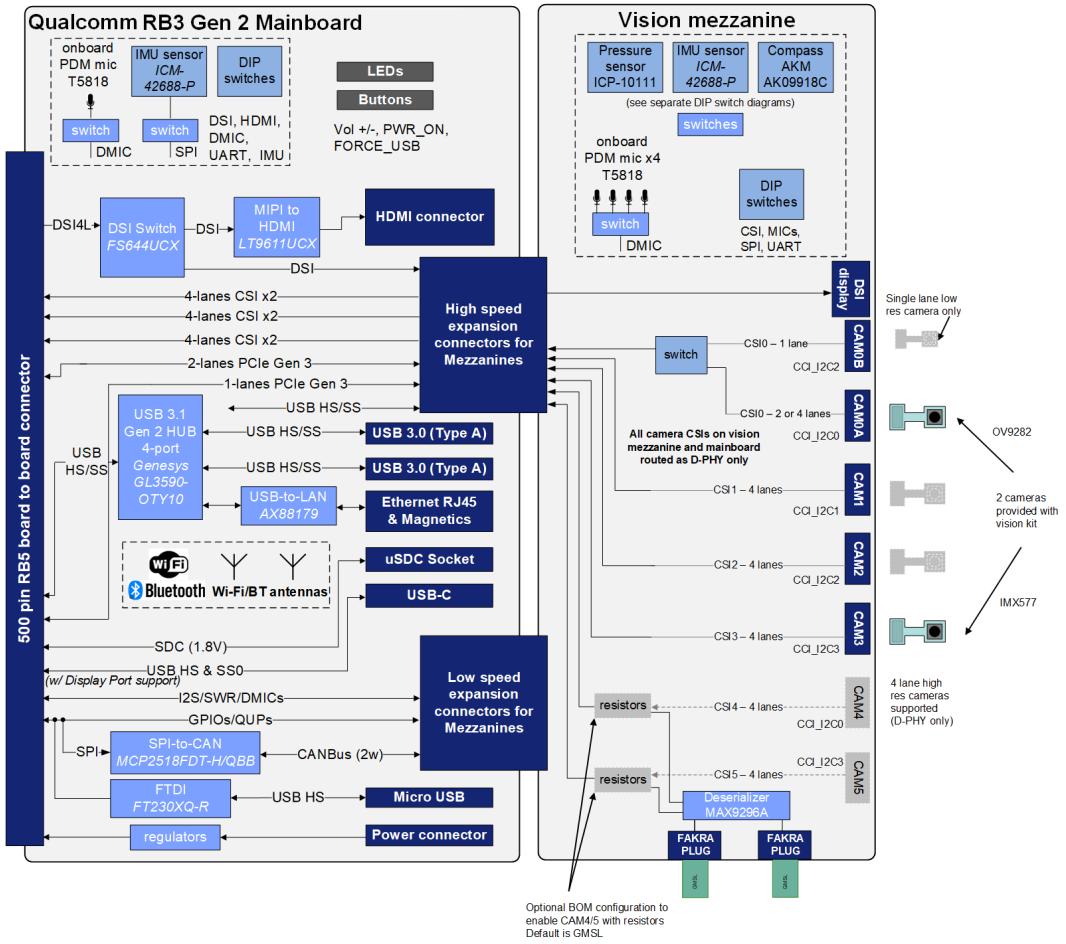
## 2.3 Vision mezzanine

The Vision mezzanine supports interfacing cameras to the RB3 Gen 2 platform through two, second-generation gigabit multimedia serial link (GMSL2) camera inputs and five CAM/CSI camera ports. This mezzanine also has four DMICs, an IMU, compass/magnetometer, and a pressure sensor.



### **Vision mezzanine**

The following block diagram shows components and connectors on the mainboard and Vision mezzanine.



### Vision mezzanine and mainboard block diagram

The following key components are supported on the Vision mezzanine:

#### Camera

- Two GMSL2 camera inputs (using MAX9296A), CSI4 and CSI5. Labels on board (GMSL1 and GMSL2) are connector names only. Both inputs are GMSL2 technology.
- Five CAM/CSI camera ports with identical pinouts: CSI0 splits into two cameras (CAM0A and CAM0B)
- CAM3 connector includes an option for a higher supply voltage of 5 V and accommodates the Panasonic TOF camera
- Main camera (IMX577); part number: CMK-IMX577-B-V2.0, connect to CAM3
- Tracking camera (OV9282); part number: CMK-VR-OV9282-V1.0, connect to CAM0A

#### Sensors

- DK ICM-42688-P IMU (located on the back side of the board)

- AKM compass/magnetometer AK09919
- TDK pressure sensor (ICP-10111)

### Audio

- Four digital PDM mics that interface directly with the RB3 Gen 2 platform
- Speaker connectors on the mezzanine are inactive. They're replaced by the speaker connectors located on the interposer. For more information, see Mainboard and interposer connectors.

## 2.4 Sensors

Sensors are available on the mainboard and the vision mezzanine. Only one IMU sensor can function at a time. If both sensors are enabled, only the Vision mezzanine IMU functions. The following table lists the sensor details and identifies the appropriate DIP switch for each sensor. See [DIP switches](#) for DIP switch locations.

**Sensor details for Mainboard and Vision Mezzanine**

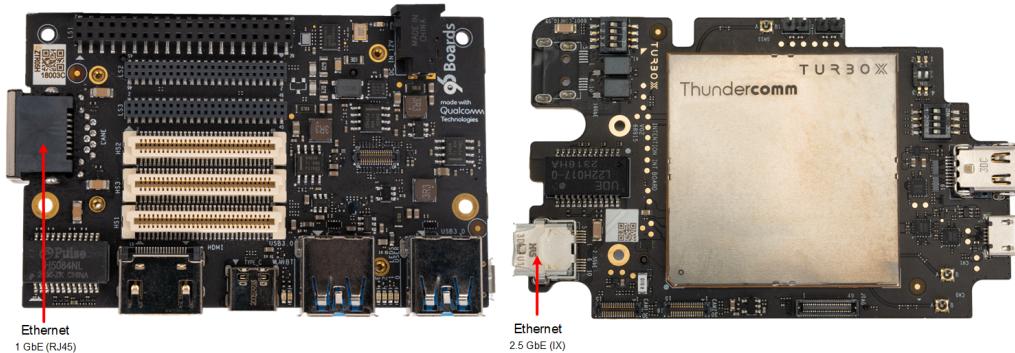
Placement	Sensor part	Sensor type	DIP switch	Name	Details	Default
Mainboard	ICM42688	Inertial Measurement (pin 5) Unit (IMU) sensor: Accelerometer and Gyroscope	DIP_SW_0	SENSOR_IM_U_TOGGLE	<ul style="list-style-type: none"> <li>• ON: on-board IMU disabled</li> <li>• OFF: on-board IMU enabled</li> </ul>	OFF

Placement	Sensor part	Sensor type	DIP switch	Name	Details	Default
Vision mezzanine	ICM42688	IMU sensor - Accelerometer and Gyroscope	DIP1 (pin 1)	SENSOR_SPI_PASSTHRU	<ul style="list-style-type: none"> <li>• ON: Snapdragon sensor core (SSC) sensor SPI routed to IMU_SPI_SELECT switch</li> <li>• OFF: IMU sensor SPI passthrough</li> </ul>	ON
			DIP2 (pin 5)	IMU_INT_1_2_SELECT_LOGIC2	<ul style="list-style-type: none"> <li>• ON: IMU INT1 to ACCEL1 INT, IMU INT2 to GYRO INT</li> <li>• OFF: IMU INT 1 and 2 disconnected</li> </ul>	OFF

Placement	Sensor part	Sensor type	DIP switch	Name	Details	Default
	ICP-10111	Pressure/Barometer	DIP1 (pin 4)	PRESS_SENS_DISCONNECT	<ul style="list-style-type: none"> <li>• ON: on-board</li> <li>• OFF: disconnected</li> </ul>	ON
	AKM9xxx	Magnetometer	DIP1 (pin 5)	MAG_SENSOR_DISCONNECT	<ul style="list-style-type: none"> <li>• ON: on-board</li> <li>• OFF: disconnected</li> </ul>	ON

## 2.5 Ethernet

The RB3 Gen 2 Development Kit has a gigabit Ethernet interface on the mainboard through an RJ45 connector and a 2.5GbE Ethernet interface on the interposer board through an IX connector. An adapter cable, which isn't part of the kit, is required to use the IX connector. An adapter cable is available as an optional accessory for additional purchase.

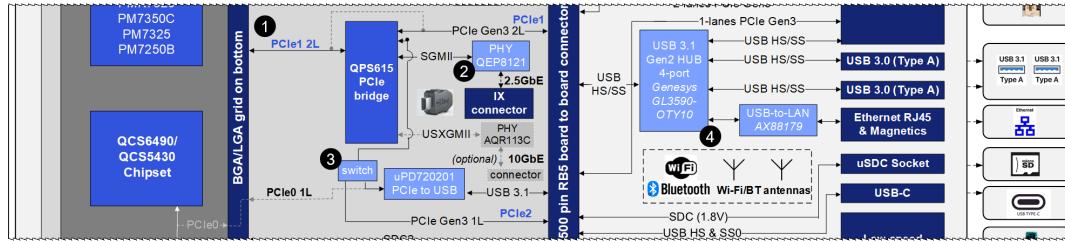


[L] Ethernet connector on top view of mainbaord, [R] Ethernet connector on bottom view of interposer

Use the following snippet of the mainboard and interposer diagram to follow along with a high-level description of the Ethernet functionality, flow, and components in the RB3 Gen 2 Development kit.

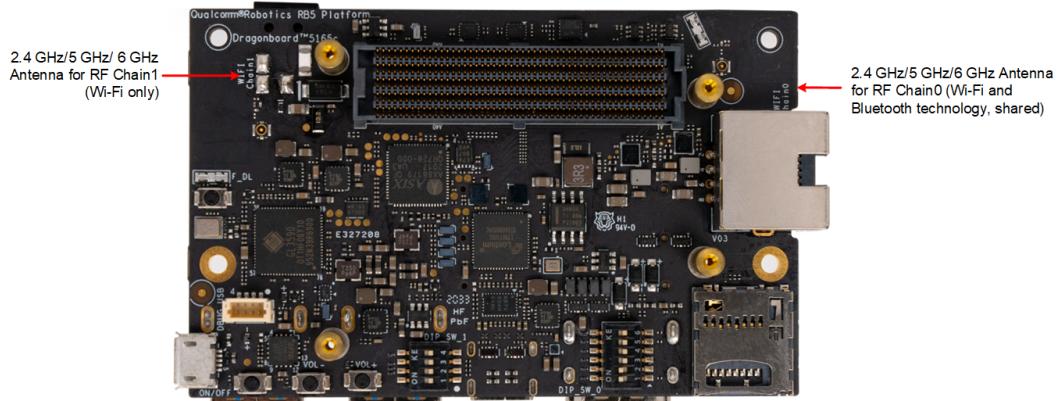
(1) On the interposer board, the PCIe1 2L signals are connected to the QPS615 (PCIe bridge). (2) SGMII signals from the QPS615 are connected to QEP8121 PHY and terminated to the IX connector supporting 2.5GbE. (3) Based on the DIP SW 3 (bit 2) settings, the QPS 1 lane PCIe

signals are connected to either PCIe to USB (uPD720201) where it is converted to USB or routed straight to the 500-pin connector. The default switch position is to select the path via PCIe to USB (uPD720201). The mainboard has the USB 3.1 Gen2 Hub (4) along with USB to LAN (AX88179) which is terminated to the RJ 45 connector.



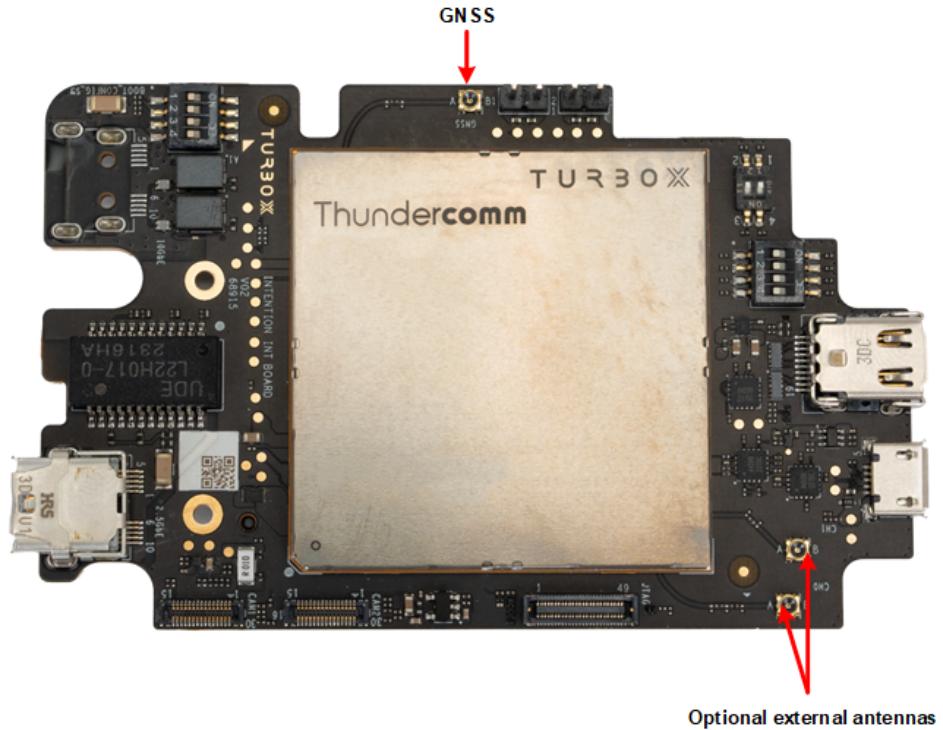
## 2.6 Mainboard RF antennas

The RB3 Gen 2 mainboard uses two dual-band, 2.4 GHz/5 GHz/6 GHz, WLAN/Bluetooth technology printed antennas on the mainboard. To avoid detuning the antennas, use nylon standoffs for mounting holes and check that there is no metal directly above or below the antennas. QCS6490/QCS5430 supports  $2 \times 2$  MIMO with 2x Wi-Fi antenna ports and 1x Bluetooth technology antenna port. The current SoM uses a shared Wi-Fi/Bluetooth technology approach on RF Chain0. The SoM has the option to route RF signals through the board-to-board connector to the mainboard to eliminate the need for external coaxial cables (current configuration).



**Dual-band RF antennas on the mainboard (bottom view)**

As shown in the following image, connectors are available on the interposer to connect high-performance external antennas (optional, not included in the kit). A GNSS connector is also available. Use Ipxel MFH-SW 23 series cables to connect external antennas.



**Dual-band RF antenna and GNSS connectors on the interposer**

## 2.7 Next steps

To get started, see the [RB3 Gen 2 Quick Start Guide](#).

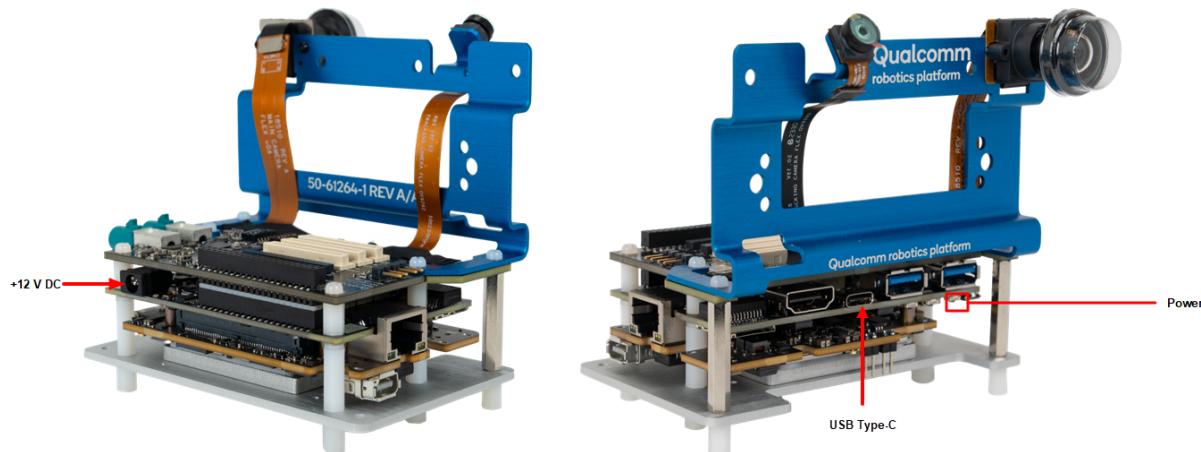
To learn more, see the [RB3 Gen 2 documents](#).

# 3 Power up and power cycle

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The RB3 Gen 2 Development Kit comes preloaded with software to set up the device. If an image isn't loaded on the device, the device enters [emergency download mode](#) when powered on.

The following image shows the location of the interfaces used to power up the device.



**Locations of power adapter input, USB Type-C, and Power button**

## 3.1 Power up

To power up the device, do the following:

1. Connect the +12 V power adapter.
2. Do one of the following:
  - Hold the power button for 2-3 seconds until the power LED stays illuminated.
  - **Plug in the USB Type-C cable.**
    - Ensure that the power adapter is connected.

- Device won't boot with only the USB Type-C cable connected.

The processor powers up and loads the boot image from internal storage UFS.

To view the bootup message logs, connect the host to the debug port (baud rate 115200) of the RB3 Gen 2 Dev Kit using a microUSB cable and use a serial terminal such as PuTTY.

## 3.2 Power cycle

To power cycle the device, do the following:

1. Disconnect the power adapter.
2. Disconnect the USB Type-C cable (if connected).
3. Follow the [power up](#) procedure.

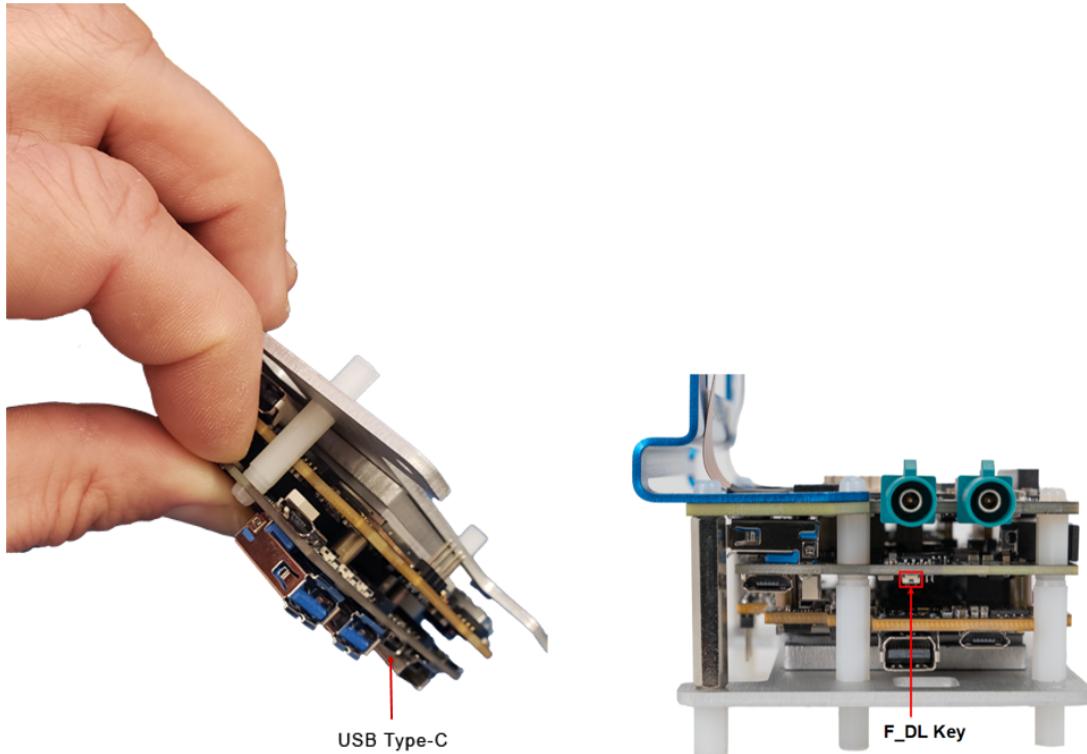
For more information about setting up the device, see [RB3 Gen 2 Quick Start Guide](#).

## 4 Force RB3 into emergency download mode

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The RB3 Gen 2 platform enters emergency download (EDL) mode after power up if there is no image on the device or if it's corrupted. In some situations, you want to force the device into EDL mode to download software because EDL mode lets you flash software images. To force the device into EDL mode, do the following:

1. Connect the device to a +12 V wall power supply.
2. Press and hold the **F\_DL** button.



3. Connect the device to the host system through the USB Type-C connector.
4. Release the **F\_DL** button. The device should now be in Qualcomm download (QDL) mode.

For this task, QDL is used interchangeably with EDL.

5. To verify whether the device has entered the QDL mode, run the following command on the host:

```
lsusb
```

#### **Sample output**

```
Bus 002 Device 014: ID 05c6:9008 Qualcomm, Inc. Gobi Wireless Modem (QDL mode)
```

# 5 References

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This section includes the following references:

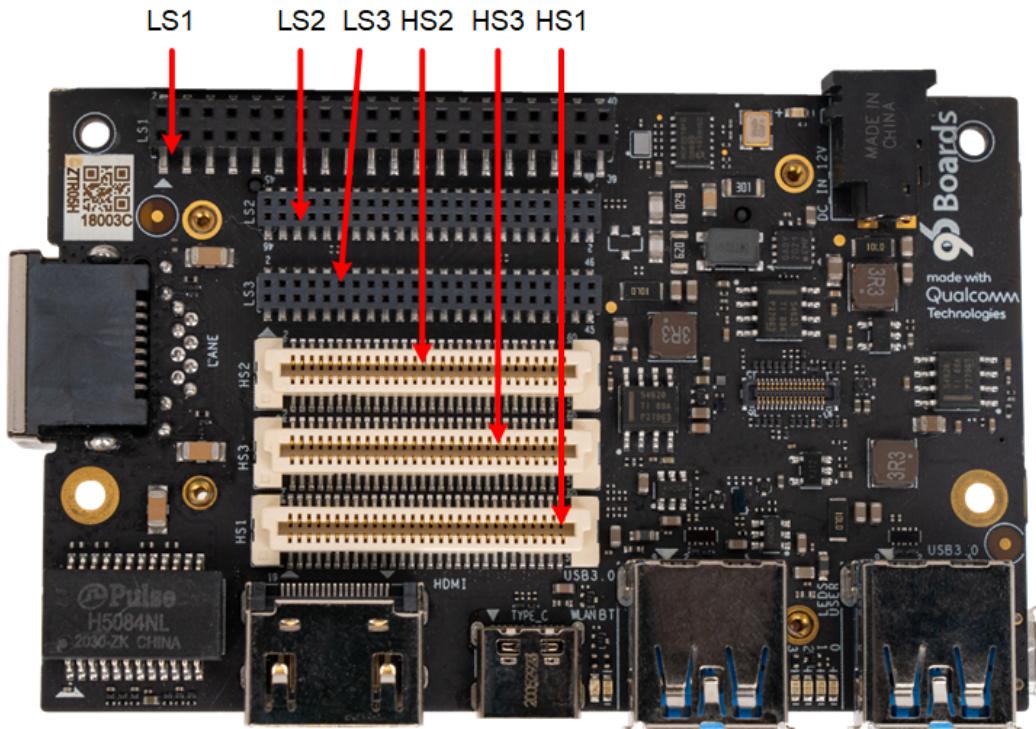
- Low-speed and high-speed expansion connector locations, GPIOs, and pin numbers
- DIP switch locations and functions
- Thermal testing details and results
- How to interface a custom camera sensor
- Reference designs and related documents
- Acronyms and terms

## 5.1 Low-speed and high-speed expansion connectors

All regular GPIOs and Qualcomm universal peripherals (QUPs) are 1.8 V logic unless otherwise specified.

The following image shows the location of the low-speed and high-speed expansion connectors on the mainboard.

## Top view of Mainboard



### Low-speed expansion connector 1 (LS1)

The LS1 connector has the following functionalities:

- UART (x2)
- I2C (x2)
- SPI
- PCM
- GPIOs (x12)
- DC power
- Ground

The GPIOs labeled QUP have additional low-speed interface capabilities (UART, SPI, I2C).

You can also use low-speed interfaces to control various peripherals, such as audio functions.

**LS1 connector details**

<b>Wake-up function</b>	<b>GPIO</b>	<b>Signal</b>	<b>Pin number</b>		<b>Signal</b>	<b>GPIO</b>	<b>Wake-up function</b>
–	–	GND	1	2	GND	–	–
Yes	16	UART0_CTS	3	4	PWR_BTN_N	KPD_PWR_N	–
Yes	18	UART0_TXD	5	6	RST_BTN_N	PM_RESIN_N	–
Yes	19	UART0_RXD	7	8	SPI0_SCLK	46	–
–	17	UART0_RTS	9	10	SPI0_MISO	44	Yes
–	22	UART1_TXD	11	12	SPI0_CS	47	Yes
Yes	23	UART1_RXD	13	14	SPI0_MOSI	45	Yes
–	9	I2C0_SCL	15	16	PCM_FS/I2S0_WS	100	–
Yes	8	I2C0_SDA	17	18	PCM_CLK/I2S0_CLK	97	–
–	5	I2C1_SCL	19	20	PCM_DO/I2S0_D1	99	–
Yes	4	I2C1_SDA	21	22	PCM_DI/I2S0_D0	98	–
Yes	36	GPIO-A/QUP-A0	23	24	GPIO-B	96	Yes
–	37	GPIO-C/QUP-A1	25	26	GPIO-D/QUP-A3	39	Yes
–	38	GPIO-E/QUP-A2	27	28	GPIO-F*	124	–
Yes	80	GPIO-G*	29	30	GPIO-H*	123	Yes
Yes	20	GPIO-I*	31	32	GPIO-J*	109	–
Yes	21	GPIO-K*	33	34	GPIO-L*	136	Yes
–	–	1.8 V-A	35	36	SYS_DCIN	–	–

Wake-up function	GPIO	Signal	Pin number		Signal	GPIO	Wake-up function
–	–	5V	37	38	SYS_DCIN	–	–
–	–	GND	39	40	GND	–	–

## Low-speed expansion connector 2 (LS2)

The LS2 connector has the following functionalities:

- Three pairs of DMICs
- Additional 4-bit I2S audio interface
- CAN-FD interface
- 2x camera CCI I2C
- PMIC PWM and ADC pins
- Configurable interface available for SPI/I2C and UART
- Spare GPIOs
- Battery ID/therm

You can also use low-speed interfaces to control various peripherals, such as audio functions.

### LS2 connector details

Wake-up function	GPIO	Signal	Pin number		Signal	GPIO	Wake-up function
Yes	78	GPIO-U	1	2	GPIO-Z	149	Yes
Yes	150	DMIC CLK1/AMIC1_P	3	4	CAN_H	–	–
Yes	151	DMIC DATA1/AMIC1_M	5	6	CAN_L	–	–
Yes	148	GPIO-V/I2S1_DATA2	7	8	1.8V-A	VREG_SYS_1P8	–
–	152	DMIC CLK2/AMIC3_P	9	10	GND	–	–

Wake-up function	GPIO	Signal	Pin number		Signal	GPIO	Wake-up function
Yes	153	DMIC DATA2/AMIC3_M	11	12	PM_GPIO-A (PWM output)	—	—
—	110	GPIO-W/I2S1_DATA3 (CAM5_RST_N)	13	14	PM_GPIO-B (PWM output)	—	—
Yes	156	DMIC_CLK3/HS_MIC_P	15	16	GPIO-M/QUP-B0	32	Yes
Yes	157	DMIC DATA3/HS_MIC_M	17	18	GPIO-N/QUP-B1	33	—
—	—	PM_GPIO-F	19	20	GPIO-O/QUP-B2 (also PWM)	34	Yes
—	74	CCI_I2C_SCL2	21	22	GPIO-P/QUP-B3	35	Yes
—	73	CCI_I2C_SDA2	23	24	GPIO-Q/I2S1_WS	145	Yes
—	76	CCI_I2C_SCL3	25	26	GPIO-R/I2S1_CLK	144	—
—	—	SPK0_P	27	28	GPIO-S/I2S1_DATA0	146	—
—	—	SKP0_M	29	30	GPIO-T/I2S1_DATA1	147	—
—	—	SPK1_P	31	32	PM_GPIO-C (ADC IN)	PM_B_AMUX2 (PM7325)	—
—	—	SPK1_M	33	34	PM_GPIO-D (ADC IN)	PM_B_AMUX4 (PM7325)	—

Wake-up function	GPIO	Signal	Pin number		Signal	GPIO	Wake-up function
Yes	75	CCI_I2C_SDA3	35	36	BATT_THERM	PM7250B	–
–	–	PM_GPIO-E	37	38	BATT_ID	PM7250B	–
–	–	VBAT	39	40	USB_VBUS	–	–
–	–	GND	41	42	GND	–	–
Yes	6	GPIO-X	43	44	GPIO-AA	25	Yes
–	137	GPIO-Y	45	46	GPIO-BB	120	–

## Low-speed expansion connector 3 (LS3)

The LS3 connector has the following functionalities:

- Four Qualcomm sensor core QUP interfaces
- Interrupts signals for sensors
- Additional GPIOs and power supplies

The GPIOs labeled QUP have additional low-speed interface capabilities (UART, SPI, I2C). Several GPIOs can be used to wake up the application processor.

**LS3 connector details**

Wake-up function	GPIO	Signal	Pin number		Signal	GPIO	Wake-up function
–	68	GPIO-KK	1	2	GPIO-TT	90	–
–	PMIC	SLEEP_CLK	3	4	CLK	PMIC	–
Yes	119	GPIO-LU	5	6	GPIO-UU	83	Yes
Yes	40	GPIO-MM	7	8	QCA_GPIO-D	112	–
Yes	41	GPIO-NN	9	10	QCA_GPIO-E	113	–
–	42	GPIO-OO	11	12	QCA_GPIO-ZZ	114	Yes

Wake-up function	GPIO	Signal	Pin number		Signal	GPIO	Wake-up function
–	111	QCA_GPIO-A GPIO-AAA	13	14	GPIO-WW	115	Yes
–	116	QCA_GPIO-B GPIO-BBB	15	16	SPI3_MISO	48	Yes
–	117	QCA_GPIO-C GPIO-CCC	17	18	SPI3_MOSI	49	–
Yes	43	GPIO-PP	19	20	SPI3_CLK	50	–
–	129	GPIO-QQ	21	22	SPI3_CS	51	Yes
Yes	165	SPI2_CLK (on SSC*)	23	24	PS_INT	104	Yes
–	164	SPI2_MOSI (on SSC*)	25	26	ACCEL_INT	103	Yes
Yes	163	SPI2_MISO (on SSC*)	27	28	GYRO_INT	102	Yes
Yes	166	SPI2_ACCEL_CS (on SSC*)	29	30	MAG_INT	142	Yes
–	161	SPI2_CS1 (on SSC*)	31	32	MAG_DRDY_INT	81	Yes
Yes	55	SPI3_CS1 (on SSC*)	33	34	I2C4_SDA (on SSC*)	159	–
–	VREG_L8C_1P8	1.8 V-B	35	36	I2C4_SCL (on SSC*)	160	–
–	–	5V	37	38	1.8 V-C	VREG_L2C_1P8	–

Wake-up function	GPIO	Signal	Pin number		Signal	GPIO	Wake-up function
–	–	VBAT	39	40	GND	–	–
–	–	GND	41	42	GND	–	–
Yes	130	GPIO-RR	43	44	SPI3_CS2	54	Yes
Yes	52	GPIO-SS	45	46	GPIO-XX	53	–

\* SSC is the sensor core running on DSP.

## High-speed expansion connector 1 (HS1)

The HS1 connector has the following functionalities:

- GPIOs
- Display serial interface (DSI)
- Camera serial interfaces (CSI) (x2)
- Camera MClk
- Camera control interface (CCI) I2C
- USB DP/DM

**HS1 connector details**

Wake-up function	GPIO	Signal	Pin number		Signal	GPIO	Wake-up function
–	61	GPIO	1	2	CSI0_C_P	–	–
–	118	GPIO	3	4	CSI0_C_M	–	–
–	138	GPIO	5	6	GND	–	–
–	63	GPIO	7	8	CSI0_D0_P	–	–
–	62	GPIO	9	10	CSI0_D0_M	–	–
–	60	GPIO	11	12	GND	–	–
–	–	GND	13	14	CSI0_D1_P	–	–
–	64	CLK0/CSI0_MCLK	15	16	CSI0_D1_M	–	–

Wake-up function	GPIO	Signal	Pin number		Signal	GPIO	Wake-up function
–	67	CLK3/CSI3_17 MCLK	18		GND	–	–
–	–	GND	19	20	CSI0_D2_P	–	–
–	–	DSI0_CLK_P	21	22	CSI0_D2_M	–	–
–	–	DSI0_CLK_M	23	24	GND	–	–
–	–	GND	25	26	CSI0_D3_P	–	–
–	–	DSI0_D0_P	27	28	CSI0_D3_M	–	–
–	–	DSI0_D0_M	29	30	GND	–	–
–	–	GND	31	32	CCI_I2C_SCL0	70	–
–	–	DSI0_D1_P	33	34	CCI_I2C_SDA0	69	–
–	–	DSI0_D1_M	35	36	CCI_I2C_SCL1	72	Yes
–	–	GND	37	38	CCI_I2C_SDA1	71	–
–	–	DSI0_D2_P	39	40	GND	–	–
–	–	DSI0_D2_M	41	42	CSI3_D0_P	–	–
–	–	GND	43	44	CSI3_D0_M	–	–
–	–	DSI0_D3_P	45	46	GND	–	–
–	–	DSI0_D3_M	47	48	CSI3_D1_P	–	–
–	–	GND	49	50	CSI3_D1_M	–	–
–	–	USB0_DP	51	52	GND	–	–

Wake-up function	GPIO	Signal	Pin number		Signal	GPIO	Wake-up function
–	–	USB0_DM	53	54	CSI3_C_P	–	–
–	–	GND	55	56	CSI3_C_M	–	–
–	–	USB1_DP / NC	57	58	GND	–	–
–	–	USB1_DM / NC	59	60	Reserved	–	–

## High-speed expansion connector 2 (HS2)

The HS2 connector has the following functionalities:

- PCIe interface and control signals
- CSI (x2)
- SPI/QUP interface
- Camera MClk (x2)
- Additional GPIOs
- SS USB signals

### HS2 connector details

Wake-up function	GPIO	Signal	Pin number		Signal	GPIO	Wake-up function
–	–	PCIE1_REFCLK_M	1	2	CSI1_C_P	–	–
–	–	PCIE1_REFCLK_P	3	4	CSI1_C_M	–	–
–	–	PCIE1_RX_M	5	6	GND	–	–
–	–	PCIE1_RX_P	7	8	CSI1_D0_P	–	–
–	–	PCIE1_TX_M	9	10	CSI1_D0_M	–	–
–	–	PCIE1_TX_P	11	12	GND	–	–

Wake-up function	GPIO	Signal	Pin number		Signal	GPIO	Wake-up function
–	87	GPIO-CC	13	14	CSI1_D1_P	–	–
Yes	88	GPIO-DD	15	16	CSI1_D1_M	–	–
Yes	89	GPIO-EE	17	18	GND	–	–
–	2	GPIO-FF	19	20	CSI1_D2_P	–	–
Yes	79	GPIO-GG	21	22	CSI1_D2_M	–	–
Yes	3	GPIO-HH	23	24	GND	–	–
–	–	GND	25	26	CSI1_D3_P	–	–
–	65	CLK1/CSI1_MCLK	27	28	CSI1_D3_M	–	–
–	66	CLK2/CSI2_MCLK	29	30	GND	–	–
–	–	GND	31	32	SPI1_CLK	58	–
–	–	CSI2_C_P	33	34	SPI1_CS	59	Yes
–	–	CSI2_C_M	35	36	SPI1_MOSI	57	–
–	–	GND	37	38	SPI1_MISO	56	Yes
–	–	CSI2_D0_P	39	40	GPIO-AA/CSI4_MCLK	68	Yes
–	–	CSI2_D0_M	41	42	GPIO-BB/CSI5_MCLK	93	Yes
–	–	GND	43	44	GPIO-II	77	Yes
–	–	CSI2_D1_P	45	46	GPIO-JJ	122	–
–	–	CSI2_D1_M	47	48	PMIC_SPMI_CLK	PMK_7325_GPIO_01	–
–	–	GND	49	50	PMIC_SPMI_DATA	PMK_7325_GPIO_02	–

<b>Wake-up function</b>	<b>GPIO</b>	<b>Signal</b>	<b>Pin number</b>		<b>Signal</b>	<b>GPIO</b>	<b>Wake-up function</b>
–	–	CSI2_D2_P	51	52	GND	–	–
–	–	CSI2_D2_M	53	54	USB0_SS_TX0_P	–	–
–	–	GND	55	56	USB0_SS_TX0_M	–	–
–	–	CSI2_D3_P	57	58	USB0_SS_RX0_P	–	–
–	–	CSI2_D3_M	59	60	USB0_SS_RX0_M	–	–

#### High-speed expansion connector 3 (HS3)

The HS3 connector has the following functionalities:

- Additional PCIe interface
- Additional camera CSI interface
- Additional display DSI interface
- Additional clock signals

#### HS3 connector details

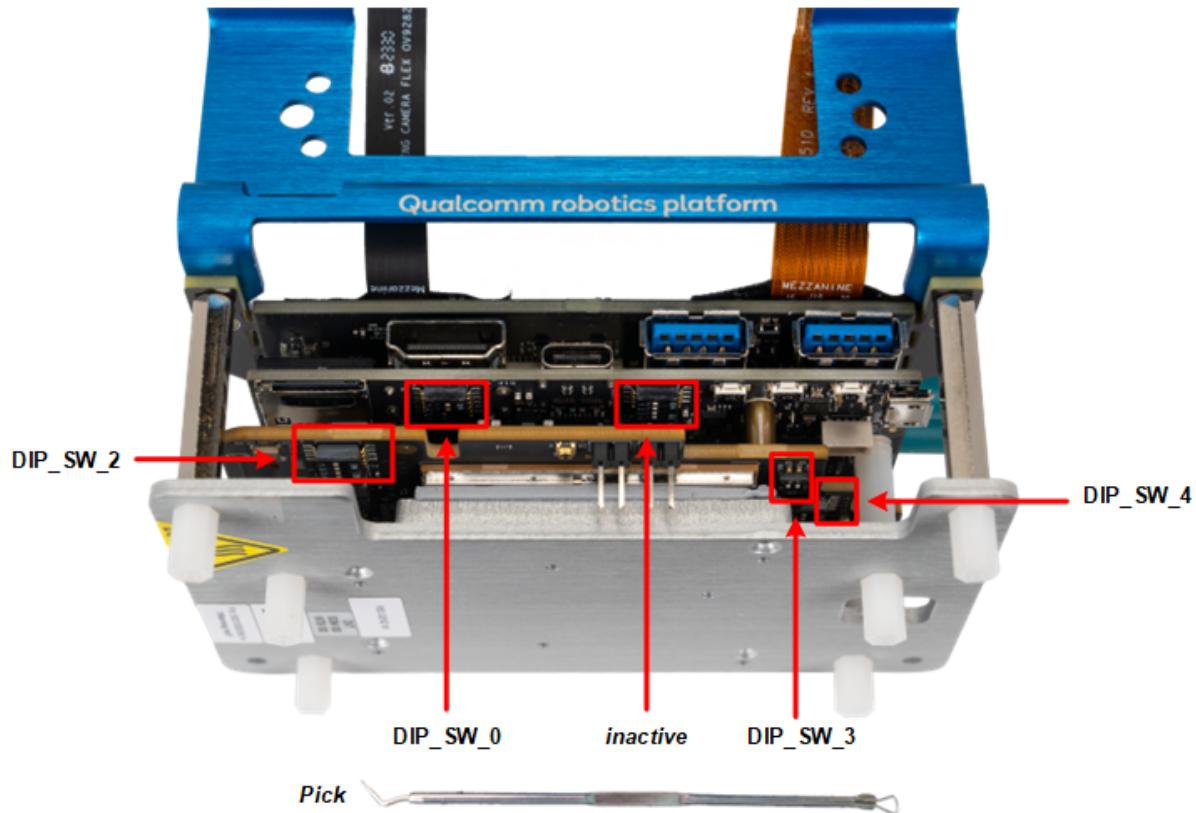
<b>Wake-up function</b>	<b>GPIO</b>	<b>Signal</b>	<b>Pin number</b>		<b>Signal</b>	<b>GPIO</b>	<b>Wake-up function</b>
–	–	CSI4_C_P	1	2	GND	–	–
–	–	CSI4_C_M	3	4	PCIE1_RX1_M	–	–
–	–	CSI4_D0_P	5	6	PCIE1_RX1_P	–	–
–	–	CSI4_D0_M	7	8	PCIE1_TX1_M	–	–
–	–	GND	9	10	PCIE1_TX1_P	–	–
–	–	CSI4_D1_P	11	12	GND	–	–

Wake-up function	GPIO	Signal	Pin number		Signal	GPIO	Wake-up function
–	–	CSI4_D1_M	13	14	PCIE2_REFCLK_M	–	–
–	–	CSI4_D2_P	15	16	PCIE2_REFCLK_P	–	–
–	–	CSI4_D2_M	17	18	PCIE2_RX0_M	–	–
–	–	CSI4_D3_P	19	20	PCIE2_RX0_P	–	–
–	–	CSI4_D3_M	21	22	PCIE2_RX1_M (not used)	–	–
–	–	GND	23	24	PCIE2_RX1_P (not used)	–	–
–	–	CSI3_D2_P	25	26	PCIE2_TX0_M	–	–
–	–	CSI3_D2_M	27	28	PCIE2_TX0_P	–	–
–	–	CSI3_D3_P	29	30	PCIE2_TX1_M (not used)	–	–
–	–	CSI3_D3_M	31	32	PCIE2_TX1_P (not used)	–	–
–	–	GND	33	34	GND	–	–
–	–	CSI5_C_P	35	36	DSI1_CLK_P	–	–
–	–	CSI5_C_M	37	38	DSI1_CLK_M	–	–
–	–	CSI5_D0_P	39	40	DSI1_D0_P	–	–
–	–	CSI5_D0_M	41	42	DSI1_D0_M	–	–

Wake-up function	GPIO	Signal	Pin number		Signal	GPIO	Wake-up function
–	–	CSI5_D1_P	43	44	DSI1_D1_P	–	–
–	–	CSI5_D1_M	45	46	DSI1_D1_M	–	–
–	–	CSI5_D2_P	47	48	GND	–	–
–	–	CSI5_D2_M	49	50	DSI1_D2_P	–	–
–	–	CSI5_D3_P	51	52	DSI1_D2_M	–	–
–	–	CSI5_D3_M	53	54	DSI1_D3_P	–	–
–	–	GND	55	56	DSI1_D3_M	–	–
–	–	PMK8002_RF_CLK1	57	58	GND	–	–
–	LNBCLK2	PMK8002_RF_CLK2	59	60	GPIO-DDD	PM_A_GPIO_05 (PM7250B)	–

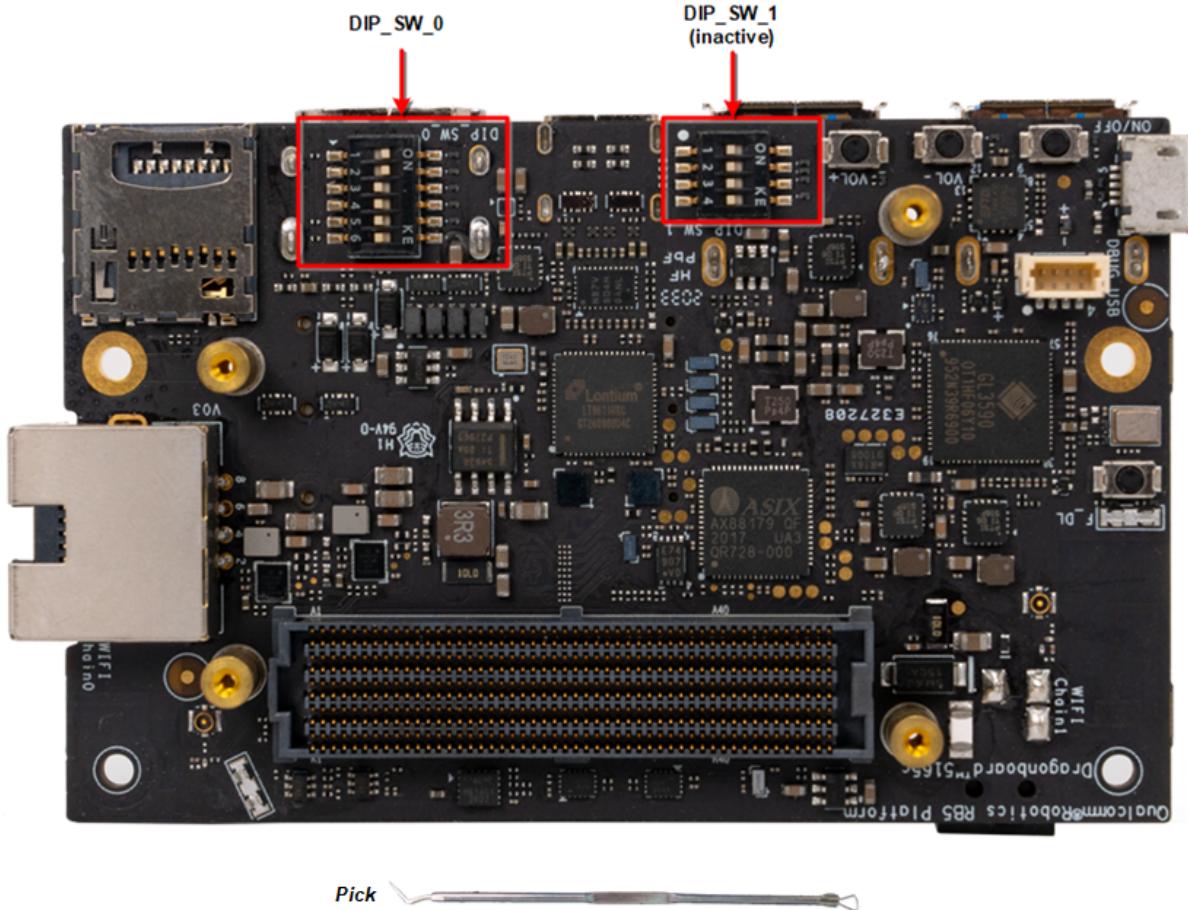
## 5.2 DIP switches

The following image shows the location of the DIP switches on the mainboard and interposer.



DIP switches are on the front, underside of the mainboard and interposer board. They're near the front, on the top side of the vision mezzanine board. A tool similar to a dental pick is provided to help access switches that might be difficult to reach.

## Mainboard DIP switches



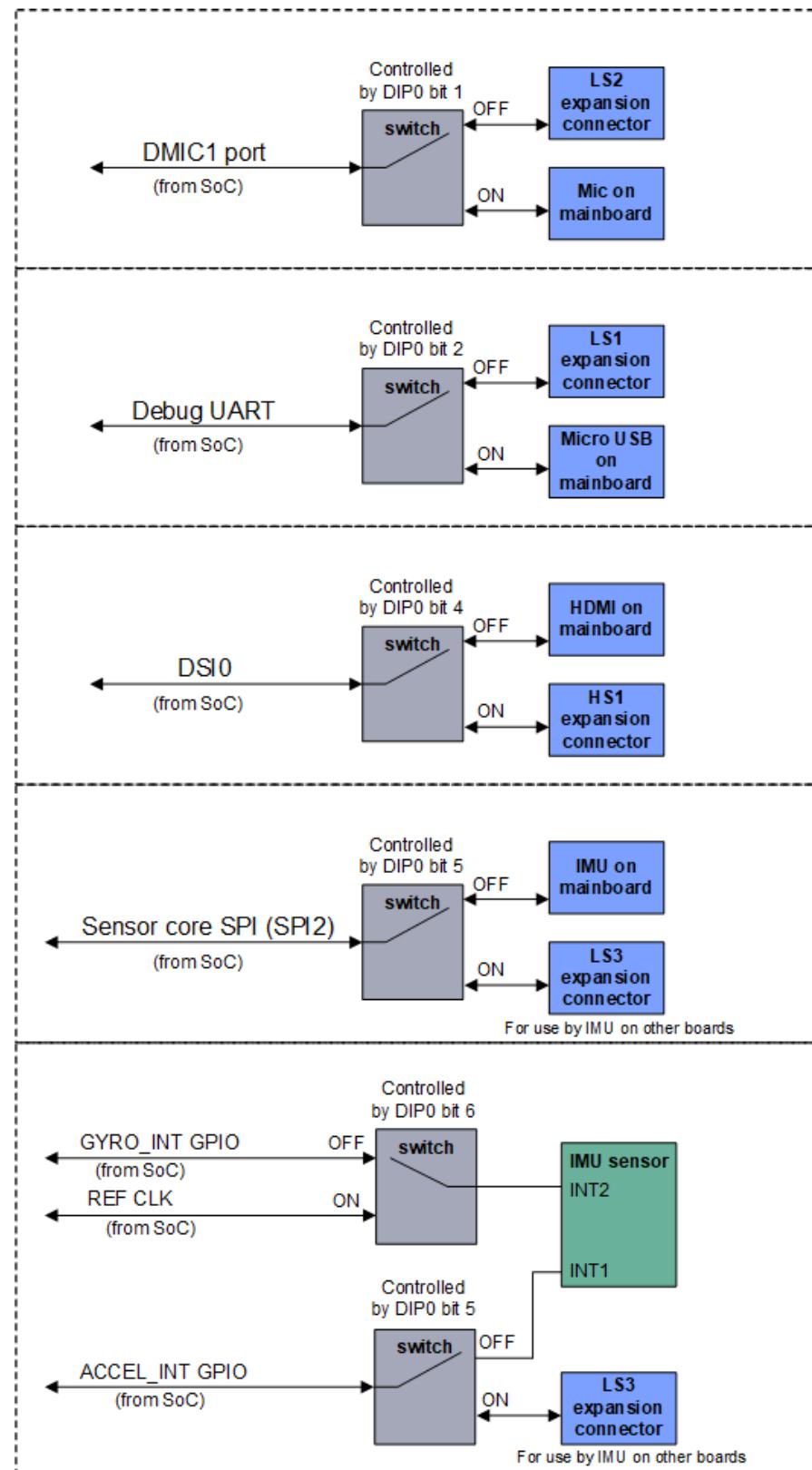
DIP\_SW\_0 contains six switches and is present on the bottom side of the mainboard. DIP\_SW\_1 is inactive. Use the pick included in the kit to help access switches that might be difficult to reach. The following table lists the switches and their functionalities.

**DIP switch selection**

DIP_SW_0	Name	Details	Default
1	Mic switch	ON: on-board DMIC OFF: off-board DMIC (LS2 connector)	ON
2	Debug UART	ON: enable serial log (debug UART) OFF: disable serial log (off-board UART)	ON
3	N/A	—	—

<b>DIP_SW_0</b>	<b>Name</b>	<b>Details</b>	<b>Default</b>
4	HDMI switch	ON: HDMI disabled OFF: HDMI enabled	OFF
5	Sensor IMU toggle	ON: on-board IMU disabled OFF: on-board IMU enabled	OFF
6	IMU external clock	ON: external clock to IMU OFF: no external clock to IMU	OFF

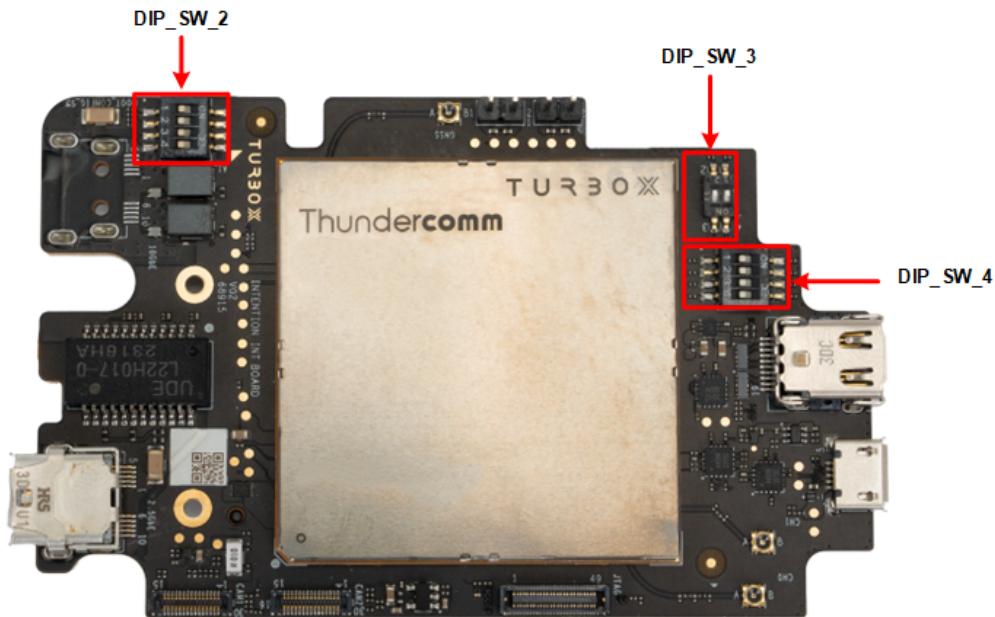
The following flowcharts show how the DIP switch settings on the mainboard control the routing of signals from/to connectors and components. Refer to the [block diagram](#) to see the signals, switches, and connectors in context.



### Circuits controlled by DIP switches on the mainboard

## Interposer DIP switches

The following image shows the location of the interposer DIP switches.



### DIP switches on the interposer

The interposer board has three boot configuration DIP switches. The following table lists the interposer DIP switches along with their functionalities:

**Interposer DIP switch selection (DIP\_SW\_2)**

DIP_SW_2	Name	Details	Default
1	BOOT_CONFIG_1 [GPIO_120]	Selects external boot devices	OFF
2	BOOT_CONFIG_2 [GPIO_122]		OFF
3	BOOT_CONFIG_3 [GPIO_124]		OFF
4	BOOT_CONFIG_0 [GPIO_118]	ON: disables watchdog OFF: enables watchdog	OFF

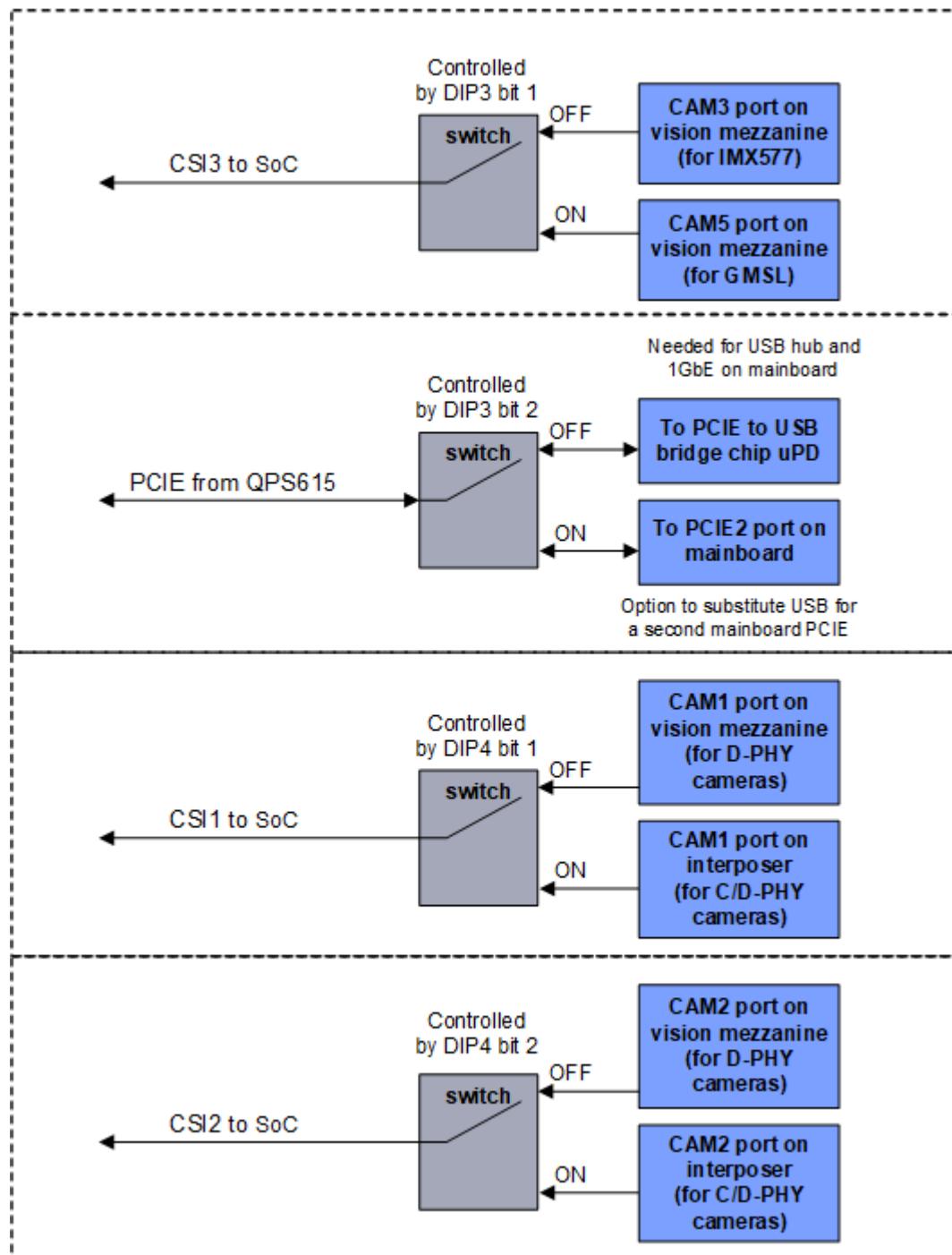
**Interposer DIP switch selection (DIP\_SW\_3)**

DIP_SW_3	Name	Details	Default
1	DIP_CSI3_SW	OFF: CSI3 input from Vision mezzanine CAM3 (IMX577) ON: CSI3 input from Vision mezzanine CAM5 (GMSL)	OFF
2	PCIE_DIP_SW	ON: QPS 1 Lane PCIe goes to mainboard 500 pin (HS expansion PCIE2) OFF: QPS 1 Lane PCIe goes to PCIE2USB (uPD)	OFF

**Interposer DIP switch selection (DIP\_SW\_4)**

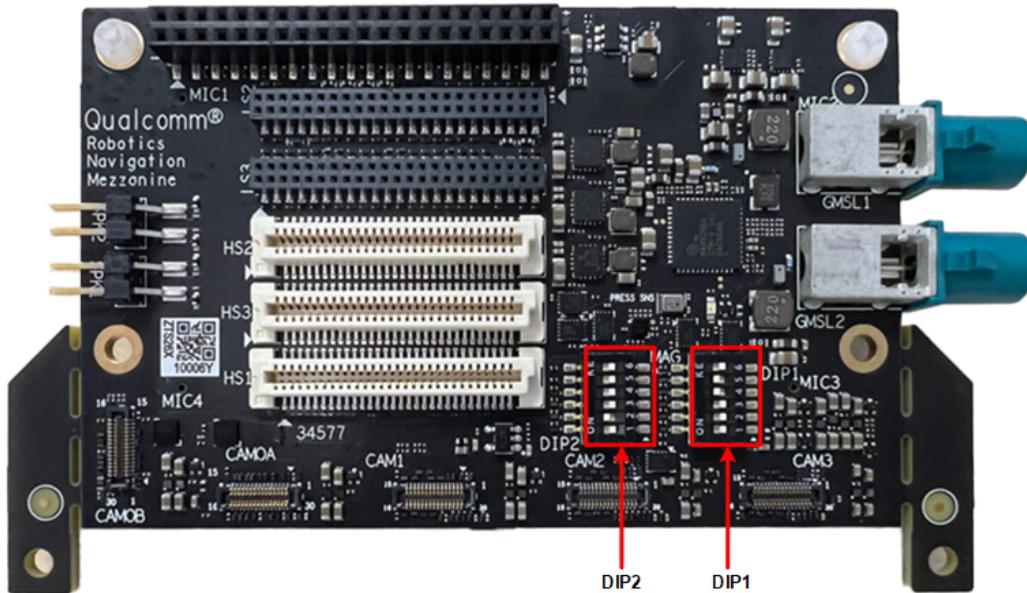
DIP_SW_4	Name	Details	Default
1	CSI1_DIP_SW	ON: CSI1 input from interposer CPHY CAM1 OFF: CSI1 input from Vision mezzanine CAM1	OFF
2	CSI2_DIP_SW	ON: CSI2 input from interposer CPHY CAM2 OFF: CSI2 input from Vision mezzanine CAM2	OFF
3	QSPI_CAN_DIP_SW	ON: not supported OFF: SPI to CAN interface on mainboard	OFF
4	QSPI_GPIO_DIP_SW	ON: not supported OFF: SPI to CAN interface on mainboard	OFF

The following flowcharts show how the DIP switch settings on the interposer control the routing of signals from/to connectors and components. Refer to the [block diagram](#) to see the signals, switches, and connectors in context.

**Circuits controlled by DIP switches on the interposer**

## Vision mezzanine DIP switches

The following image shows the location of the DIP switches on the Vision mezzanine.



**Vision mezzanine DIP switches**

**Vision mezzanine DIP switches (DIP1)**

DIP1	Name	Details	Default
1	SENSOR_SPI_PASSTHRU	ON: Snapdragon sensor core (SSC) sensor SPI routed to IMU_SPI_SELECT switch OFF: IMU sensor SPI passthrough	OFF
2	APPS_SPI_PASSTHRU	ON: Application processor SPI routed to IMU_SPI_SELECT switch OFF: passthrough	OFF
3	CAM2_APPS_SPI_PASSTHRU	ON: SPI to CAM2 connector OFF: passthrough	OFF
4	PRESS_SENS_DISCONNECT	ON: on-board OFF: disconnected	ON

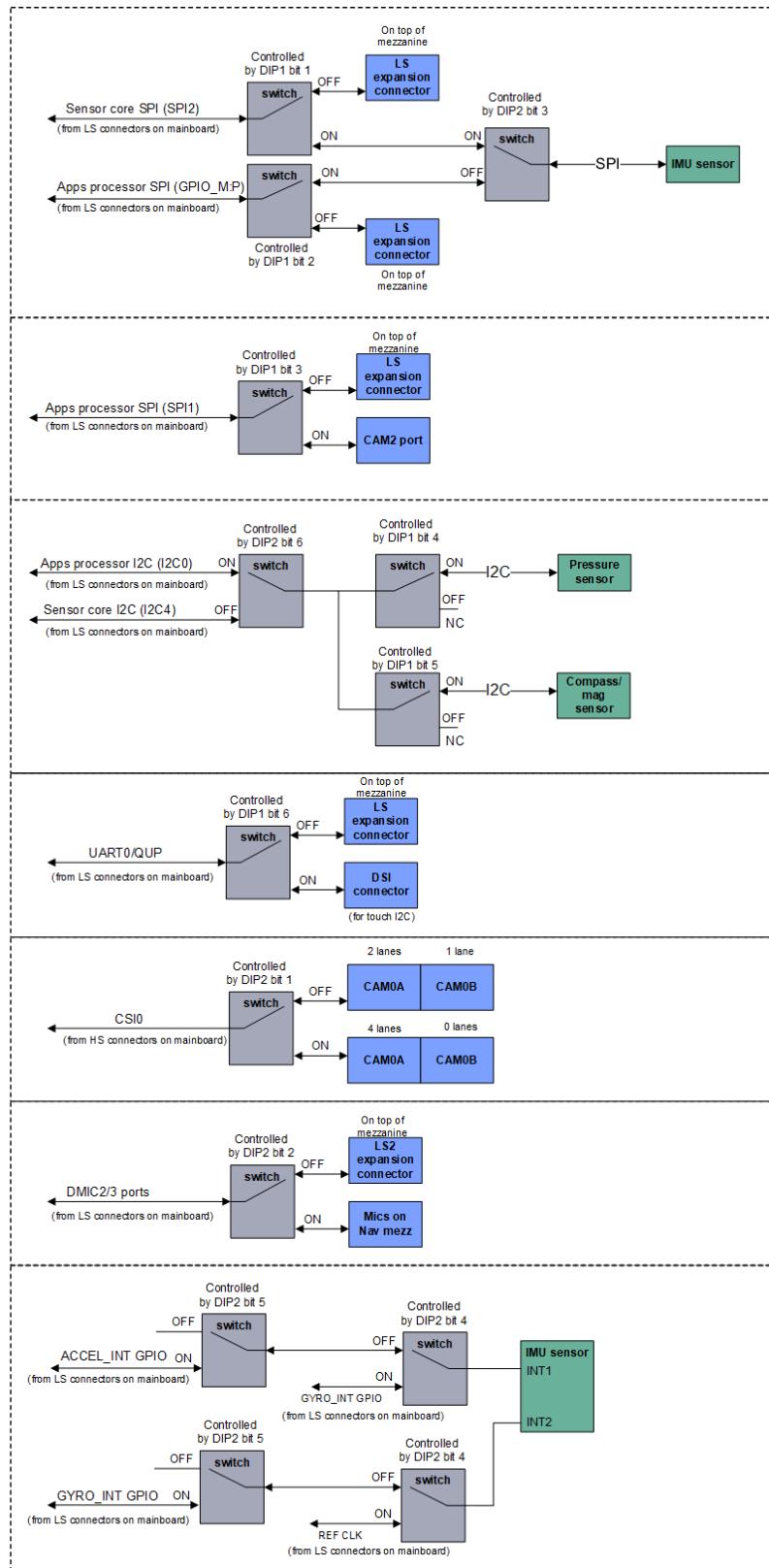
<b>DIP1</b>	<b>Name</b>	<b>Details</b>	<b>Default</b>
5	MAG_SENSOR_DISCONNECT	ON: on-board OFF: disconnected	ON
6	UART0_PASSTHRU	ON: on-board OFF: passthrough	OFF

**Vision mezzanine DIP switches (DIP2)**

<b>DIP2</b>	<b>Name</b>	<b>Details</b>	<b>Default</b>
1	DIP_CSI0A_B_SWITCH	ON: CSI0 all 4 lanes to CAM0A OFF: CSI0 2 lanes to CAM0A, 1 lane to CAM0B	OFF
2	MIC_DISCONNECT	ON: DMIC 2/3 connects to on-board mics OFF: DMIC 2/3 passthrough	ON
3	IMU_SPI_SELECT	ON: connects IMU to APPS SPI – only if DIP 1:2 is ON OFF: connects IMU to SSC SPI – only if DIP 1:1 is ON	OFF
4	IMU_INT_1_2_SELECT_LOGIC1	ON: IMU INT1 to GYRO_INT, IMU INT2 to PMIC clock OFF: IMU INT1 and 2 connected to IMU sensor switch	OFF
5	IMU_INT_1_2_SELECT_LOGIC2	ON: IMU INT1 to ACCEL_INT, IMU INT2 to GYRO_INT OFF: IMU INT 1 and 2 disconnected	OFF

DIP2	Name	Details	Default
6	PRESSURE_COMPASS_SELECT	ON: Pressure/Compass connected to APPS I2C OFF: Pressure/Compass connected to sensor core I2C	OFF

The following flowcharts show how the DIP switch settings on the Vision mezzanine control the routing of signals from/to connectors and components. Refer to the [block diagram](#) as necessary to see the signals, switches, and connectors in context.



### Circuits controlled by DIP switches on the Vision mezzanine

## 5.3 Thermal testing and results

The RB3 Gen 2 Development Kit has significant capabilities and can get hot under load. It's not meant to be held for extended periods of time. The baseplate can reach temperatures up to 50-55°C, which is a generally accepted industry standard for non-handheld devices. For more information about maximum touch temperatures, see *How Hot is too Hot?*

<<https://www.boydcorp.com/blog/maximum-touch-temperature.html>>

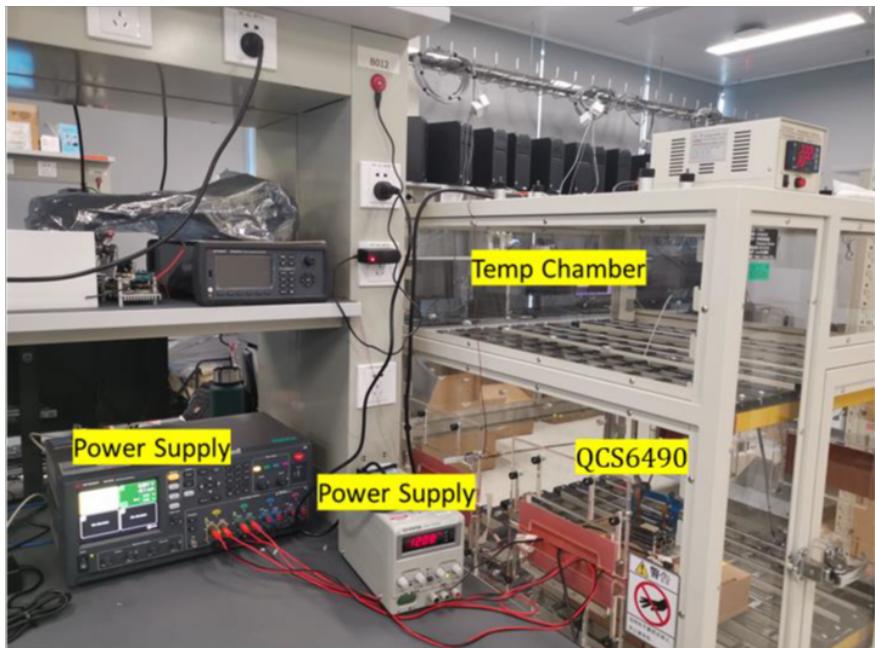
The following image shows the location of temperature warning stickers on the baseplate.



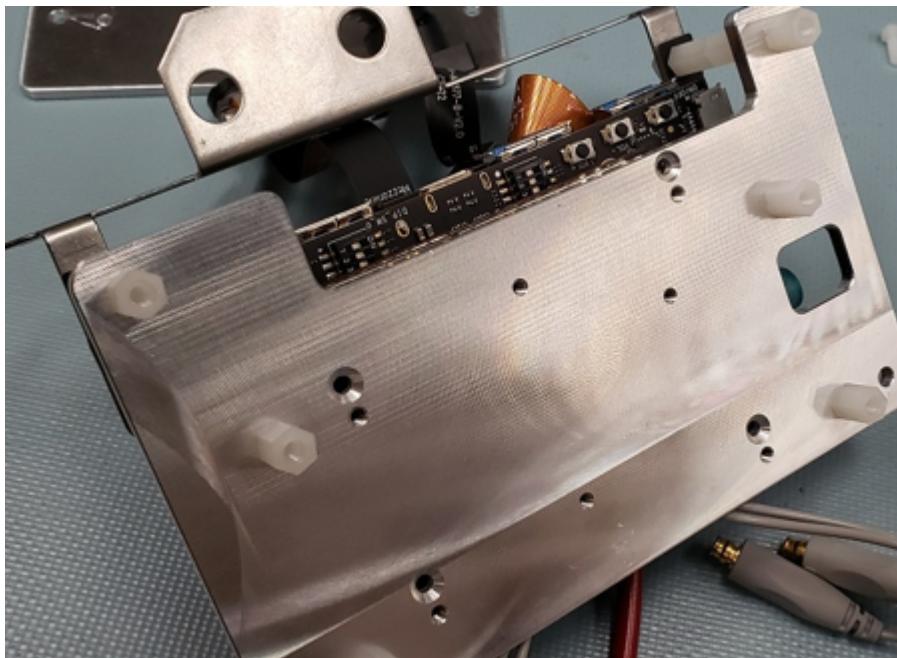
Temperature warning stickers on baseplate

## Test environment

The following image shows the thermal test setup used in these test cases.

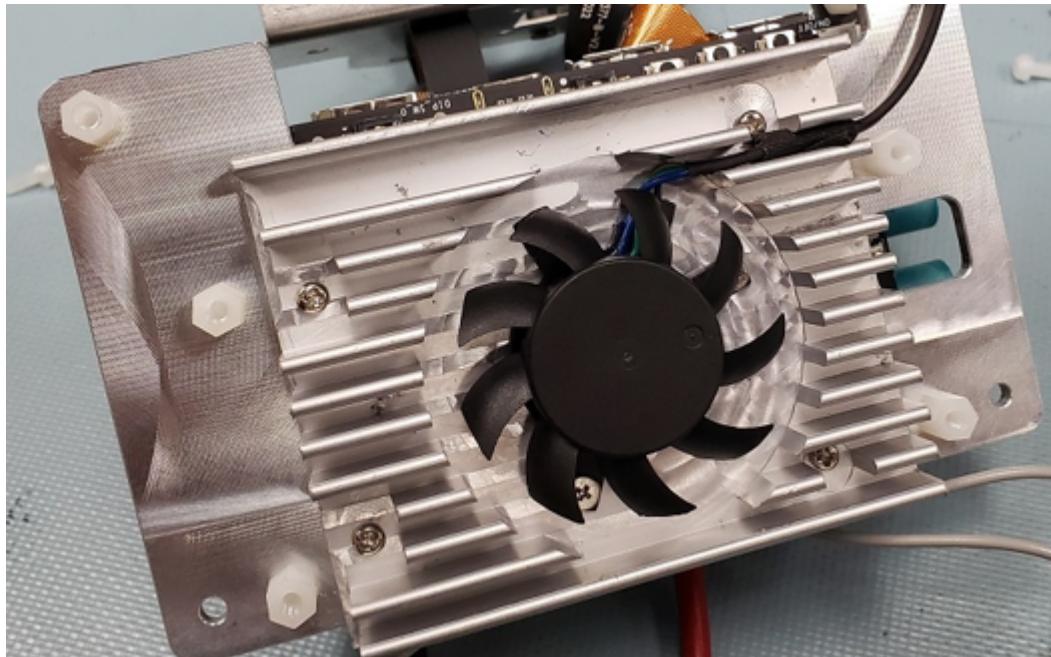


**Thermal test setup**



**Setup 1: Heatsink – only baseplate**

SoM + interposer can support up to 7.45W at 95C T<sub>j</sub> limit with above design.



**Setup 2: Heatsink – baseplate with fan**

SoM + interposer can support up to 11W at 95C T<sub>j</sub> limit with above design.

## **Test scenario - example 1**

- Power supply: 4.2v for SoM and interposer, 12v for others
  - Power measure : SoM power and interposer power
  - Ta setting : 25C with a temperature chamber
  - vML for GPU and HTP is running Tflite+QNN
  - v5Camera is 3xIMX577 720p30fps preview + recording 2xOV9282 720p30fps RDI dump
-

Area	Test cases
------	------------

## Test case

Sample use cases for test case example 1.

Case 1

Area	Test cases
Case1 (5camera+2 AI + Iperf3+Display+BT+wlan wlan+Audio)	IMX577 <a href="#">camera1_720p@30fps_preview+recording</a>
	IMX577 <a href="#">camera2_720p@30fps_preview+recording</a>
	IMX577 <a href="#">camera3_720p@30fps_preview+recording</a>
	OV9282 <a href="#">Camera1_720p@30fps RDI_dump</a>
	OV9282 <a href="#">Camera2_720p@30fps RDI_dump</a>
	2ML QNN running on HTP(Benchmark)
	GPU run with Weston sample
	Iperf3 1Gbps via ethernet
	HDMI with Weston launch
	BT paired
	WLAN connected and Ping
	Audio playback over speaker

Case 2

Area	Test cases
Case2 (5camera+1 AI +GPU GPU+Display+BT+wlan wlan+Audio)	IMX577 <a href="#">camera1_720p@30fps_preview+recording</a>
	IMX577 <a href="#">camera2_720p@30fps_preview+recording</a>
	IMX577 <a href="#">camera3_720p@30fps_preview+recording</a>
	OV9282 <a href="#">Camera1_720p@30fps RDI_dump</a>
	OV9282 <a href="#">Camera2_720p@30fps RDI_dump</a>
	1ML QNN running on HTP(Benchmark)
	GPU run with Weston sample
	HDMI with Weston launch
	BT paired
	WLAN connected and Ping
	Audio playback over speaker

## Thermal profile summary - test case example 1

**Setup-1: Only baseplate heatsink thermal solution**

Case	SoM power * (W)	Interposer power ** (W)	T <sub>j</sub> _Avg (°C)	quiet-therm-usr (°C)	Comment
CPU drystone 30%+1GPU +1HTP +5camera	4.87	2.04	78.75	68.89	No trigger LMH
CPU drystone 45%+1GPU +1HTP +5camera	5.31	2.03	84.48	72.60	No trigger LMH
CPU drystone 60%+1GPU +1HTP +5camera	5.39	2.06	86.33	73.91	No trigger LMH

**Setup-2 : Baseplate with fan thermal solution**

Case	SoM power * (W)	Interposer power ** (W)	T <sub>j</sub> _Avg (°C)	quiet-therm-usr (°C)	Comment
CPU drystone 30%+1GPU +1HTP +5camera	4.31	2.03	52.6	44.50	No trigger LMH
CPU drystone 45%+1GPU +1HTP +5camera	4.6	2.03	55.27	45.87	No trigger LMH
CPU drystone 60%+1GPU +1HTP +5camera	5.77	2.02	64.37	48.83	No trigger LMH

\* SoM power includes: SoC, PMICs, memory (RAM+FLASH), Wifi, GNSS (if used)

\*\* Interposer power includes: QPS615 PCIE bridge chip, PCIE to USB bridge chip, Ethernet PHY chips for 2.5GbE/10GbE (if used)

## Thermal profile summary - test case example 2

**Setup-1: Only baseplate heatsink thermal solution**

SoM @4.2V(in W)	Interposer@ 4.2V(in W)	Ta	Tj start	last5m in_Tj_Avg(°C)	Tj_Max(°C)	LMH	cdsp loading	GPU loading	CPU loading	Comment
5Camera (3xIMX577 720p30fps preview + recording,2x OV9282 720p30fps RDI dump)	a6.12	2.07	26.20	33.90	91.49	95.0	Yes (Triggered five times during last 5 mins and then recovered)	97.22%	91.08%	Total CPU Util: 64.67% CPU0 Util: 83.87% CPU4 Util: 54.23% CPU7 Util:20.52% 1.Test duration: ~40 min
2 QNN run on HTP										
1 QNN run on GPU										
Cpu Drystone 95%										
BT paired										
Audio playback										
Iperf3 100M bps via wifi										
Iperf3 1Gbps via ethernet										

**Setup-2: Baseplate with fan thermal solution**

Case	SoM @4.2V (in W)	interposer @4.2V (in W)	T <sub>j</sub> start	last 5min_T <sub>j</sub> _Avg (°C)	T <sub>j</sub> _Max (°C)	LMH	cdsp loading	GPU loading	CPU loading	Comment
5Camera (3xIMX577 720p30fps preview + recording, 2x OV9282 720p30fps RDI dump)	8.56	2.31	26.00	33.60	81.30	85.30	No	99.21%	97.39%	Total CPU Util - 99.13% limited to CPU4~85Mbps Util:99.97% CPU4_ lperf3 Util: via 98.69% ethernet CPU7 throughput Util:98.70% limited to 500~650Mbps Test duration ~40 min
4ML QNN run on HTP										
2 QNN run on GPU										
Cpu drystone 95%										
BT paired										
Audio playback										
Iperf3 100Mbps via wifi										
Iperf3 1Gbps via ethernet										

Test results subject to change with different design and total system power.

Note:

- SoM power includes: SoC, PMICs, memory (RAM+FLASH), Wifi, GNSS (if used)
- Interposer power includes: QPS615 PCIe bridge chip, PCIe to USB bridge chip, Ethernet PHY chips for 2.5GbE/10GbE (if used)

### Test case example 1 and 2: Detailed summary table

**Internal thermal test results on QCS6490 RB3 Gen 2 platform**

Iterations	Use case	System Power SoM+Interposer (W)	SoM power SOC+PMIC+DDR +wifi+Gnss(if used) (W)	Thermal solutions
Case 1	vML for GPU and HTP is running Tflite + QNN v5 camera is 3xIMX577 720p30fps preview +recording, 2xOV9282 720p30fps RDI dump) CPU drystone 30%+1GPU+1HTP +5camera	4.87+2.04 = 6.91	4.87	Baseplate heatsink
Case 2	vML for GPU and HTP is running Tflite + QNN v5 camera is 3xIMX577 720p30fps preview +recording, 2xOV9282 720p30fps RDI dump) CPU drystone 45%+1GPU+1HTP +5camera	5.31+2.03=7.34	5.31	Baseplate heatsink

<b>Iterations</b>	<b>Use case</b>	<b>System Power SoM+Interposer (W)</b>	<b>SoM power SOC+PMIC+DDR +wifi+Gnss(If used) (W)</b>	<b>Thermal solutions</b>
Case 3	vML for GPU and HTP is running Tflite + QNN v5 camera is 3xIMX577 720p30fps preview +recording, 2xOV9282 720p30fps RDI dump) CPU drystone 60%+1GPU+1HTP +5camera	5.39+2.06=7.45	5.39	Baseplate heatsink
Case 4	5Camera(3xIMX577 720p30fps preview + recording,2xOV9282 720p30fps RDI dump) 2 QNN run on HTP 1 QNN run on GPU CPU drystone 60%	7.12+2.07 = 8.19	6.12	Baseplate heatsink

<b>Iterations</b>	<b>Use case</b>	<b>System Power SoM+Interposer (W)</b>	<b>SoM power SOC+PMIC+DDR +wifi+Gnss(If used) (W)</b>	<b>Thermal solutions</b>
Case 5	vML for GPU and HTP is running Tflite + QNN v5 camera is 3xIMX577 720p30fps preview +recording, 2xOV9282 720p30fps RDI dump) CPU drystone 30%+1GPU+1HTP +5camera	4.31+2.03 =6.34	4.31	Baseplate Heatsink +
Case 6	vML for GPU and HTP is running Tflite + QNN v5 camera is 3xIMX577 720p30fps preview +recording, 2xOV9282 720p30fps RDI dump) CPU drystone 60%+1GPU+1HTP +5camera	4.6+2.03 = 6.63	4.6	Baseplate Heatsink +

<b>Iterations</b>	<b>Use case</b>	<b>System Power SoM+Interposer (W)</b>	<b>SoM power SOC+PMIC+DDR +wifi+Gnss(If used) (W)</b>	<b>Thermal solutions</b>
Case 7	vML for GPU and HTP is running TfLite + QNN v5 camera is 3xIMX577 720p30fps preview +recording, 2xOV9282 720p30fps RDI dump) CPU drystone 80%+1GPU+1HTP +5camera	5.77+2.02 = 7.79	5.77	Baseplate Heatsink +
Case 8	5Camera(3xIMX577 720p30fps preview +recording, 2xOV9282 720p30fps RDI dump) 4ML QNN run on HTP 2QNN run on GPU CPU drystone 95% BT paired Audio playback Iperf3 100Mbps via wifi Iperf3 1Gbps via ethernet	78.56+2.31 = 10.87	8.56	Baseplate Heatsink +

## FAQs

### How to assign power in thermal model of chipset?

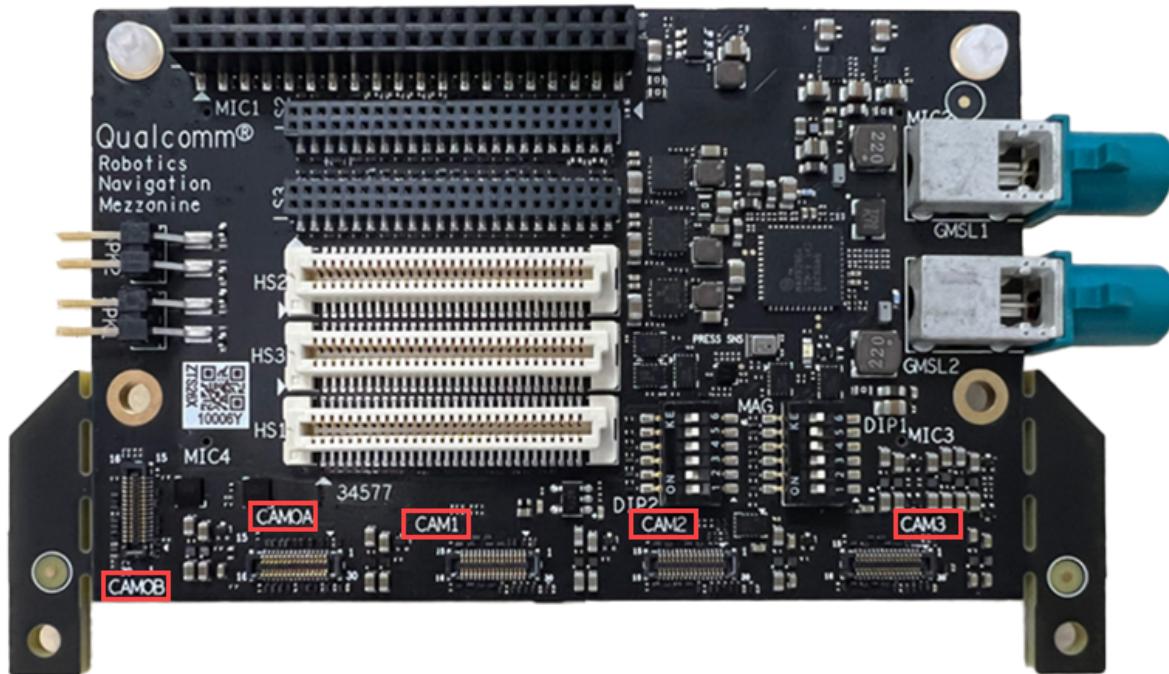
For all Qualcomm chipsets, thermal models are available in Icepak(.tzr) and FloTHERM(pdml) format. Assign the power to the heat source in the thermal model. The dimension of the heat source changes with thermal model.

### What are the use cases that need to be considered for QCS6490?

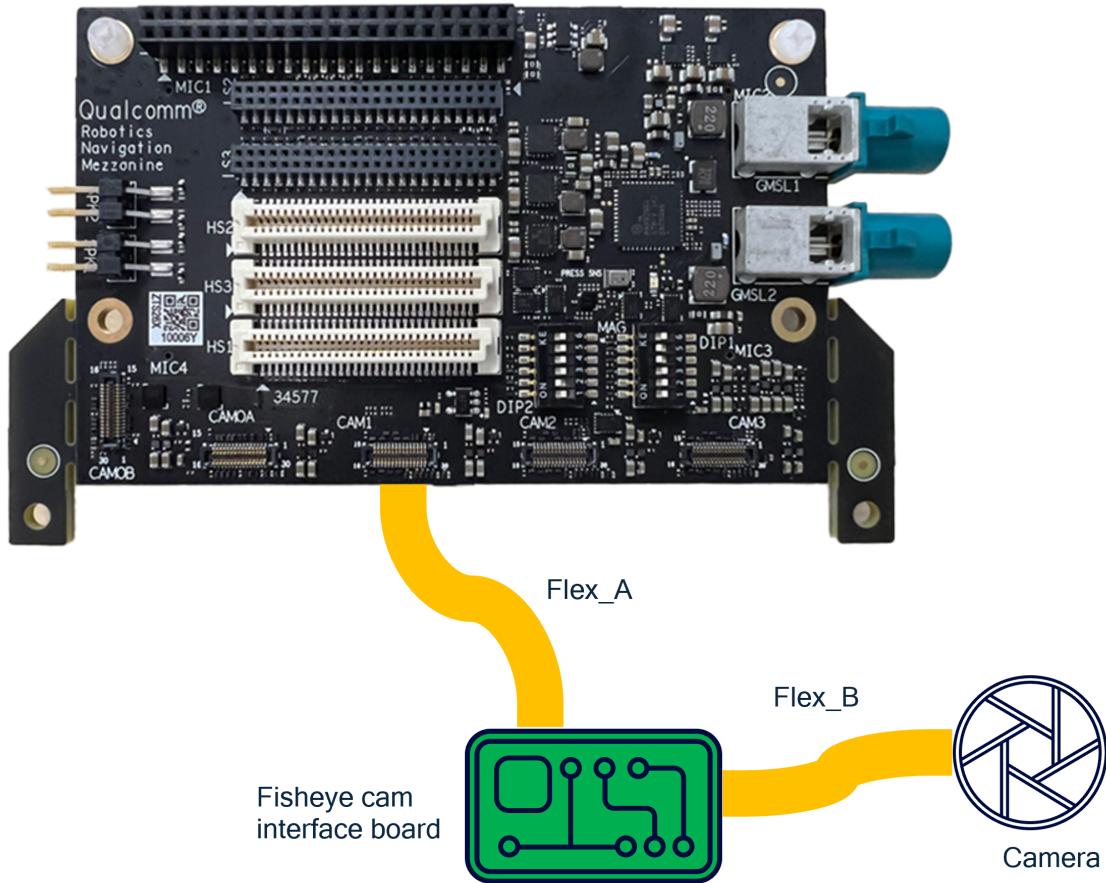
See the thermal power projection table in [QCM6490 and QCS6490, QCM5430 and QCS5430 Technical Reference Manual](#) for all the high-power use cases. CPU intensive (Drystone) is the worst-case scenario.

## 5.4 Connect a custom camera sensor

If your camera sensor's connector matches the RB3 Gen 2 board, you can use it directly. See [Design Package, RB5/RB5GEN2/RB3GEN2 Navigation Mezzanine](#) for connector details.



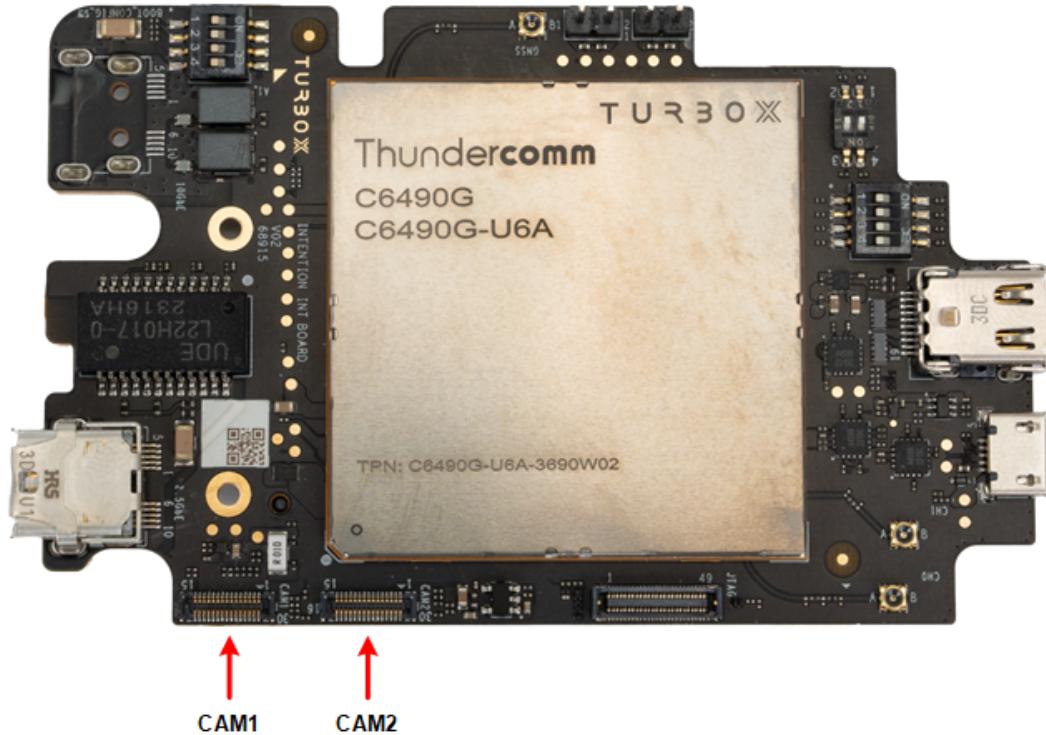
Otherwise, create an interface PCB to convert the pinout from the Vision mezzanine to match your camera sensor signals. The example below assumes a "fisheye camera" to be tested with RB3 Gen 2. Two different flex cables (Flex\_A and Flex\_B) would also be needed.



A custom-vision-mezzanine board can also be designed to host more than one camera connector.  
See [Design Package, RB5 Generic Mezz Card Schematic and Layout, IOT](#).

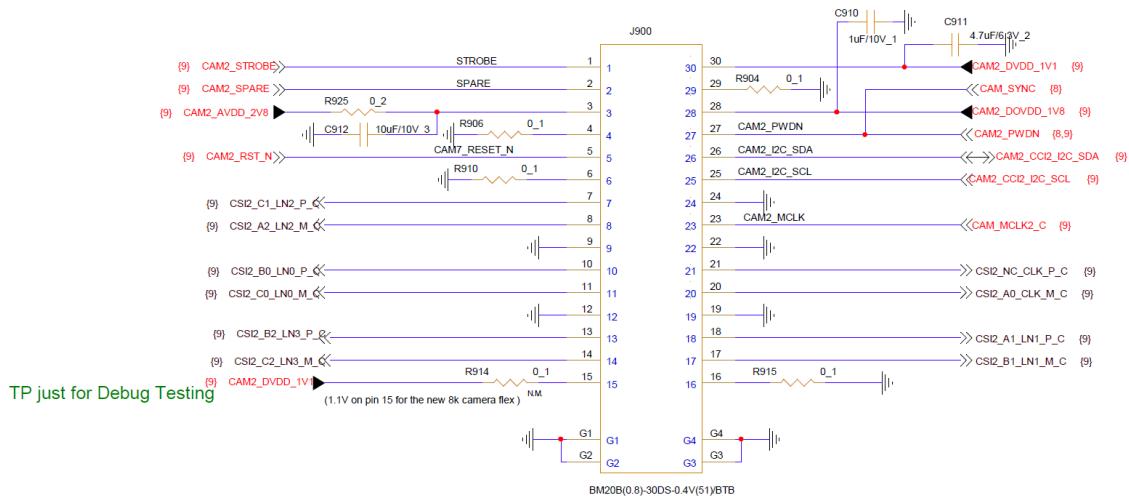
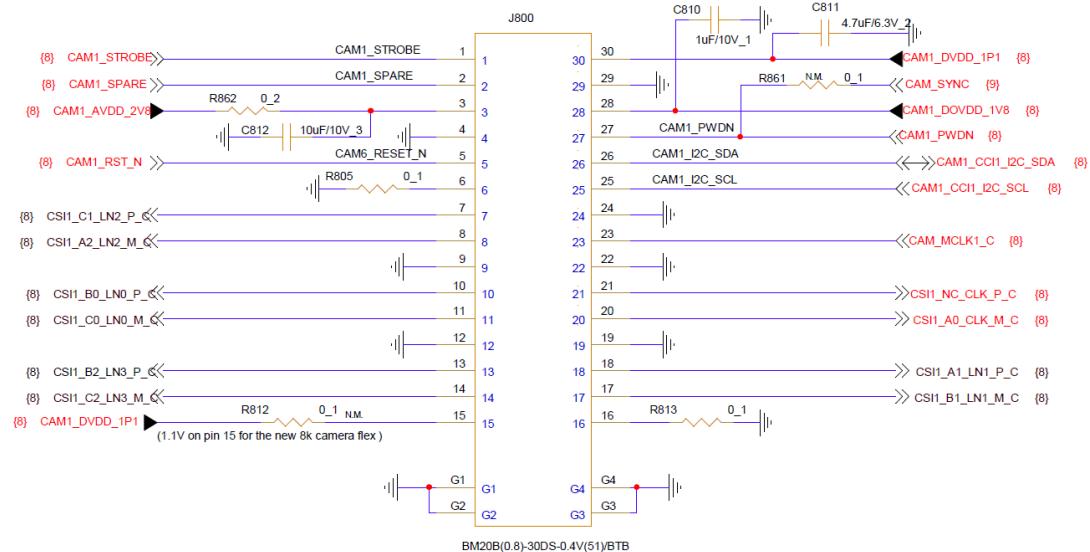
## Connectors on RB3 Gen 2

The CAM1 and CAM2 connectors on the interposer (*see below*) are C/D-PHY. The connectors on the [Vision Mezzanine](#) are D-PHY only.



**Interposer camera connectors**

The following images show details for the CAM1 and CAM2 connectors on the interposer.



## Vision Mezzanine pinouts

The following table lists the pinout locations on the Vision Mezzanine.

<b>RB5 4 Lane MIPI CSI Connectors</b>					
<b>Pin</b>	<b>CAM0A</b>	<b>CAM1</b>	<b>CAM2</b>	<b>CAM3</b>	<b>Notes</b>
1	Strobe (GPIO)	Strobe (GPIO)	Strobe (GPIO)	Strobe (GPIO)	strobe not typically used by most modules
2	Spare (GPIO)	Spare (GPIO)	Spare (GPIO), Optionally SPI_CLK	Spare (GPIO)	spare not typically used by most modules
3	2V8	2V8	2V8	2V8 or 5V	
4	GND	GND	Optionally SPI_MOSI	GND	
5	Reset (GPIO)	Reset (GPIO)	Reset (GPIO)	Reset (GPIO)	Key GPIO
6	GND	GND	GND, For CAM2, this pin can be remapped to a 32kHz SLEEP_CLK. GND is the default.	GND	
7	CSI_D2_P	CSI_D2_P	CSI_D2_P	CSI_D2_P	
8	CSI_D2_M	CSI_D2_M	CSI_D2_M	CSI_D2_M	
9	GND	GND	GND	GND	
10	CSI_D0_P	CSI_D0_P	CSI_D0_P	CSI_D0_P	
11	CSI_D0_M	CSI_D0_M	CSI_D0_M	CSI_D0_M	
12	GND	GND	GND	GND	
13	CSI_D3_P	CSI_D3_P	CSI_D3_P	CSI_D3_P	
14	CSI_D3_M	CSI_D3_M	CSI_D3_M	CSI_D3_M	

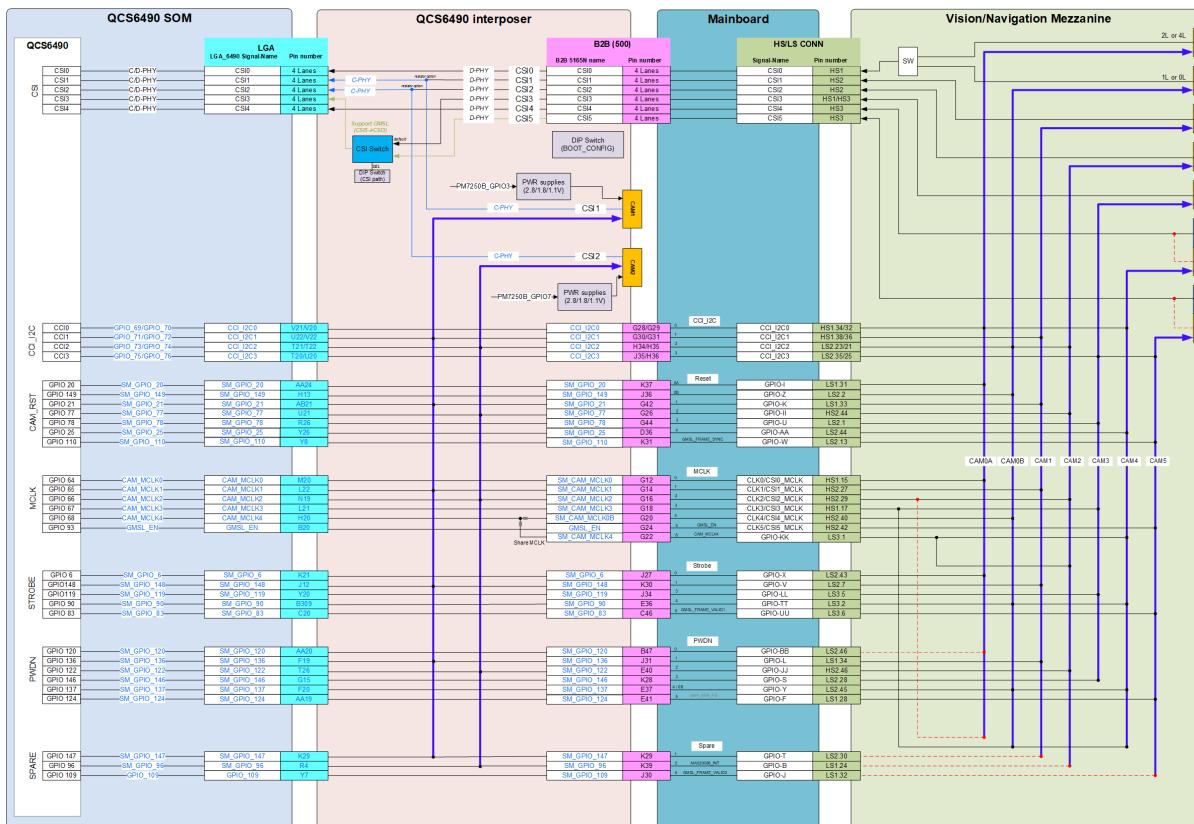
<b>RB5 4 Lane MIPI CSI Connectors</b>					
<b>Pin</b>	<b>CAM0A</b>	<b>CAM1</b>	<b>CAM2</b>	<b>CAM3</b>	<b>Notes</b>
15	CAM_PWR_SWITCH	CAM_PWR_SWITCH	CAM_PWR_SWITCH	CAM_PWR_SWITCH	Controls 1V1 or 1V2 selection on pin 30. Pull low to GND for 1.1V, pull high to 1V8 rail on the flex for 1V2.
16	0R to GND	0R to GND	0R to GND	CAM_PWR_SWITCH2	CAM3 Only: Pull low to GND for normal operation (1V1/1V2, 1V8, 2V8). Pull high to Pin 28 for 5V on all three power pins.
17	CSI_D1_M	CSI_D1_M	CSI_D1_M	CSI_D1_M	
18	CSI_D1_P	CSI_D1_P	CSI_D1_P	CSI_D1_P	
19	GND	GND	GND	GND	
20	CSI_C_M	CSI_C_M	CSI_C_M	CSI_C_M	
21	CSI_C_P	CSI_C_P	CSI_C_P	CSI_C_P	
22	GND	GND	GND	GND	
23	MCLK	MCLK	MCLK	MCLK	Key GPIO
24	GND	GND	GND	GND	
25	SCL	SCL	SCL	SCL	Key GPIO
26	SDA	SDA	SDA	SDA	Key GPIO
27	PWDN/Sync to CAM0B	PWDN	Optionally SPI_CS	PWDN	PWDN not typically used by most modules
28	1V8	1V8	1V8	1V8 or 5V	
29	GND	GND	Optionally SPI_MISO	GND	
30	1V1 or 1V2	1V1 or 1V2	1V1 or 1V2	1V2 or 5V	

## RB5 4 Lane MIPI CSI Connectors

Pin	CAM0A	CAM1	CAM2	CAM3	Notes
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**General Notes:**

Only Camera interfaces with 4 D-PHY lanes are shown. QC software only uses RST and MCLK. The other GPIO pins can be used for other purposes as they are not nominally routed to anything in the software. CAM0A and CAM0B can be synchronized via pin 27. Optional SPI bus on CAM2 is connected to the apps processor block, not the DSP block.



RB3 Gen 2

## 5.5 Reference designs and related documents

List of reference designs, schematics, and related documents.

- RB3 Gen 2 Quick Start Guide
- Design Package, RB3 Gen 2 SOM and Interposer

- Design Package, RB3G2 Vision Kit, Mechanical 3D Model, IOT
- Design Package, RB5 Generic Mezz Card Schematic and Layout, IOT
- Design Package, RB5/RB5GEN2/RB3GEN2 Main Board
- Design Package, RB5/RB5GEN2/RB3GEN2 Navigation Mezzanine
- Design Package, RB3GEN2 Industrial Mezzanine

## 5.6 Acronyms and terms

List of acronyms and terms used in this document.

Term	Description
DMIC	Digital microphone interface
EDL/QDL	Emergency download mode or Qualcomm download mode
GMSL	Gigabit multimedia serial links
GNSS	Global navigation satellite system
GPIO	General-purpose input/output
QUP	Qualcomm universal peripheral
SoC	System-on-chip
SoM	System-on-module
UART	Universal asynchronous receiver/transmitter

# 6 Development regulatory notice

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