Pattern Detection

The purpose of this project was to understand the different types of FSMs and the effect on synthesis and simulation results.

A) Two always block style with combinational outputs

Files - PatternDetector1.sv, PatternDetector1_tb.sv, input_data.txt

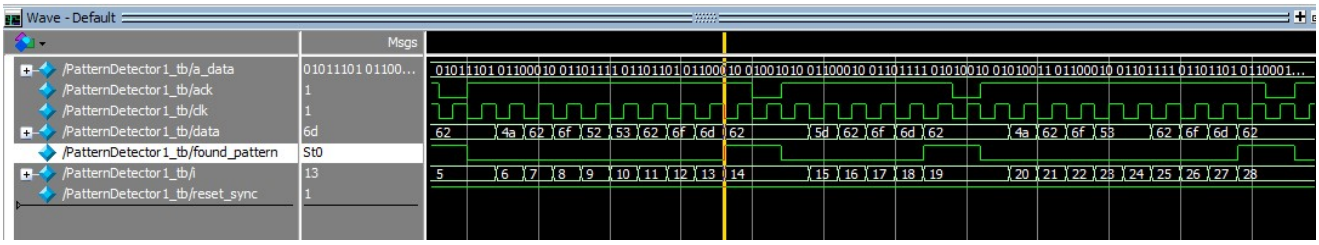

Figure 1: Simulation Result

As can be observed from the Figure 1, the output found_pattern goes high in the same cycle as the last matching input

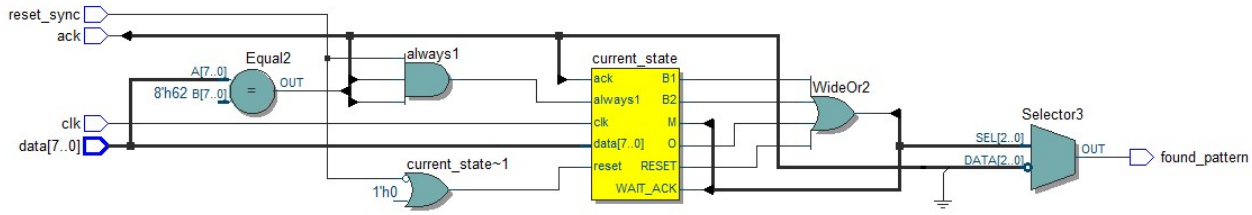

Figure 2: Synthesis Result

As can be observed the synthesis result, the output is not registered, confirming the understanding from the simulation results.

B) One sequential always block style with registered outputs

Files - PatternDetector2.sv, PatternDetector2_tb.sv, input_data2.txt

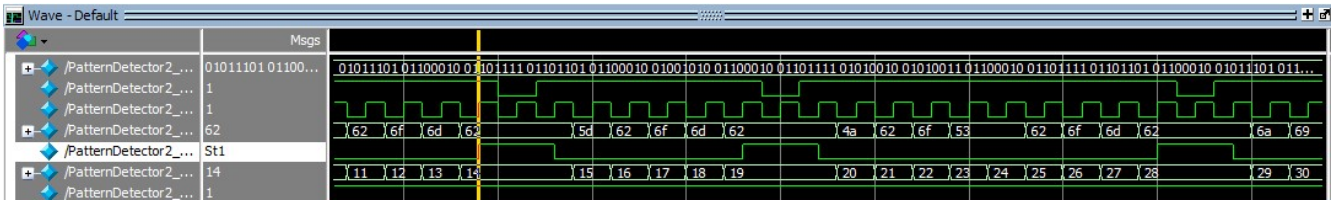

Figure 3: Simulation Result

As can be observed from the simulation waveform, the output found_pattern goes high in the next clock edge after the last matching input arrives.

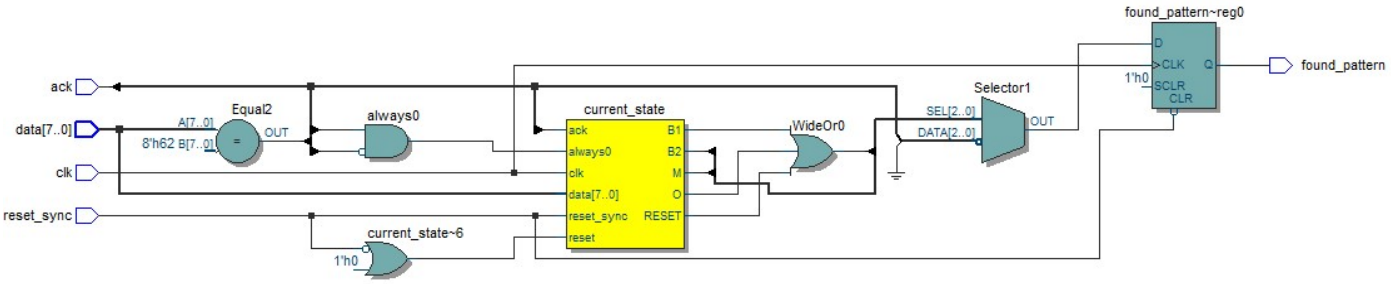

Figure 4: Synthesis Result

As can be observed from the synthesis result, the output found_pattern is registered, as per the FSM coding style.

C) Three always block style with registered outputs

Files - PatternDetector3.sv, PatternDetector3_tb.sv, input_data3.txt

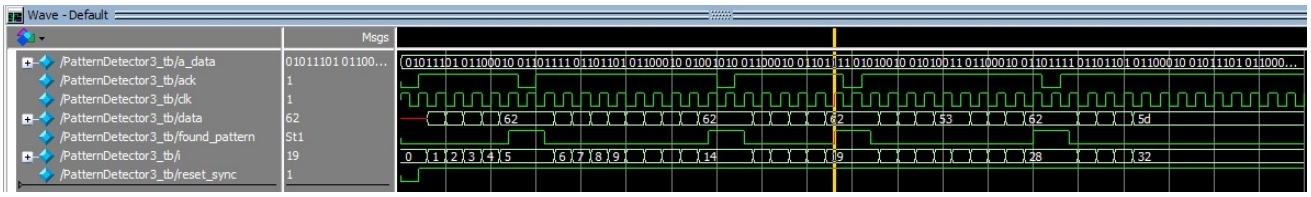

Figure 5: Simulation Result

As can be observed from the simulation waveform, the output found_pattern goes high in the next clock edge after the last matching input arrives as expected from the coding style used.

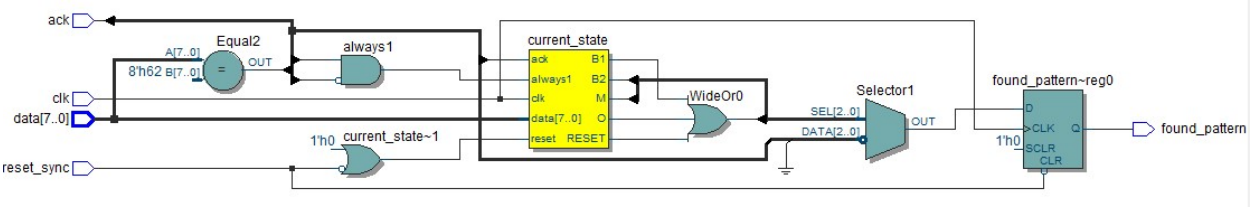

Figure 6: Synthesis Result

As can be observed from the synthesis result, the output found_pattern is registered, as per the FSM coding style. The results from (B) and (C) are same for simulation as well as synthesis.

D) Two always block style with combinational outputs, but output matched with the registered output style FSM

Files - PatternDetector4.sv, PatternDetector4_tb.sv, input_data4.txt

Figure 7: Simulation Result

As can be observed from the simulation waveform, the output found_pattern goes high in the next clock edge after the last matching input arrives. This is done to match the registered output simulation results, using the combinational output FSM style.

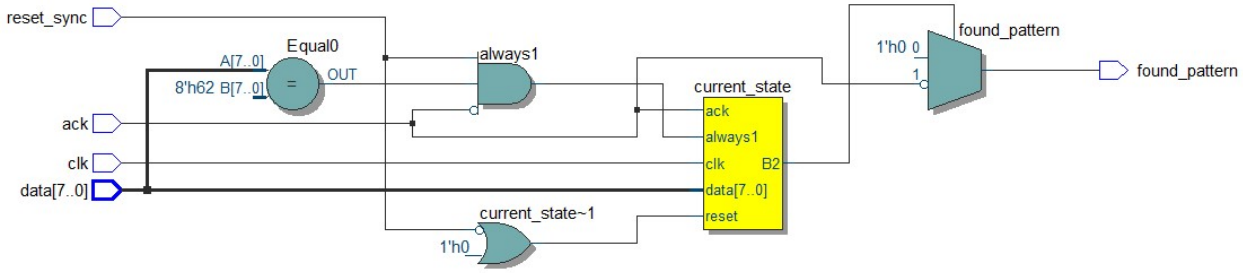

Figure 8: Synthesis Result

As can be observed from the synthesis result, the output found_pattern is not registered, as per the FSM coding style.