# Aniket Das

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## RESEARCH INTERESTS

Computer architecture; memory & storage systems; processing-in-memory; non-volatile memory reliability; emerging memory technologies

## EDUCATION

**University of Illinois Urbana-Champaign**                    **August 2025 – Present**
*Ph.D. in Computer Science*
*Advisor: Saugata Ghose*

**University of Illinois Urbana-Champaign**                    **August 2021 – May 2025**
*B.S. in Computer Science and Philosophy, Highest Distinction*
*Minor in Linguistics*
- *Senior Thesis:* **A Reliable In-Storage Search Primitive for Large-Scale Data Processing**
- *GPA:* 3.94 / 4.00, Dean's List for five semesters
- *Relevant Coursework:*
  **CS 598:** Storage Systems; **CS 534:** Architectures for Mobile and Edge Computing; **CS 533:** Parallel Computer Architecture; **CS 437:** Wireless IoT Systems; **CS 433:** Computer System Organization; **CS 426:** Compiler Construction; **ECE 408:** Applied Parallel Programming; **ECE 385:** Digital Systems Laboratory

## PROFESSIONAL EXPERIENCE

**ARCANA Research Group**                    **August 2024 – May 2025**
*Undergraduate Researcher*                    *Urbana, IL*
*Advisor: Saugata Ghose*
- Investigated in-storage processing-using-memory (PUM) with solid-state drive (SSD) technology
- Developed a Python NAND flash model to explore conventional I/O and digital PUM operation reliability
- Demonstrated increase of PUM search accuracy from 0.08% to 100% with proposed reliability enhancement

**University of Illinois, Department of Computer Science**                    **January 2024 – May 2025**
*Course Assistant*                    *Urbana, IL*
*CS 433: Computer System Organization*
- Taught advanced computer architecture concepts in a team of four to five course staff members
- Collaboratively developed and graded six homework assignments and two exams per semester
- Enhanced student comprehension during biweekly in-person office hours, averaging six attendees

**KeeperAI *(keeperai.com)***                    **May 2024 – August 2024**
*Machine Learning Intern*                    *New York, NY*
- Enhanced codebase to build a profile recommendation feature with Python scikit-learn and pandas libraries
- Integrated Google Firestore Database API to perform NoSQL queries on real-time user data

**CirrusLabs**                    **May 2022 – August 2022**
*DevOps Intern*                    *Alpharetta, GA*
- Worked as a member of a six-person team on a FinOps project focused on reducing cloud spend
- Built market research-based software in Python to normalize cloud data and optimize VM costs

## PUBLICATIONS

R. Wong, N. Kim, **A. Das**, K. M. Higgs, E. Ipek, S. Agarwal, S. Ghose, and B. Feinberg. **"ANVIL: An In-Storage Accelerator for Name–Value Data Stores"**, 52nd International Symposium on Computer Architecture **(ISCA)**, June 2025

## PRESENTATIONS

*Poster:* **A Reliable In-Storage Search Primitive for Large-Scale Data Processing**          **April 2025**
*Undergraduate Research Symposium, University of Illinois Urbana-Champaign*          *Urbana, IL*

## AWARDS

**Andrew and Shana Laursen Fellowship**          **August 2025 – May 2026**
*University of Illinois Urbana-Champaign*

**Graduate College Block Grant Fellowship**          **August 2025 – May 2026**
*University of Illinois Urbana-Champaign*

## PROJECTS

**CS 598 Term Project**          **September 2025 – December 2025**
*Accelerating Latency-Critical OLTP Databases with Tail-Aware SMT*
- Created a system for parallelized database transactions with multicore CPUs in a three-member team
- Designed hardware scheduling policies based on application behavior with the SniperSim simulator in C++
- Evaluated hardware-software co-design through profiling and simulation with YCSB and TPC benchmarks

**CS 533 Term Project**          **February 2025 – May 2025**
*Applying Perceptron-Based Prefetch Filtering to a Variety of Hardware Prefetchers*
- Extended hardware prefetcher designs in C++ in a four-member team using the ChampSim simulator
- Implemented a machine learning architecture in the Bingo spatial data prefetcher
- Explored design space through evaluation on traces from the SPEC CPU 2017 benchmark suite

**CS 534 Term Project**          **February 2024 – May 2024**
*Variable Block Size Cache: Optimizing Cache Utilization Through Prediction Mechanisms*
- Designed a cache with dynamic data sizing using perceptron prediction in a four-member team
- Implemented the hardware design for decision mechanisms in C++ using the gem5 simulator
- Adapted design to improve compatibility using full-system simulation with SPEC CPU 2017 programs

**ECE 385 Project**          **February 2024 – March 2024**
*Simple Computer SLC-3.2*
- Utilized SystemVerilog to create a 16-bit microprocessor implementing a subset of the LC-3 ISA
- Developed an instruction decoder to generate control signals for accurate program execution
- Configured Block Memory IP Core in Vivado to integrate on-chip memory and memory-mapped I/O

## SKILLS

- **Coding**: Python; C++; C; Bash; SystemVerilog; CUDA; MIPS Assembly; Java
- **Tools**: SniperSim; ChampSim; gem5; Ramulator; McPAT; Vivado Design Suite; Git; GDB; Linux