Department of Electrical Engineering
EE614 – Solid State Devices I

Course Project Statement

- All parts are compulsory.
- The submission must be in the form of a detailed ***IEEE-style paper*** highlighting the observations and contributions of each member of the team.
- There needs to be only **ONE** report per team. Teams in Group A will do the project for an n-channel device and in Group B will do it for a p-channel device.
- Project viva 10 – 15 minutes will be done before the end sem (Tentative Date: 14/11/2024)
- Tools Needed: ATLAS Silvaco, Cadence Spectre

Deadline of Submission: **10/11/2024** at **11:59 pm**.

Part 1: Device Design and Simulation in TCAD.
Simulate an FDSOI MOSFET in the TCAD environment for a gate length (L_G) of 50 nm, silicon layer thickness (T_{Si}) of 10 nm, and a 3 nm thick gate oxide (T_{OX}) for a nominal supply voltage (V_{DD}) = 1 V. Use SiO_2 for the gate oxide material.

After simulating the device in TCAD, implement the following variations and observe the effects on device characteristics:

1. Variation in L_G: Simulate the device for L_G = 20 nm to 70 nm in steps of 10 nm.
2. Variation in V_{DD}: Simulate the device for V_{DD} = 0.65 V, 0.7 V, 0.8 V, 1.0 V, 1.2 V and 1.35 V.
3. Variation in T_{Si}: 7 nm, 10 nm, 15 nm.

Simulate the device's current characteristics and capacitances (esp. C_{GS} and C_{GD}) for all the above-mentioned variations. Using the constant current method, extract the threshold voltage (V_{TH}) for all the variations along with the device ON-state current (I_{ON}), OFF-state current (I_{OFF}), and the subthreshold swing (SS). Clearly state all your observations along with the physical reasoning behind the trends.

Part 2: Verilog-A LUT Device Model Implementation.
Use the following device parameters to develop the Look-Up Table (LUT) based Verilog-A device model: L_G = 50 nm, T_{Si} = 10 nm, T_{OX} = 3 nm, V_{DD} = 1 V.

Verify the device characteristics obtained from the VA model, against the results obtained from the TCAD simulations. Report the percentage error in the results from the VA model compared to TACD.

Part 3: Circuit Implementations and Simulations.
Using the LUT Verilog-A model developed in Part 2, simulate the DC and transient characteristics for an Inverter and calculate the various power and performance metrics.