Simulation-Based Analysis of DC and AC Characteristics in FDSOI MOSFETs

***Abstract*—This paper aims to design and simulate an FDSOI MOSFET in the TCAD environment. The effects on device characteristics are observed by varying design parameters like gate length, silicon layer thickness and supply voltage. The simulations of device's current characteristics and capacitances are also checked. All the observations from the TCAD model are cross verified with the Look-Up Table (LUT) based Verilog-A device model which is also developed parallelly. The DC and transient characteristics for an Inverter is also simulated using the LUT based Verilog-A device model.**

***Index Terms*—FDSOI MOSFET, TCAD, simulations,Verilog-A device model**

I. Introduction

A. SOI MOSFETs

Silicon-on-Insulator (SOI) MOSFETs are widely used in microelectronics for their enhanced performance over bulk MOSFETs. Built on a thin silicon layer over an insulating oxide layer, SOI MOSFETs reduce parasitic capacitance, boost speed, and lower power consumption. [1]

B. Types of SOI MOSFETs

- **Partially Depleted SOI (PDSOI)**: Only part of the silicon layer depletes during operation, providing stability suited for high-radiation environments like aerospace.
- **Fully Depleted SOI (FDSOI)**: The thin silicon layer depletes entirely, offering strong control over the channel, reduced leakage, and lower power consumption—ideal for consumer electronics. [2]

C. FDSOI MOSFET

FDSOI MOSFETs feature a thin silicon layer on an ultra-thin buried oxide (BOX) layer, enabling excellent channel control and reducing short-channel effects. The structure is designed to improve electrostatic control and minimize short-channel effects. The key elements of an FDSOI MOSFET structure include:

- **Thin Silicon Channel**: A very thin silicon layer (typically a few nanometers) forms the channel, which allows for complete depletion of carriers during operation, leading to improved channel control and reduced leakage currents.
- **Ultra-Thin Buried Oxide (BOX) Layer**: Below the silicon channel is a thin insulating layer of silicon dioxide (typically around 10-25 nm thick). This BOX layer isolates the channel from the bulk substrate, reducing parasitic capacitances and further improving electrostatic control.
- **Back Gate (or Substrate)**: The bulk silicon substrate beneath the BOX layer acts as a "back gate." By applying a voltage to this substrate, the threshold voltage of the device can be dynamically adjusted, a feature known as "back biasing." This allows FDSOI MOSFETs to switch between high-performance and low-power modes, making them ideal for energy-efficient applications.

This structure gives FDSOI MOSFETs their distinct advantages: lower power consumption, reduced short-channel effects, and flexible performance tuning. [3]

II. Device Design and Simulation in TCAD

The study explores the effects of variations in gate length (L_G), supply voltage (V_{DD}), and silicon thickness (T_{Si}) on the device's current characteristics, capacitances (C_{GS} and C_{GD}), threshold voltage (V_{TH}), ON-state current (I_{ON}), OFF-state current (I_{OFF}), and subthreshold swing (SS).

The FDSOI MOSFET was simulated under various conditions to analyze the effects of different parameters on device characteristics. The following variations were studied:

- **Variation in Gate Length (L_G)**: Simulations were performed with L_G values ranging from 20 nm to 70 nm in increments of 10.
- **Variation in Supply Voltage (V_{DD})**: V_{DD} was varied with values of 0.65 V, 0.7 V, 0.8 V, 1.0 V, 1.2 V, and 1.35 V.
- **Variation in Silicon Thickness (T_{Si})**: Simulations were conducted with T_{Si} values of 7 nm, 10 nm, and 15 nm.

For each variation, the device's current characteristics and capacitances (C_{GS} and C_{GD}) were observed, and the threshold voltage (V_{TH}) was extracted using the constant current method. The ON-state current (I_{ON}), OFF-state current (I_{OFF}), and subthreshold swing (SS) were also analyzed. The results and observations are detailed below.

A. Effect of L_G Variation

The device was simulated for different gate lengths (L_G) from 20 nm to 70 nm in steps of 10. This variation affects current characteristics, capacitances (C_{GS} and C_{GD}), and threshold voltage (V_{TH}). The AC characteristics, including capacitance-voltage (C-V) measurements and frequency response, along with the DC characteristics, are plotted for different gate lengths. Analyzing capacitances, particularly the gate-to-source (C_{GS}) and gate-to-drain (C_{GD}) capacitances, is essential for understanding the device's speed and signal integrity.

From the plots, the following characteristics are derived :

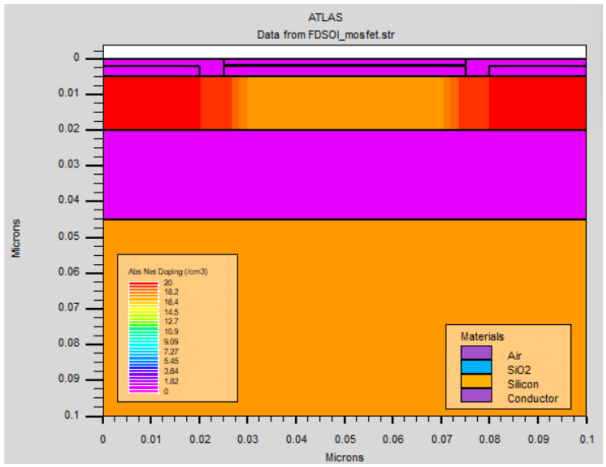

Fig. 1. Absolute Doping Concentration map of FDSOI in TCAD

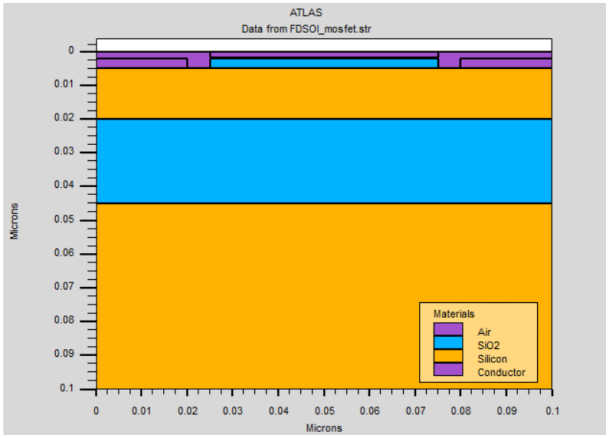

Fig. 2. Cross-sectional view of FDSOI in TCAD

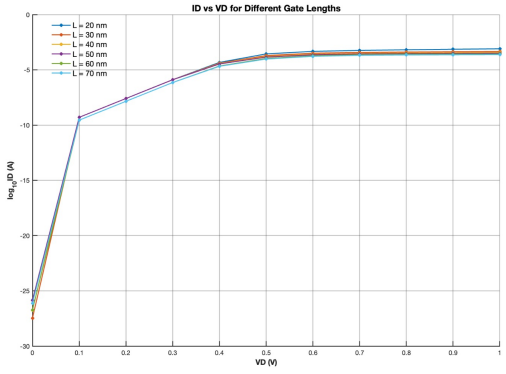

Fig. 3. **DC Characteristics** : I_D vs V_D

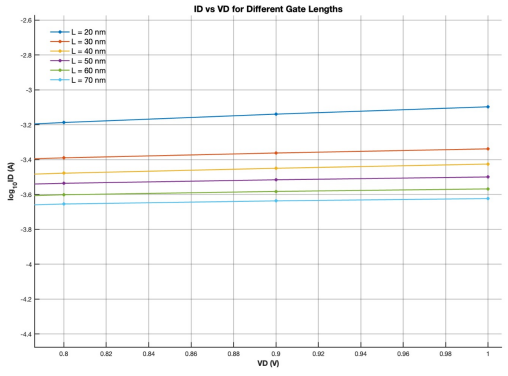

Fig. 4. **DC Characteristics** : I_D vs V_D zoomed

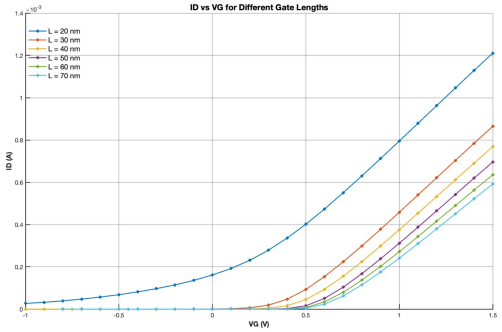

Fig. 5. **DC Characteristics** : I_D vs V_G

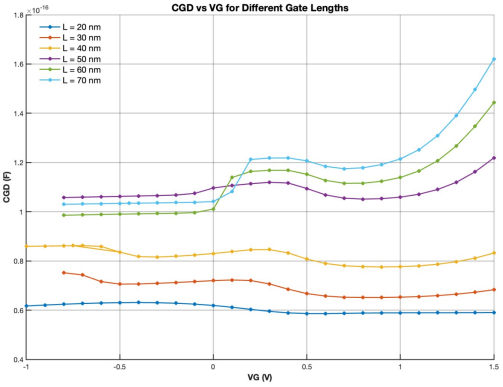

Fig. 6. **AC Characteristics** : C_{GD} vs V_G

TABLE I

Variation with L_G				
L_G	V_{th}	I_{ON}**(per um)**	I_{OFF}**(per um)**	SS
20 nm	$\leq -1V$	0.68 mA	65.99 uA	431.95 mV/dec
30 nm	-0.124 V	0.4 mA	0.4796 uA	168.22 mV/dec
40 nm	0.1088 V	0.38 mA	14.37 nA	122.93 mV/dec
50 nm	0.248 V	0.319 mA	0.31227 nA	98.5 mV/dec
60 nm	0.323 V	0.2 mA	16.67 pA	83.46 mV/dec
70 nm	0.357 V	0.2 mA	2.56 pA	76.45 mV/dec

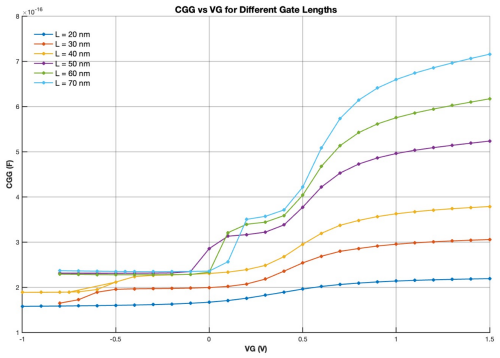

Fig. 7. **AC Characteristics** : C_{GG} vs V_G

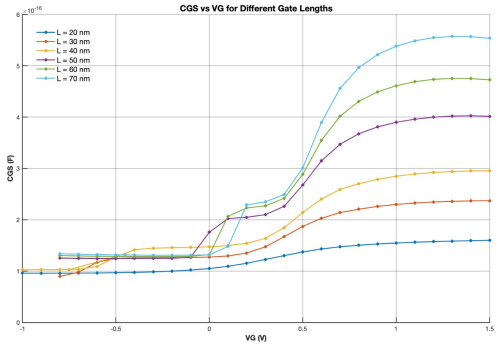

Fig. 8. **AC Characteristics** : C_{GS} vs V_G

Observations and Analysis:

The variations in V_{TH},I_{ON},I_{OFF},SS are given in Table I.

- I_D vs V_D: When L_G is increased, I_D decreases its value for a fixed V_D.Current is inversely proportional to Gate length.
- I_D vs V_G: When L_G is increased, I_D decreased its value for a fixed V_G.Current is inversely proportional to Gate length.
- C_{GS} vs V_G, C_{GD} vs V_G, C_{GG} vs V_G: All the three capacitances values increased when L_G is increased for a fixed V_G. Increase in capacitance is due to increase in area when gate length is increased.
- A good I_{ON}/I_{OFF} ratio for MOSFET is about the order of more than 10^3 . We can observe that as L_g increases, I_{ON}/I_{OFF} increases drastically which implies a better switching characteristics in FDSOI MOSFETs. We can note that at gate length of 20 nm, the I_{ON}/I_{OFF} ratio is around 10 which is very poor in digital circuits application.
- Subthreshold swing is a measure of how effectively the gate voltage can control the channel in a MOSFET when it is in the subthreshold (weak inversion) region, where the device conducts only leakage current. As gate length increases, subthreshold swing decreases due to better gate control.
- Due to greater subthreshold swing as gate length decreases, which implies shift in threshold voltage towards left. This is due to the fact now more negative gate voltage is required for getting the same current.

B. Effect of V_{DD} Variation

The device was simulated for different V_{DD} values (0.65 V, 0.7 V, 0.8 V, 1.0 V, 1.2 V, 1.35 V) to study their influence on device characteristics.

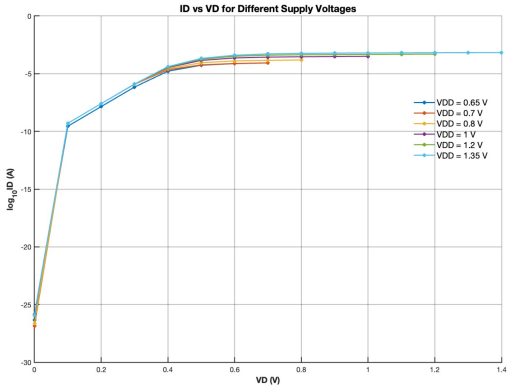

Fig. 9. **DC Characteristics** : I_D vs V_D

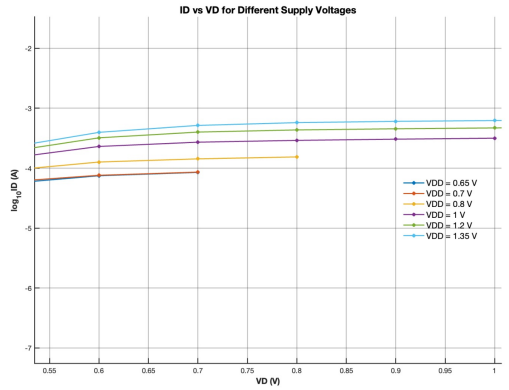

Fig. 10. **DC Characteristics** : I_D vs V_D zoomed

TABLE II

Variation with V_{DD}				
V_{DD}	V_{th}	I_{ON}**(per um)**	I_{OFF}**(per um)**	SS
0.65 V	0.287 V	60.15 uA	0.109 nA	96.08 mV/dec
0.7 V	0.282 V	87.27 uA	0.128 nA	96.3 mV/dec
0.8 V	0.27 V	0.156 mA	0.174 nA	97 mV/dec
1 V	0.248 V	0.319 mA	0.31227 nA	98.5 mV/dec
1.2 V	0.228 V	0.49 mA	0.5409 nA	100.31 mV/dec
1.35 V	0.213 V	0.6 mA	0.8027 nA	101.53 mV/dec

From the plots, the following characteristics are derived :

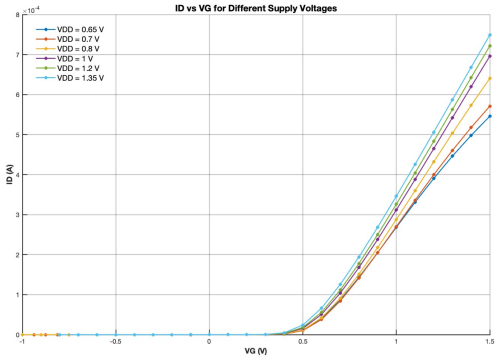

Fig. 11. **DC Characteristics** : I_D vs V_G

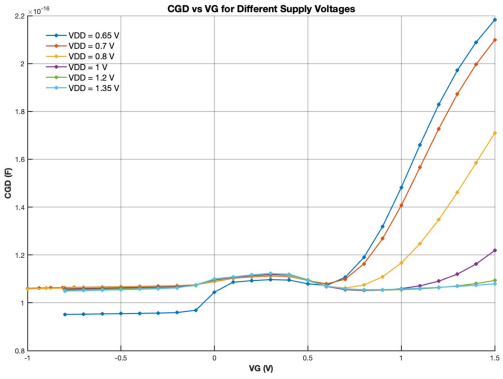

Fig. 12. **AC Characteristics** : C_{GD} vs V_G

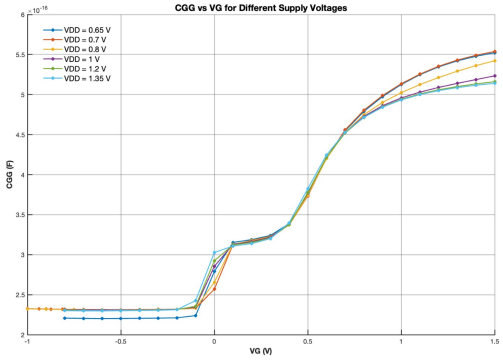

Fig. 13. **AC Characteristics** : C_{GG} vs V_G

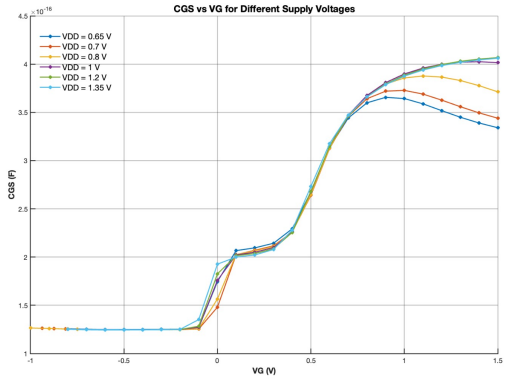

Fig. 14. **AC Characteristics** : C_{GS} vs V_G

Observations and Analysis:

Table II shows the variations of V_{TH},I_{ON},I_{OFF},SS when V_{DD} is changed.

- I_D vs V_D: For this simulation, V_G has been set to V_{DD} and V_D is varied. I_D increases its value for a fixed V_D as a higher gate voltage V_{DD} leads to higher current.
- I_D vs V_G: For this simulation V_D has been set as V_{DD} and gate voltage is varied. I_D depends weakly on V_D in saturation region and strongly depends on V_D in linear region. As V_{DD}(drain voltage) is increased, I_D increases with V_{DD} for a fix V_G. The difference is more prominent for higher V_G where transistor is in linear region.
- I_{OFF} with V_{DD} : The change in off current is very negligible as I_{OFF} is proportional to $\left(1 - e^{-\frac{V_{DD}}{\phi_t}}\right)$ in the subthreshold region.
- C_{GD} vs V_G ,C_{GG} vs V_G : We can observe from the plots that the variation in capacitances are almost negligible in accumulation and depletion region. The variation is prominent when in inversion region. As V_{DD} increases, the level of inversion in channel decreases which leads to decrease in capacitances.

C. Effect of T_{Si} Variation

The device was simulated for silicon thicknesses of T_{Si} = 7 nm, 10 nm, and 15 nm to analyze their impact on current characteristics and capacitances.

TABLE III

Variation with T_{Si}				
T_{Si}	V_{th}	I_{ON}**(per um)**	I_{OFF}**(per um)**	SS
7 nm	0.25 V	0.336 mA	0.1424 nA	87.80 mV/dec
10 nm	0.248 V	0.319 mA	0.3127 nA	98.5 mV/dec
15 nm	0.245 V	0.299 mA	0.8169 nA	111.36 mV/dec

From the plots, the following characteristics are derived :

Observations and Analysis:

- I_D vs V_D: I_D decreases as value of silicon thickness increases.This dependence of drain current on T_{Si} is due

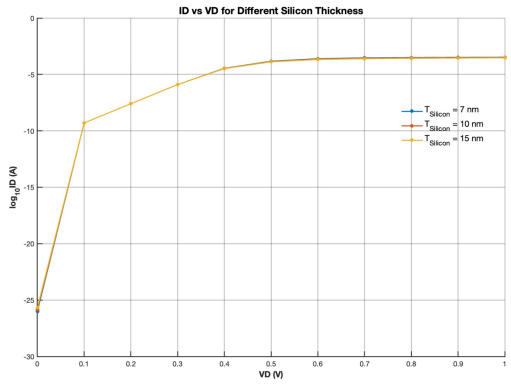

Fig. 15. **DC Characteristics** : I_D vs V_D

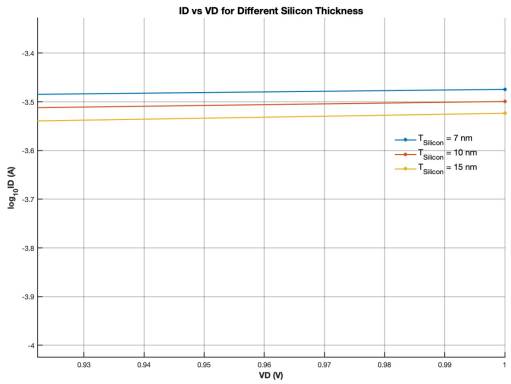

Fig. 16. **DC Characteristics** : I_D vs V_D zoomed

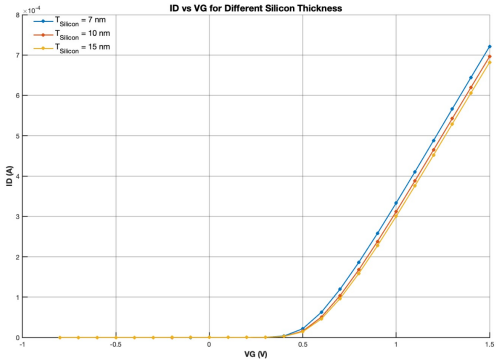

Fig. 17. **DC Characteristics** : I_D vs V_G

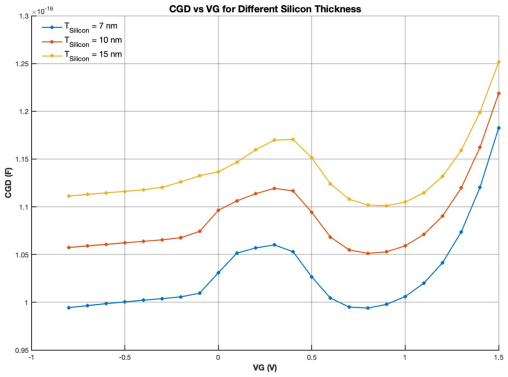

Fig. 18. **AC Characteristics** : C_{GD} vs V_G

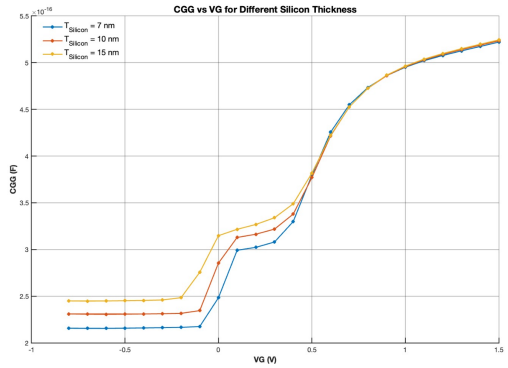

Fig. 19. **AC Characteristics** : C_{GG} vs V_G

to the decrease in qVg and also due to the decrease in induced charge carriers in the channel. [4]

- I_D vs V_G: I_D decreases as value of silicon thickness increases.
- C_{GS} vs V_G, C_{GD} vs V_G, C_{GG} vs V_G: Capacitance values increases as silicon thickness increases.
- I_{OFF} inreases due to Subthreshold swing increase, with proportional to increasing silicon thickness.

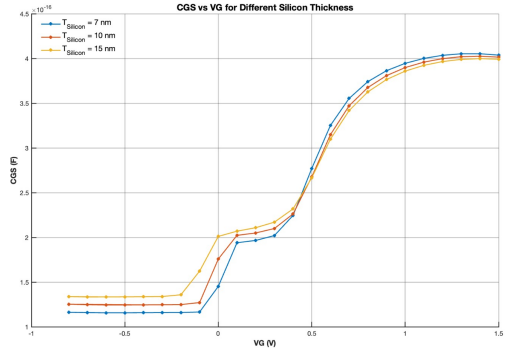

Fig. 20. **AC Characteristics** : C_{GS} vs V_G

III. Verilog-A LUT Device Model Implementation

Here, using the device parameters, L_G = 50 nm, T_{Si} = 10 nm, T_{OX} = 3 nm, V_{DD} = 1 V, a Look up Table based Verilog-A Model is developed.

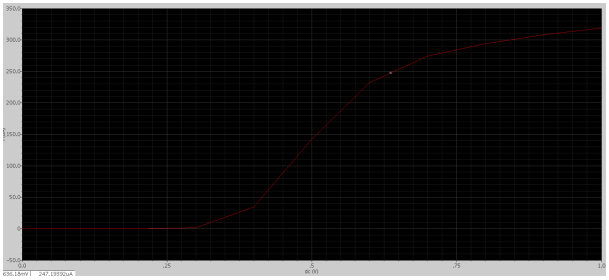

Fig. 21. **DC Characteristics** : I_D vs V_D

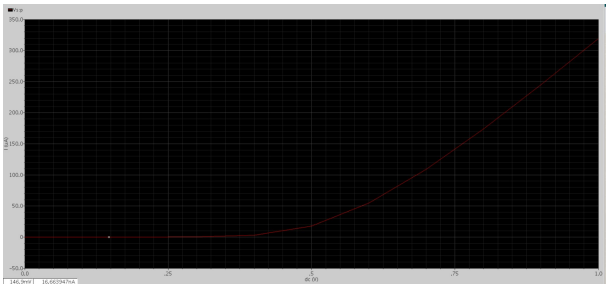

Fig. 22. **DC Characteristics** : I_D vs V_G

TABLE IV

Verilog-A Model			
V_{th}	I_{ON}**(per um)**	I_{OFF}**(per um)**	SS
222.7 mV	0.319 mA	0.313 nA	99.52 mV/dec

A. Verification of result with the TCAD simulation

From the TCAD simulation of the given device parameters, we compare the device characteristics:

1) V_{TH}*:* Percentage error compared to TCAD is 10.20 %

2) I_{ON}*:* Percentage error compared to TCAD is 0.03 %

3) I_{OFF}*:* Percentage error compared to TCAD is 0.09 %

4) SS: Percentage error compared to TCAD is 1.03 %

IV. Circuit Implementations and Simulations

The study utilizes the LUT Verilog-A model of the FDSOI MOSFET developed previously to implement a NMOS inverter consisting of the above FDSOI MOSFET, resistor(R_L), capacitor(C_L) and voltage sources(V_G and V_{DD}) for biasing.

The circuit is simulated and analysed for various characteristics in DC and transient conditions.

A. DC Analysis

- **Voltage Transfer Characteristics**
  The Voltage Transfer Characteristic (VTC) curve of an inverter is a critical aspect in understanding its behavior and performance. The VTC represents the relationship between the input voltage (V_{in}) and the output voltage (V_{out}) of the inverter. In an ideal inverter, the output transitions sharply from the high logic level (V_{DD}) to the low logic level (0 V) as the input voltage crosses the threshold. However, practical inverters exhibit a gradual transition due to device characteristics.

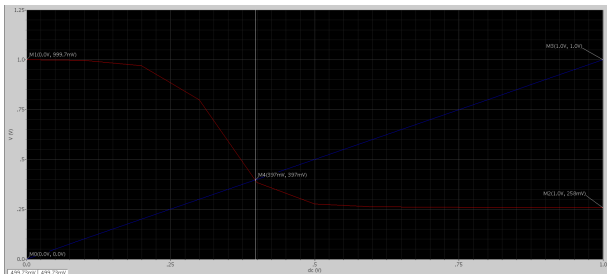

Fig. 23. **DC Characteristics** : VTC

- **Output High Voltage** (V_{OH}) The NMOS inverter was able to pull up V_{OH} to very close of V_{DD}. The value of V_{OH} was marked in Fig.23 and it was found to be 0.997mV.

$$V_{OH} = 997mV$$

- **Output Low Voltage** (V_{OL}) The NMOS inverter was not able to pull down V_{OL} successfully to 0. The value of V_{OL} is marked in Fig.23 and it is found to be 258mV.

$$V_{OH} = 258mV$$

B. Transient Analysis

In transient analysis, supply voltage (V_{DD}) was fixed at 1V, and a square waveform with a maximum value of 1V and a minimum value of 0V, with a time period of 20ns and a 0.5 duty cycle, was given as gate voltage (V_G). The various circuit performance metrics, namely speed, as measured by rise time, fall time, and transition delays, and power dissipation, given by static and dynamic power dissipation, were found at the above bias conditions. Variation of gate and drain voltage is given in Fig.24.

- **Low to High Transition Delay** (t_{plh})
  The low to high transition delay was calculated as the time interval between the moment the output reaches average of V_{OH} and V_{OL} from V_{OL} from the moment when the input reaches average of input high and input low from input high. In Fig.25, necessary points for calculating t_{plh} is marked and t_{plh} was calculated.

$$t_{plh} = 0.82ns$$

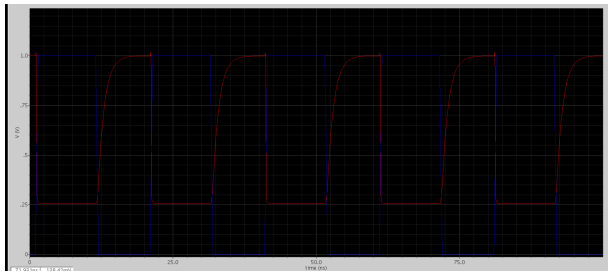

Fig. 24. **Transient Characteristics** : V_G and V_{DD} v/s Time

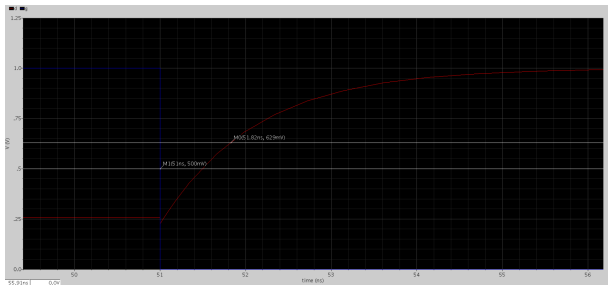

Fig. 25. **Transient Characteristics** : Low to High Transition Delay (t_{plh})

- **High to Low Transition Delay (t_{phl})**
  The high to low transition delay was calculated as the time interval between the moment the output reaches average of V_{OH} and V_{OL} from V_{OH} from the moment when the input reaches average of input high and input low from input low. In Fig.26, necessary points for calculating t_{phl} is marked and t_{phl} was calculated.

$$t_{phl} = 2ps$$

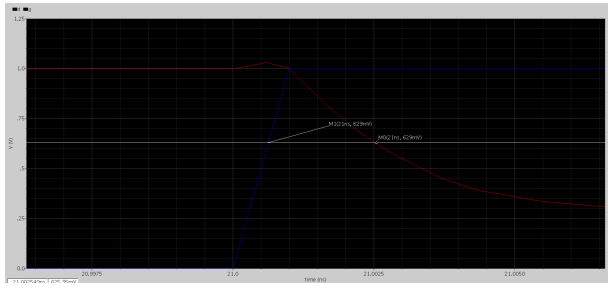

Fig. 26. **Transient Characteristics** : High to Low Transition Delay (t_{phl})

- **Fall time (t_f)**
  Fall time was defined here as the time it takes to reach from V_{OH} to the voltage obtained by adding 20% of difference between V_{OH} and V_{OL} to V_{OL}. It was obtained from the plot given in Fig. 27.

$$t_f = 0.05ns$$

- **Rise time (t_r)**
  Rise time was defined here as the time it takes to reach from V_{OL} to the voltage obtained by subtracting 20% of difference between V_{OH} and V_{OL} from V_{OH}. It was obtained from the plot given in Fig. 28.

$$t_r = 1.55ns$$

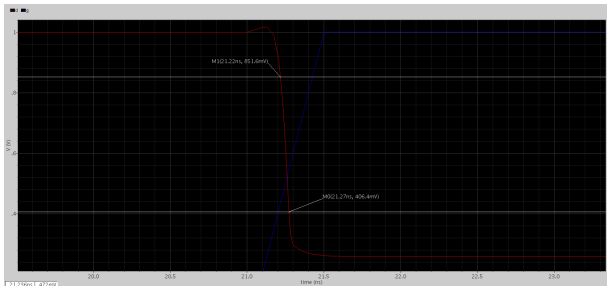

Fig. 27. **Transient Characteristics** : Fall time (t_f)

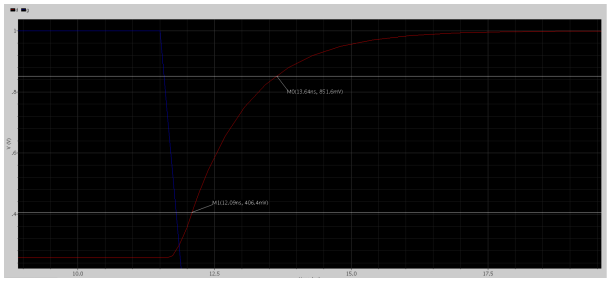

Fig. 28. **Transient Characteristics** : Rise time (t_r)

C. Power Performance Metrics

several important parameters that determine the power efficiency of the NMOS inverter. The key metrics that were considered are listed below.

- **Dynamic Power Consumption ($P_{dynamic}$)** // Dynamic power was due to the power consumed due to charging and discharging of capacitor loads due to gate voltage switching. It was found out from the formula given below.

$$P_{\text{dynamic}} = \alpha \cdot C_L \cdot V_{DD} \cdot (V_{DD} - V_{OL}) \cdot f$$

  where:
  - $\alpha = 1$ is the activity factor (frequency of switching between 0 and 1),
  - $C_L = 1fF$ is the load capacitance,
  - $V_{DD} = 1$ is the supply voltage,
  - $V_{OL} = 0.258$ is the output low voltage,
  - $f = 50MHz$ is the switching frequency.

$$P_{\text{dynamic}} = 37.1nW$$

- **Static Power Consumption (P_{static})**
  Static power was taken to be the power consumed due to flow of current over active elements of the circuits, namely NMOS and resistive load R_L. It was found by taking the product of supply voltage and average current through supply voltage in a period.

$$P_{\text{static}} = V_{DD} \cdot I_{DS_{avg}}$$

When transistor was on current through it was 792nA and the leakage current when transistor was off was negligible compared to this. Since 0.5 duty cycle is used average current was the mean of on current and off current. Since off current was negligible, average current was taken to be half of on current, 392nA. Therefore, P_{static} came out to be;

$$P_{\text{static}} = 392nA$$

- **Power-Delay Product (PDP)**
  Power-Delay Product was taken to be the product of dynamic power and average propagation delay. The average propagation delay was calculated to be the mean of t_{plh} and t_{phl}. Dynamic power was taken instead of static power in this product since it provided a balanced measure of the circuit's switching performance when it comes to delay and power. The equations of average delay and dynamic power was given below.

$$t_{\text{delay}} = \frac{t_{PLH} + t_{PHL}}{2}$$

$$\text{PDP} = P_{\text{dynamic}} \cdot t_{\text{delay}} = P_{\text{dynamic}} \cdot \frac{t_{PLH} + t_{PHL}}{2}$$

$$\text{PDP} = 37.1nW \cdot \frac{0.82ns + 0.002ns}{2} = 15.2481 \cdot 10^{-18} J$$

ACKNOWLEDGMENT

The authors would like to thank Prof. Avinash Lahgere, IIT Kanpur for his invaluable guidance and support throughout this project. We also express our gratitude to Exploratory Devices and Circuits Lab (EDCL), IIT Kanpur for providing access to the TCAD simulation software and computational resources essential for this work. Special thanks to Mr.Hafeez Raza, EDCL, IIT Kanpur for his insightful discussions and assistance.

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