Quiz Digital System Design (unit 3 and 4)

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Questions

How is a J-K flip-flop made to toggle? *

- ○ J = 0, K = 0
- ○ J = 1, K = 0
- ○ J = 0, K = 1
- ◉ J = 1, K = 1

Which statement BEST describes the operation of a negative-edge-triggered D flip-flop? *

- ◉ The logic level at the D input is transferred to Q on negative edge of CLK.
- ○ The Q output is ALWAYS identical to the CLK input if the D input is HIGH.
- ○ The Q output is ALWAYS identical to the D input when CLK is positive edge triggered.
- ○ The Q output is ALWAYS identical to the D input.

Master-slave J-K flip-flops are called pulse-triggered or level-triggered devices because input data is read during the entire time the clock pulse is at a LOW level. *

- ○ True
- ◉ False

A J-K flip-flop is in a "no change" condition when *

- ○ J = 1, K = 1
- ○ J = 1, K = 0
- ○ J = 0, K = 1
- ◉ J = 0, K = 0

Edge-triggered flip-flops must have: *

- ○ very fast response times.
- ○ at least two inputs to handle rising and falling edges.
- ◉ a pulse transition detector.
- ○ active-LOW inputs and complemented outputs.

As a general rule for stable flip-flop triggering, the clock pulse rise and fall times must be: *

- ○ very long.
- ○ very short.
- ○ at a maximum value to enable the input control signals to stabilize.
- ◉ of no consequence as long as the levels are within the determinate range of value.

The term CLEAR always means that Q = 0 *

- ◉ True
- ○ False

PRESET and CLEAR inputs are normally synchronous. *

- ○ True
- ◉ False

Assume a J-K flip-flop has logic 1s on the J and K inputs. The next clock pulse will cause the output to _____. *

- ○ Set
- ○ Reset
- ○ Latch
- ◉ Toggle

The asynchronous inputs are normally labeled _____ and _____, and are normally active-_____ inputs. *

- ◉ PRE, CLR, LOW
- ○ ON, OFF, HIGH
- ○ START, STOP, LOW
- ○ SET, RESET, HIGH

How many flip flops are required to build a binary counter circuit to count from 0 to 1023? *

- ○ 6
- ◉ 10
- ○ 24
- ○ 12

Counter is a *

- [ ] combinational circuit
- [x] sequential circuit.
- [ ] none

Master-slave flip flop consists of _____ flip-flop(s) *

- [ ] 1
- [ ] 4
- [x] 2
- [ ] 3

Which flip-flop plays a vital role by functioning as the basic building block of a ripple counter *

- [ ] S-R flip-flop
- [ ] J-K flip-flop
- [ ] D flip-flop
- [x] T flip-flop

In which type of counter, complement of the output is fed back to the D input of first state *

- [ ] Ring counter
- [x] Johnson counter
- [ ] Decade counter
- [ ] Binary counter

In which counter the output of Flip-flop do not change states at exactly the same time, as they do not have common clock pulse *

- ○ Ripple counter
- ◉ Synchronous counter
- ○ Twisted ring Counter
- ○ Shift register

How many flip-flops are required to construct a decade counter *

- ◉ 4
- ○ 8
- ○ 5
- ○ 10

How many different states does a 2-bit asynchronous counter have *

- ○ 1
- ◉ 4
- ○ 2
- ○ 8

Number of flip-flops required to make a MOD-32 binary counter *

- ○ 3
- ○ 4
- ◉ 5
- ○ 31

A 3-bit binary counter has a maximum modulus of *

- ○ 3
- ◉ 8
- ○ 7
- ○ 2

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