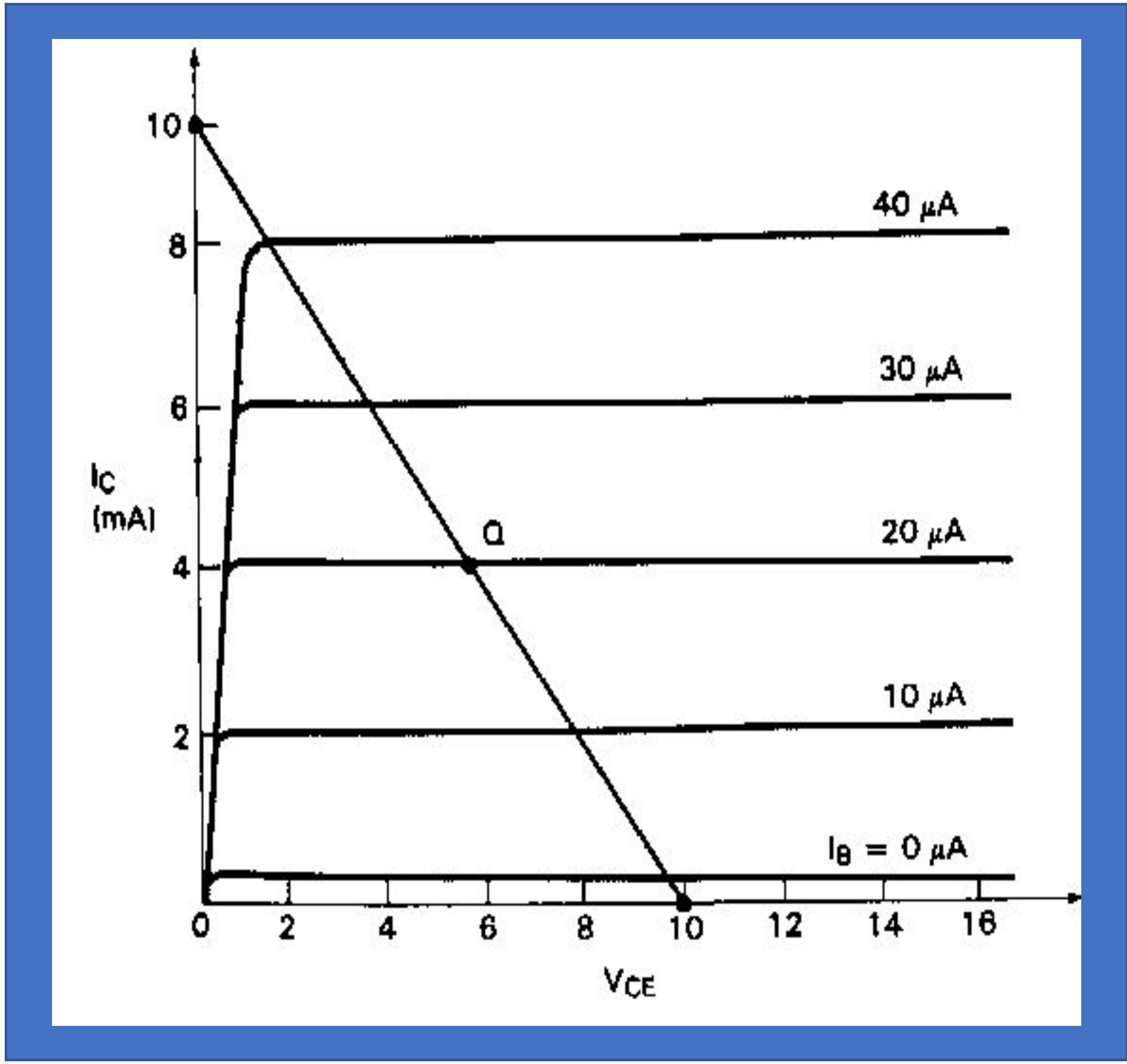
CHAPTER 3- SMALL SIGNAL ANALYSIS

Mrs Rasika B. Naik

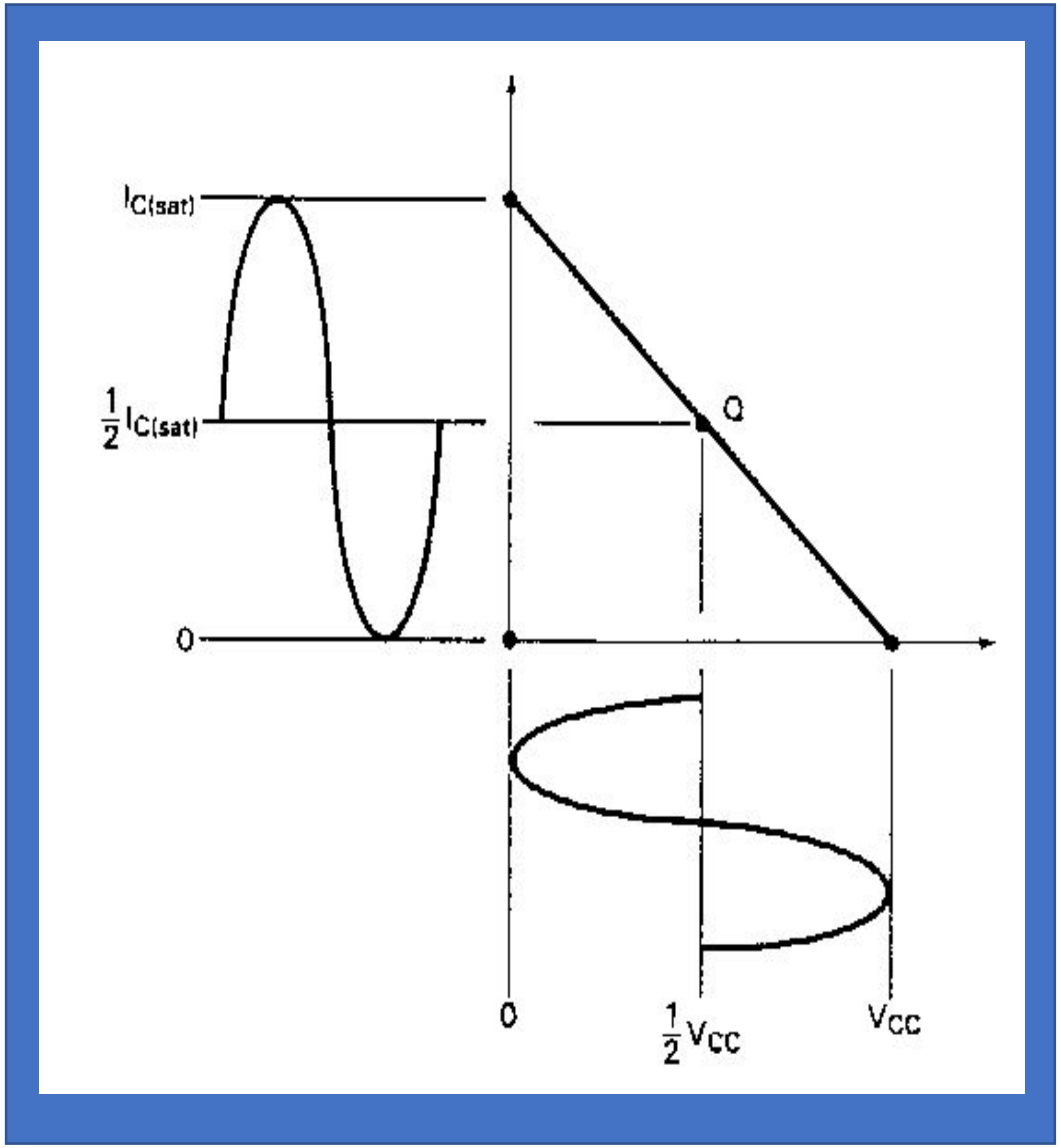
Q-POINT (DC LOAD LINE)

- The intersection of the dc bias value of I_B with the dc load line determines the Q-point.
- It is desirable to have the Q-point centered on the load line. Why?
- When a circuit is designed to have a centered Q-point, the amplifier is said to be midpoint biased.
- Midpoint biasing allows optimum ac operation of the amplifier.

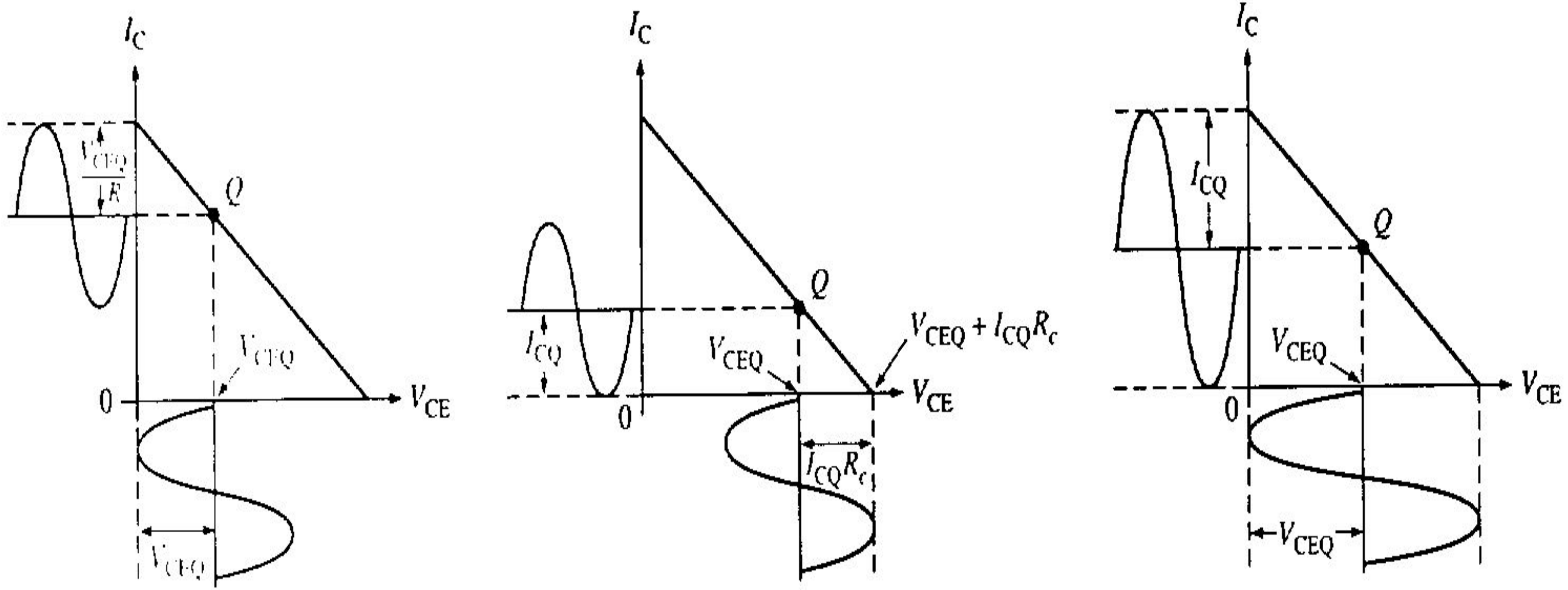


DC BIASING + AC SIGNAL

- When an **ac signal** is applied to the base of the transistor, I_C and V_{CE} will both vary around their Q-point values.
- When the Q-point is **centered**, I_C and V_{CE} can both make the **maximum** possible transitions above and below their initial dc values.
- When the Q-point is **above** the center on the load line, the input signal may cause the transistor to saturate. When this happens, a part of the output signal will be ***clipped*** off.
- When the Q-point is **below** midpoint on the load line, the input signal may cause the transistor to cutoff. This can also cause a portion of the output signal to be clipped.



DC Biasing + AC Signal

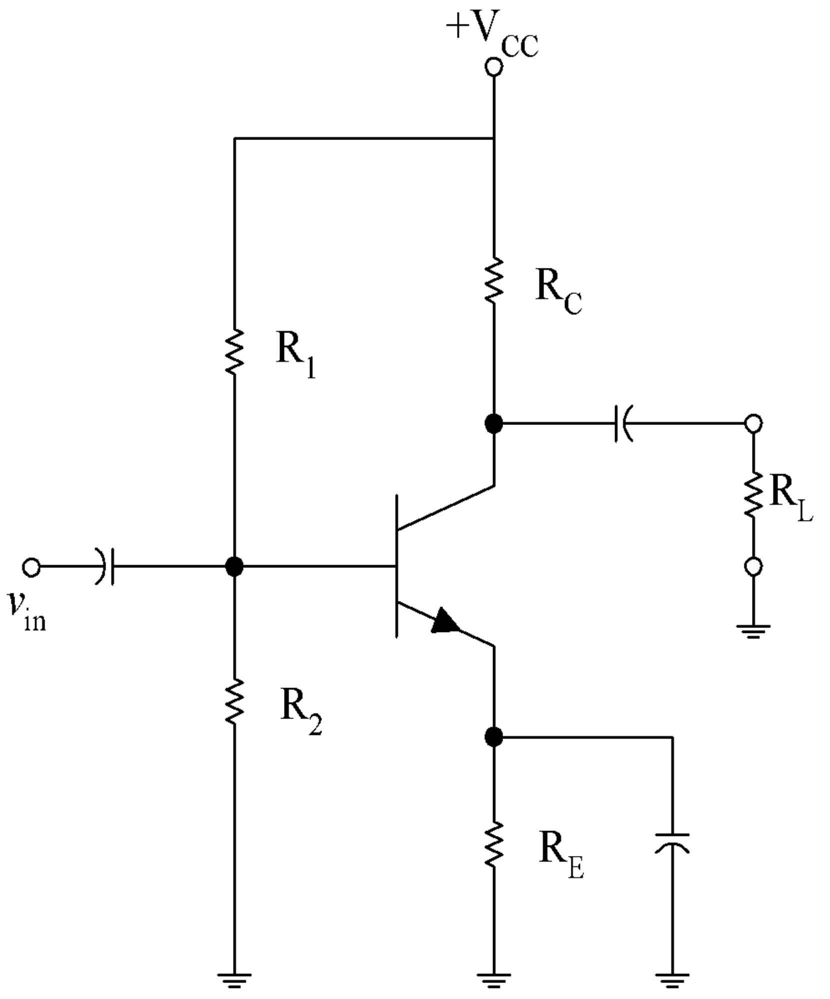


(a) Limited by saturation

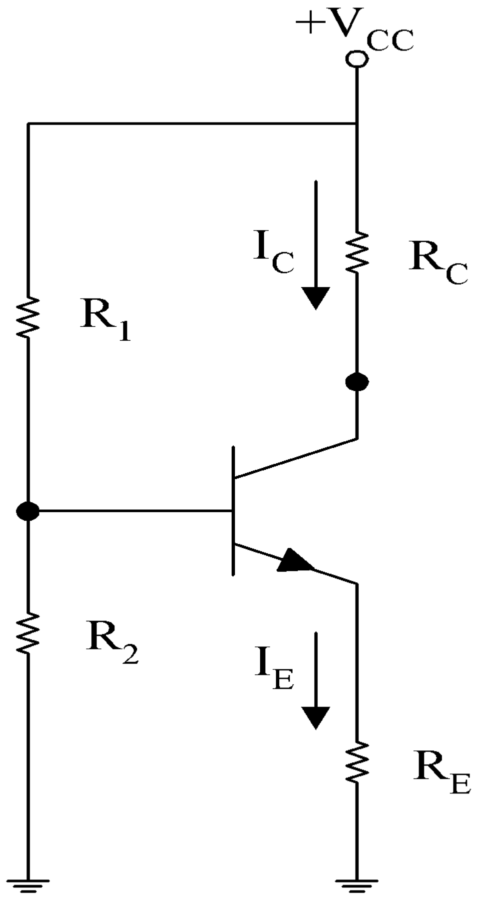
(b) Limited by cutoff

(c) Centered Q-point

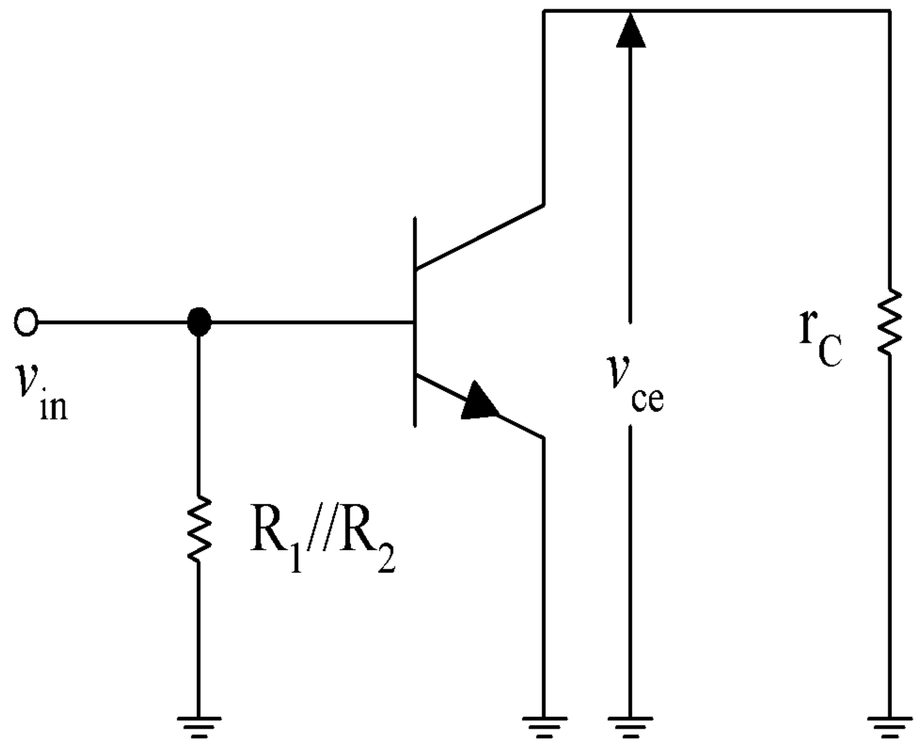
DC AND AC EQUIVALENT CIRCUITS



Bias Circuit



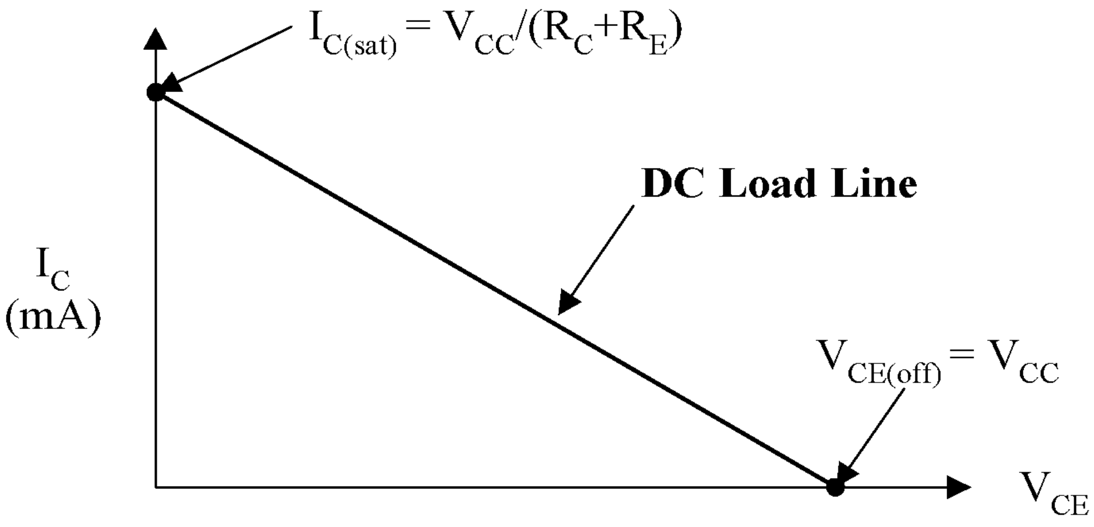
DC equivalent circuit

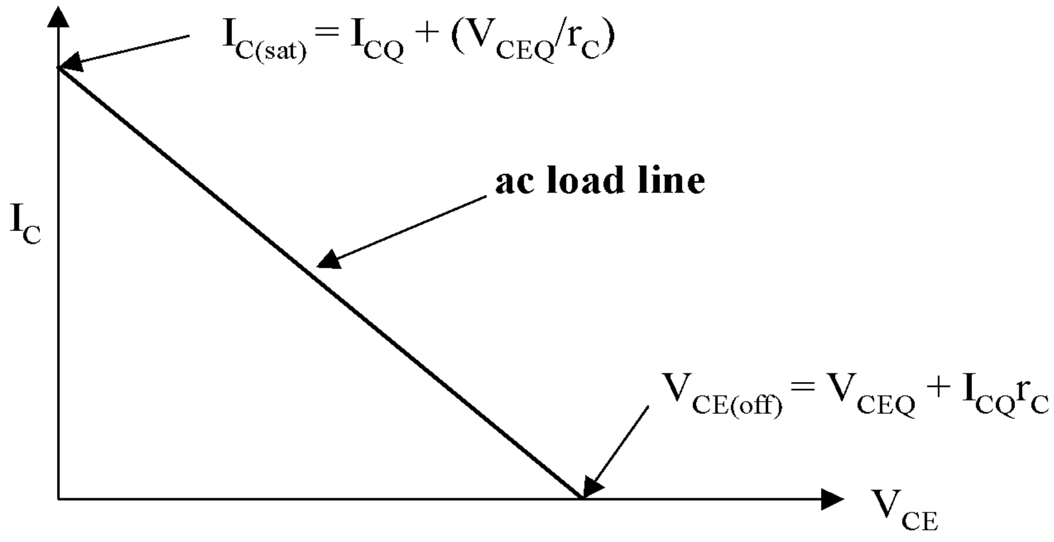


$r_C = R_C // R_L$

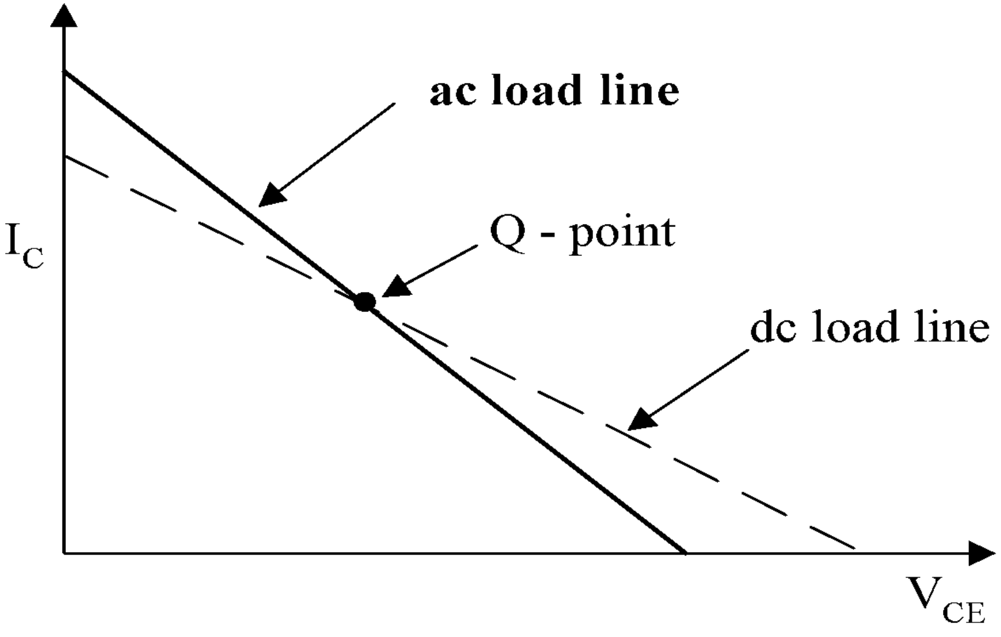
AC equivalent circuit

AC LOAD LINE





- The ac load line of a given amplifier will **not follow** the plot of the dc load line.
- This is due to the dc load of an amplifier is different from the ac load.



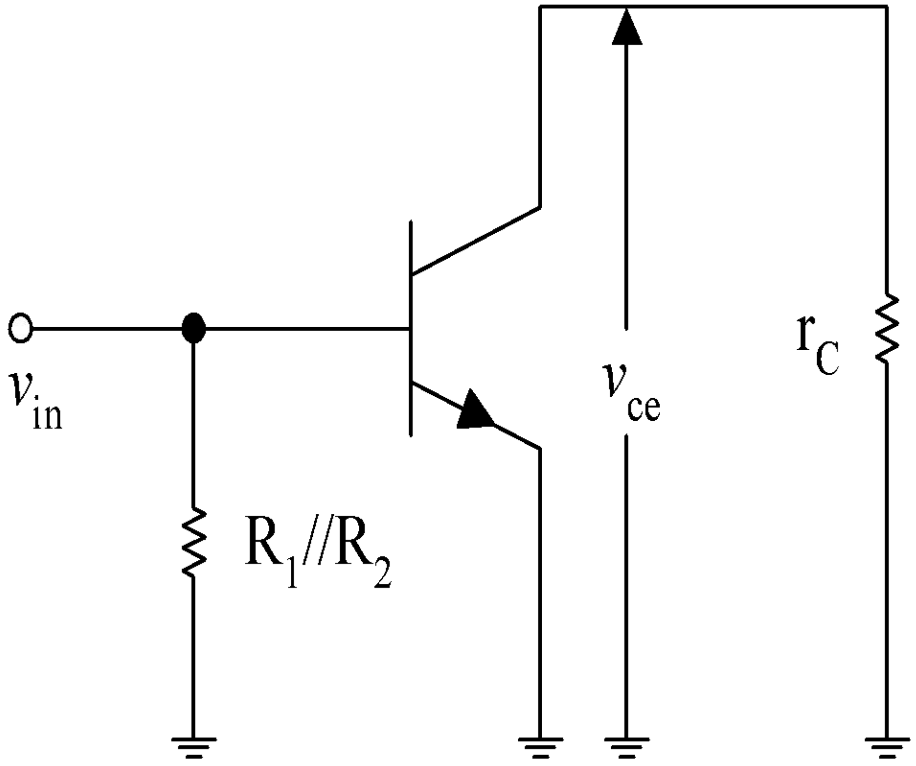
AC Load Line

What does the ac load line tell you?

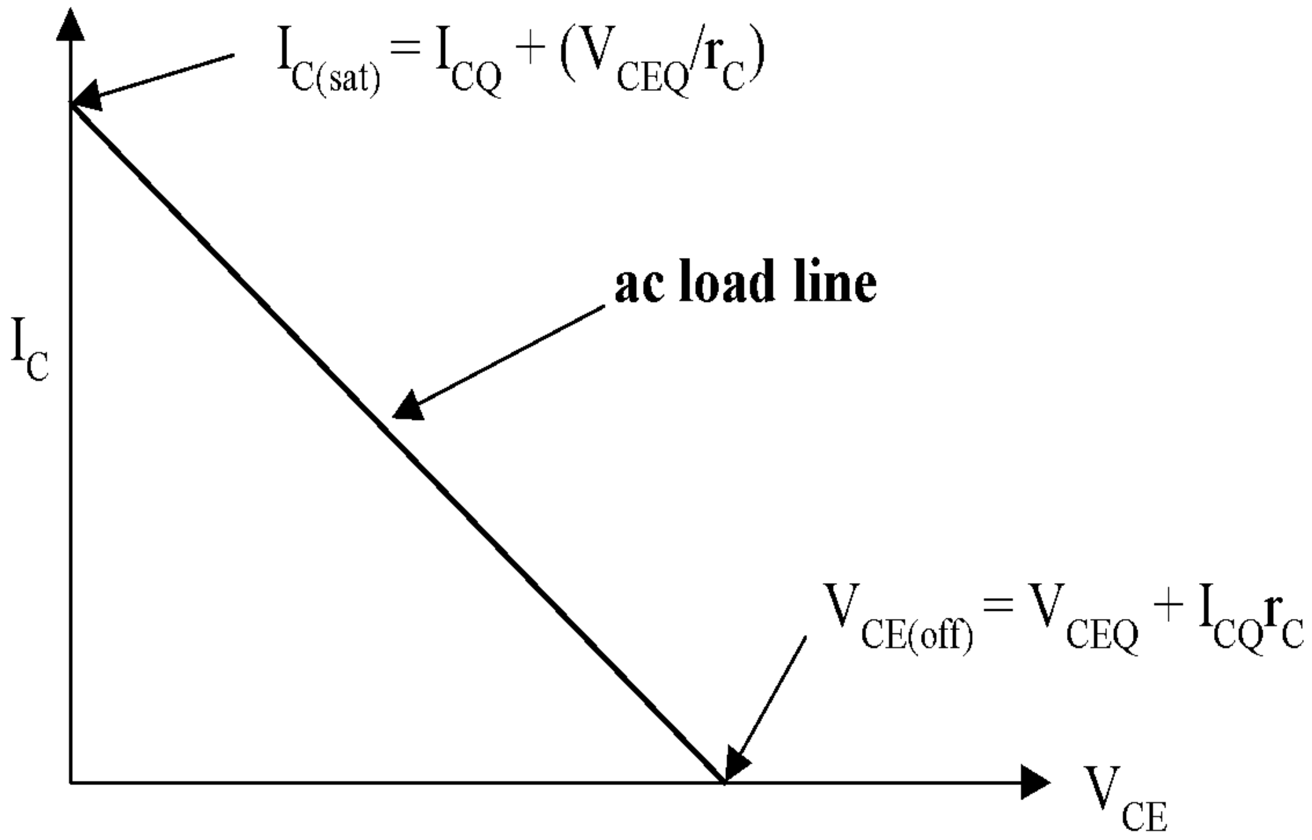
- The ac load line is used to tell you the maximum possible output voltage swing for a given common-emitter amplifier.
- In other words, the ac load line will tell you the maximum possible peak-to-peak output voltage (V_{pp}) from a given amplifier.
- This maximum V_{pp} is referred to as the **compliance** of the amplifier.

(AC Saturation Current $I_{c(sat)}$, AC Cutoff Voltage $V_{CE(off)}$)

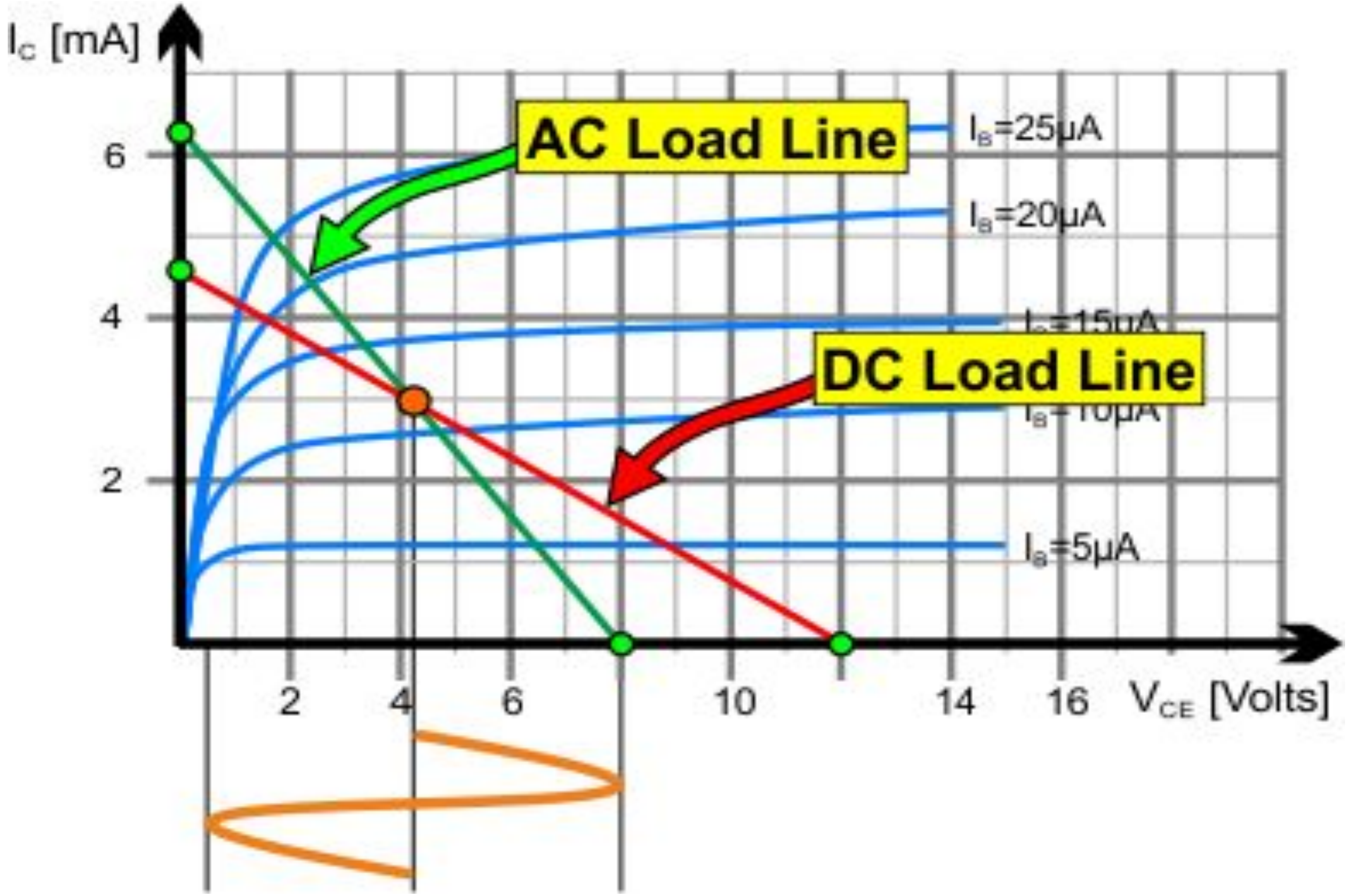
AC Saturation Current and AC Cutoff Voltage



$$r_C = R_C//R_L$$



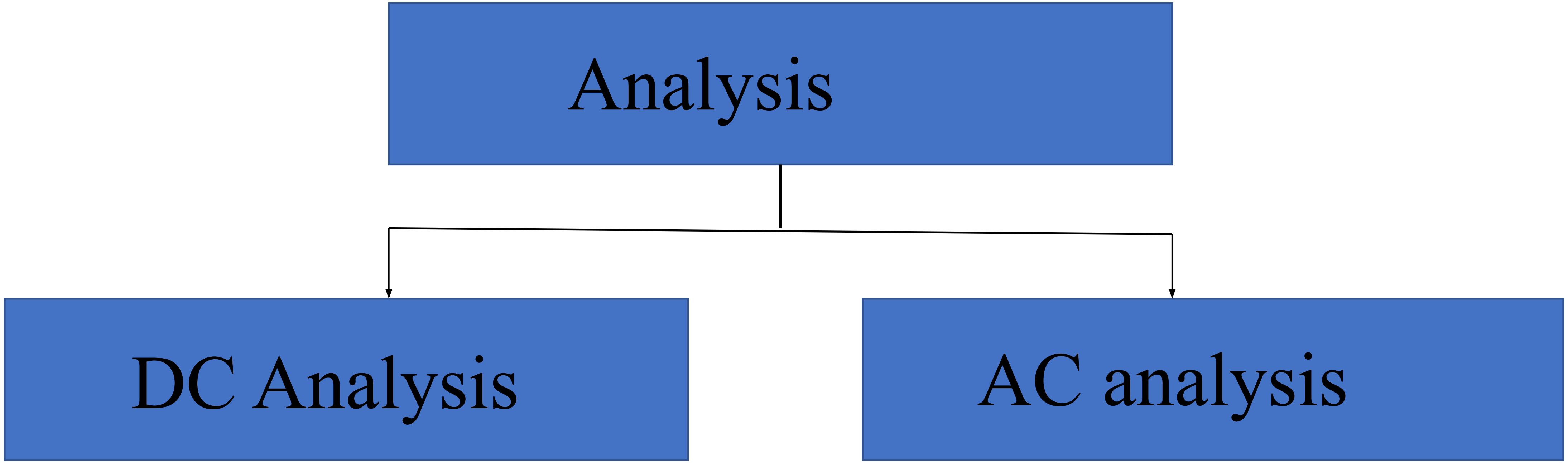
AC LOAD LINE ANALYSIS



- Slope of AC load Line = -1/(Rc || RL) corresponding to AC load resistance $R_{ac} = R_C || R_L$.

- Slope of DC load Line = -1/(Rc + RL)

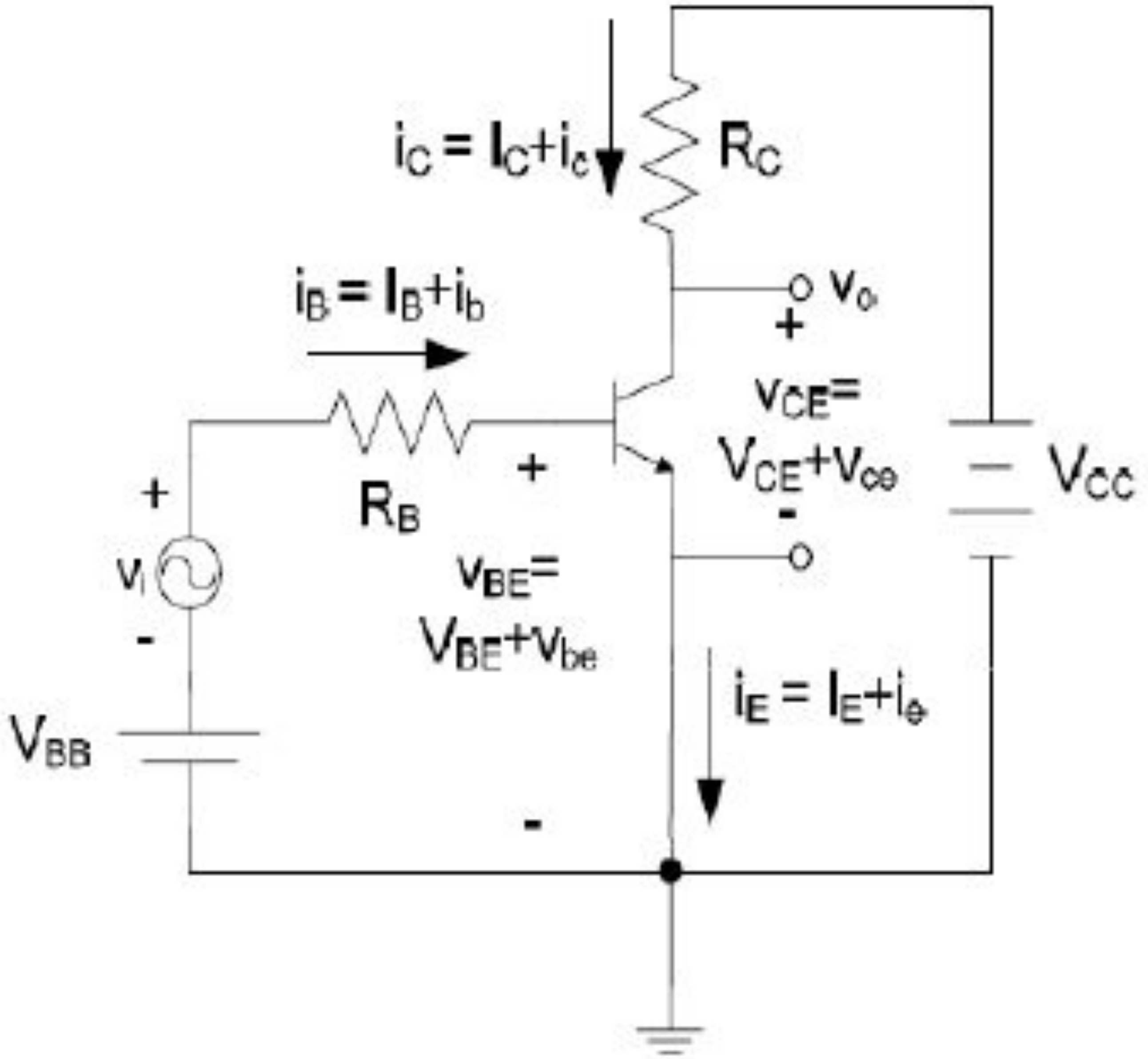
ANALYSIS



DC Values: ICQ and VCEQ

AC values: Zi, Zo, Av, Ai

BJT with AC input signal



$i_B = I_B + I_b$
$i_E = I_E + i_e$
$i_C = I_C + i_c$

I_B, I_C, I_E - D.C. currents
I_b, i_c, i_e – A.C. currents
i_B, i_C, i_E – D.C + A.C. currents

Similarly,
V_{BE}, V_{CE} – D.C. Voltages
v_{be}, v_{ce} – A.C.Voltages
v_{BE}, v_{CE} – D.C+ A.C Voltages

BJT WITH SMALL AC INPUT SIGNAL

Small ac signal refers to the input signal (v_{be}) whose magnitude is much small than thermal voltage (V_T) i.e. $v_{be} << V_T$

Magnitude of the ac signal applied for amplification must be small so that

- the transistor operates in the linear region for the whole cycle of input (called as a linear amplifier)
- the transistor is never driven into saturation or cut-off region

- On the other hand, if the input signal is too large. The fluctuations along the load line will drive the transistor into either saturation or cut off. This clips the peaks of the input and the amplifier is no longer linear.

BJT TRANSISTOR MODELLING

A model is the combination of circuit elements, properly chosen, that best approximates the actual behavior of a semiconductor device under specific operating conditions.

Once the ac equivalent circuit has been determined, the graphical symbol of the device can be replaced in the schematic by this circuit and the basic methods of ac circuit analysis (mesh analysis, nodal analysis, and Thévenin's theorem) can be applied to determine the response of the circuit.

BJT Circuit Analysis using small signal model

1. Determine the DC operating point of the BJT and in particular, the collector current I_C
2. Calculate small-signal model parameters g_m, r_π, & r_e for this DC operating point
3. Eliminate DC sources
   - Replace DC voltage sources with short circuits
   - Replace DC current sources with open circuits
4. Replacing all capacitors by a short circuit equivalent and remove all elements bypassed by the short circuit equivalents.
5. Replace BJT with an equivalent small-signal model
6. Analyze the resulting circuit to determine the required quantities e.g. voltage gain, input resistance…etc.

HYBRID PI MODEL OF BJT

- The **hybrid**-pi **model** is a linearized two-port network approximation to the BJT using the small-signal base-emitter voltage and collector-emitter voltage, as independent variables, and the small-signal base current, and collector current, as dependent variables.
- It is the intrinsic representation of BJT.

HYBRID PI MODEL OF BJT

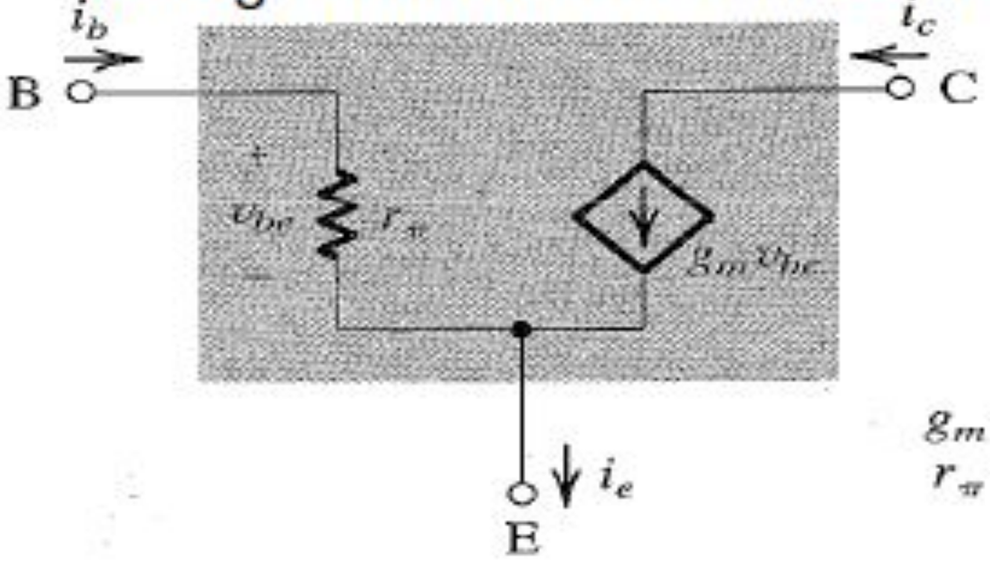
This model represents that transistor as a voltage controlled current source with control voltage v_{be} and include the input resistance looking into the base.

$$r_\pi = \frac{v_{be}}{i_b} = \frac{\beta}{g_m} = \frac{V_T}{I_B}$$

$$r_e = \frac{v_{be}}{i_e} = \frac{\alpha}{g_m} = \frac{V_T}{I_E}$$

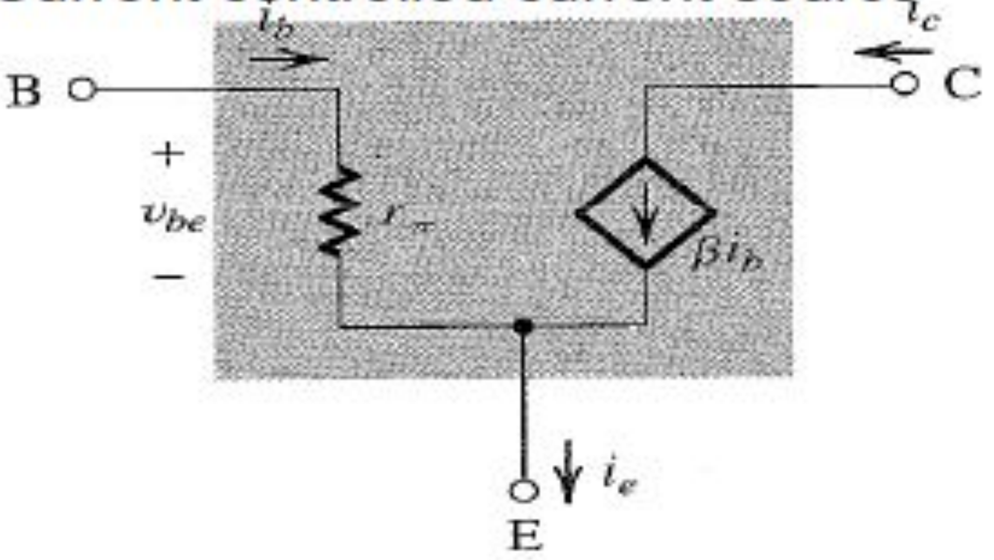
$$g_m = \frac{i_c}{v_{be}} = \frac{I_C}{V_T}$$

Voltage controlled current source

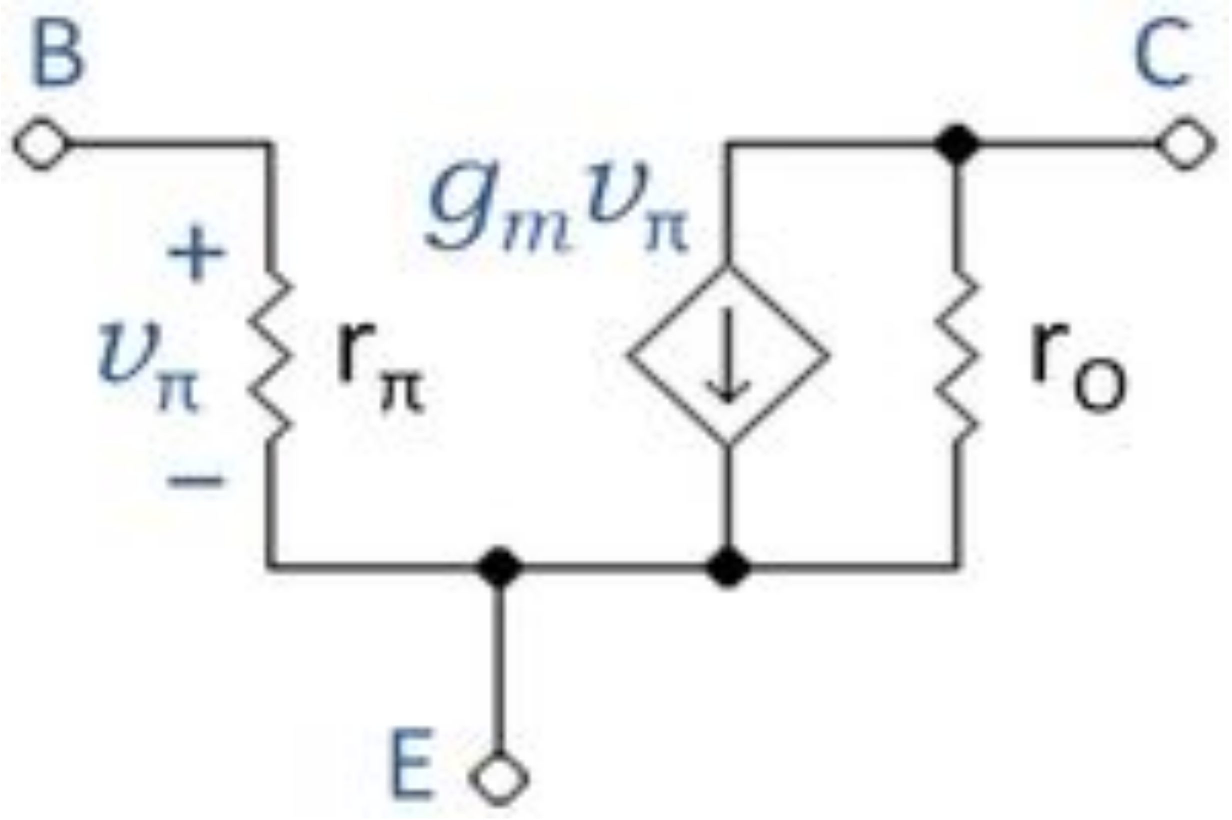


$$g_m = I_C/V_T$$
$$r_\pi = \beta/g_m$$

Current controlled current source

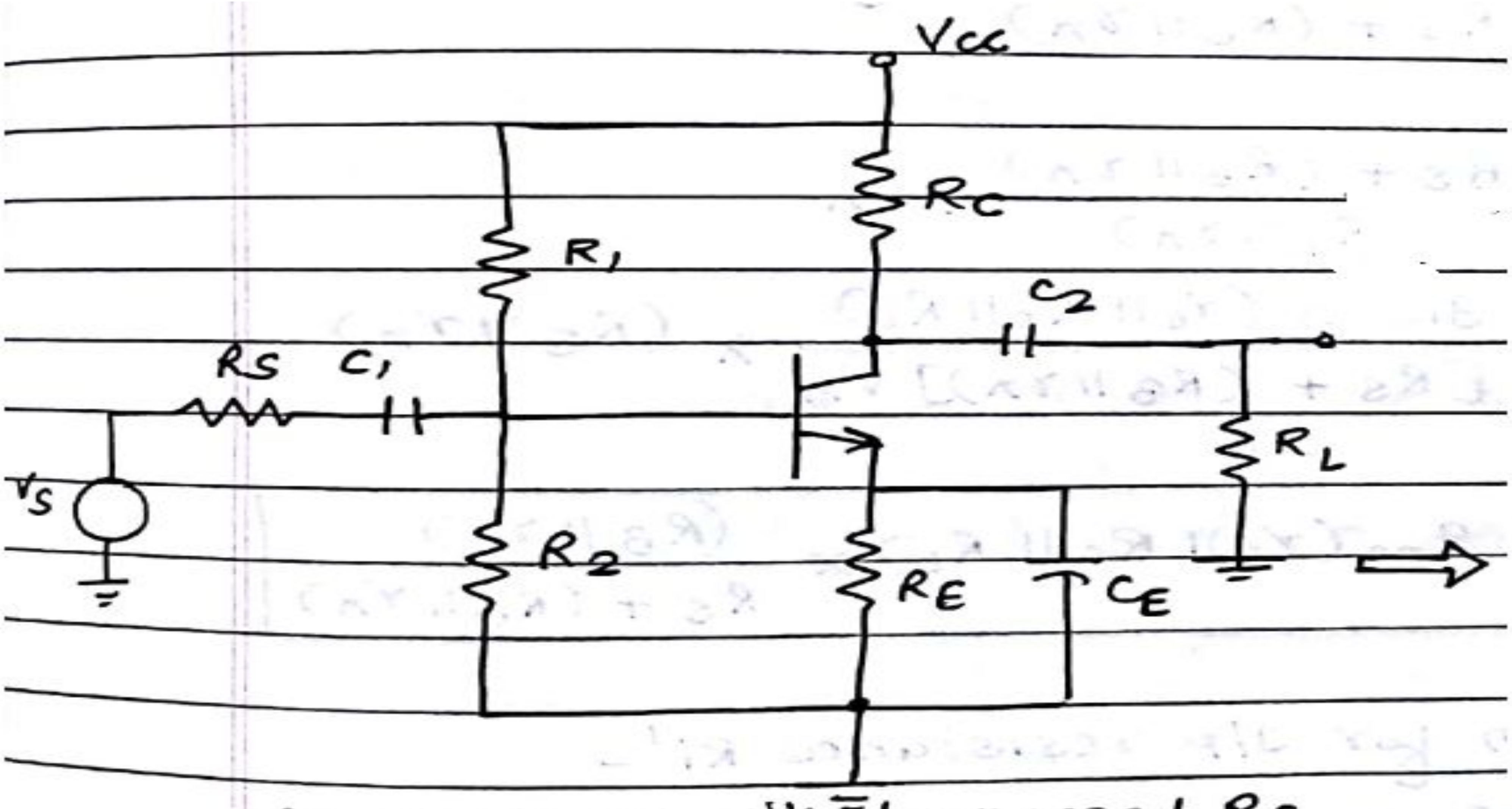


HYBRID PI MODEL OF BJT USING EARLY EFFECT



$$r_o \equiv \left[\left. \frac{\partial i_C}{\partial v_{CE}} \right|_{v_{BE}=\text{constant}} \right]^{-1} \qquad r_o = \frac{V_A}{I'_C}$$

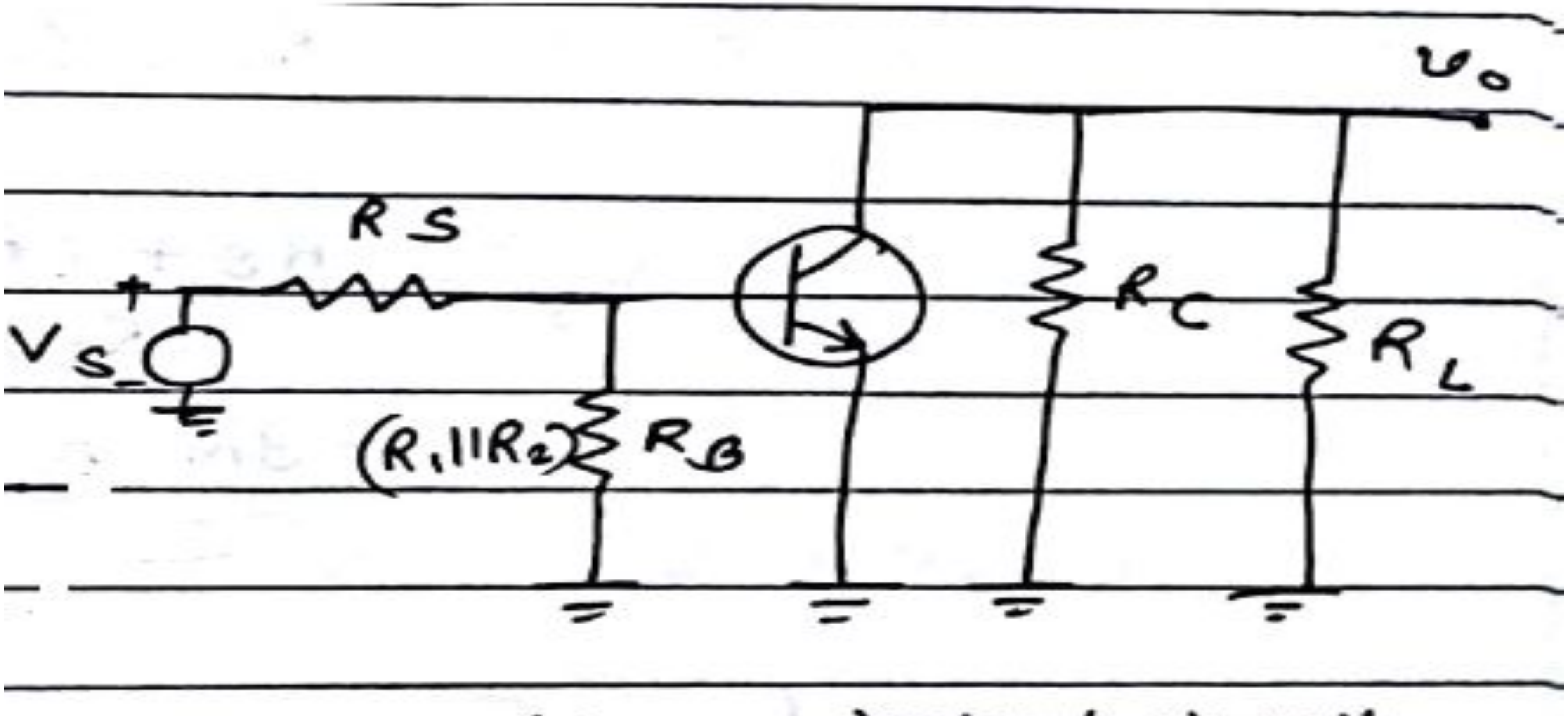
SMALL SIGNAL ANALYSIS OF CE AMPLIFIER USING HYBRID PI MODEL



CE Amplifier with bypassed RE

SMALL SIGNAL ANALYSIS OF CE AMPLIFIER USING HYBRID PI MODEL

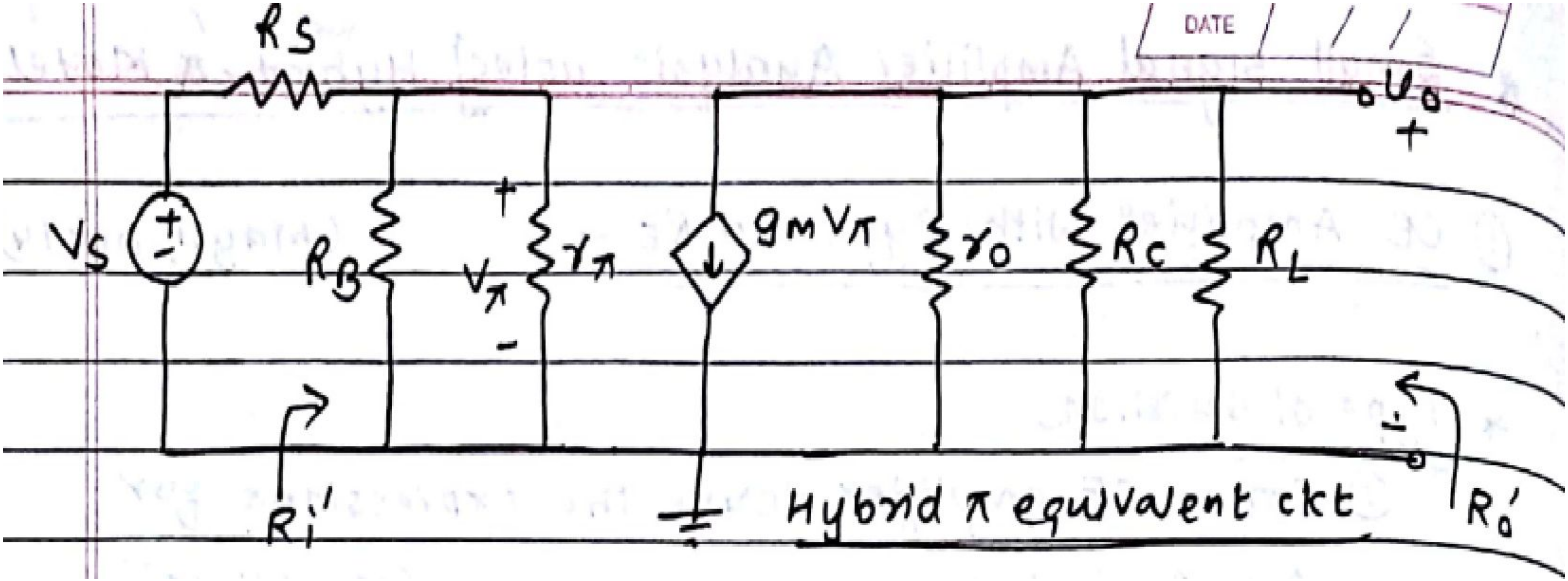
STEP 1: Draw AC equivalent circuit of CE amplifier with bypassed RE



AC equivalent circuit

SMALL SIGNAL ANALYSIS OF CE AMPLIFIER USING HYBRID PI MODEL

Step 2: Draw Hybrid pi model of CE amplifier with bypassed RE



SMALL SIGNAL ANALYSIS OF CE AMPLIFIER USING HYBRID PI MODEL

Step ③ - Expression for voltage gain (A_{VS}) -

$$A_{VS} = \frac{V_o}{V_s}$$

$$v_o = -g_m V_\pi (r_o \parallel R_C \parallel R_L)$$

$$V_\pi = \frac{(R_B \parallel r_\pi)}{R_S + (R_B \parallel r_\pi)} \times V_s \qquad (R_B = R_1 \parallel R_2)$$

$$V_s = \frac{R_S + (R_B \parallel r_\pi)}{(R_B \parallel r_\pi)} \times V_\pi$$

$$= \frac{-g_m V_\pi (r_o \parallel R_C \parallel R_L)}{[R_S + (R_B \parallel r_\pi)] V_\pi} \times (R_B \parallel r_\pi)$$

$$\boxed{A_{VS} = -g_m (r_o \parallel R_C \parallel R_L) \times \frac{(R_B \parallel r_\pi)}{R_S + (R_B \parallel r_\pi)}}$$

SMALL SIGNAL ANALYSIS OF CE AMPLIFIER USING HYBRID PI MODEL

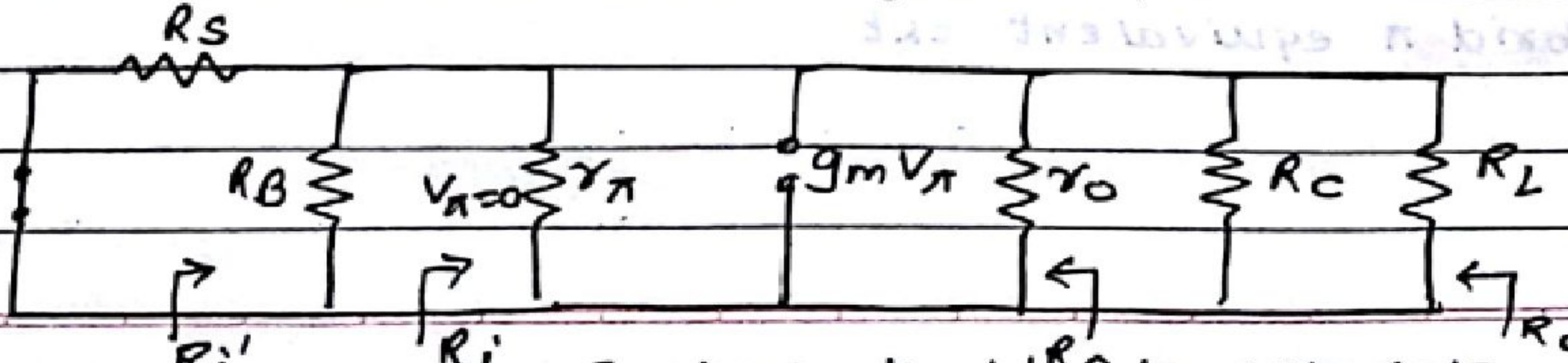
Step 4 Expression for i/p resistance R_i' –

$$R_i' = (R_B \parallel r_\pi) = (R_1 \parallel R_2 \parallel r_\pi)$$

also $R_i = r_\pi$

Step 5 Expression for output Resistance R_o' –

R_o' is obtained by setting $V_S = 0$, As $V_S = 0$, $V_\pi = 0$, $g_m V_\pi = 0$



Equivalent ckt to calculate R_o'

SMALL SIGNAL ANALYSIS OF CE AMPLIFIER USING HYBRID PI MODEL

o/p Resistance back into o/p terminal,

$R_o' = (r_o \| R_C \| R_L)$ also $R_o = r_o$

step ⑥ Expression for current gain (A_{IS}) -

$$A_{IS} = \frac{I_o}{I_i}$$

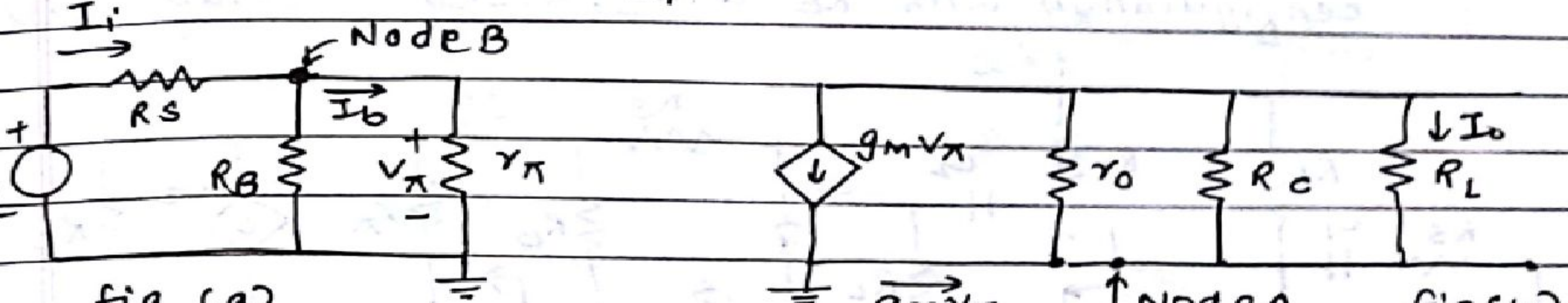


fig (a) fig (b)

using current division Rule, $$I_o = \frac{-g_m V_\pi (r_o \| R_C)}{(r_o \| R_C) + R_L} \quad (1)$$

SMALL SIGNAL ANALYSIS OF CE AMPLIFIER USING HYBRID PI MODEL

from fig a) $V_\pi = I_b r_\pi$ — (2)

using current division Rule, $I_b = \frac{R_B}{R_B + r_\pi} \times I_i$ Put in (2)

$$\therefore V_\pi = \frac{R_B r_\pi}{(R_B + r_\pi)} \times I_i = (R_B \parallel r_\pi) I_i$$

Put value of V_π in eq^n (1)

$$I_o = \frac{-g_m (r_o \parallel R_C)}{R_L + (r_o \parallel R_C)} \times (R_B \parallel r_\pi) I_i$$

current gain

$$\boxed{A_{IS} = \frac{I_o}{I_i} = \frac{-g_m (r_o \parallel R_C)(R_B \parallel r_\pi)}{R_L + (r_o \parallel R_C)}}$$

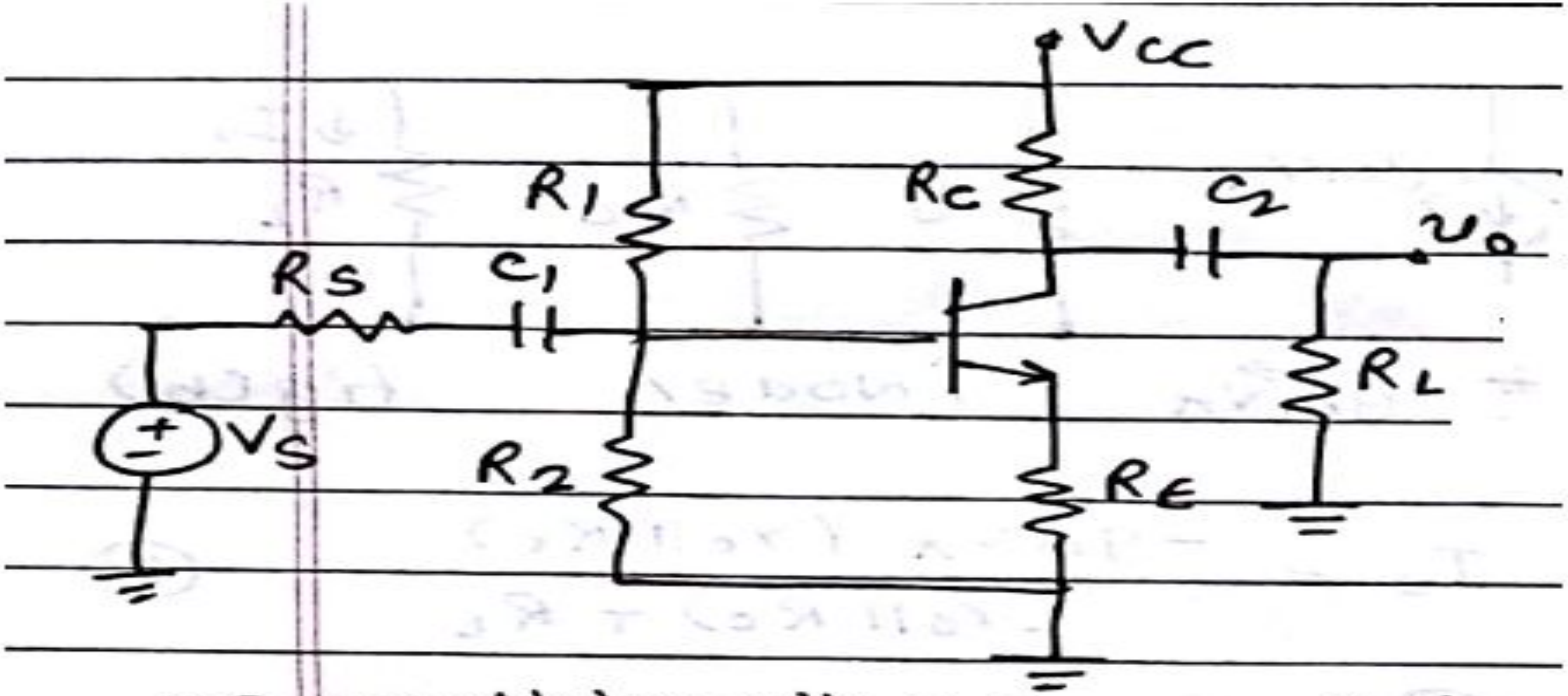
SMALL SIGNAL ANALYSIS OF CE AMPLIFIER USING HYBRID PI MODEL

Advantage - provides high volltage gain (due to low R_i)

Disadvantage - low i/p Resistance

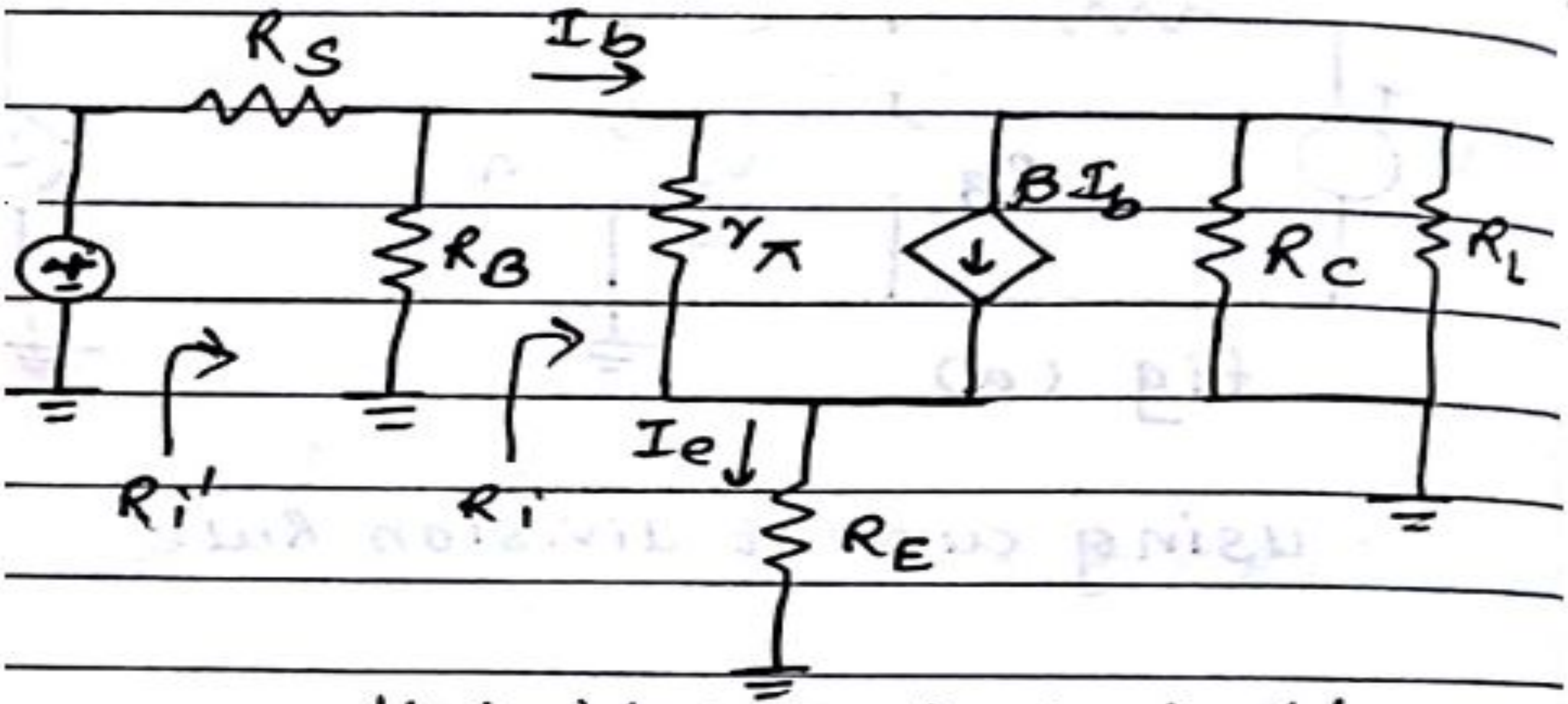
$\boxed{R_i = r_\pi}$ & $\boxed{R_i' = R_1 \| R_2 \| r_\pi}$

SMALL SIGNAL ANALYSIS OF CE AMPLIFIER WITH UN-BYPASSED RE USING HYBRID PI MODEL



CE amplifier with unbypassed RE

SMALL SIGNAL ANALYSIS OF CE AMPLIFIER WITH UN-BYPASSED RE USING HYBRID PI MODEL



Hybrid π equivalent ckt

SMALL SIGNAL ANALYSIS OF CE AMPLIFIER WITH UN-BYPASSED RE USING HYBRID PI MODEL

$\boxed{\text{step } 1}$ obtain expression for R_i & R_i'

$$R_i = \frac{V_b}{I_b} \quad \text{--- (1)}$$

But $V_b = I_b r_\pi + I_e R_E$

$$= I_b r_\pi + (1+\beta) I_b R_E$$

$V_b = I_b [r_\pi + (1+\beta) R_E]$ Put in eq^n (1)

$$R_i = \frac{I_b [r_\pi + (1+\beta) R_E]}{I_b}$$

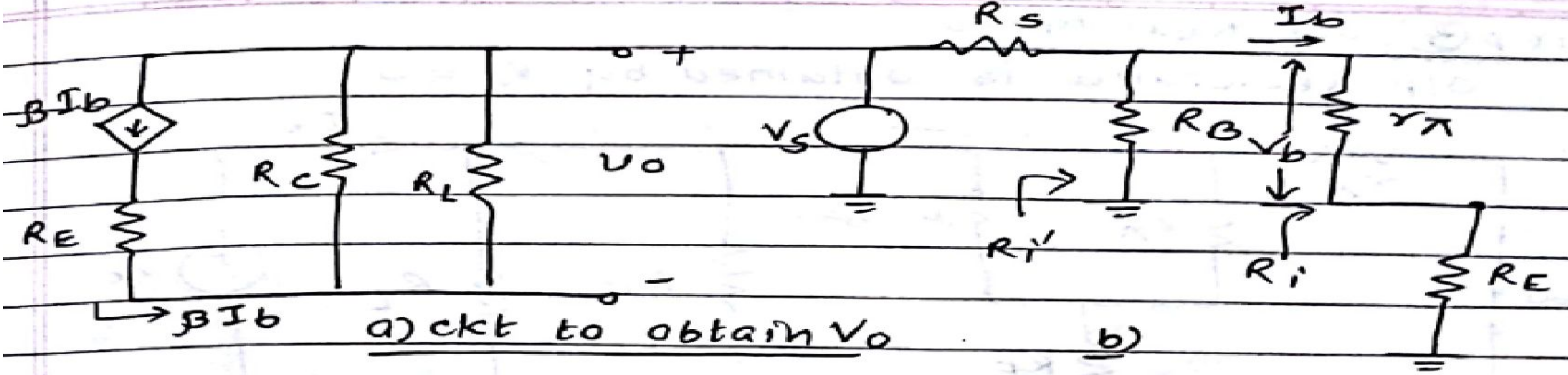
$$\boxed{R_i = r_\pi + (1+\beta) R_E}$$

$$R_i' = R_B \parallel R_i = (R_1 \parallel R_2) \parallel [r_\pi + (1+\beta) R_E]$$

SMALL SIGNAL ANALYSIS OF CE AMPLIFIER WITH UN-BYPASSED RE USING HYBRID PI MODEL

step (2) obtain expression of voltage gain A_{vs} –

$$A_{vs} = \frac{V_o}{V_s}$$



a) ckt to obtain V_o b)

$$V_o = -\beta I_b (R_c \| R_L)$$

from fig b), $V_b = I_b R_i$ or $I_b = V_b / R_i$

Small Signal Analysis of CE Amplifier with Un-bypassed RE using Hybrid Pi Model

$$V_o = \frac{-\beta V_b (R_c \parallel R_L)}{R_i'} \quad \text{But } V_b = \frac{R_i'}{R_i' + R_S} \times V_s$$

$$V_o = \frac{-\beta R_i' V_s}{(R_i' + R_s)} \times \frac{(R_c \parallel R_L)}{R_i}$$

$$\frac{V_o}{V_s} = A_{V_s} = \frac{-\beta R_i'}{(R_i' + R_s)} \times \frac{(R_c \parallel R_L)}{R_i}$$

But $R_i = r_\pi + (1+\beta) R_E$

$$\boxed{A_{V_s} = \frac{-\beta (R_c \parallel R_L)}{r_\pi + (1+\beta) R_E} \times \frac{R_i'}{(R_i' + R_s)}}$$

Exact expression

SMALL SIGNAL ANALYSIS OF CE AMPLIFIER WITH UN-BYPASSED RE USING HYBRID PI MODEL

But if $R_i' >> R_S$ & $(1+\beta) >> r_\pi$ then

$$A_{V_S} \approx \frac{-\beta (R_C \parallel R_L)}{(1+\beta) R_E} \quad \text{if } \beta = (1+\beta)$$

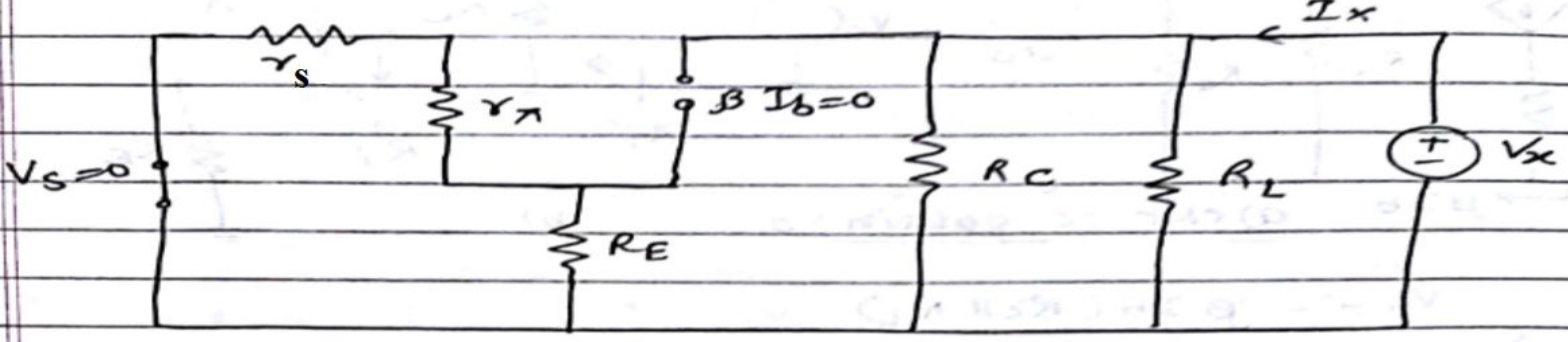
$$\boxed{A_{V_S} = \frac{-(R_C \parallel R_L)}{R_E}}$$

Approximate voltage gain

SMALL SIGNAL ANALYSIS OF CE AMPLIFIER WITH UN-BYPASSED RE USING HYBRID PI MODEL

step ③ o/p Resistance

o/p Resistance is obtained by $V_S = 0$



Circuit to obtain output Resistance

As $V_S = 0$, $I_b = 0$ $\therefore \beta I_b = 0$

$$\boxed{R_o' = \frac{V_x}{I_x} = R_C \parallel R_L}$$

SMALL SIGNAL ANALYSIS OF CE AMPLIFIER WITH UN-BYPASSED RE USING HYBRID PI MODEL

Advantages -

- It increases I/p impedance (R_i')
- stability of A_v increases w.r.t β

Disadvantage -

Reduction in voltage gain (A_v)

Summary of analysis of CE amplifier with bypassed R_E :

Sr. No.	Parameter	Expression
1.	Voltage gain	$A_{VS} = \dfrac{-g_m (r_o \parallel R_C \parallel R_L) \times (R_B \parallel r_\pi)}{R_S + (R_B \parallel r_\pi)}$
2.	Input resistance	$R_i = r_\pi$ $R_i' = R_B \parallel r_\pi = (R_1 \parallel R_2) \parallel r_\pi$
3.	Output resistance	$R_o = r_o$ $R_o' = r_o \parallel R_C \parallel R_L$
4.	Current gain	$A_{IS} = \dfrac{-g_m (r_o \parallel R_C)(R_B \parallel r_\pi)}{R_L + (r_o \parallel R_C)}$

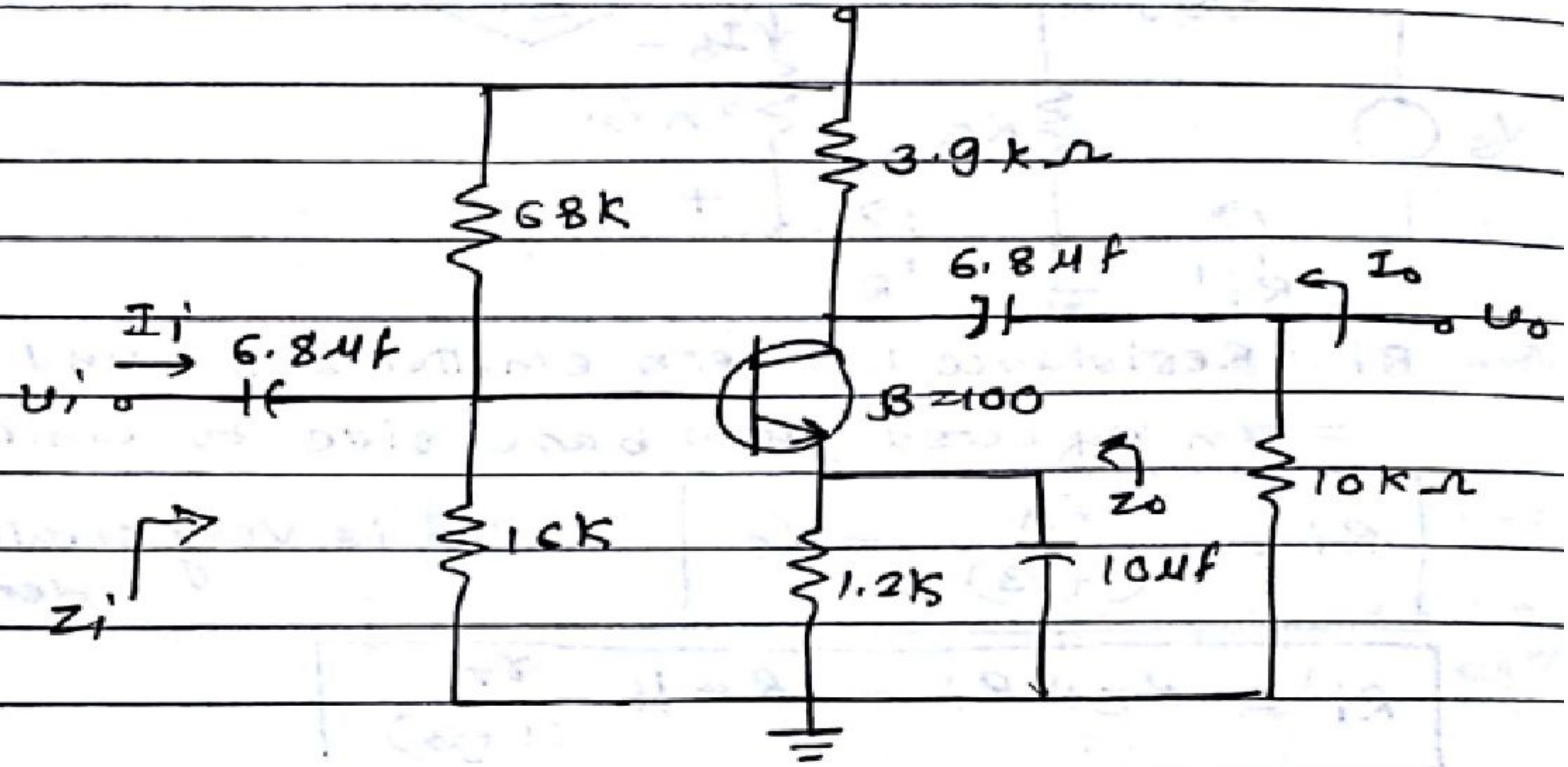
Summary of Analysis of CE Amplifier with unbypassed R_E

Sr No.	Parameter	Expression
1.	Input Resistance	$R_i = r_\pi + (1+\beta) R_E$ $R_i' = R_1 \parallel R_2 \parallel [r_\pi + (1+\beta) R_E]$
2.	Voltage Gain	$A_{V_S} = \dfrac{-\beta (R_C \parallel R_L)}{r_\pi + (1+\beta) R_E} \times \dfrac{R_i'}{(R_i' + R_S)}$ $= \dfrac{-\beta (R_C \parallel R_L)}{(1+\beta) R_E} = \dfrac{-(R_C \parallel R_L)}{R_E}$
3.	Output Resistance	$R_o' = R_C \parallel R_L$

EXAMPLE 1

Ex 1. For the given circuit find,

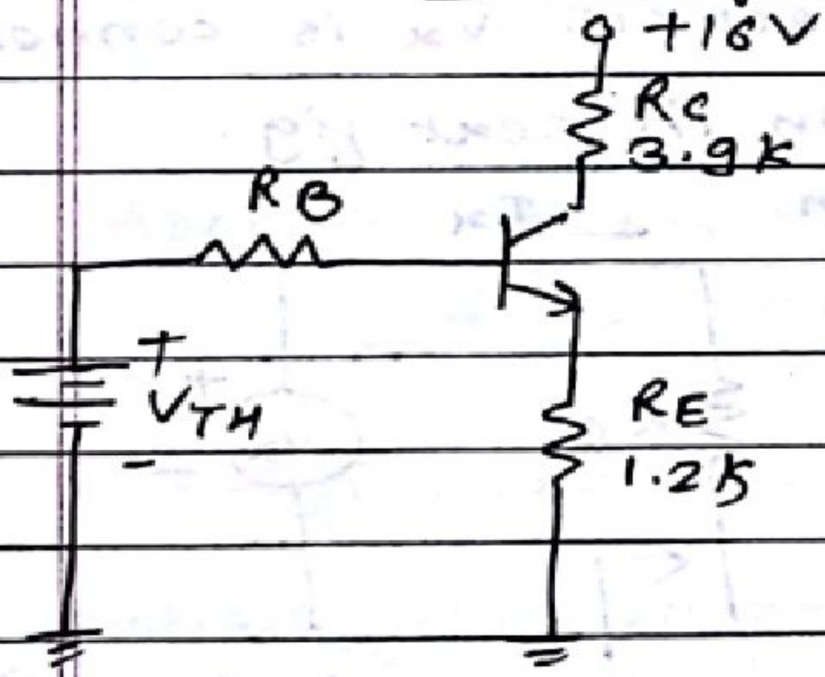
1. Determine Z_i, Z_o & A_v no load
2. A_v with load
3. A_i



SOLUTION

Soln- ckt - CE amplifier with bypassed R_E

step ① DC analysis-



Thevenin's DC equivalent

$$V_{TH} = \frac{R_2}{R_1 + R_2} \times V_{cc}$$

$$= \frac{16}{16 + 68} \times 16 = 3V$$

$$R_B = R_1 \parallel R_2 = 16 \parallel 68 = \frac{16 \times 68}{16 + 68}$$

$$R_B = 12.95 k\Omega$$

$$I_B = \frac{V_{Th} - V_{BE}}{R_B + (1+\beta) R_E} = \frac{3 - 0.7}{12.95k + (101 \times 1.2k)} = 17.15 \mu A$$

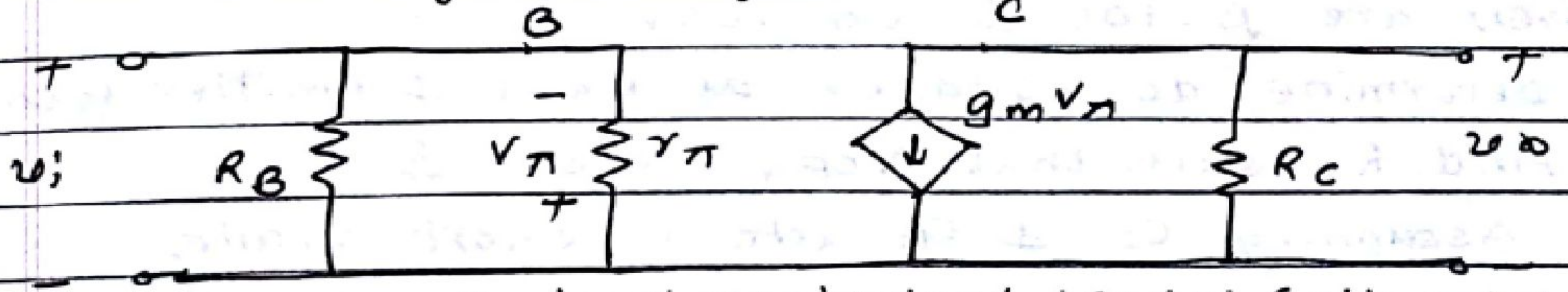
$$I_{CQ} = \beta I_B = 100 \times 17.15 \mu A = \underline{1.715 mA}$$

SOLUTION

Let $V_T = 26mV$ $\quad r_\pi = \frac{V_T \beta}{I_{CQ}} = \frac{26 \times 100}{1.715} = 1.516 k\Omega$

$g_m = \frac{I_{CQ}}{V_T} = \frac{1.715}{26 \times 10^{-3}} = 65.96 mA/V$, $r_o = \frac{V_A}{I_{CQ}} = \infty$

step ② Small signal Analysis -



small signal equivalent Model (without load)

$R_i = r_\pi = 1.516 k\Omega$

$R_i' = R_B \| R_i = 1.516k \| 12.95k = 1.357 k\Omega$

SOLUTION

$$A_V = \frac{V_o}{V_i} = \frac{-g_m V_\pi R_C}{V_\pi} = -g_m R_C = -65.96 \times 3.9$$

$$= -257.244$$

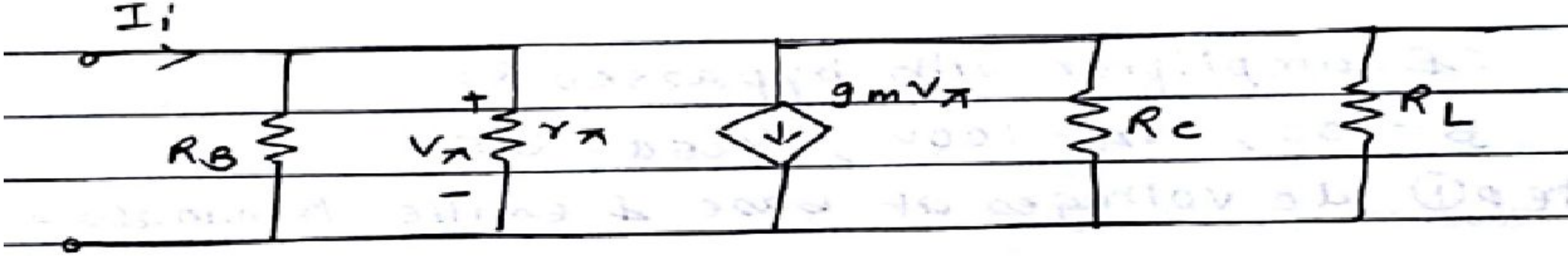
$$R_o = \infty$$

$$R_o' = R_C = 3.9\,k\Omega$$

$$A_V = -g_m(R_C \parallel R_L) = -65.96(3.9 \parallel 10)$$

$$= -65.96 \times 2.805 = -185$$

SOLUTION



$$A_i = \frac{I_o}{I_b} = \frac{I_o}{I_c} \times \frac{I_c}{I_b} \quad \text{But } I_o = \frac{-R_C}{R_C + R_L} \times I_c$$

$$\frac{I_o}{I_c} = \frac{-R_C}{R_C + R_L} \quad , \quad \frac{I_c}{I_b} = \frac{g_m V_\pi}{V_\pi / r_\pi} = g_m r_\pi$$

$$A_i = \frac{-R_C}{R_C + R_L} \times g_m r_\pi$$

$$A_i = (-65.96 \times 1.516) \times \frac{3.9}{3.9 + 10} = \underline{-28.05}$$

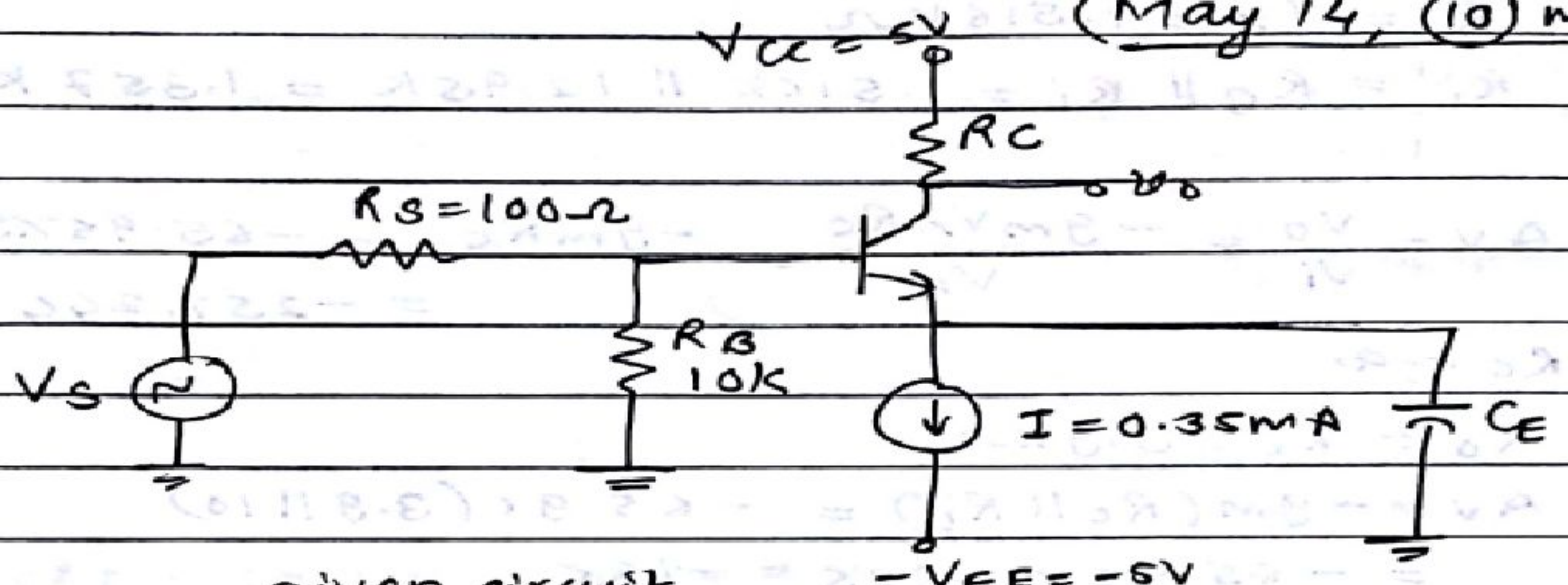
EXAMPLE 2

Ex② The parameters of the 'transistor' in the circuit given are $\beta = 100$ & $V_A = 100V$

1. Determine dc voltages at base & emitter terminals
2. Find R_C such that $V_{CEQ} = 3.5V$ &
3. Assuming C_C & C_E acts as short circuit, Determine small signal voltage gain $A_V = \frac{V_O}{V_S}$

(May 14, 10 marks)

Soln-



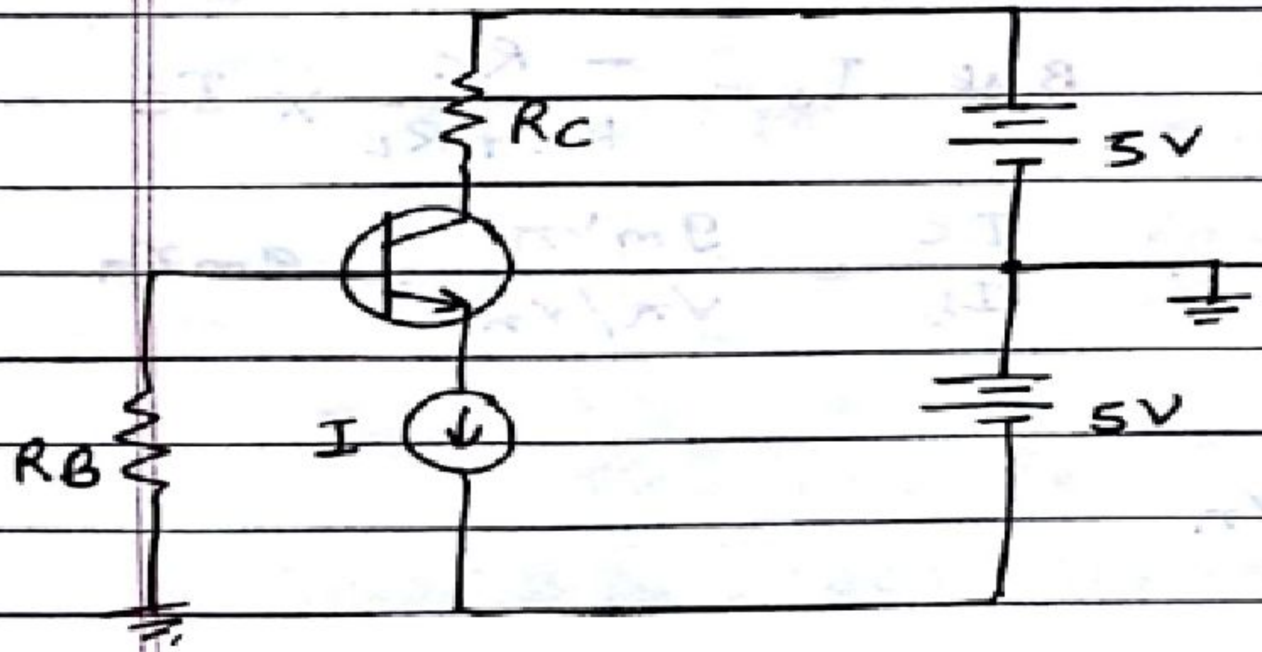
given circuit

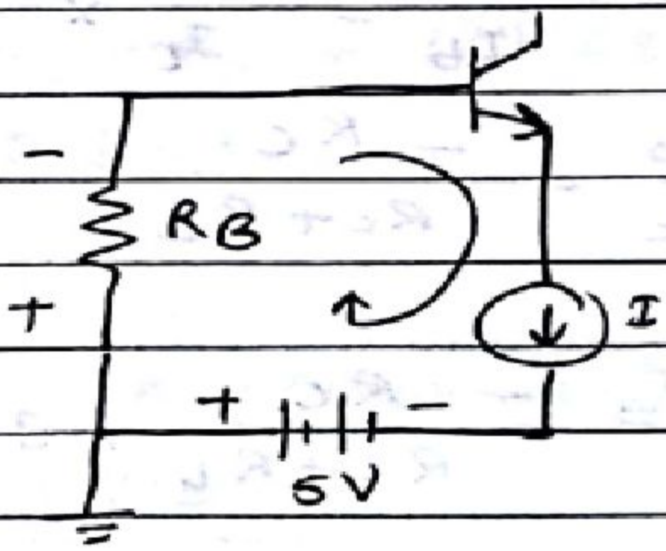
SOLUTION

Soln – CE amplifier with bypassed R_E

$\beta = 100$, $V_A = 100V$, $V_{CEQ} = 3.5V$

Step ① dc voltages at base & emitter terminals –





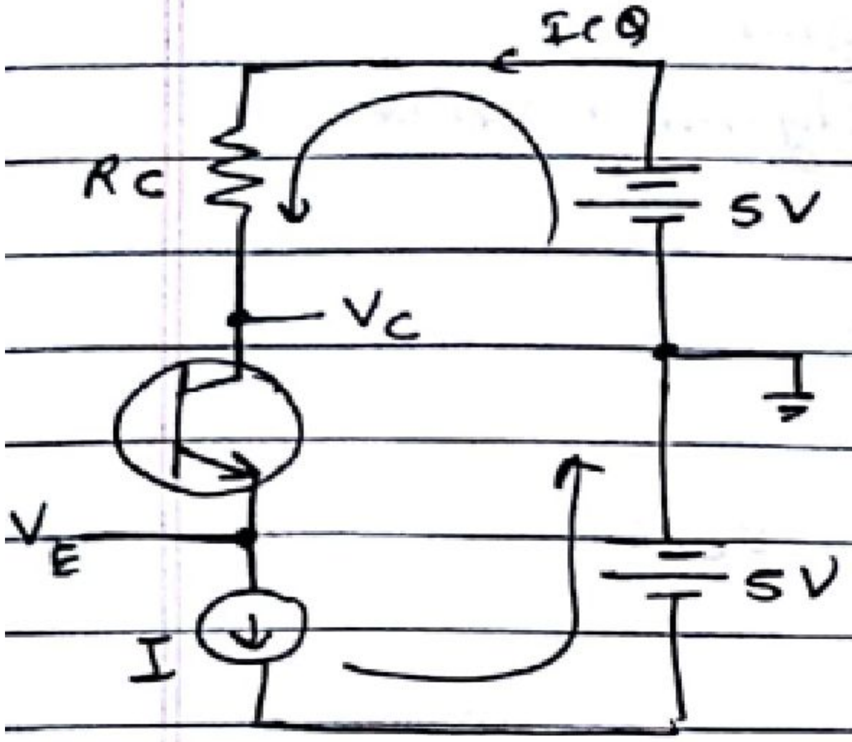
$$I_B = \frac{I_E}{1+\beta} = \frac{I}{1+\beta} = \frac{0.35 \times 10^{-3}}{101} = 3.47 \mu A$$

SOLUTION

$$V_B = -I_B R_B = -3.47 \times 10^{-6} \times 10 \times 10^{3} = -0.0347\,V$$

$$V_E = V_B - 0.7 = -0.0347 - 0.7 = -0.7347\,V$$

step ② find R_C



$V_{CEQ} = 3.5\,V$

$V_{CEQ} = V_C - V_E$

$3.5\,V = V_C - (-0.7347)$

$$\boxed{V_C = 2.77\,V}$$

$$R_C = \frac{5V - V_C}{I_{CQ}}$$

assuming $I_{CQ} = I = 0.35\,mA$

$$R_C = \frac{5 - 2.77}{0.35 \times 10^{-3}} = 6.37\,k\Omega$$

SOLUTION

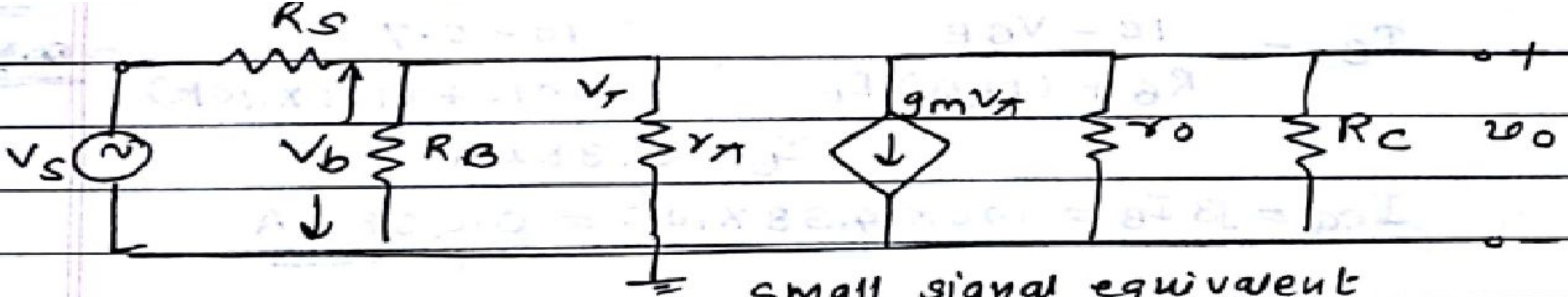
$\boxed{\text{step } 3}$ $r_\pi = \dfrac{V_T \cdot \beta}{V_{CQ}}$ assume $V_T = 26mV$

$$r_\pi = \frac{26 \times 10^{-3} \times 100}{0.35 \times 10^{-3}} = 7.43 K\Omega$$

$$r_0 = \frac{V_A}{I_{CQ}} = \frac{100}{0.35 \times 10^{-3}} = 285.7 K\Omega$$

$$g_m = \frac{I_{CQ}}{V_T} = \frac{0.35\, mA}{26 \times 10^{-3} V} = 13.46\, mA/V$$

SOLUTION



Small signal equivalent

Voltage gain $A_V = \frac{V_o}{V_b} = \frac{-g_m V_\pi (r_o \parallel R_C)}{V_b}$ But $V_b = V_\pi$

$\therefore A_V = -g_m (r_o \parallel R_C) = -13.46 [285.7K \parallel 6.37K] = \underline{-83.87}$

$A_{VS} = \frac{V_o}{V_s} = \frac{R_i}{R_i + R_s} \cdot A_V$ where $R_i = R_B \parallel r_\pi$

$= 10k \parallel 7.43K$

$= 4.26 K\Omega$

$A_{VS} = \frac{v_o}{v_i} = \frac{4.26}{4.26 + 0.1} \times -83.87 = \underline{-81.94}$

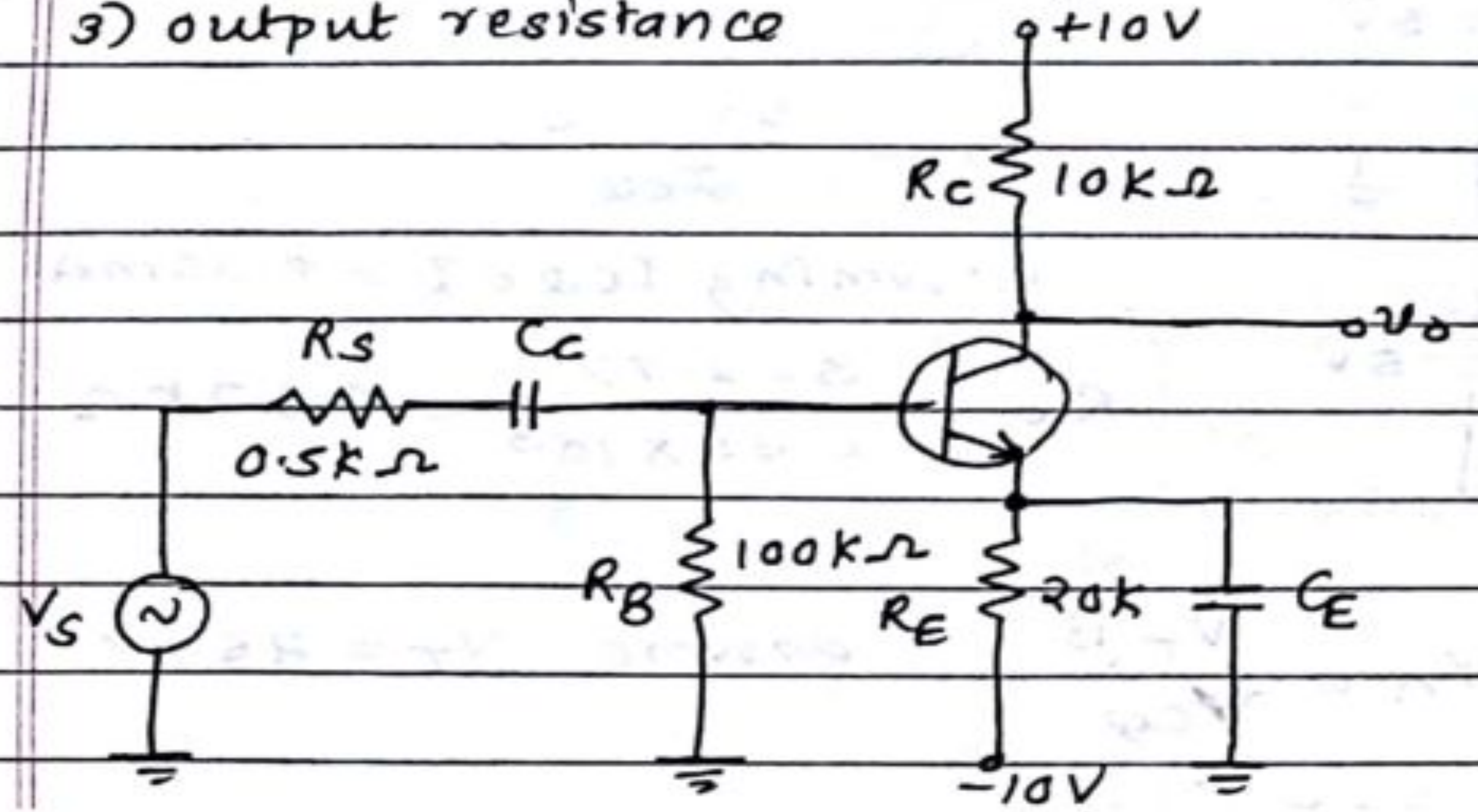
EXAMPLE 3

Ex ③ For the circuit shown in fig, let $\beta = 100$, $V_A = 100V$, $V_{BE(ON)} = 0.7V$

determine 1) small signal voltage gain

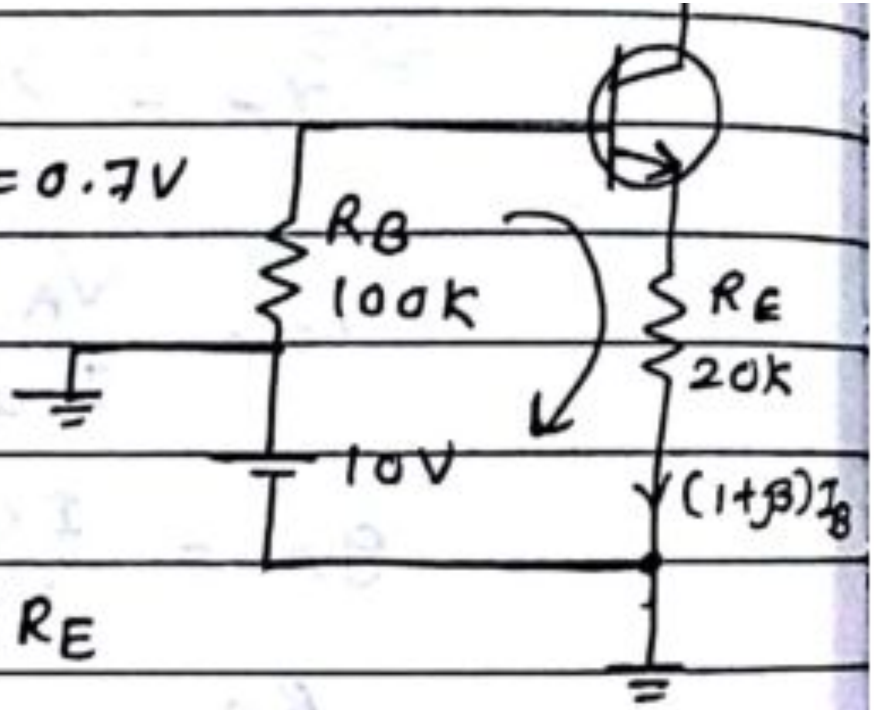
2) Input resistance seen by the signal source

3) output resistance



SOLUTION

Sol^n:- given $\beta = 100$, $V_A = 100V$, $V_{BE(ON)} = 0.7V$



DC Analysis -

① find I_{CQ} -

Apply KVL to Base loop,

$$10V = I_B R_B + V_{BE} + (1+\beta) I_B R_E$$

$$I_B = \frac{10 - V_{BE}}{R_B + (1+\beta) R_E} = \frac{10 - 0.7}{100k + (101 \times 20k)} =$$

$$I_B = 4.38\,\mu A$$

$$I_{CQ} = \beta I_B = 100 \times 4.38 \times 10^{-6} = \underline{0.438\,mA}$$

SOLUTION

step 2 calculate g_m r_π & r_o -

$$r_\pi = \frac{V_T \beta}{I_{CQ}} = \frac{26 \times 100}{0.438} = 5.94\,k\Omega$$

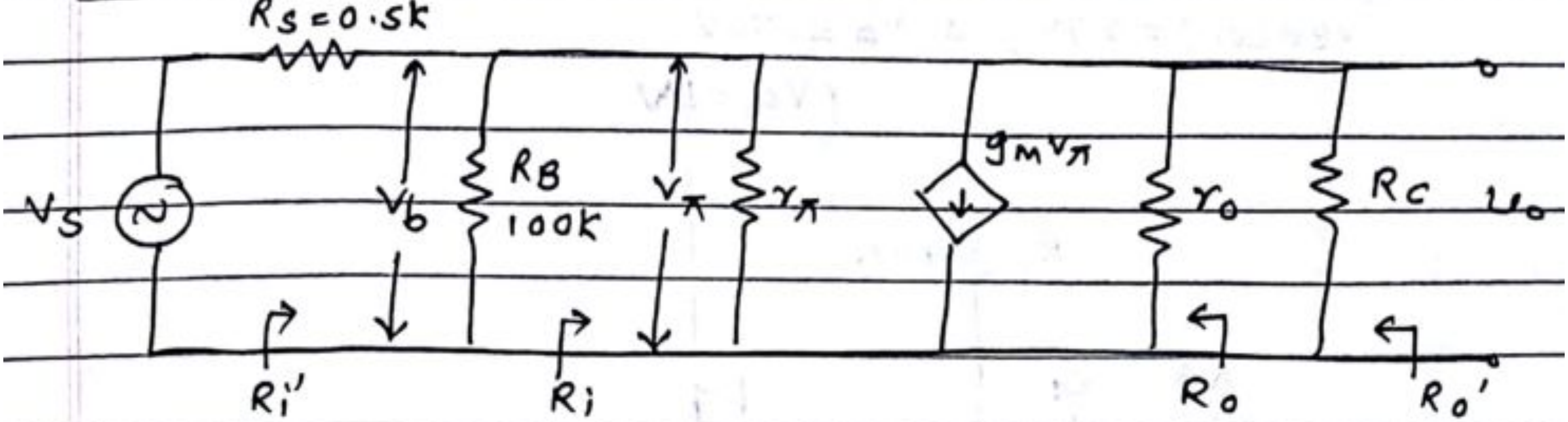
$$g_m = \frac{I_{CQ}}{V_T} = \frac{0.438}{26 \times 10^{-3}} = 16.85\,mA/V$$

$$r_o = \frac{V_A}{I_{CQ}} = \frac{100}{0.438 \times 10^{-3}} = 228.3\,k\Omega$$

SOLUTION

AC Analysis -

Step ③ Draw hybrid π equivalent ckt



i/p resistance - $R_i = r_\pi = 5.94\,k\Omega$

$R_i' = R_i \| R_B = 5.94k \| 100k = 5.6\,k\Omega$

SOLUTION

step ④ Voltage gain (A_{Vs}) –

$$A_{Vs} = \frac{V_o}{V_s} = \frac{V_o}{V_\pi} \times \frac{V_\pi}{V_s}$$

$$V_o = -g_m V_\pi (r_o \parallel R_c)$$

$$\frac{V_o}{V_\pi} = -g_m (r_o \parallel R_c)$$

$$V_\pi = \frac{R_i'}{R_s + R_i'} \cdot V_s$$

$$\frac{V_\pi}{V_s} = \frac{R_i'}{R_s + R_i'}$$

$$A_{Vs} = -g_m (r_o \parallel R_c) \times \frac{R_i'}{R_i' + R_s}$$

$$= -16.85 (228.3K \parallel 10K) \frac{5.6}{(5.6 + 0.5)}$$

$$\boxed{A_{Vs} = -148.2}$$

SOLUTION

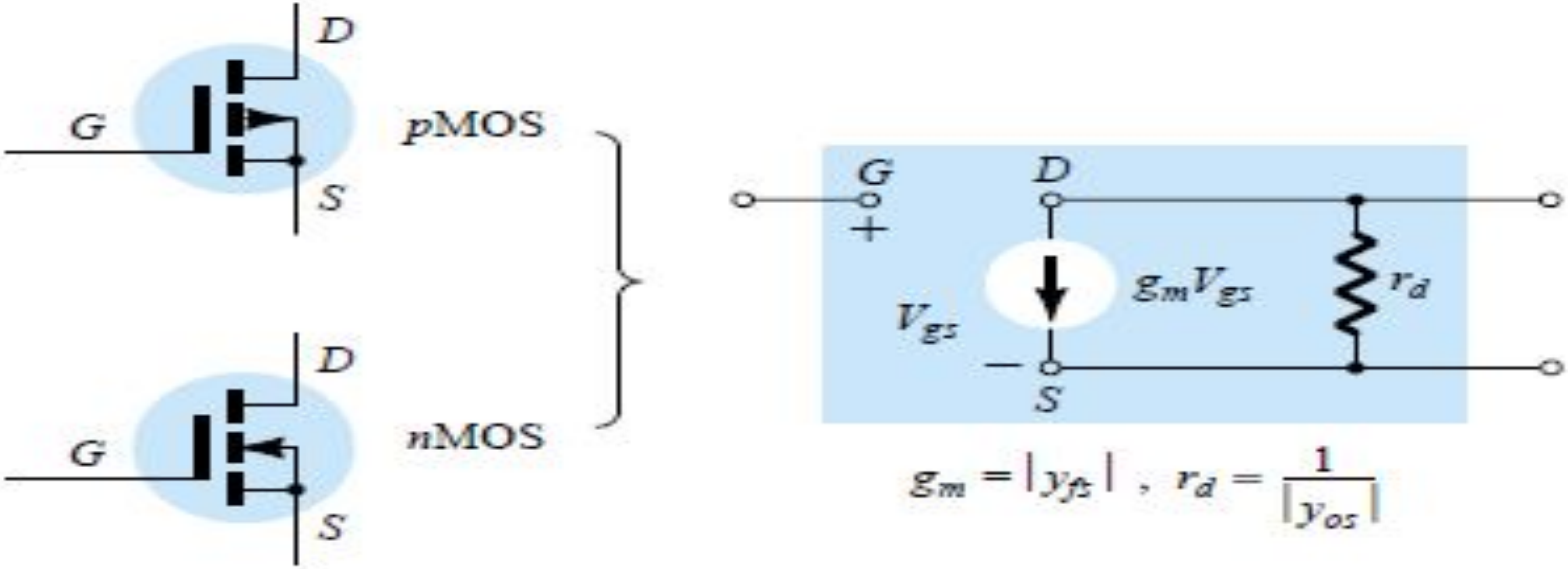
Step 5 <u>output Resistance</u>-

$$R_o = r_o = 228.3k\Omega$$

$$R_o' = r_o \parallel R_C = 228.3k \parallel 10k$$

$$\boxed{R_o' = 9.58k\Omega}$$

HYBRID PI MODEL OF EMOSFET



$$g_m = |y_{fs}|\ ,\ r_d = \frac{1}{|y_{os}|}$$

Figure Enhancement MOSFET ac small-signal model.

There is an output impedance from drain to source r_d, which is usually provided on specification sheets as an admittance y_{os}. The device transconductance, g_m, is provided on specification sheets as the forward transfer admittance, y_{fs}.

HYBRID PI MODEL OF EMOSFET

For E-MOSFETs, the relationship between output current and controlling voltage is defined by

$$I_D = k(V_{GS} - V_{GS(\mathrm{Th})})^2$$

Since g_m is still defined by

$$g_m = \frac{\Delta I_D}{\Delta V_{GS}}$$

we can take the derivative of the transfer equation to determine g_m as an operating point. That is,

$$g_m = \frac{dI_D}{dV_{GS}} = \frac{d}{dV_{GS}} k(V_{GS} - V_{GS(\mathrm{Th})})^2 = k \frac{d}{dV_{GS}} (V_{GS} - V_{GS(\mathrm{Th})})^2$$

$$= 2k(V_{GS} - V_{GS(\mathrm{Th})}) \frac{d}{dV_{GS}} (V_{GS} - V_{GS(\mathrm{Th})}) = 2k(V_{GS} - V_{GS(\mathrm{Th})})(1 - 0)$$

and

$$\boxed{g_m = 2k(V_{GS_Q} - V_{GS(\mathrm{Th})})}$$

SMALL SIGNAL ANALYSIS OF CS EMOSFET WITH DRAIN FEEDBACK CONFIGURATION

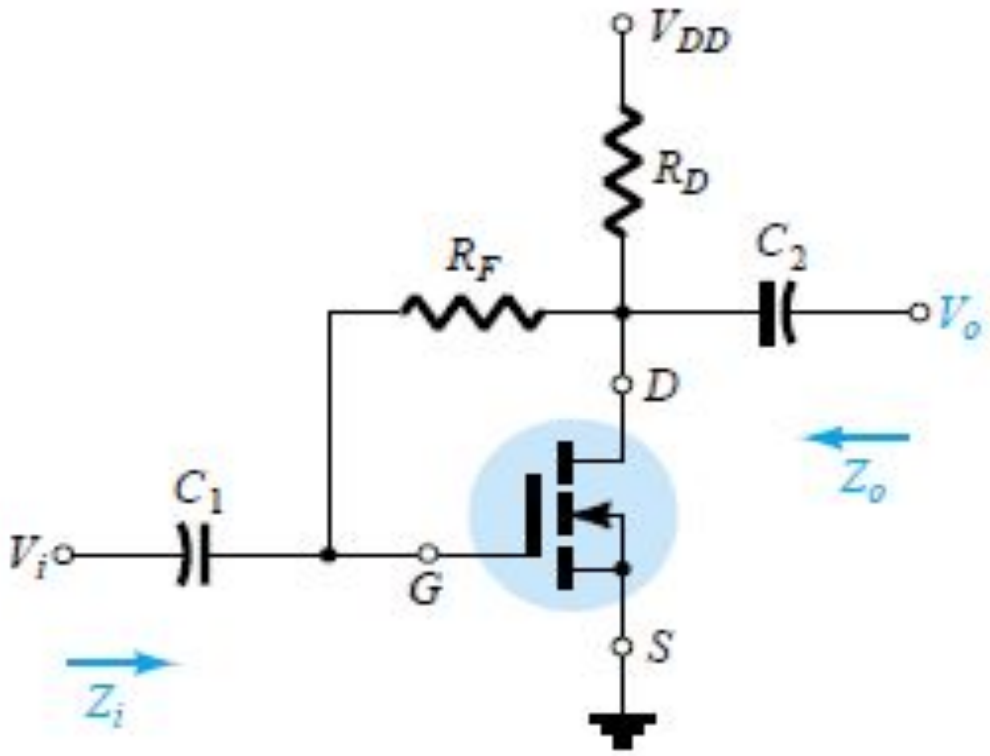


Figure 9.37 E-MOSFET drain-feedback configuration.

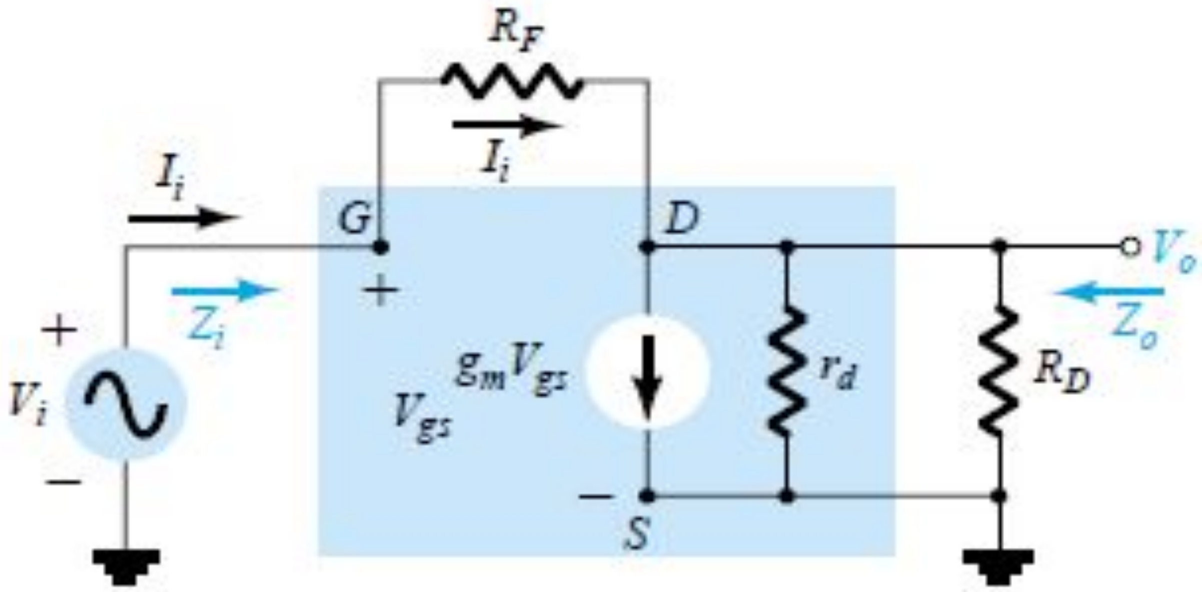


Figure 9.38 AC equivalent of the network of Fig. 9.37.

Substituting the ac equivalent model for the device will result in the network of Fig. 9.38. Note that R_F is not within the shaded area defining the equivalent model of the device but does provide a direct connection between input and output circuits.

SMALL SIGNAL ANALYSIS OF CS EMOSFET WITH DRAIN FEEDBACK CONFIGURATION

Input Impedance

Z_i: Applying Kirchhoff's current law to the output circuit (at node D in Fig. 9.38) results in

$$I_i = g_m V_{gs} + \frac{V_o}{r_d \| R_D}$$

and
$$V_{gs} = V_i$$

so that
$$I_i = g_m V_i + \frac{V_o}{r_d \| R_D}$$

or
$$I_i - g_m V_i = \frac{V_o}{r_d \| R_D}$$

Therefore,
$$V_o = (r_d \| R_D)(I_i - g_m V_i)$$

SMALL SIGNAL ANALYSIS OF CS EMOSFET WITH DRAIN FEEDBACK CONFIGURATION

Input Impedance

with $$I_i = \frac{V_i - V_o}{R_F} = \frac{V_i - (r_d \| R_D)(I_i - g_m V_i)}{R_F}$$

and $$I_i R_F = V_i - (r_d \| R_D) I_i + (r_d \| R_D) g_m V_i$$

so that $$V_i[1 + g_m(r_d \| R_D)] = I_i[R_F + r_d \| R_D]$$

and finally, $$\boxed{Z_i = \frac{V_i}{I_i} = \frac{R_F + r_d \| R_D}{1 + g_m(r_d \| R_D)}}$$

Typically, $R_F \gg r_d \| R_D$, so that

$$Z_i \cong \frac{R_F}{1 + g_m(r_d \| R_D)}$$

For $r_d \geq 10R_D$,

$$\boxed{Z_i \cong \frac{R_F}{1 + g_m R_D}}$$

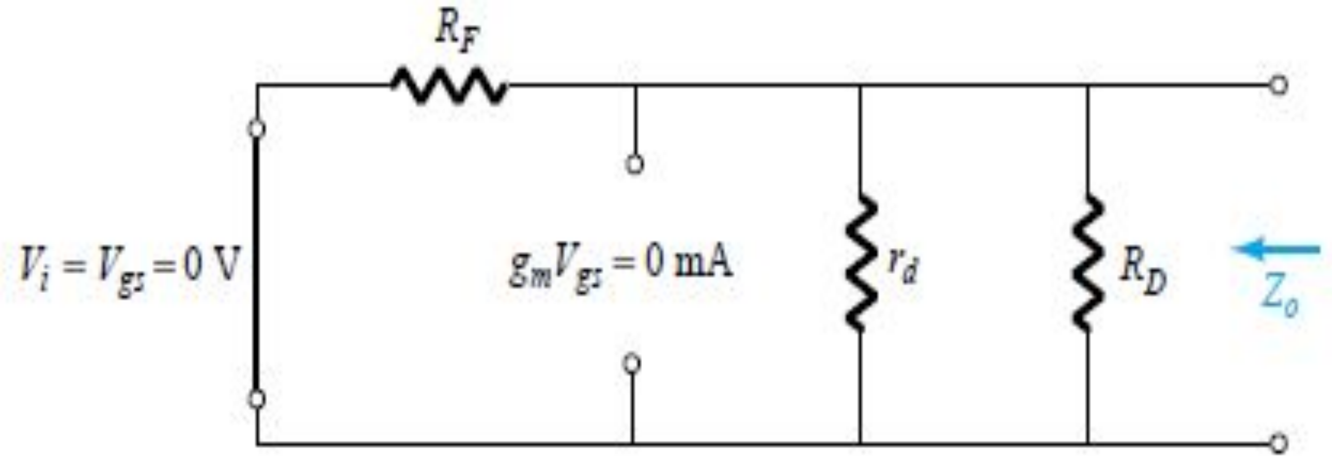
$R_F \gg r_d \| R_D$, $r_d \geq 10R_D$

SMALL SIGNAL ANALYSIS OF CS EMOSFET WITH DRAIN FEEDBACK CONFIGURATION

Output Impedance

Z_o: Substituting $V_i = 0$ V will result in $V_{gs} = 0$ V and $g_m V_{gs} = 0$, with a short-circuit path from gate to ground as shown in Fig. 9.39. R_F, r_d, and R_D are then in parallel and

$$\boxed{Z_o = R_F \| r_d \| R_D}$$



Determining Z_o for the network of Fig. 9.37.

Normally, R_F is so much larger than $r_d \| R_D$ that

$$Z_o \cong r_d \| R_D$$

nd with $r_d \geq 10R_D$,

$$\boxed{Z_o \cong R_D}_{R_F \gg r_d \| R_D,\ r_d \geq 10R_D}$$

Small Signal Analysis of CS EMOSFET with Drain Feedback Configuration

Voltage Gain

A_v: Applying Kirchhoff's current law at node D of Fig. 9.38 will result in

$$I_i = g_m V_{gs} + \frac{V_o}{r_d \| R_D}$$

but $$V_{gs} = V_i \text{ and } I_i = \frac{V_i - V_o}{R_F}$$

so that $$\frac{V_i - V_o}{R_F} = g_m V_i + \frac{V_o}{r_d \| R_D}$$

and $$\frac{V_i}{R_F} - \frac{V_o}{R_F} = g_m V_i + \frac{V_o}{r_d \| R_D}$$

so that $$V_o\left[\frac{1}{r_d \| R_D} + \frac{1}{R_F}\right] = V_i\left[\frac{1}{R_F} - g_m\right]$$

SMALL SIGNAL ANALYSIS OF CS EMOSFET WITH DRAIN FEEDBACK CONFIGURATION

Voltage Gain

$$A_v = \frac{V_o}{V_i} = \frac{\left[\frac{1}{R_F} - g_m\right]}{\left[\frac{1}{r_d \| R_D} + \frac{1}{R_F}\right]}$$

but

$$\frac{1}{r_d \| R_D} + \frac{1}{R_F} = \frac{1}{R_F \| r_d \| R_D}$$

and

$$g_m \gg \frac{1}{R_F}$$

so that

$$\boxed{A_v = -g_m(R_F \| r_d \| R_D)}$$

Since R_F is usually >> $r_d \| R_D$ and if $r_d \geq 10R_D$,

$$\boxed{A_v \cong -g_m R_D} \quad R_F \gg r_d \| R_D,\ r_d \geq 10R_D$$

Phase Relationship: The negative sign for A_v reveals that V_o and V_i are out of phase by 180°.

EXAMPLE 1

$k = 0.24 \times 10^{-3}$ A/V^2, $V_{GS_Q} = 6.4$ V, and $I_{D_Q} = 2.75$ mA.

(a) Determine g_m.
(b) Find r_d.
(c) Calculate Z_i with and without r_d. Compare results.
(d) Find Z_o with and without r_d. Compare results.
(e) Find A_v with and without r_d. Compare results.

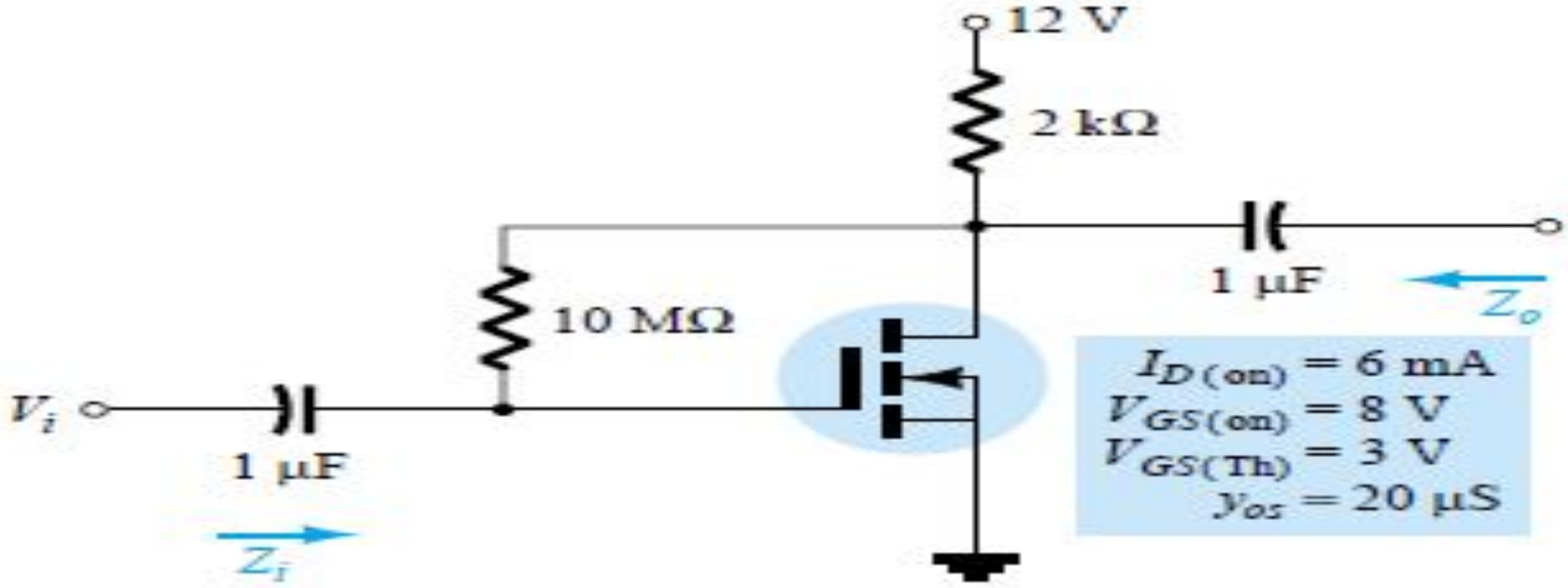


Figure 9.40 Drain-feedback amplifier

SOLUTION

(a) $g_m = 2k(V_{GS_Q} - V_{GS(\text{Th})}) = 2(0.24 \times 10^{-3}\ \text{A/V}^2)(6.4\ \text{V} - 3\ \text{V})$
$= \mathbf{1.63\ mS}$

(b) $r_d = \dfrac{1}{y_{os}} = \dfrac{1}{20\ \mu\text{S}} = \mathbf{50\ k\Omega}$

(c) With r_d:

$$Z_i = \frac{R_F + r_d \| R_D}{1 + g_m(r_d \| R_D)} = \frac{10\ \text{M}\Omega + 50\ \text{k}\Omega \| 2\ \text{k}\Omega}{1 + (1.63\ \text{mS})(50\ \text{k}\Omega \| 2\ \text{k}\Omega)}$$
$$= \frac{10\ \text{M}\Omega + 1.92\ \text{k}\Omega}{1 + 3.13} = \mathbf{2.42\ M\Omega}$$

SOLUTION

Without r_d:

$$Z_i \cong \frac{R_F}{1 + g_m R_D} = \frac{10\ \text{M}\Omega}{1 + (1.63\ \text{mS})(2\ \text{k}\Omega)} = \mathbf{2.53\ M\Omega}$$

revealing that since the condition $r_d \geq 10R_D = 50\ \text{k}\Omega \geq 40\ \text{k}\Omega$ is satisfied, the results for Z_o with or without r_d will be quite close.

(d) With r_d:

$$\begin{aligned} Z_o &= R_F \| r_d \| R_D = 10\ \text{M}\Omega \| 50\ \text{k}\Omega \| 2\ \text{k}\Omega = 49.75\ \text{k}\Omega \| 2\ \text{k}\Omega \\ &= \mathbf{1.92\ k\Omega} \end{aligned}$$

Without r_d:

$$Z_o \cong R_D = \mathbf{2\ k\Omega}$$

again providing very close results.

SOLUTION

(e) With r_d:

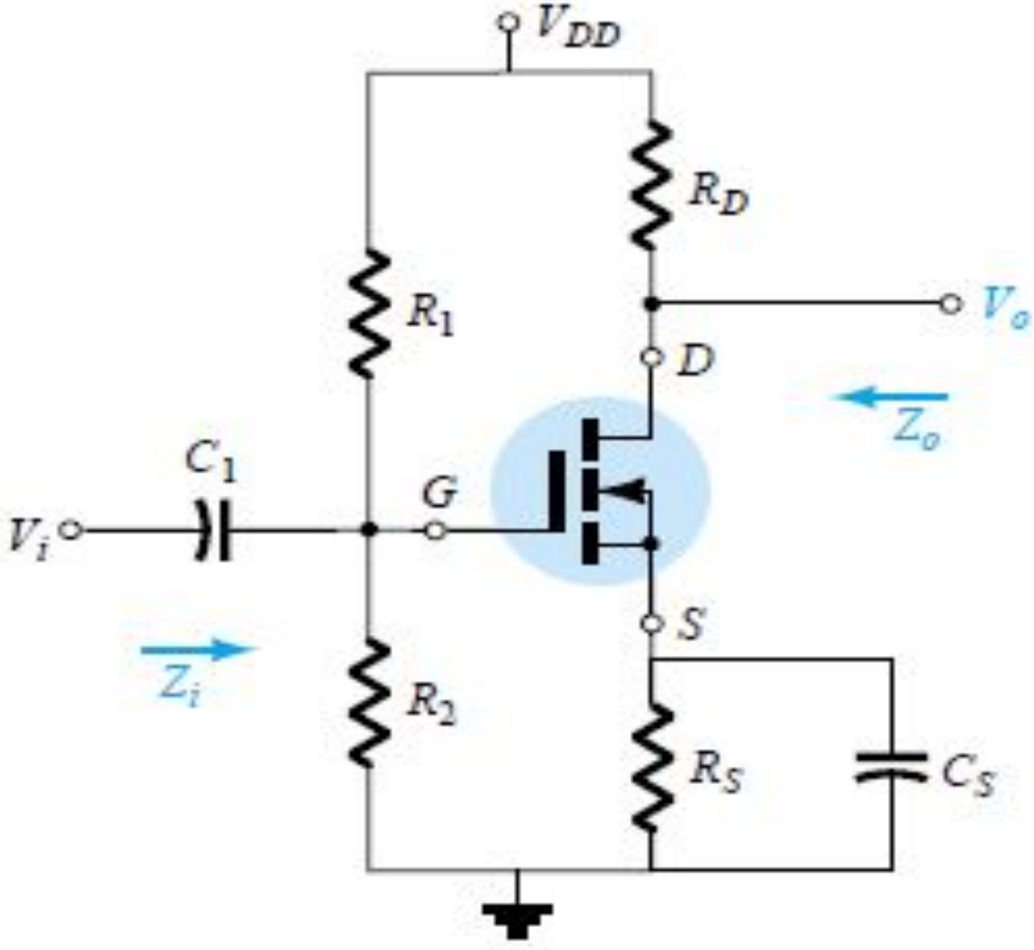
$$\begin{aligned} A_v &= -g_m(R_F \| r_d \| R_D) \\ &= -(1.63 \text{ mS})(10 \text{ M}\Omega \| 50 \text{ k}\Omega \| 2 \text{ k}\Omega) \\ &= -(1.63 \text{ mS})(1.92 \text{ k}\Omega) \\ &= \mathbf{-3.21} \end{aligned}$$

Without r_d:

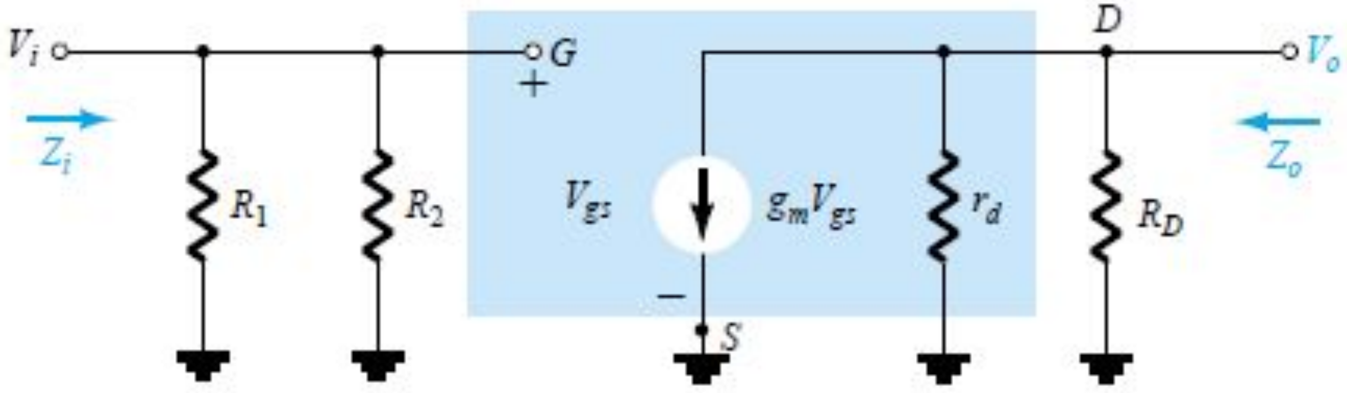
$$\begin{aligned} A_v &= -g_m R_D = -(1.63 \text{ mS})(2 \text{ k}\Omega) \\ &= \mathbf{-3.26} \end{aligned}$$

which is very close to the above result.

Small Signal Analysis of CS EMOSFET with Voltage Divider Configuration



E-MOSFET
voltage-divider configuration.



AC equivalent network for the configuration of Fig.

SMALL SIGNAL ANALYSIS OF CS EMOSFET WITH VOLTAGE DIVIDER CONFIGURATION

Z_i:

$$\boxed{Z_i = R_1 \| R_2}$$

Z_o:

$$\boxed{Z_o = r_d \| R_D}$$

For $r_d \geq 10R_D$,

$$\boxed{Z_o \cong R_D}_{r_d \geq 10R_D}$$

A_v:

$$\boxed{A_v = \frac{V_o}{V_i} = -g_m(r_D \| R_D)}$$

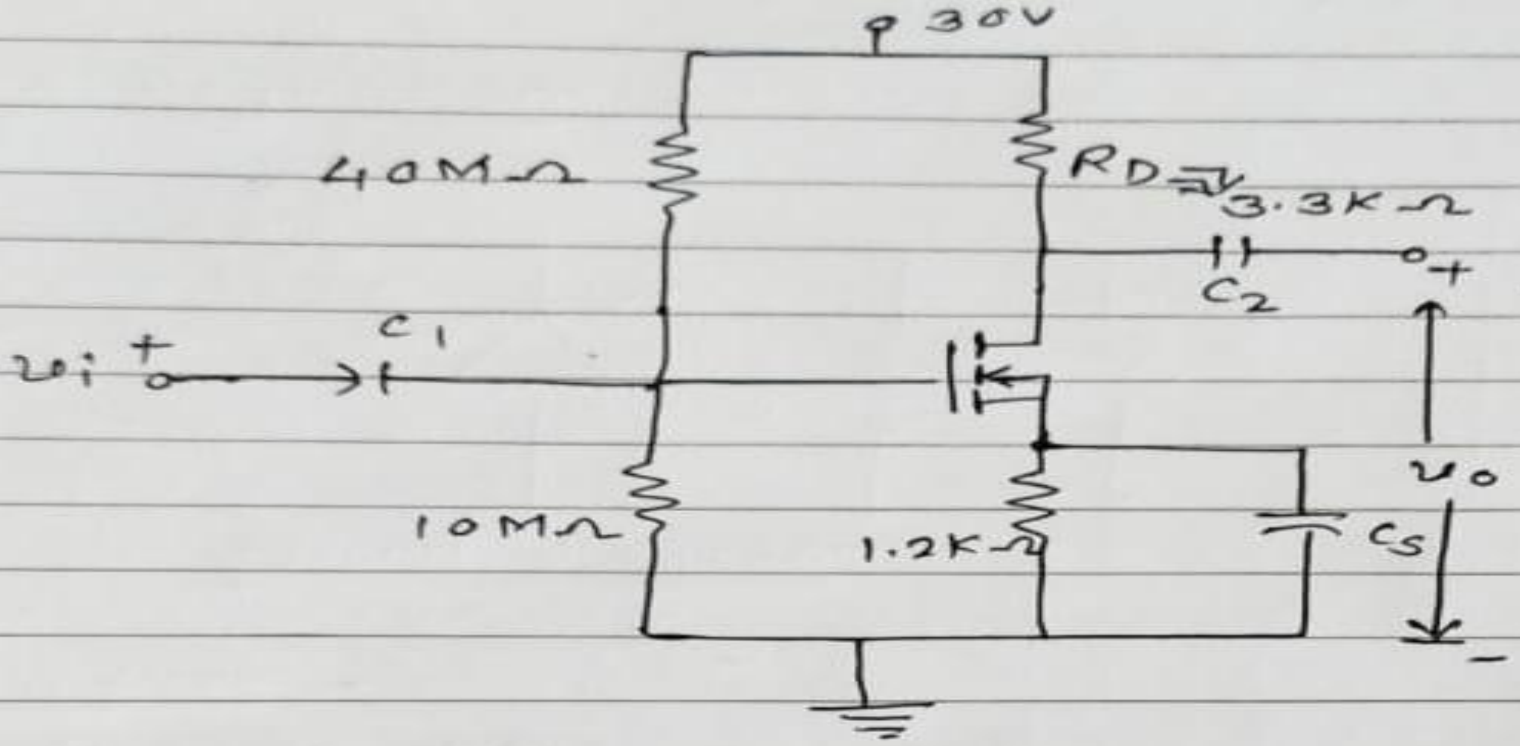
and if $r_d \geq 10R_D$,

$$\boxed{A_v = \frac{V_o}{V_i} \cong -g_m R_D}$$

classmate

Date ______
Page ______

* Determine the output voltage for network given below. If $V_i = 0.8\,mV$ & $r_d = 40\,k\Omega$



$V_{GS(Th)} = 3V$

$K = 0.4 \times 10^{-3}$

<u>solution</u> - <u>Given</u> -

$R_1 = 40\,M\Omega$ $R_D = 3.3\,k\Omega$

$R_2 = 10\,M\Omega$ $R_S = 1.2\,k\Omega$

$r_d = 40\,k\Omega$ $V_i = 0.8\,mV$

$V_{GS(Th)} = 3V$ $K = 0.4 \times 10^{-3}$

o/p voltage $V_o = A_V \cdot V_i$

& $A_V = -g_m (r_d \parallel R_D)$

& $g_m = 2K (V_{GSQ} - V_{GS(Th)})$ — (1)

$$V_G = \frac{R_2}{R_1 + R_2} \times V_{DD} = \frac{10 \times 10^6}{50 \times 10^6} \times 30 = 6V$$

$$V_{GS} = V_G - I_D R_S$$

$$V_{GS} = 6 - I_D \times 1.2 \times 10^3$$

Solve quadratic equation using mathematical approach.

find $I_{DQ} = 1.7mA$ & $V_{GSQ} = 4.2V$ — Put in eqⁿ (1)

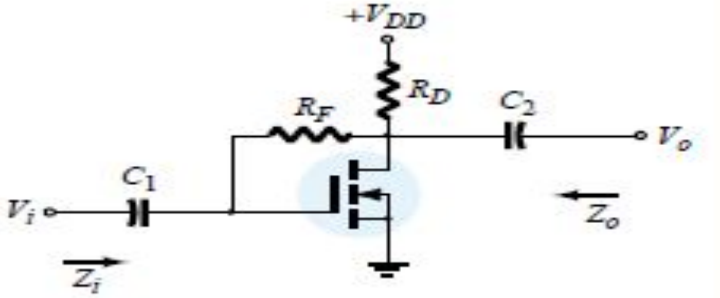
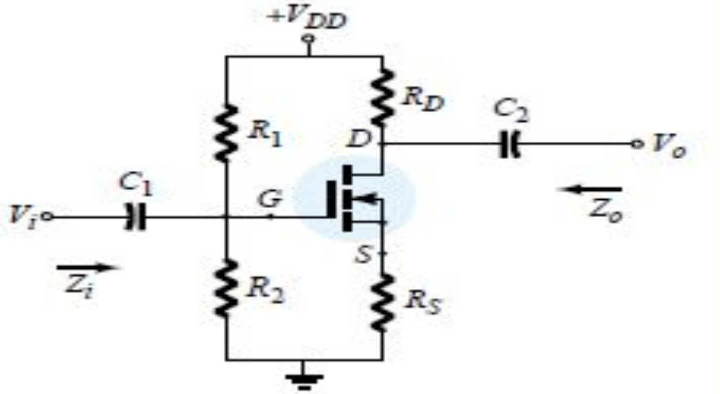
$g_m = 2 \times 0.4 \times 10^{-3} (4.2 - 3) = 1.336 \times 10^{-3}$

$A_V = -g_m (r_d \parallel R_D) = -4.072$ $\therefore V_o = A_V \times V_i$

$= -4.072 \times 0.8 mV$

$\boxed{V_o = 3.25 mV}$

Summary Table

Configuration	Z_i	Z_o	$A_v = \frac{V_o}{V_i}$
Drain-feedback bias **E-MOSFET** 	Medium (1 MΩ) $= \boxed{\frac{R_F + r_d \| R_D}{1 + g_m(r_d \| R_D)}}$ $\cong \boxed{\frac{R_F}{1 + g_m R_D}}$ $(r_d \geq 10\, R_D)$	Medium (2 kΩ) $= \boxed{R_F \| r_d \| R_D}$ $\cong \boxed{R_D}$ $(R_F, r_d \geq 10\, R_D)$	Medium (−10) $= \boxed{-g_m(R_F \| r_d \| R_D)}$ $\cong \boxed{-g_m R_D}$ $(R_F, r_d \geq 10\, R_D)$
Voltage-divider bias **E-MOSFET** 	Medium (1 MΩ) $= \boxed{R_1 \| R_2}$	Medium (2 kΩ) $= \boxed{R_D \| r_d}$ $\cong \boxed{R_D}$ $(r_d \geq 10\, R_D)$	Medium (−10) $= \boxed{-g_m(r_d \| R_D)}$ $\cong \boxed{-g_m R_D}$ $(r_d \geq 10\, R_D)$

Multistage Amplifiers

In many applications, a single amplifier cannot provide all the gains that is required to drive a particular kind of load.

- e.g. a loudspeaker represents a 'heavy' load (low R_L) in an audio amplifier system & several amplifier stages may be required to boost a signal originating at a microphone or magnetic tape head to a level sufficient to provide a large amount of power to the speaker.

- When the output of one amplifier stage is connected to the input of another amplifier, the amplifier stages are said to be in cascade.

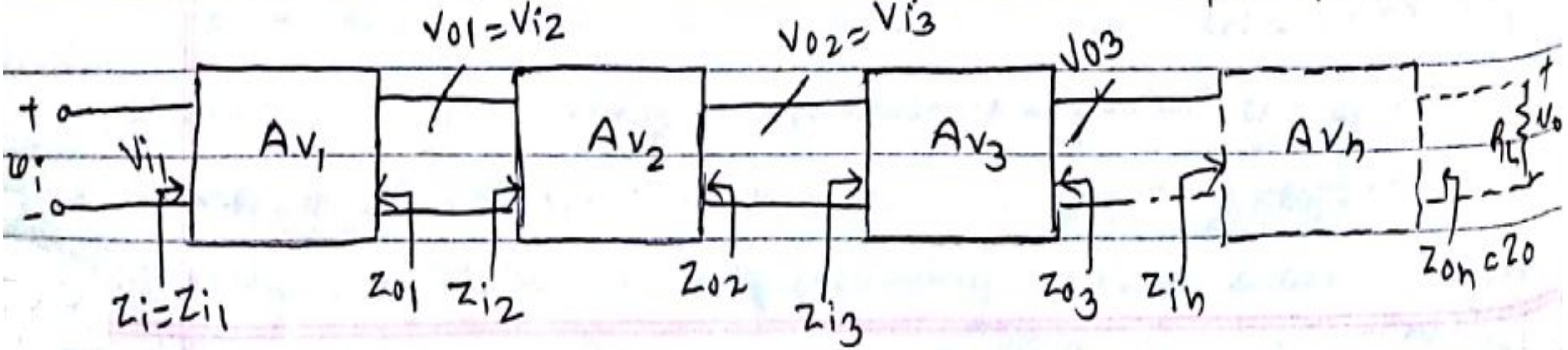
$\boxed{Z_i}$ - overall input impedance of a multistage amplifier = input impedance of the first stage.

Note: i/p stage is normally an FET amplifier or Darlington connected BJT amplifier for high i/p impedance applications.

$\boxed{Z_o}$ - overall output impedance of a multistage amplifier = output impedance of the last stage.

$\boxed{\text{Note}}$: The last stage is normally a common collector power stage or a CE transformer coupled power stage for driving a low resistance load such as a loudspeaker.

$Av_T = Av_1 \cdot Av_2 \cdot Av_3 \cdots$



Multistage Amplifiers

In many applications, a single amplifier cannot provide all the gains that is required to drive a particular kind of load.

- e.g. a loudspeaker represents a 'heavy' load (low R_L) in an audio amplifier system & several amplifier stages may be required to boost a signal originating at a microphone or magnetic tape head to a level sufficient to provide a large amount of power to the speaker.

- When the output of one amplifier stage is connected to the input of another amplifier, the amplifier stages are said to be in cascade.

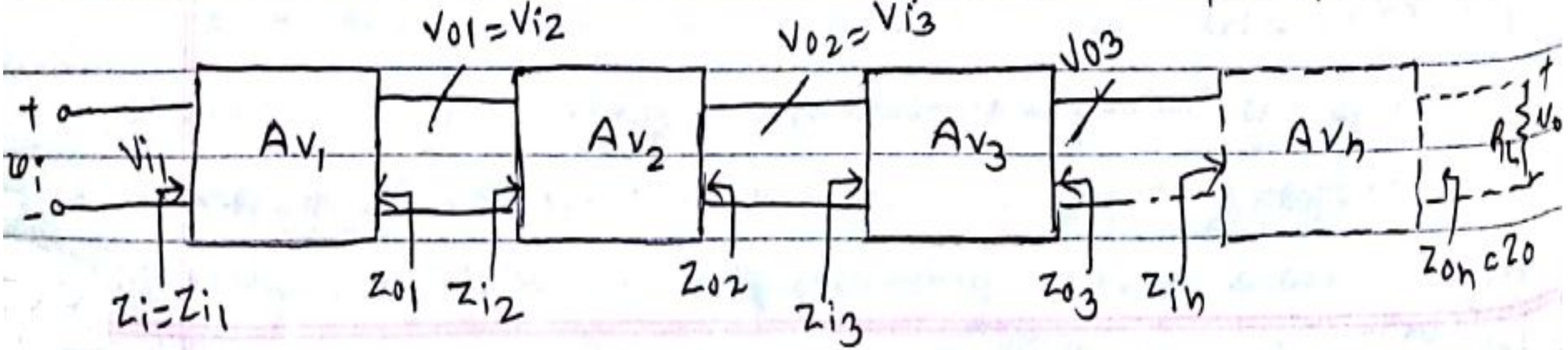
Z_i - overall input impedance of a multistage amplifier = input impedance of the first stage.

Note: i/p stage is normally an FET amplifier or Darlington connected BJT amplifier for high i/p impedance applications.

$\boxed{Z_o}$ - overall output impedance of a multistage amplifier = output impedance of the last stage.

$\boxed{\text{Note}}$: The last stage is normally a common collector power stage or a CE transformer coupled power stage for driving a low resistance load such as a loudspeaker.

$A_{V_T} = A_{V_1} \cdot A_{V_2} \cdot A_{V_3} \ldots$



Voltage Gain of a multistage Amplifier :-

If there are three stages cascaded,

$$A_v = \frac{v_o}{v_i} = \frac{v_{o3}}{v_{i_1}} = \frac{A_{v_3} \cdot v_{i_3}}{v_{i_1}}$$

$$= \frac{A_{v_3} \cdot v_{o2}}{v_{i_1}} = \frac{A_{v_3} \cdot A_{v_2} \cdot v_{i_2}}{v_{i_1}}$$

$$= \frac{A_{v_3} \cdot A_{v_2} \cdot v_{o1}}{v_{i_1}} = \frac{A_{v_3} \cdot A_{v_2} \cdot A_{v_1} \cdot \cancel{v_{i_1}}}{\cancel{v_{i_1}}}$$

$$A_v = A_{v_1} \cdot A_{v_2} \cdot A_{v_3}$$

$$\therefore \boxed{\frac{v_o}{v_s} = A_{v_s} = A_{v_1} \cdot A_{v_2} \cdot A_{v_3} \cdot \left(\frac{Z_i}{Z_i + R_s}\right)}$$

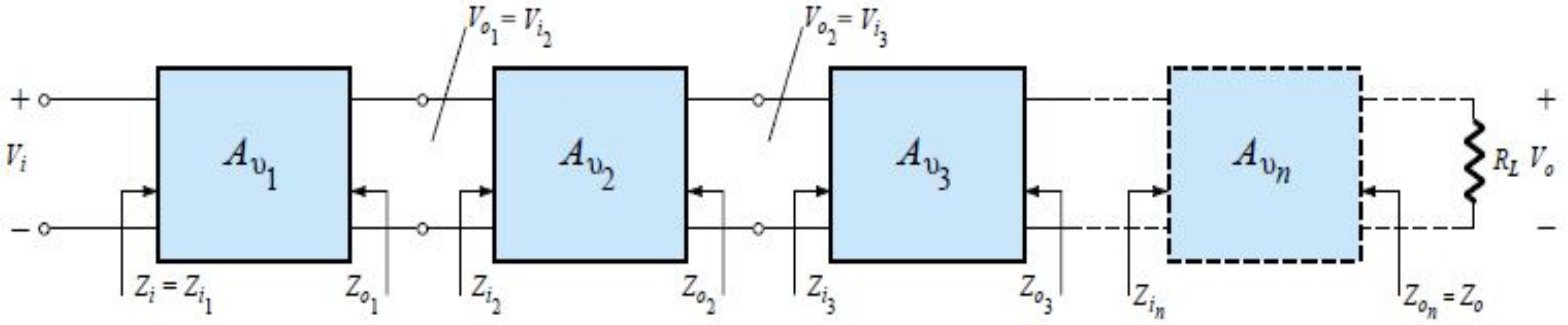
Where $A_{v_1} = g_{m_1} (Z_{o_1} \| Z_{i_2})$

$A_{v_2} = g_{m_2} (Z_{o_2} \| Z_{i_3})$

$A_{v_3} = g_{m_3} (Z_o \| R_L)$

NEED OF MULTISTAGE AMPLIFIERS

- The voltage gain or current gain obtained from single transistor amplifier is usually not sufficient for most of the applications.
- Hence several amplifier stages are connected in cascade. i.e connected such that the output of one stage forms input of the next stage. Such multistage amplifiers provide desired voltage or current gain.
- A multistage amplifier by cascading amplifiers is shown below:



REQUIREMENTS OF MULTISTAGE AMPLIFIER

Requirements of multistage amplifier

- Gain should be sufficiently high
- Input impedance should match with source impedance
- Output impedance should match with load resistance
- Bandwidth should be adequately large

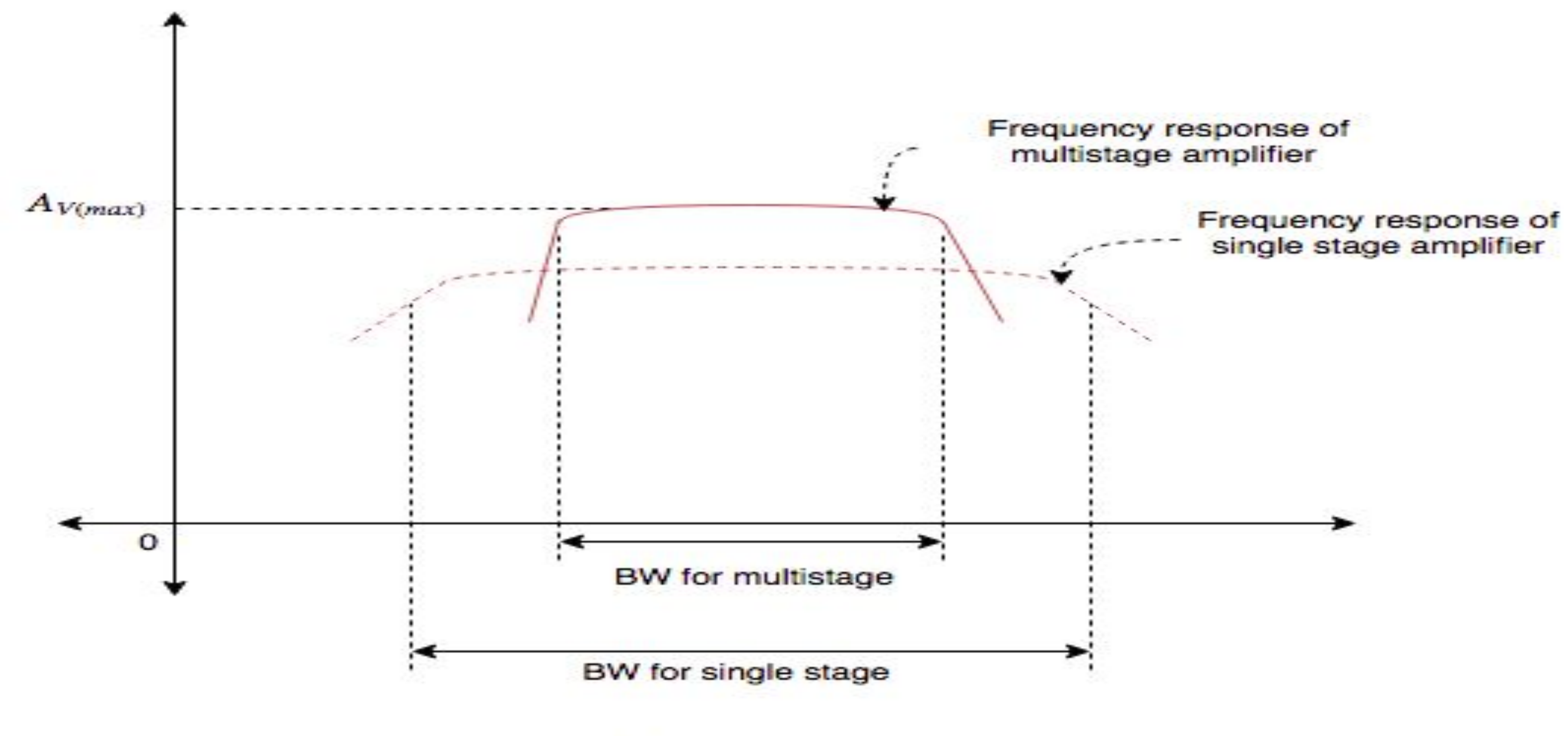
- In multistage amplifiers, total gain is the product of gains of individual stages

$$A = A_1 \times A_2 \times A_3 \times \ldots\ldots \times A_n$$

- The cascading of amplifiers increases the gain but it reduces bandwidth.

EFFECT OF CASCADING ON BANDWIDTH

- The cascading of amplifiers increases the gain but it reduces bandwidth.



Comparison of BW

* Advantages of Cascaded Multistage Amplifiers :-

① control over the input impedance :-

The i/p stage is usually required to provide a high i/p resistance in order to avoid loss of signal level when the amplifier is fed from a high resistanc voltage source.

In a differential amplifier, the i/p stage must also provide large common-mode rejection.

② control over the output impedance :-

The main function of the last (i.e o/p) stage of an amplifier is to provide a low o/p resistance (if o/p is a vtg signal) in order to avoid loss of gain when a low valued load resistance is connected to the amplifie

Also, the o/p stage should be able to supply the current required by the load in an efficient manner. i.e without dissipating an unduly large amount of power in the o/p transistors.

③ controlling the voltage gain, $A_v = A_{v1} \cdot A_{v2} \cdot A_{v3} \cdot \ldots$

The function of the middle (intermediate) stages of an amplifier cascade is to provide the bulk of the voltage gain.

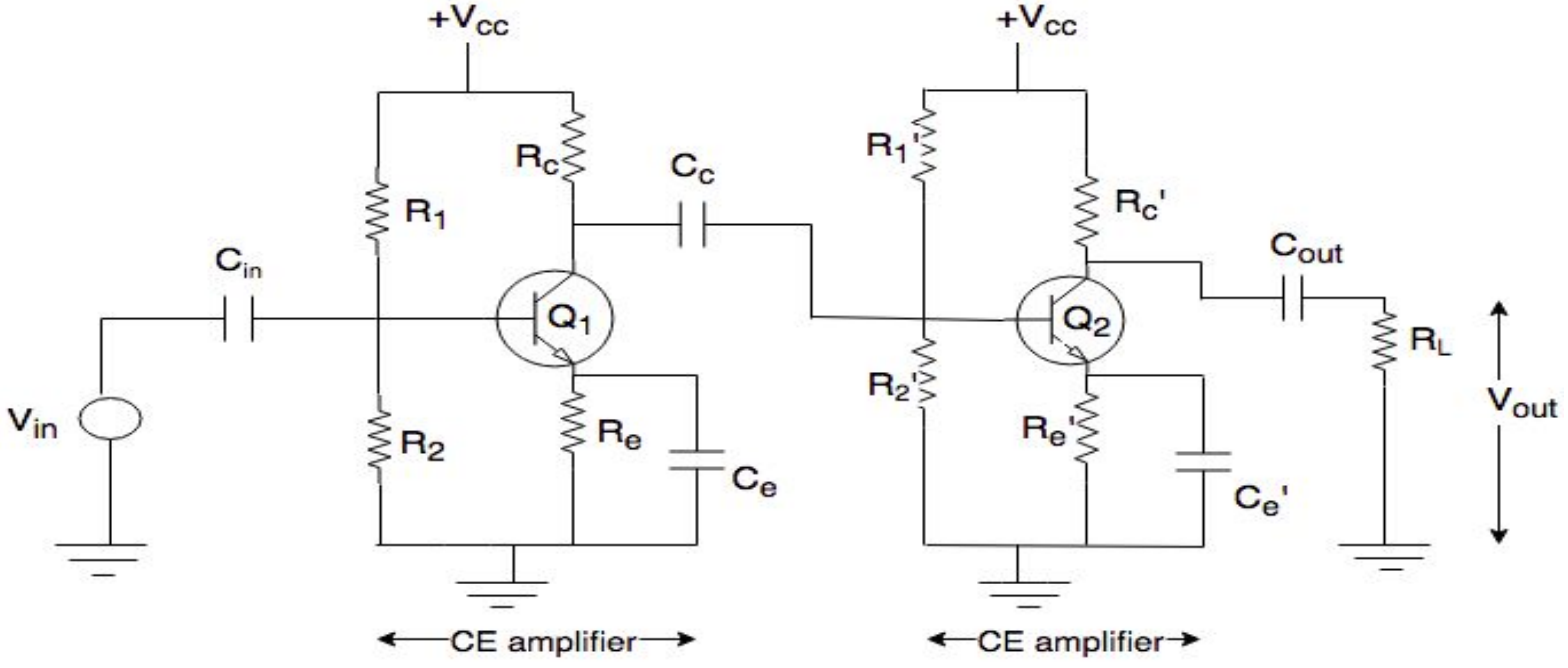
In addition, the middle stages provide such other functions as the conversion of the signal from differential mode to single ended mode & the shifting of the dc level of the signal.

④ Controlling the bandwidth :-
eg CE-CB or CS-CG configuration for wideband frequency applications.

* Types of coupling :-

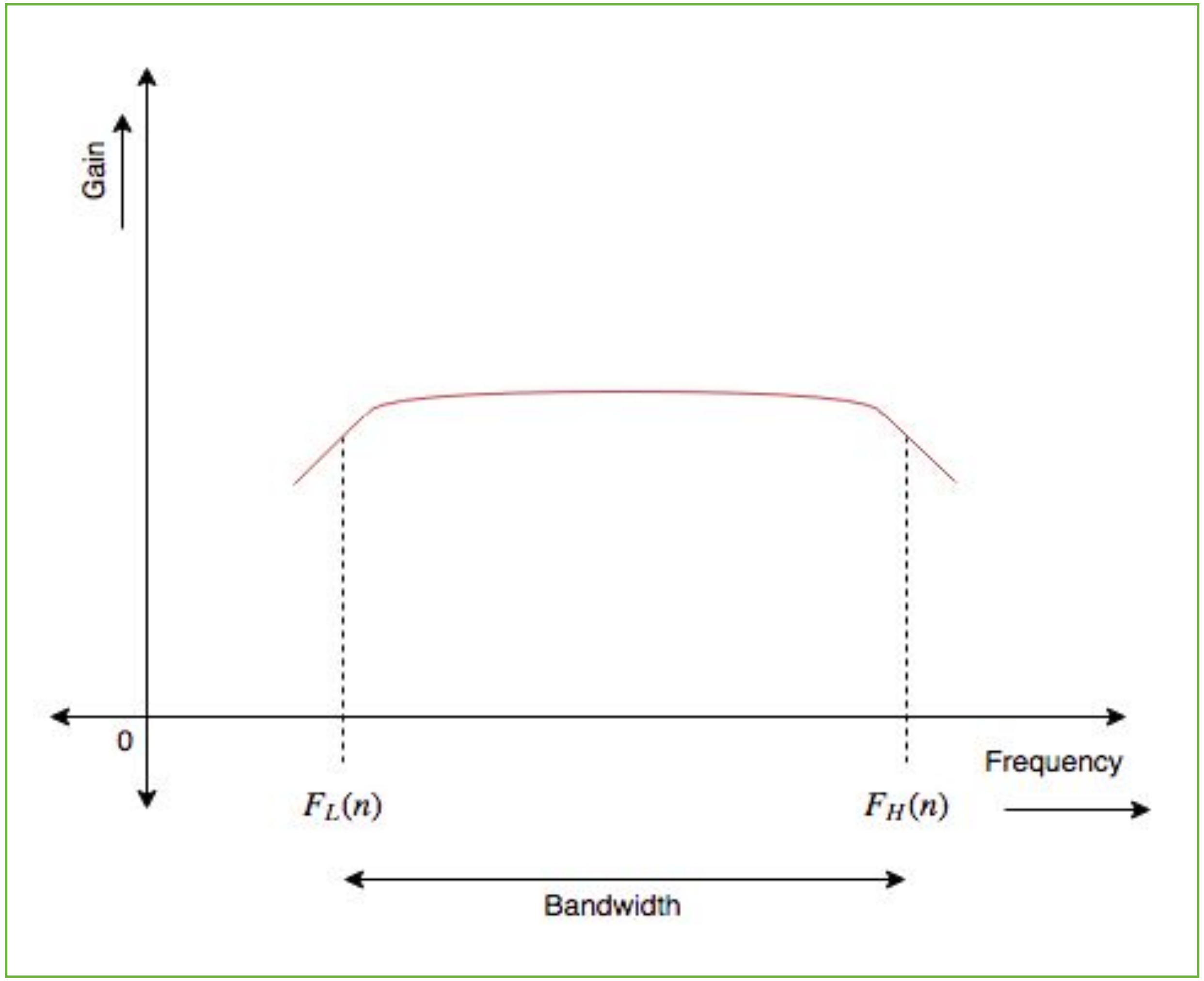
There are three types of coupling
① RC coupling
② Direct coupling
③ Transformer coupling

1. RC COUPLED



RC-coupled amplifier(2-stage)

1. RC COUPLED



Advantages:

- Wide frequency response
- Most convenient way of coupling
- Inexpensive way of coupling
- Provides less frequency distortion

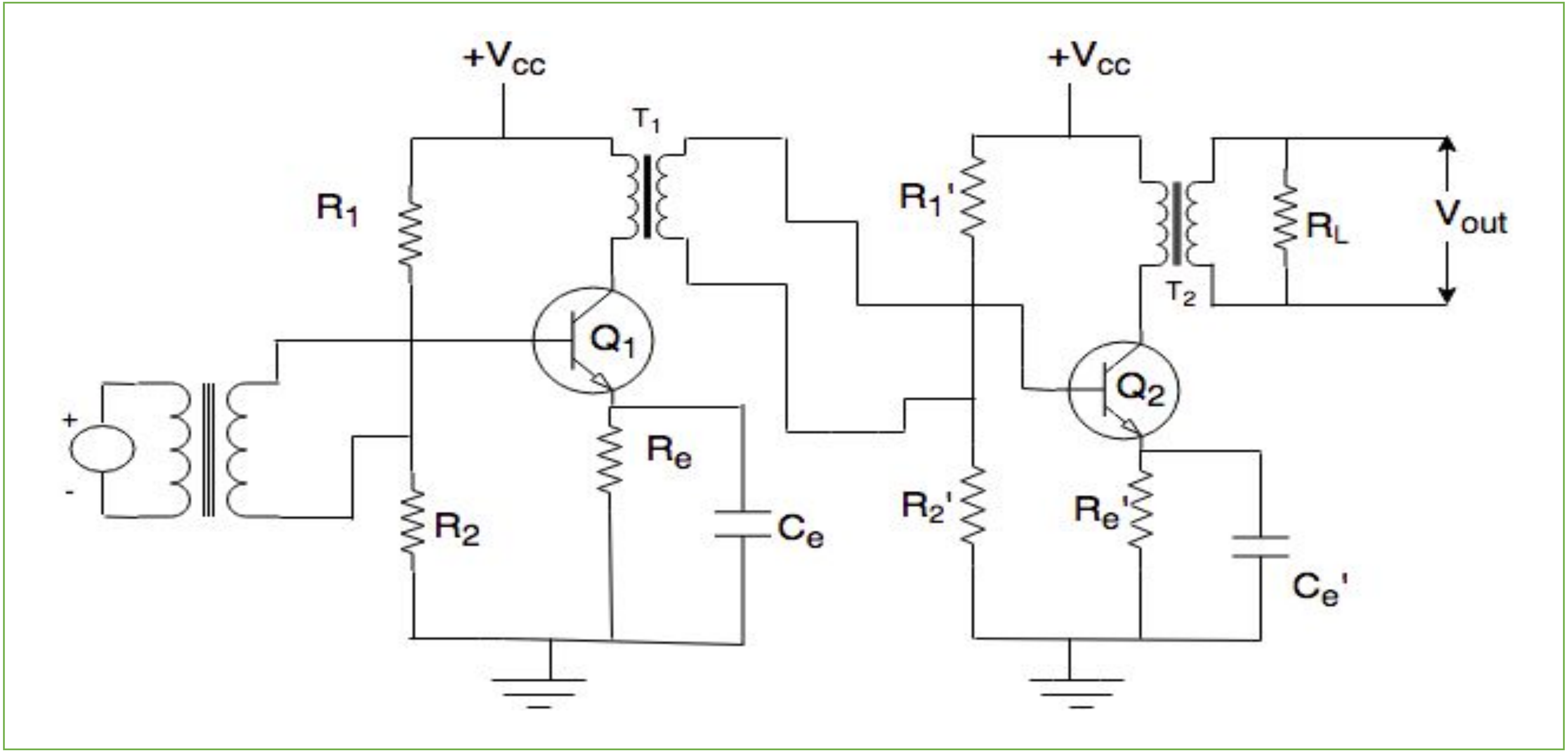
Disadvantages:

- Overall gain is less
- Tendency to become noisy with age.
- Poor impedance matching

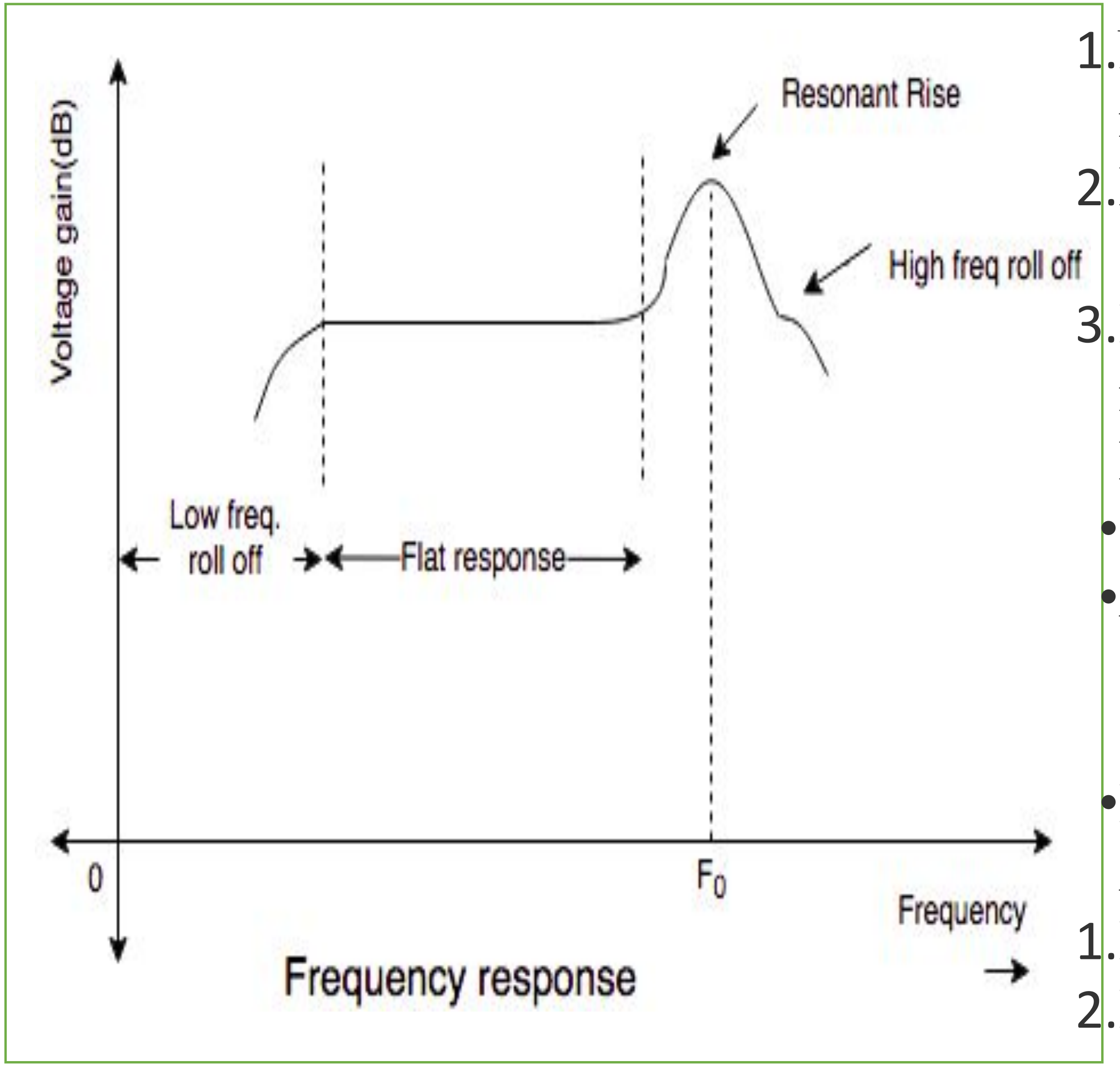
Applications:

- In P.A system
- T.V, VCR and CD players

2. TRANSFORMER COUPLED



2. Transformer Coupled



Advantages:

1. No signal power is lost in collector base resistor.
2. Provides higher voltage gain than RC coupled amplifier
3. It provides excellent resistance(or impedance) matching between the stages.

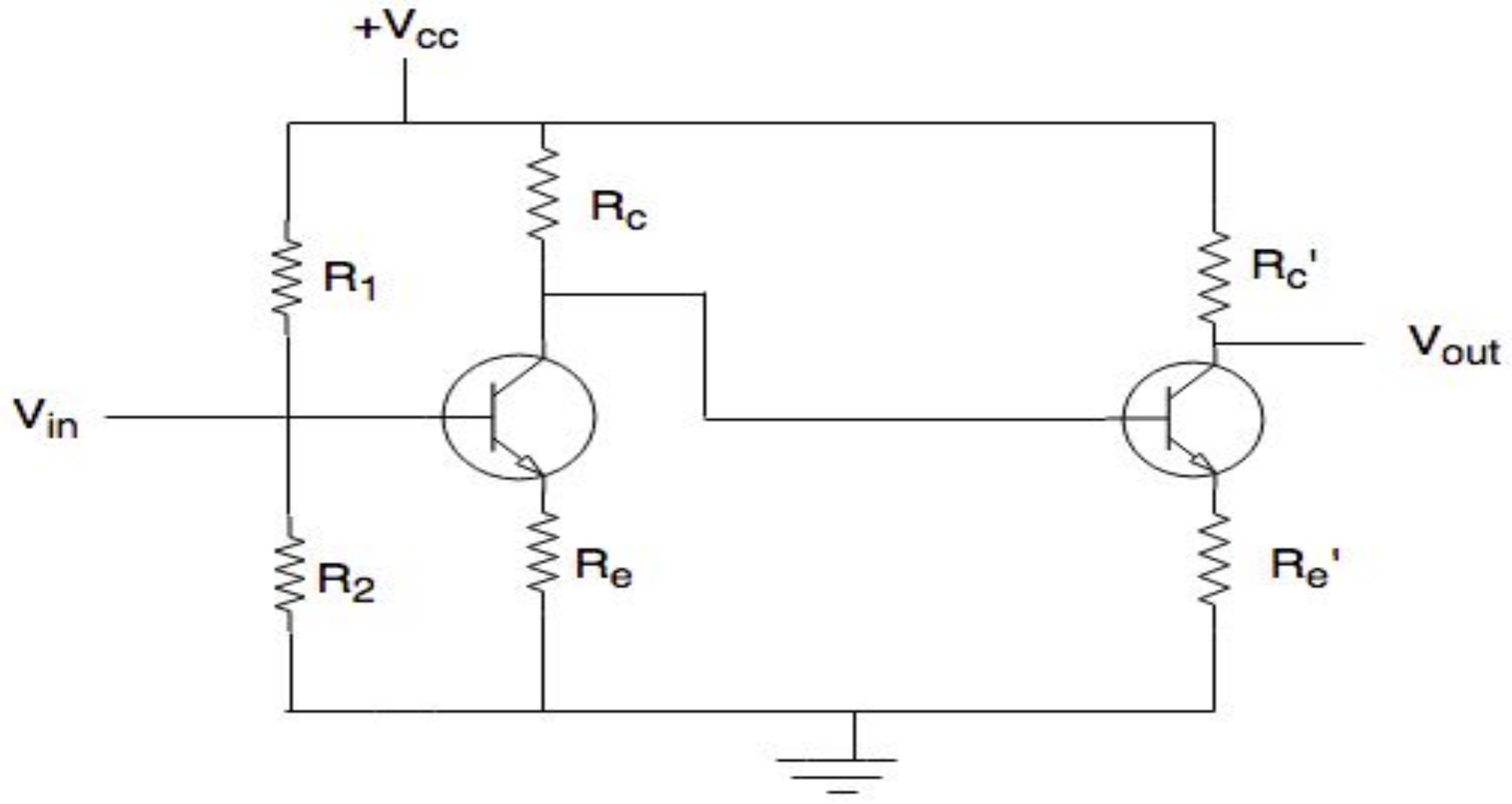
Disadvantages:

- Transformer coupling is expensive and bulky.
- At radio frequencies, winding inductances and distributed capacitors produces reverse frequency distortion.
- It tends to produce 'hum' in the circuit.

Applications:

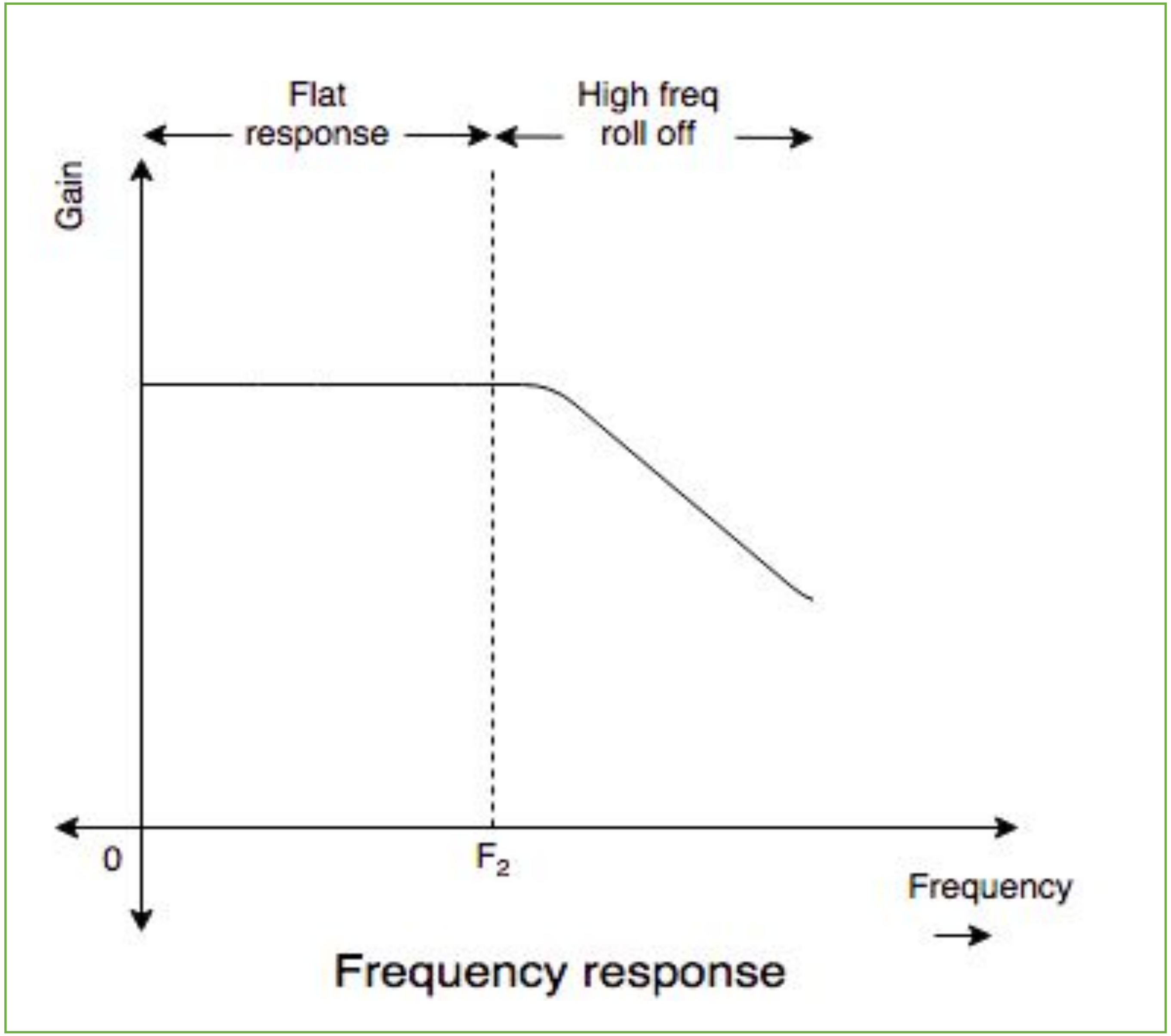
1. Impedance matching circuit
2. In power amplifiers

3. DIRECT COUPLED



DC coupled amplifier

3. DIRECT COUPLED



Advantages:

- simple circuit
- Low cost
- can be used to amplify low frequency components

Disadvantages:

- cannot amplify high frequency signal
- poor temperature stability

Applications:

- In power supply
- Linear IC's

DISADVANTAGES OF MULTISTAGE AMPLIFIERS

The Disadvantage is

1. The loading of one stage to the previous stage that may affect the Q point and hence distortion
2. The type of coupling that will affect gain in particular frequency in coupling methods

Cascode Amplifier & Darlington Pair Amplifier