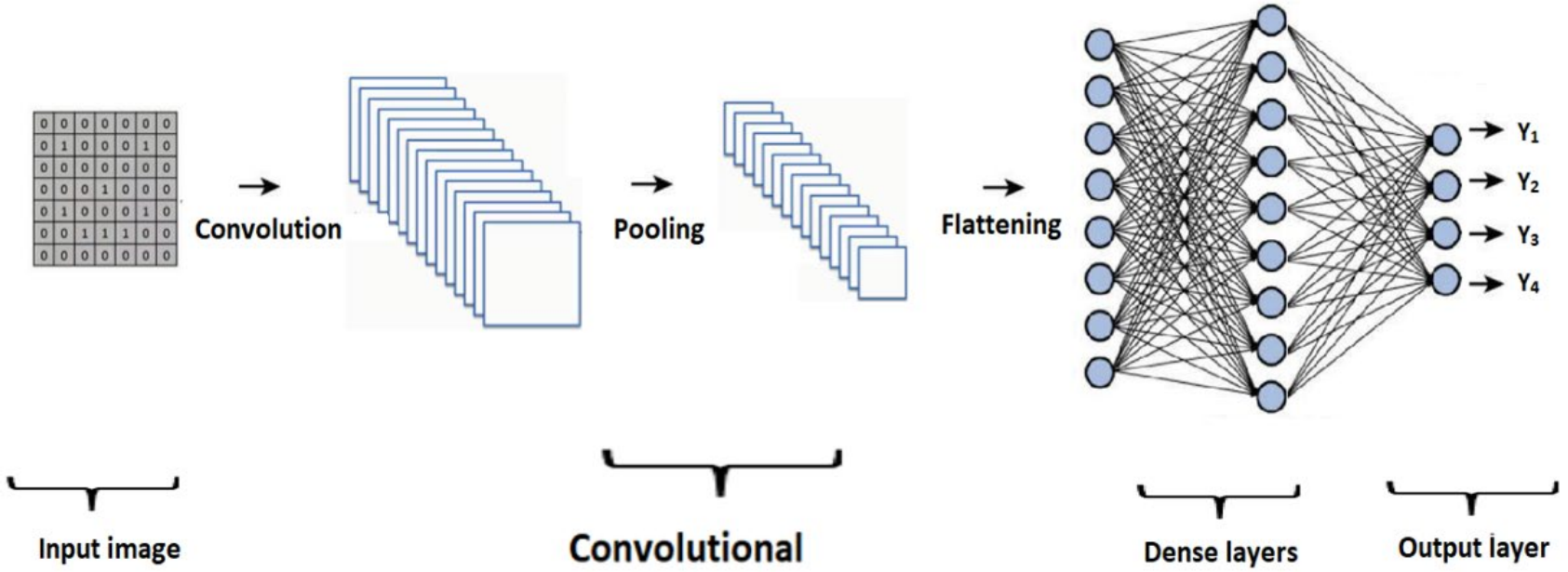
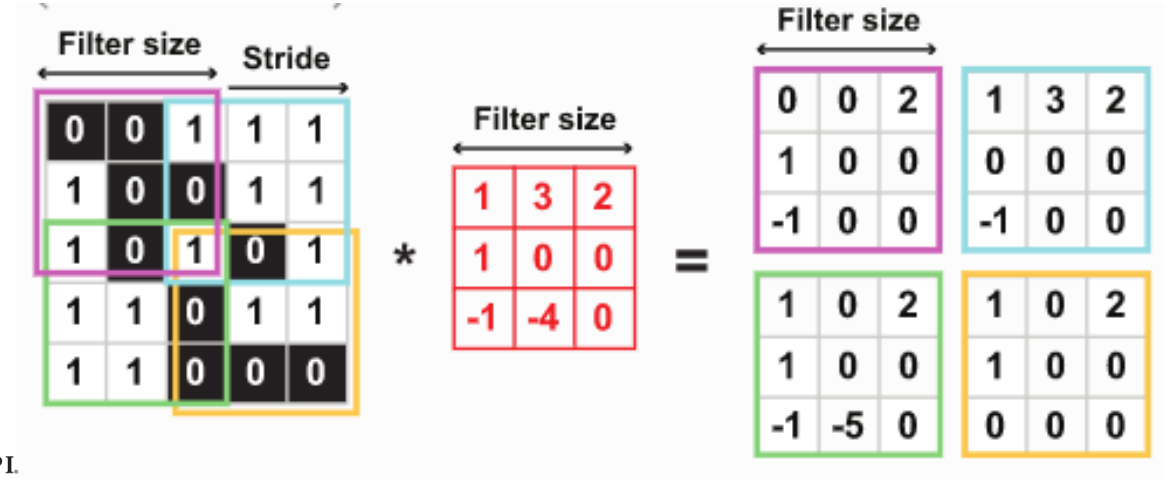
Convolutional layer & GPUs

Convolutional layer

- The convolutional layer prepares the input data for the fully connected neurons (hidden layers)
- Procedures happening the convolutional layer:
  - Filtering
  - Pooling
  - Flatten &

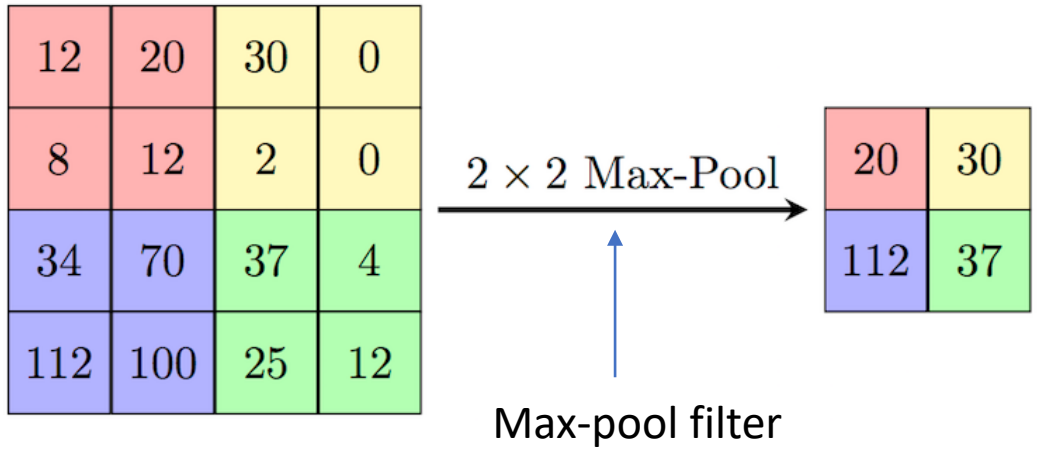


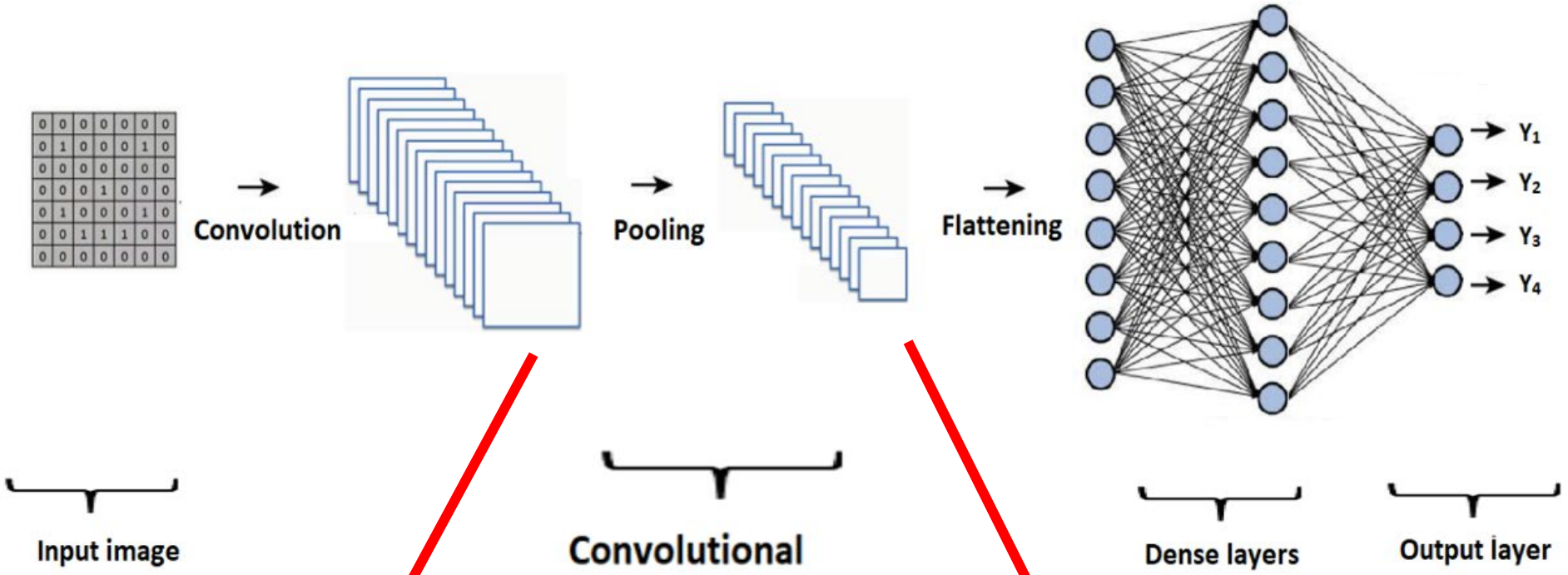
- Filters (kernel):
  - In charge to detect features
    - In images:
      - Can detect for example, lines, corners
      - Can also be specific: eyes, hair, etc.
  - Is a matrix of m * n. Size of the matrix depends on the application
    - Initialized randomly
    - Stride: how many “cells” the filter moves for a dot product
  - Operation:
    - A dot product operation is executed between the input data and the filter

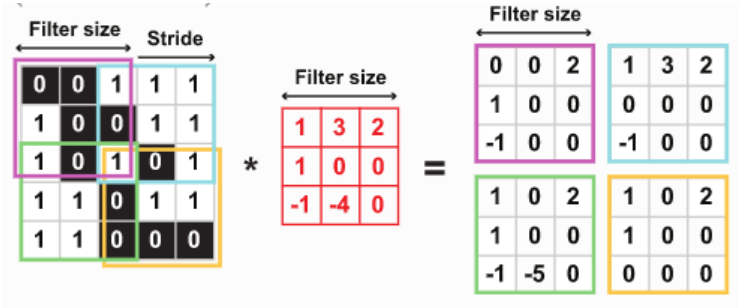


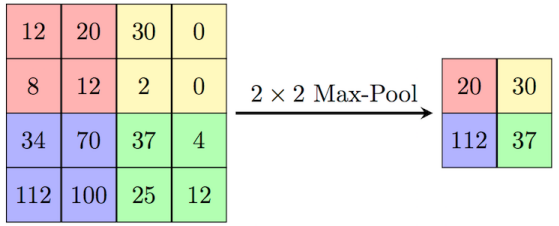
- Pooling:
  - To reduce dimensionality
  - Eliminates noise from data

  - Max pooling: after the dot product of the filter and input is executed
    - A max pooling filter (of m*n) selects the max value and creates a new max pool.

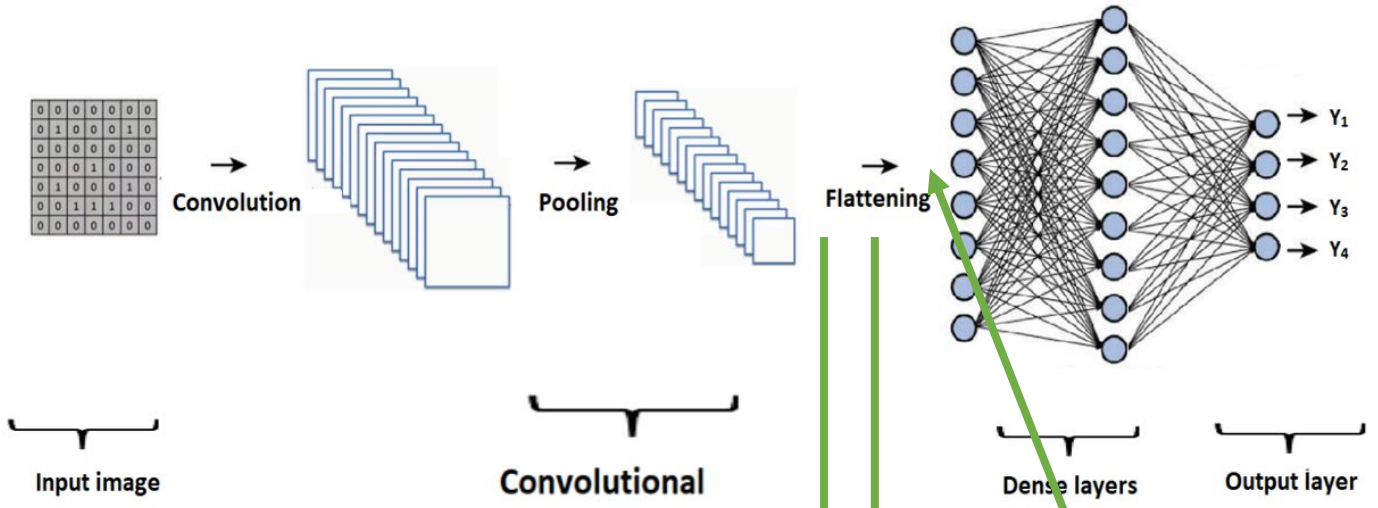



Convolution
Pooling
Flattening
Y1
Y2
Y3
Y4
Input image
Convolutional
Dense layers
Output layer


Filter size
Stride
Filter size
Filter size


2 × 2 Max-Pool

- Flatten & Dense:
  - Flatten: For the neurons to perform their own operations, the input data needs to be an appropriate format:



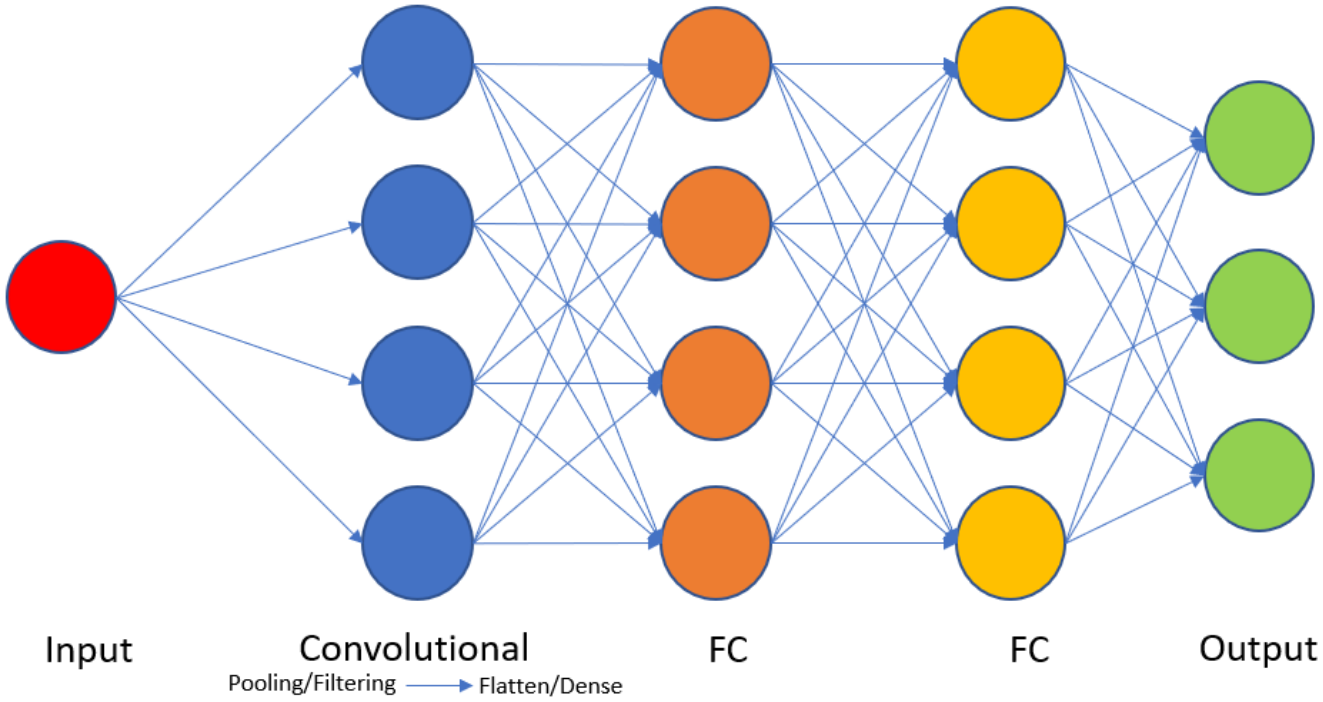
The output will be the classification
based on the features extracted through the previous layers and their different filters (classification: outputs are mapped to labels)

The vector (tensor) is passed as input of the FC

The output if the max-pool is a matrix
Can be of n-dimensions

Flattening: "Converts" n-dimension into a "readable" vector (tensor)

- Dense:
  - Method to create a fully connected neural network
  - Specifies the number of neurons per layer and activation method



- How is a CNN processed when GPUs are available?

GPU ARCHITECTURE

Streaming Multiprocessor (SM)

Many CUDA Cores per SM

Architecture dependent

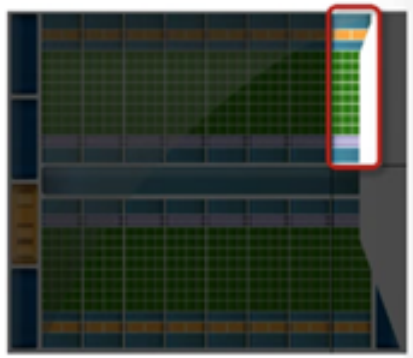
H100 SM has 128 cores

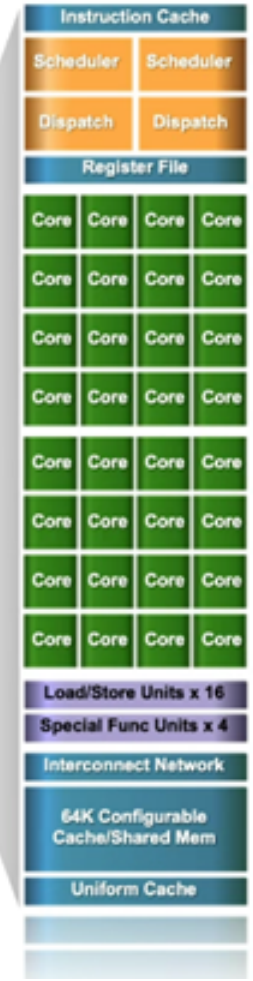
Special-function units

cos/sin/tan, etc.

Shared mem + L1 cache

Thousands of 32-bit registers





H100 PCIe has a total of 14,592 cores

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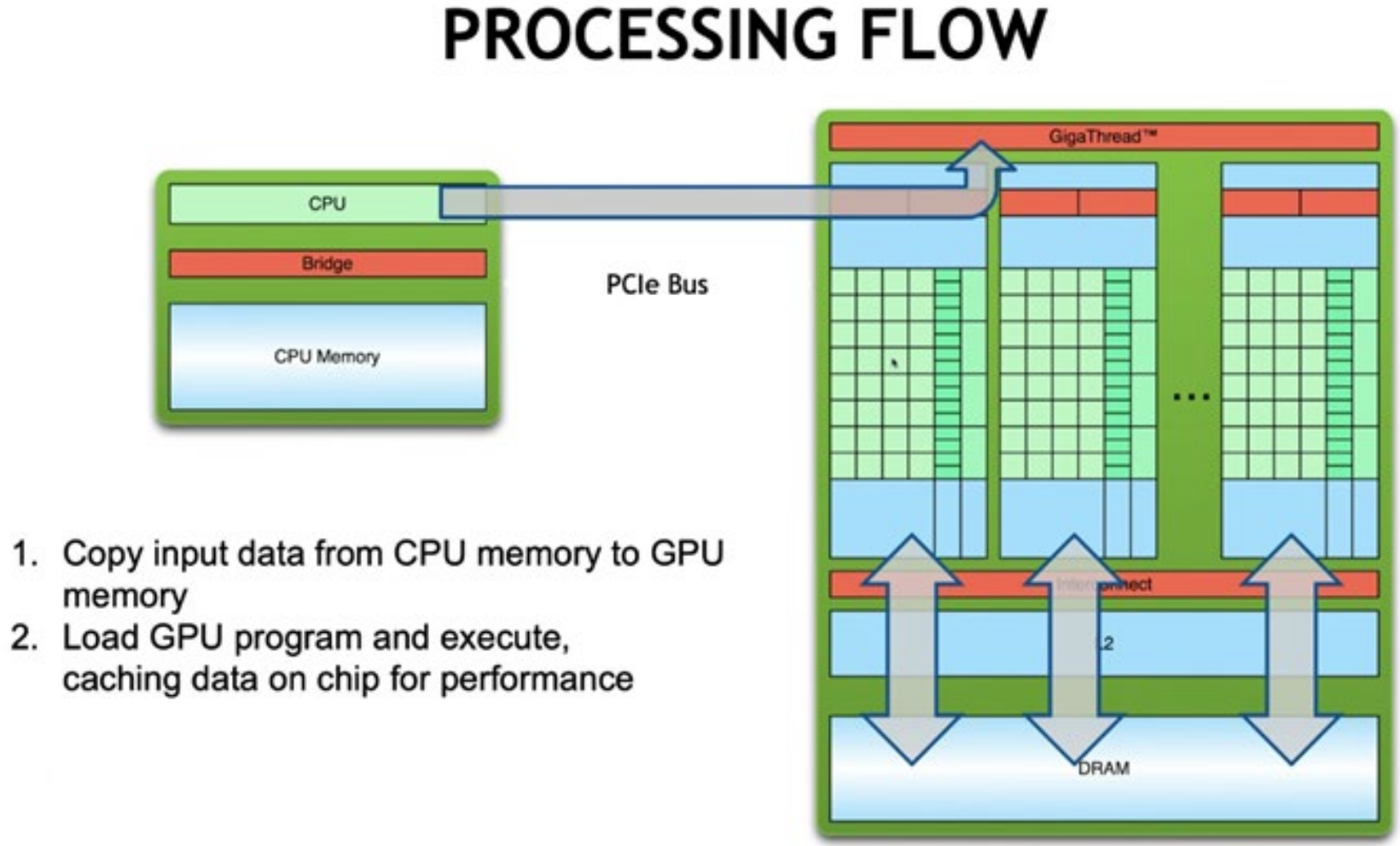

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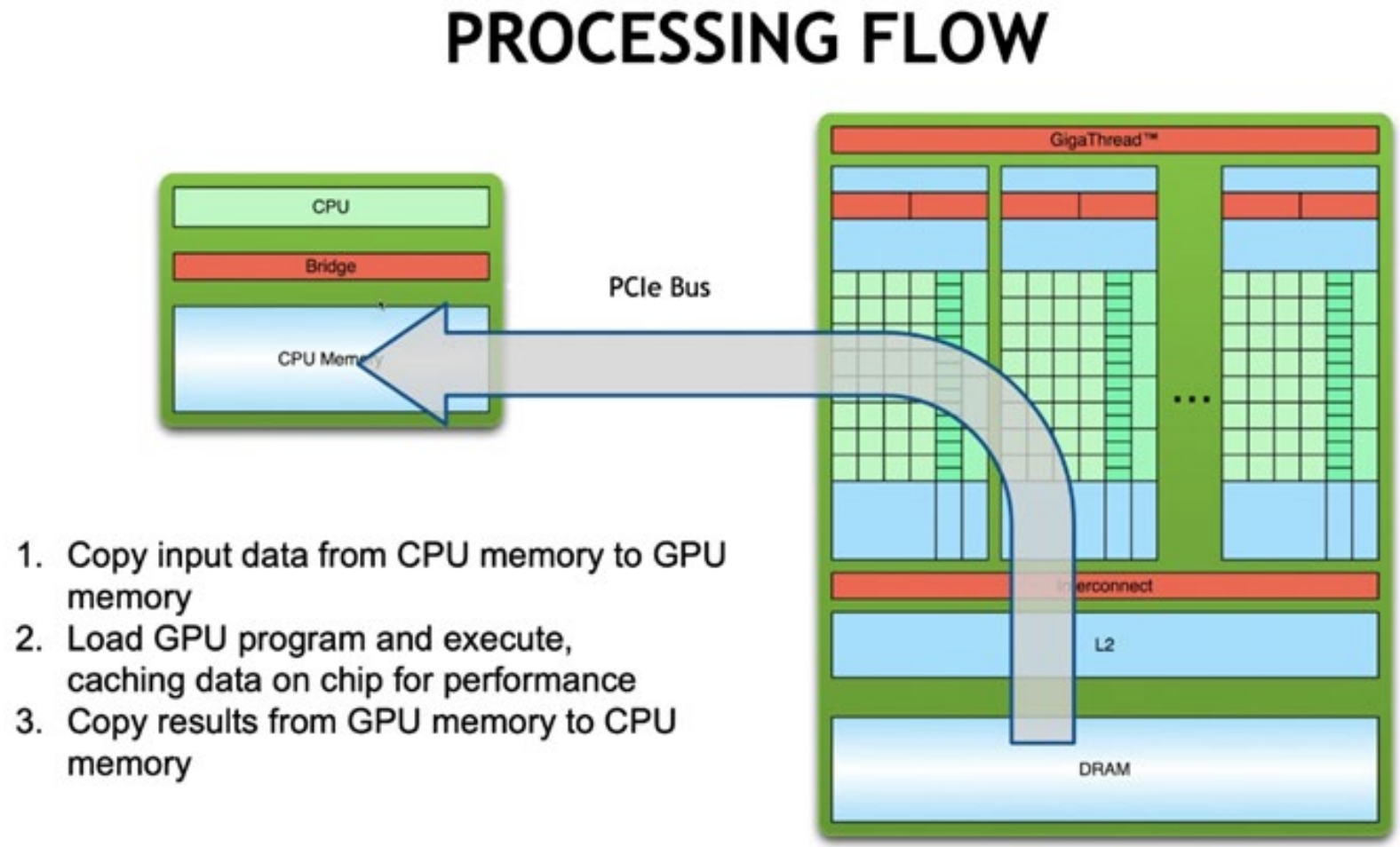

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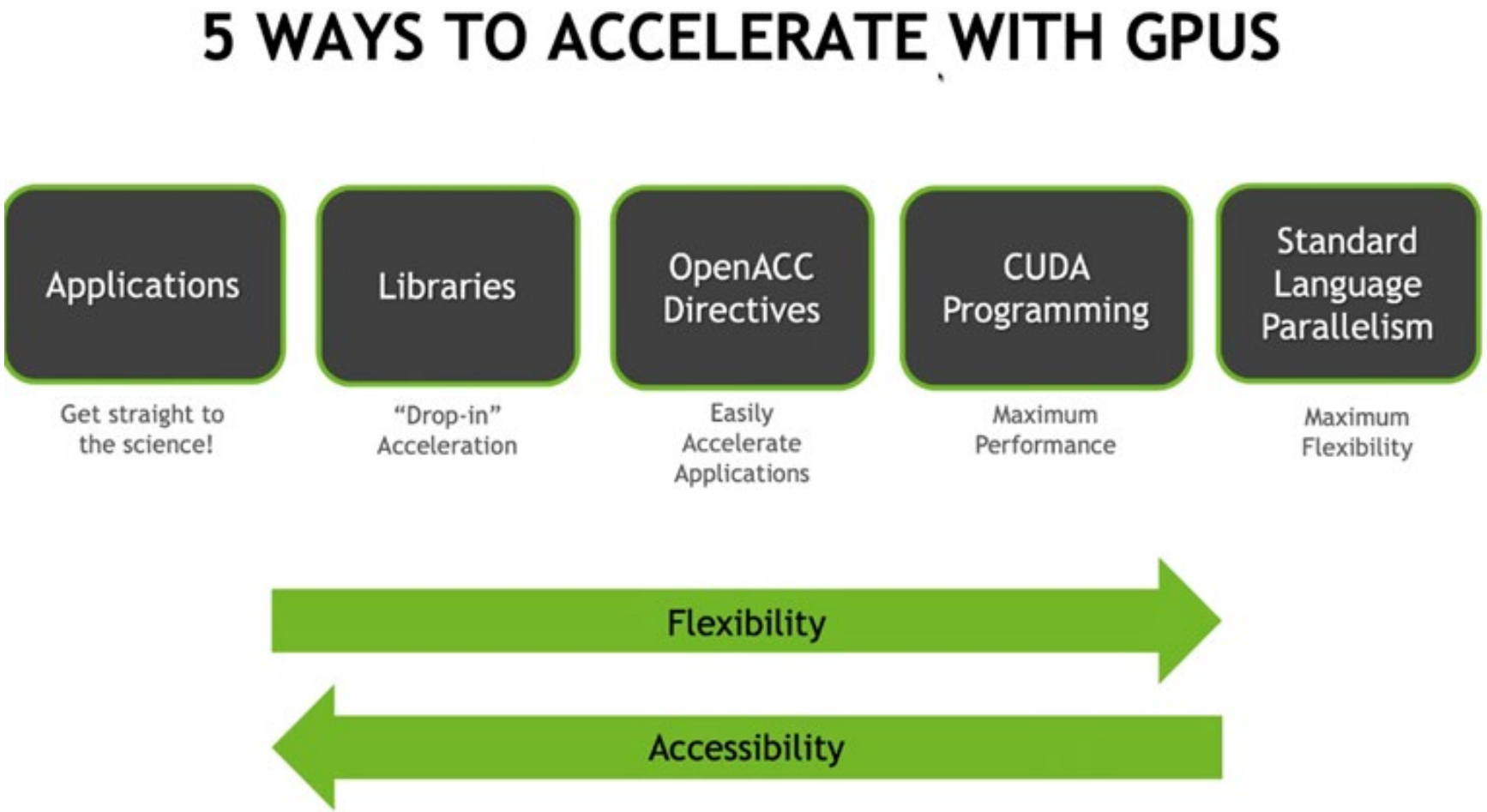

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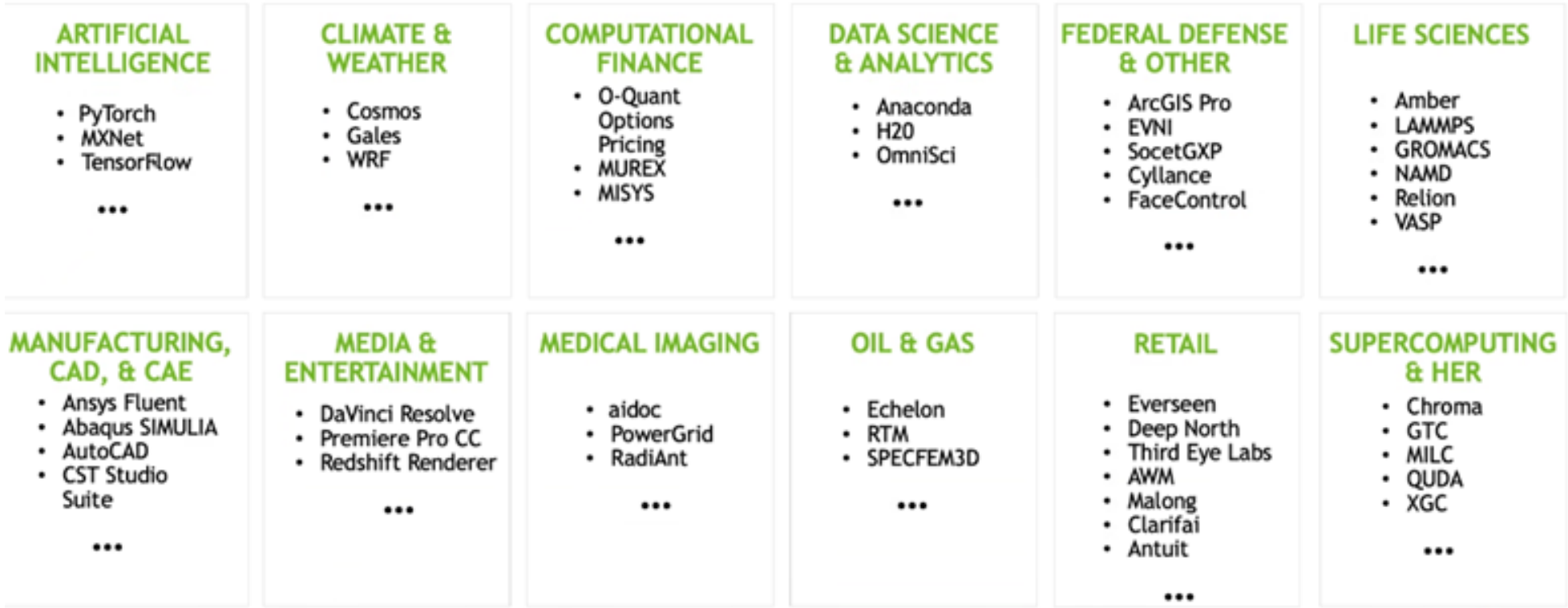

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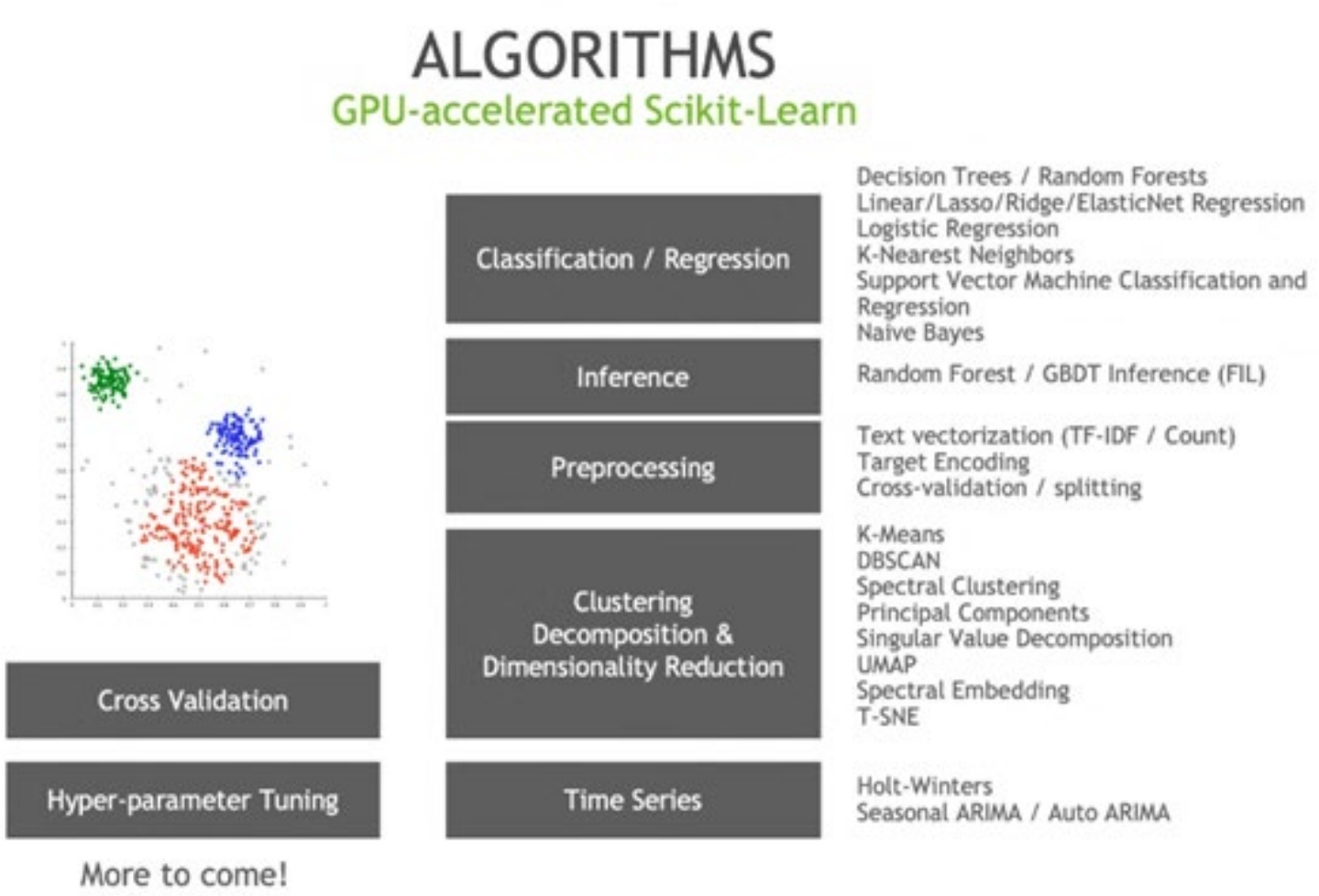

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