

Commands to Run Verilog Open-Source Using iverilog

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Icarus Verilog + GTKWave Workflow

The basic workflow to compile, simulate, and view waveforms for a Verilog module using **Icarus Verilog** and **GTKWave** is as follows:

1. Compile the Verilog code

Command:

```
iverilog -o <output_executable> <source_files>
```

Explanation:

- **iverilog** : Icarus Verilog compiler
- **-o <output_executable>** : Name of the compiled simulation executable
- **<source_files>** : List of Verilog files (module + testbench)

Example:

```
iverilog -o dff_tb dff_sync_reset.v tb_dff_sync_reset.v
```

Here, **dff-sync-reset.v** is the DFF module and **tb-dff-sync-reset.v** is the testbench. The output executable is **dff_tb**.

2. Run the simulation

Command:

```
vvp <output_executable>
```

Explanation:

- **vvp** : Runs the compiled simulation
- Generates a **.vcd** waveform file if **\$dumpfile** and **\$dumpvars** are used in the testbench

Example:

```
vvp dff_tb
```

3. View the waveform

Command:

```
gtkwave <vcd_file>
```

Explanation:

- **gtkwave** : Opens GTKWave waveform viewer
- **<vcd_file>** : Waveform file generated by simulation

Example:

```
gtkwave dff_sync_reset.vcd
```

Full Example Workflow

```
# 1. Compile  
iverilog -o dff_tb dff_sync_reset.v tb_dff_sync_reset.v  
  
# 2. Run simulation  
vvp dff_tb  
  
# 3. View waveform  
gtkwave dff_sync_reset.vcd
```