BANGLADESH UNIVERSITY OF ENGINEERING AND TECHNOLOGY
DEPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING

EEE 466 (July 2023)

Analog Integrated Circuits and Design Laboratory

Final Project Report

Section: G2 Group: 04

8:1 Analog Multiplexer Design

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1 Abstract

This project presents the design and implementation of an 8:1 multiplexer (mux) analog integrated circuit (IC). The proposed IC is designed to efficiently route one of eight analog input signals to a single output based on digital control inputs. The design employs CMOS technology to achieve low power consumption and high-speed operation. Various design considerations including transistor sizing, layout optimization, and signal routing techniques are discussed to ensure optimal performance. Simulation results demonstrate the functionality and performance of the designed multiplexer, including input signal fidelity, bandwidth, and power efficiency. The proposed IC holds promise for integration into various analog signal processing applications, such as data acquisition systems, sensor interfaces, and communication systems, where efficient signal routing is essential.

2 Introduction

Multiplexers are fundamental components in analog and digital systems, allowing multiple input signals to be selectively routed to a single output based on control inputs. The 8:1 mux to be designed in this project will provide the capability to switch between eight analog input channels, offering flexibility and scalability in signal routing.The use of Cadence Virtuoso tools provides a comprehensive platform for analog IC design, offering advanced simulation, layout, and verification capabilities. Leveraging these tools, we aim to achieve a robust design that meets performance requirements while adhering to design constraints such as power consumption, area, and manufacturing considerations.

This project encompasses various stages of IC design, including conceptualization, schematic capture, circuit simulation, meeting specifications and design verification. Through systematic design iterations and optimization techniques, we aim to achieve a reliable and efficient 8:1 mux IC that meets specifications and performance targets.

The successful completion of this project not only demonstrates proficiency in analog IC design but also provides a valuable insight into the practical application of Cadence Virtuoso tools in the development of complex analog circuits. Furthermore, the designed multiplexer holds potential for integration into diverse electronic systems, contributing to advancements in signal processing and communication technologies.

3 Design

3.1Problem Formulation (PO(b))

3.1.1 Identification of Scope

1. **Application Flexibility**: Design the 8:1 multiplexer with provisions for adaptable input/output configurations, enabling its integration into diverse applications such as instrumentation, communication systems, and data acquisition.

2. **Low Power Design**: Emphasize low-power design techniques to minimize energy consumption, making the multiplexer suitable for battery-operated devices and energy-efficient electronic systems.

3. **High-Speed Operation**: Optimize the multiplexer for high-speed operation to facilitate rapid signal routing, catering to applications requiring real-time data processing and high-frequency signal transmission.

4. **Robustness and Reliability**: Ensure robustness and reliability in the multiplexer design to withstand environmental variations, aging effects, and voltage fluctuations, enhancing the longevity and stability of the integrated circuit.

5. **Noise Immunity**: Incorporate noise suppression techniques to enhance the signal-to-noise ratio and immunity to external interference, enabling the multiplexer to maintain signal integrity in noisy operational environments.

6. **Ease of Integration**: Design the multiplexer with standardized interfaces and compatibility with common electronic components to facilitate ease of integration into existing circuit designs and systems.

7. **Cost-Effectiveness**: Optimize the design for cost-effective manufacturing and assembly processes, considering factors such as material selection, layout complexity, and fabrication yield to ensure affordability and scalability.

8. **Temperature and Process Variations**: Address temperature and process variations in the design to ensure consistent performance across different operating conditions, enhancing the reliability and resilience of the multiplexer IC.

3.1.2 Literature Review

The literature on designing analog 8:1 multiplexers using Cadence tools covers various aspects including the significance of analog multiplexers, design considerations, Cadence tools used, previous methodologies, challenges, and recent advancements. Key points include understanding the importance of analog multiplexers in electronic circuits, considering factors like input/output specifications and power consumption in design, utilizing Cadence tools like Virtuoso and Spectre for simulation and layout, addressing challenges such as signal integrity issues and noise, and exploring recent advancements like novel circuit topologies

3.1.3 Formulation of Problem

The primary objective of this project is to design and implement an 8:1 multiplexer (mux) analog integrated circuit (IC) using Cadence Virtuoso tools. The project encompasses the following key aspects:

- **Performance Specifications**: Clearly define the performance requirements of the multiplexer IC, including parameters such as input/output voltage ranges, bandwidth, switching on time, input capacitance, charge injection, on-resitance and power dissipation.
- **Technology Selection:** Evaluate different semiconductor technologies (e.g., CMOS, BiCMOS) and select the most suitable one based on considerations such as power consumption, speed, and fabrication process compatibility.
- **Schematic Design**: Develop a detailed schematic representation of the 8:1 mux circuit, ensuring compatibility with the selected technology and meeting the specified performance requirements.
- **Simulation and Analysis**: Utilize Cadence Virtuoso simulation tools to perform comprehensive analyses of the designed circuit, including DC, AC, and transient

simulations to validate functionality and performance.

- **Optimization and Iteration**: Iteratively refine the circuit design and layout based on simulation results and feedback, aiming to optimize performance, minimize area, and improve manufacturability.

By addressing these aspects, the project aims to demonstrate proficiency in analog IC design using Cadence Virtuoso tools, culminating in the successful implementation of a high-performance 8:1 mux IC suitable for various analog signal routing applications.

3.2Design Method (PO(a))

We formulated the design of the multiplexer utilizing CMOS transmission gate logic, chosen for its suitability to accommodate the multiplexer's 8 input channels. To enable access to any of these input channels, we determined that 3 select pins were necessary. Consequently, we implemented this design using a total of 24 CMOS transmission gates. Within each input channel, 3 transmission gates were allocated. The selection of the appropriate output is contingent upon the state of the select pins. The operational logic of the multiplexer is described by the following equation:

$$V_{out} = \bar{A}\bar{B}\bar{C}S_0 + \bar{A}\bar{B}CS_1 + \bar{A}B\bar{C}S_2 + \bar{A}BCS_3 + A\bar{B}\bar{C}S_4 + A\bar{B}CS_5 + AB\bar{C}S_6 + ABCS_7$$

This multiplexer employs a configuration of 6 transistors to manage three selection lines. Among these transistors, 3 are CMOS transistors, with their gate voltages and outputs serving as control signals for the 24 transmission gates. The design consistes of two logical frameworks: CMOS logic and transmission gate logic. The CMOS logic component can be described as follows:

CMOS Logic: CMOS (Complementary Metal-Oxide-Semiconductor) logic is a widely used digital logic family in integrated circuit design. It consists of both PMOS (P-type Metal-Oxide-Semiconductor) and NMOS (N-type Metal-Oxide-Semiconductor) transistors, arranged in a complementary manner to achieve low power consumption and high noise immunity.
In CMOS logic, a high logic level (logical '1') is represented by a voltage close to the supply voltage (VDD), typically denoted as '1'. Conversely, a low logic level (logical '0') is represented by a voltage close to the ground voltage (GND), typically denoted as '0'.

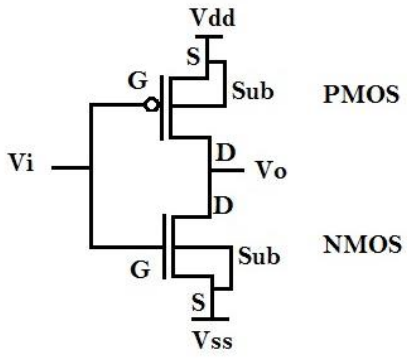

Figure 1: CMOS inverter circuit

We have used Vdd as 3 V and Vss as -3 V to implement the CMOS inverter.

CMOS Inverter Circuit:

- The basic building block of CMOS logic is the CMOS inverter, which consists of

both PMOS and NMOS transistors connected in series between Vdd and Vss.

- The gate of the PMOS transistor is connected to the input signal (Vin), while the gate of the NMOS transistor is connected to the complement of the input signal (Vin').
- When the input voltage Vin is high, the NMOS transistor conducts and pulls the output voltage Vout low;
- When Vin is low, the PMOS transistor conducts and pulls Vout high.

Transmission Gate Logic: This logic also known as pass gate logic, is a digital logic technique that employs transmission gates to control the flow of signals. Transmission gates are composed of complementary metal-oxide-semiconductor (CMOS) transistors – one NMOS and one PMOS – connected in parallel. These gates act like switches, allowing or blocking the passage of signals based on a control input.

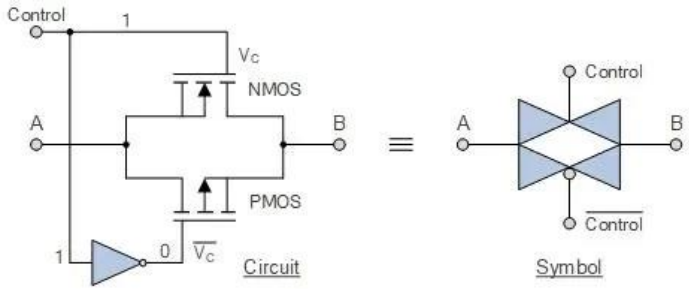

Figure 2: Transmission Gate Circuit

In transmission gate logic, a transmission gate consists of two complementary transistors – one NMOS and one PMOS – connected in parallel. The gate of the NMOS transistor is connected to the control signal (usually denoted as "EN" for enable), while the gate of the PMOS transistor is connected to the complement of the control signal ("EN_bar"). When the control signal is high (logical '1'), the NMOS transistor conducts, allowing the passage of signals from input to output. Simultaneously, the PMOS transistor is off, ensuring minimal resistance in the conducting path. Conversely, when the control signal is low (logical '0'), the NMOS transistor is off, and the PMOS transistor conducts, enabling signal flow from output to input. This bidirectional capability makes transmission gates versatile for various applications.

3.3 Circuit Diagram

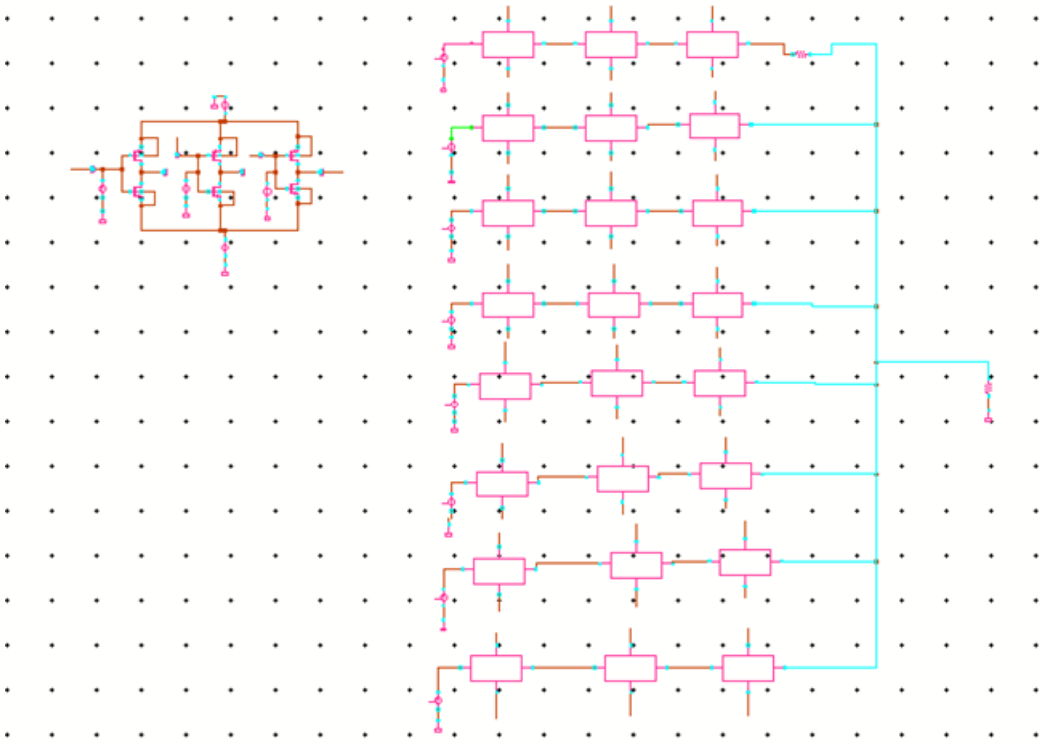

Figure: Circuit using Transmission Gates as switches

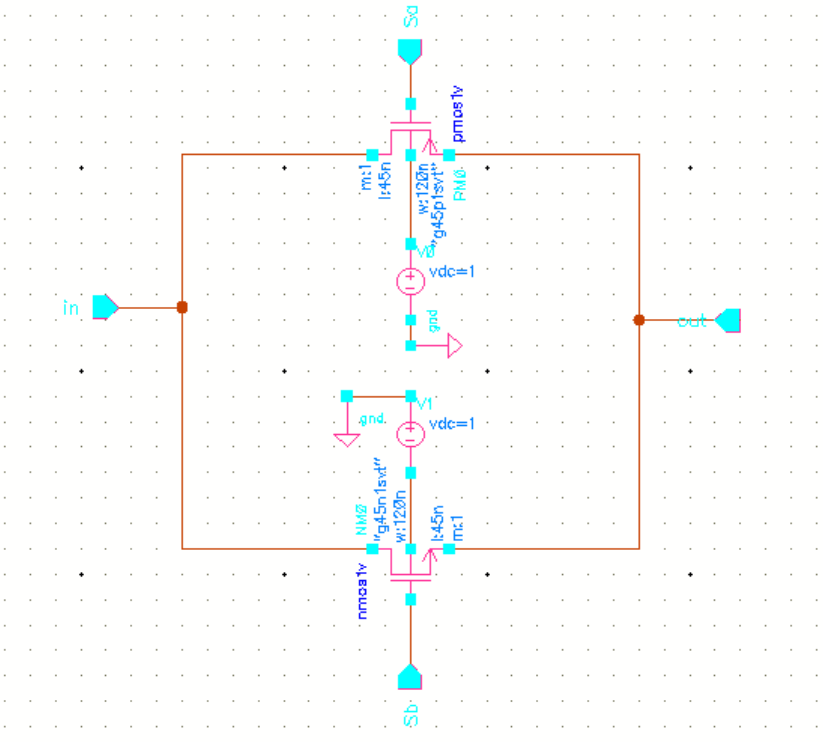

Figure: Transmission Gate Symbol

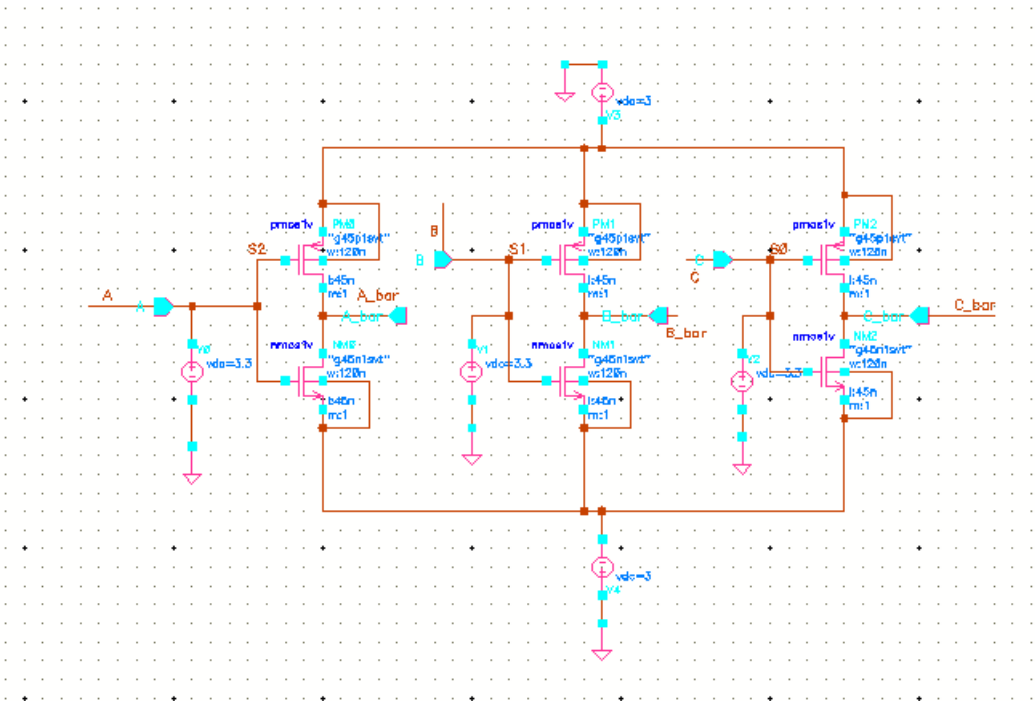

Figure: Creation of Selection Bits

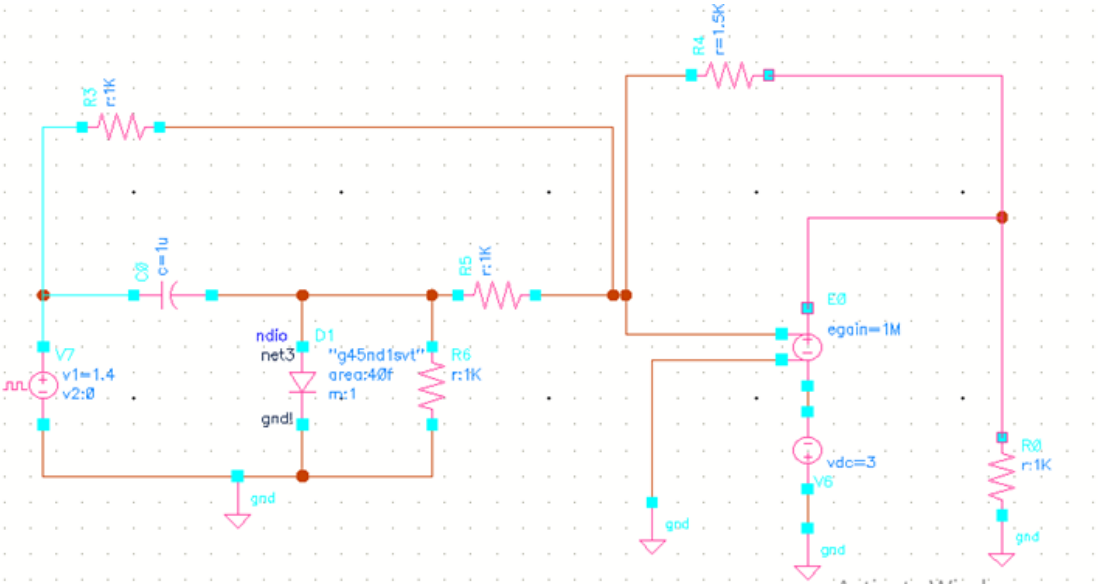

Figure: Creation of Adder Circuit to maintain LOGIC LEVEL 0-1.4V

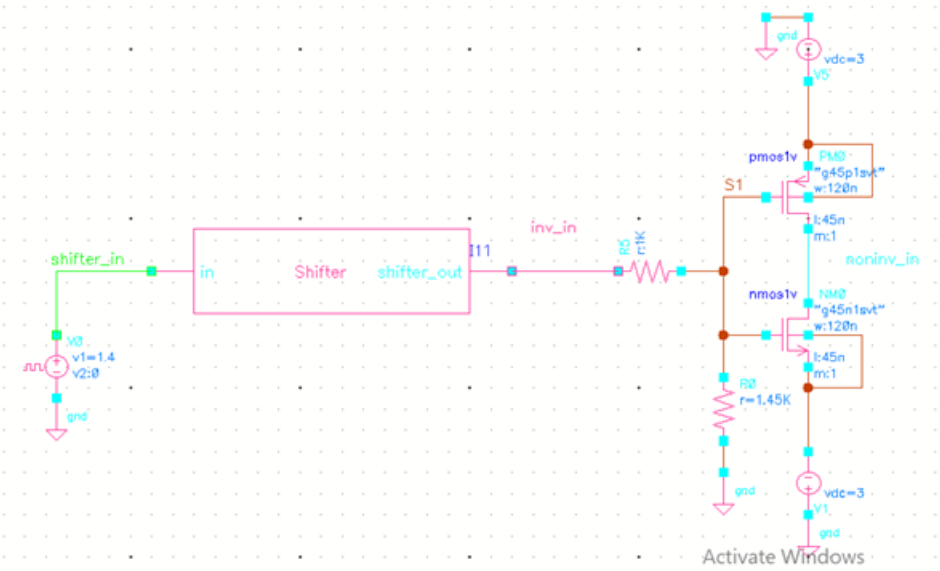

Figure: Creation of Selection Bits using Shifter Circuit

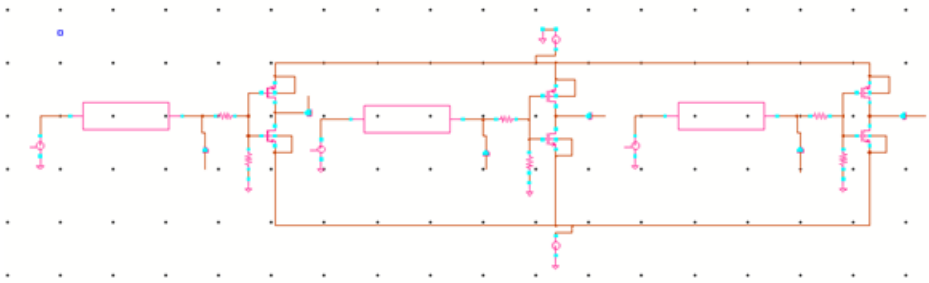

Figure: Creation of Selection Bits using Three Shifter Circuits

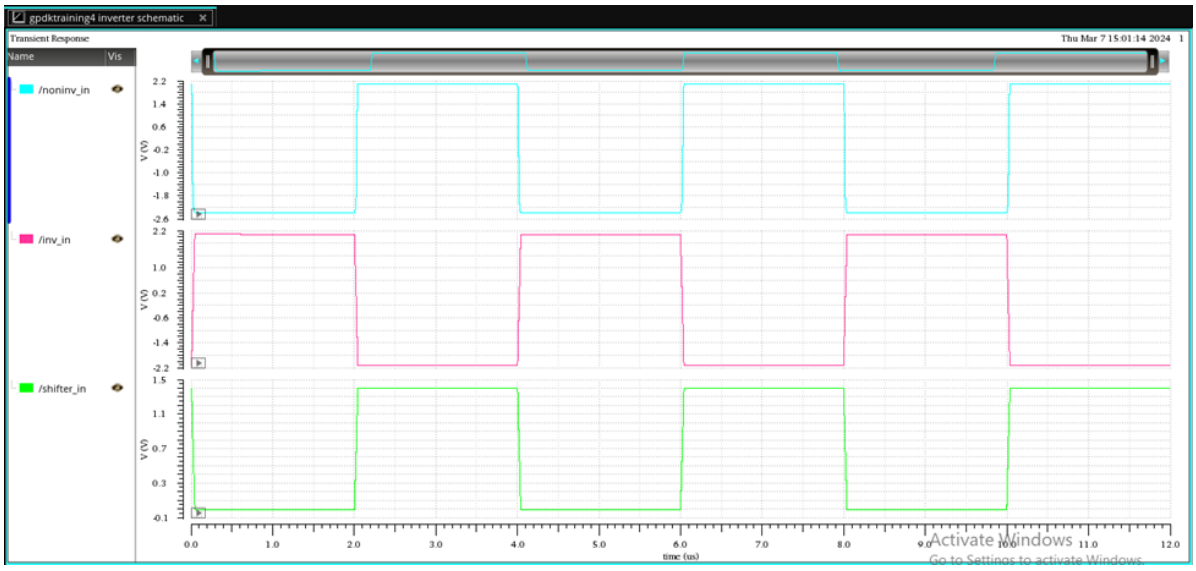

Figure: Output of Selection bits found from Logic Level Shifter Circuit

4 Implementation

4.1 Description

We implemented 8:1 analog multiplexer using transmission gates. To meet the required specifications, we took logic high voltage as 1.4V and logic low voltage as 0V. We then implemented a logic level shifter to obtain an analog signal of -2 to 2 V which is our input as selection bits. Using the inverters we reverted the input selection bits and provided as selectors in transmission gates. The output of 8:1 multiplexer follows the analog signal according to the combination of selector bits as provided in the theory. We then measured Bandwidth, on resistance, input capacitance, switching on time etc. by analyzing the circuit with the help of cadence virtuoso.

Design an 8:1 analog multiplexer.

Specification:

Supply Voltage	+/-3	V
Logic High Level	1.4	V
Logic Low Level	0	V
Input Capacitance (max)	50	pF
Charge Injection over the full signal swing range (max)	5	pC
Switching On time (t_{ON})(at R_L = 1k Ω, C_L = 10 pF) (max)	100	ns
Analog Signal Range	-2 to 2	V
Power Dissipation (max)	10	mW
On-Resistance	10	Ω
Bandwidth, -3 dB	1	MHz

5 Design Analysis and Evaluation

5.1 Design Considerations (PO(c))

5.1.1 Results and Analysis

- **All Outputs:**

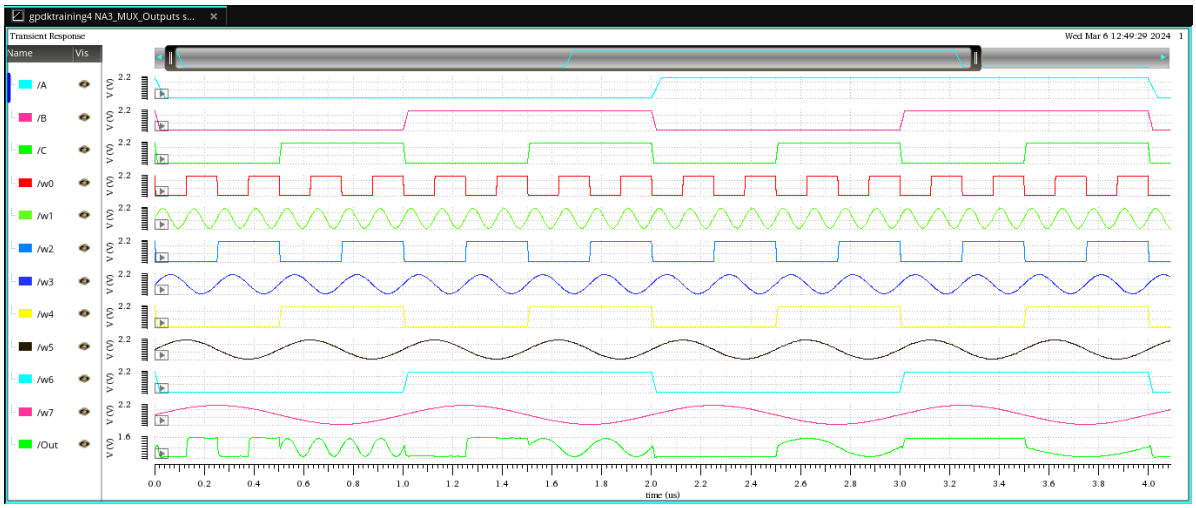

Figure: All Outputs: (W=3µm)

- **Bandwidth:**

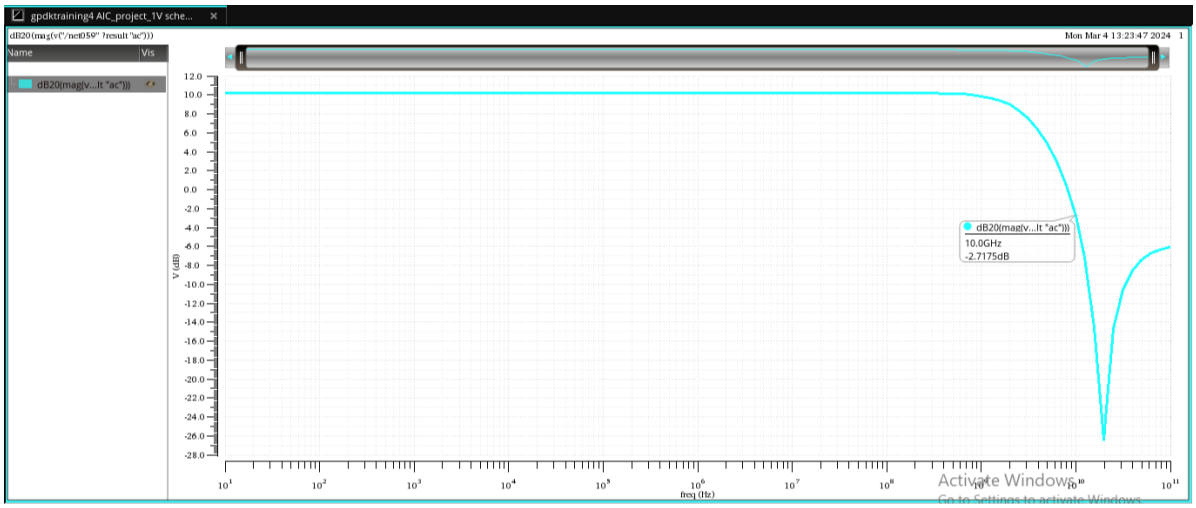

Figure: Bandwidth (100 MHz) [without capacitance]

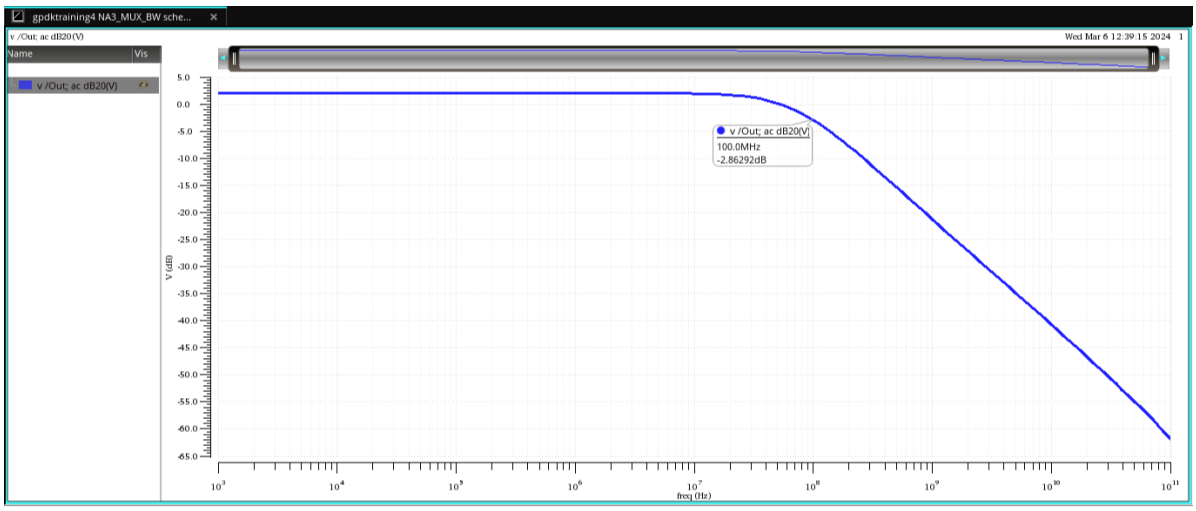

Figure: Bandwidth (100 MHz)[with 0.1 pF capacitance in load terminal]

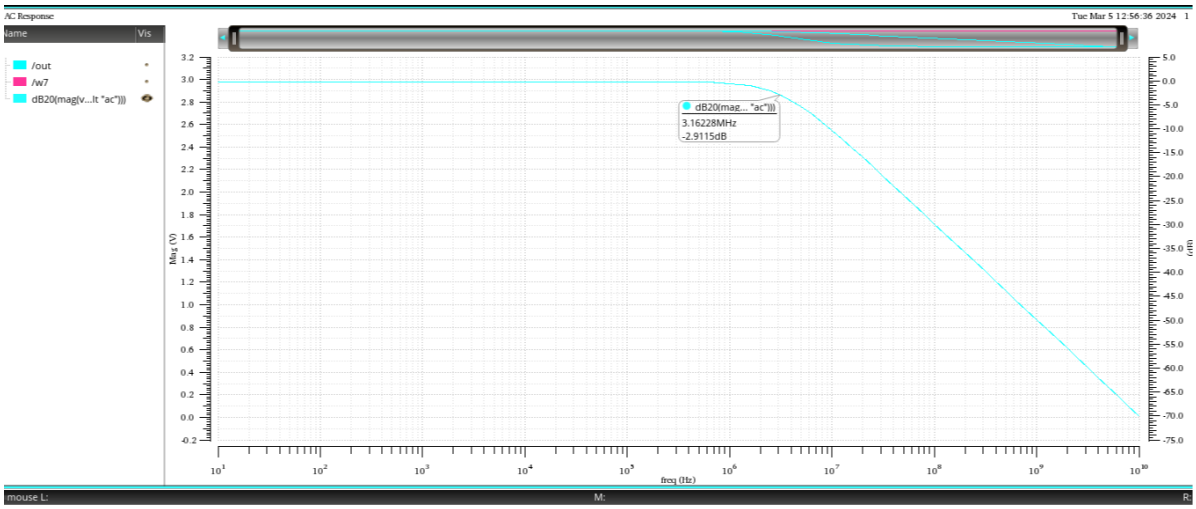

Figure: Bandwidth (~3 MHz)[with 10 pF capacitance in load terminal]

- **On Resistance:**

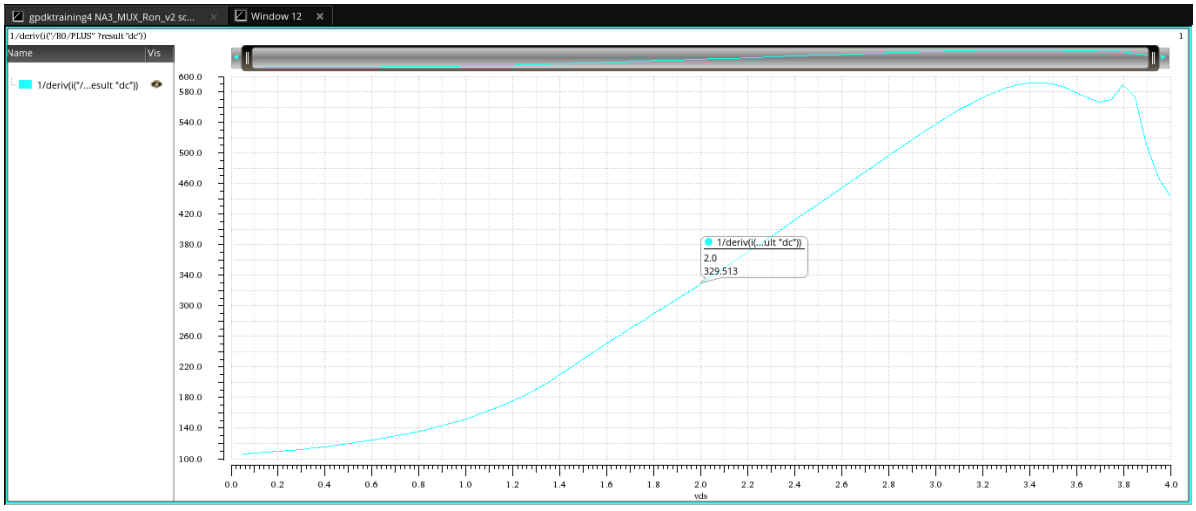

Figure: ON-Resistance = 329.513 Ω (30um width)

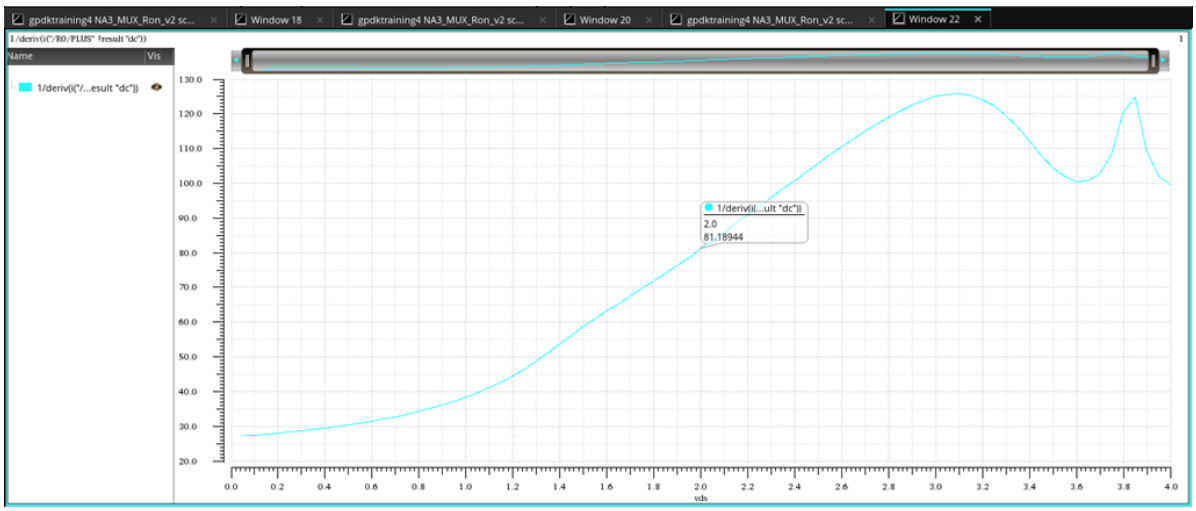

Figure: ON-Resistance = 81.189 Ω (30um width)

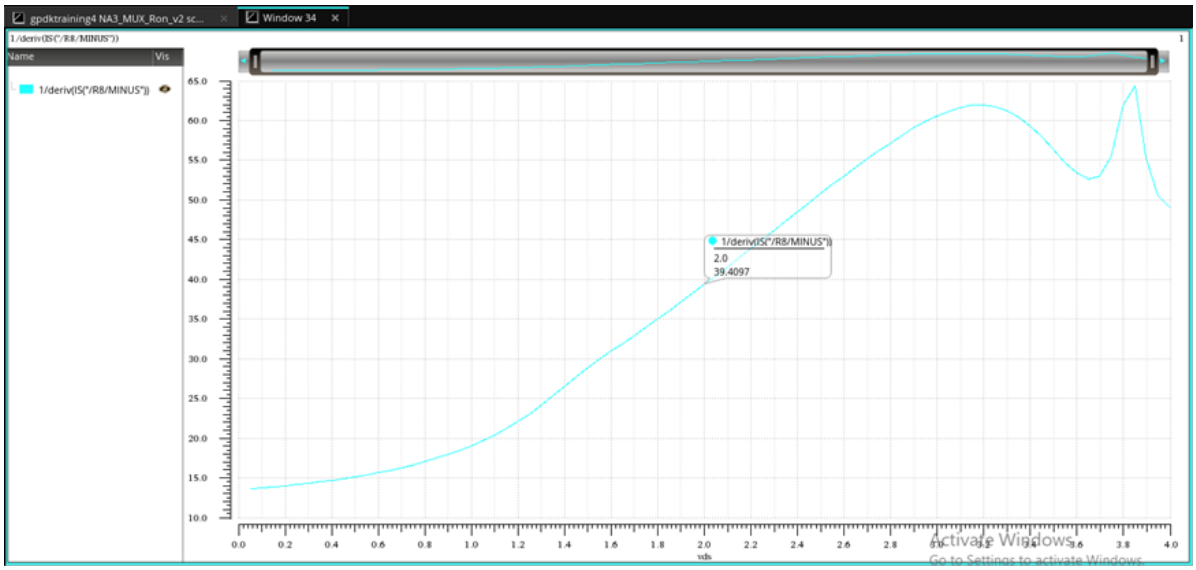

Figure: ON-Resistance = 39.41 Ω (60um width)

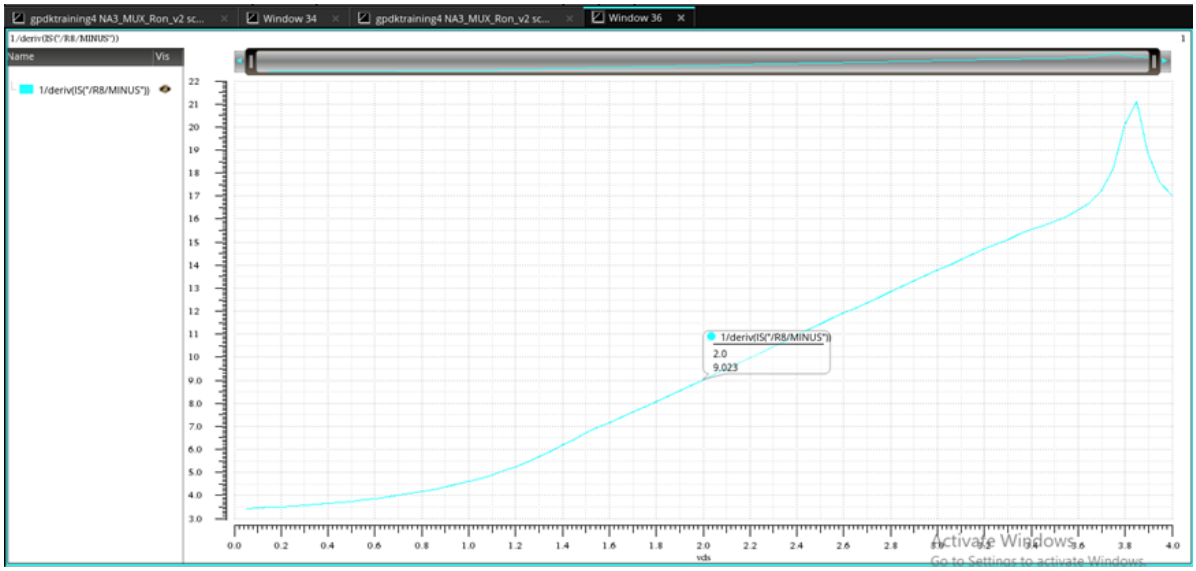

Figure: ON-Resistance = 9.02 Ω (240um width)

- **Switching On Time:**

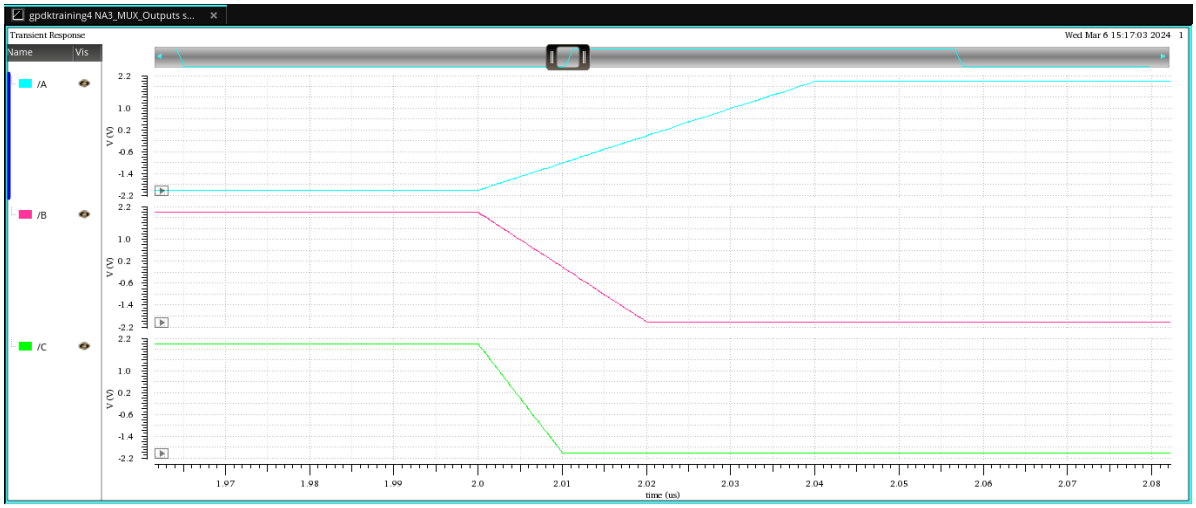

Figure: Switching ON time (0.04 µs)

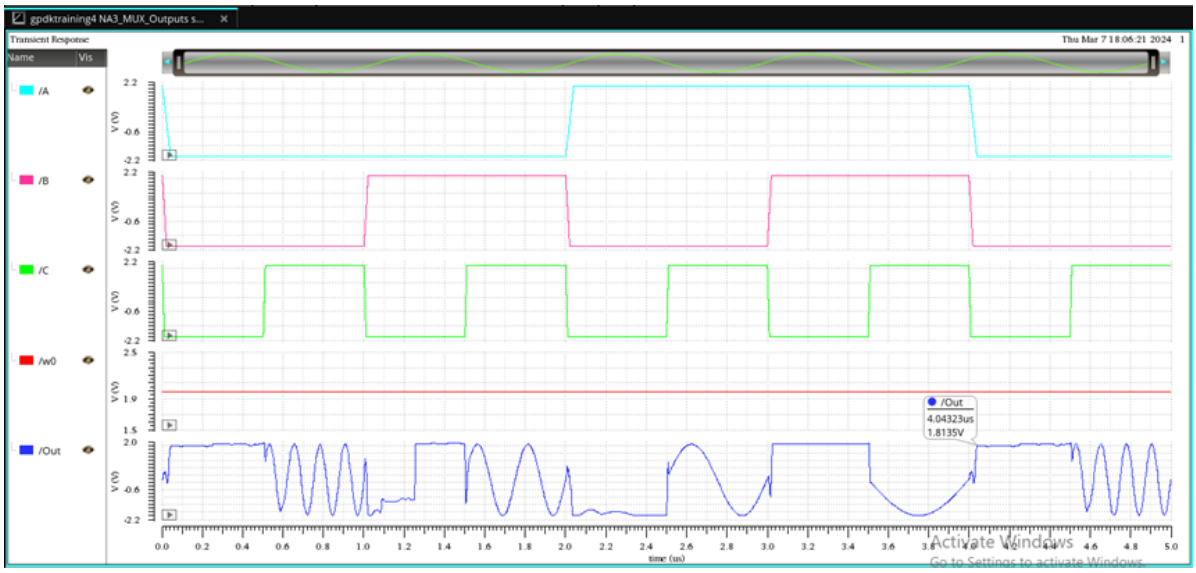

Figure: Switching ON time by following the output (0.0432 µs)

- **Input Capacitance:**

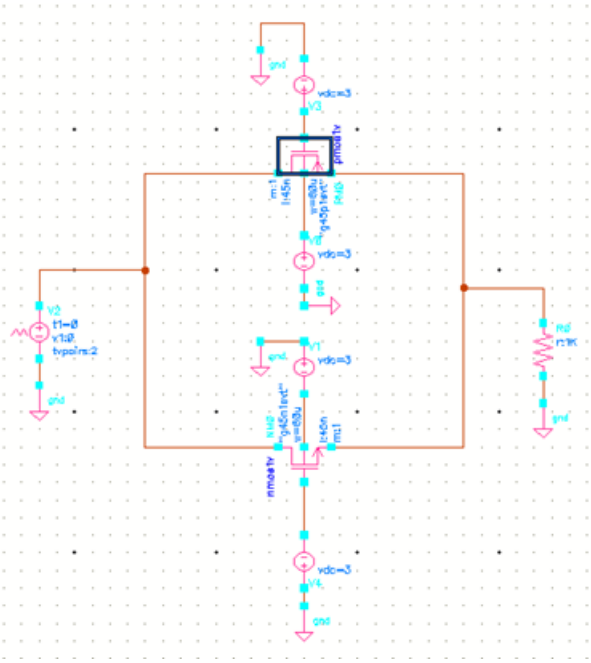

Figure: Circuit for Input capacitance (W=60um)

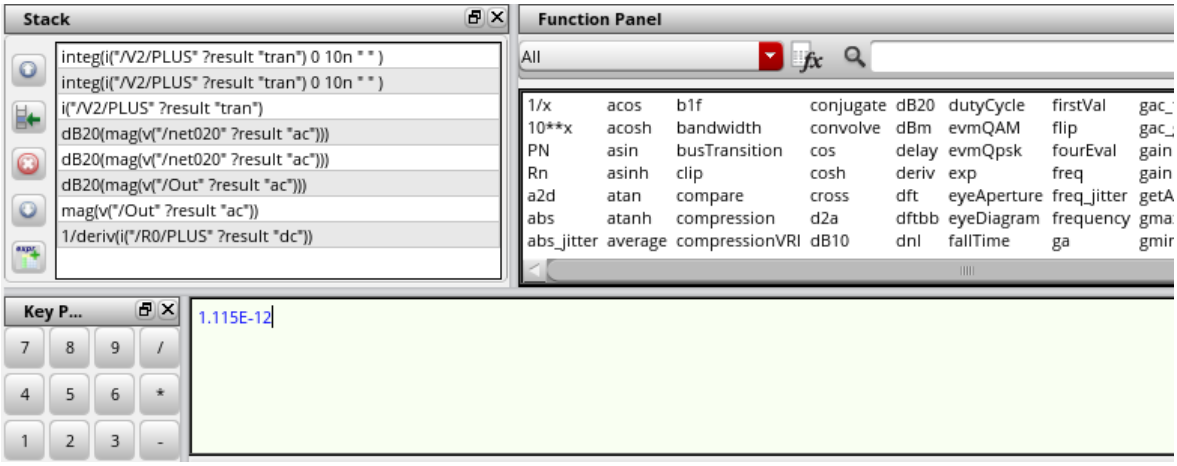

Figure: Input capacitance (W=60um): 1.15pF

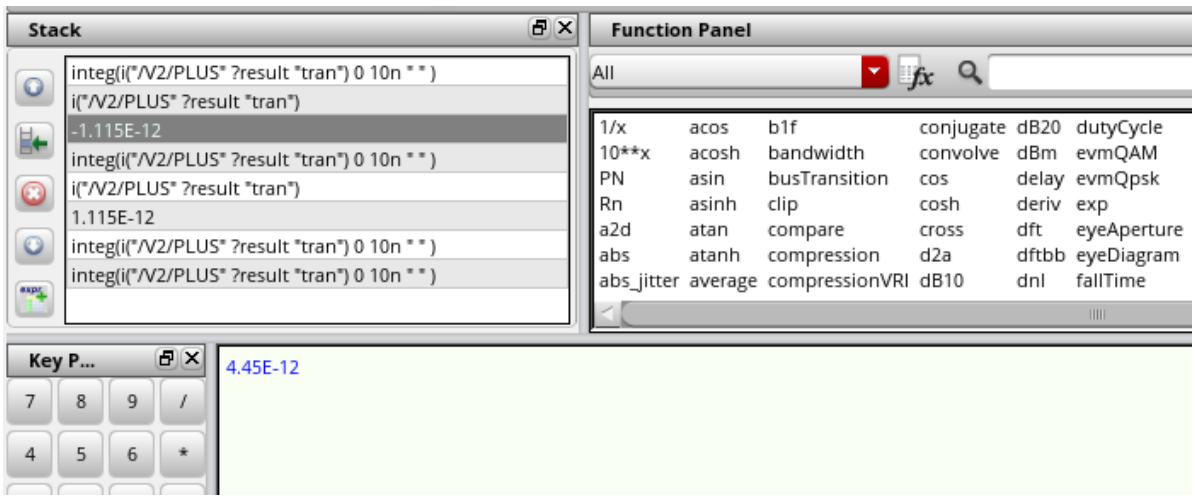

Figure: Input capacitance (W=240um): 4.45pF

- **Power Dissipation:**

ON current is: 4.4657 mA
Power Dissipation: $P = I^2R$ = 4.4657 mA * 9.02ohms = 0.18 mW

5.1.2 Interpretation and Conclusions on Data

Parameter Name	Required Parameter	Obtained Parameter
Supply Voltage	+/-3 V	+/-3V
Logic High Level	1.4V	1.4V
Logic Low Level	0V	0V
Input Capacitance (max)	50pF	4.45pF
Charge Injection over full signal swing range (max)	5pC	Did not calculate
Switching On time (t_{ON}) at R_L = 1kΩ, C_L = 10pF) (max)	100ns	43.2ns
Analog Signal Range	-2 to 2V	-2 to 2V
Power Dissipation (max)	10mW	0.18mW
On-Resistance	10Ω	9.02Ω
Bandwidth, -3dB	1MHz	3.16228MHz

5.2 Limitations of Tools (PO(e))

Initially we attempted to build the multiplexer using nmos2v and pmos2v, but could not obtain complete simulation because of library error. nmos2v and pmos2v requires a different library file that was not included in 'gpdk045_v_3_5'.

6 Reflection on Individual and Team work (PO(i))

6.1 Mode of TeamWork

We worked together in the AIC lab and the central library since it requires BUET wifi to log into the session for cadence virtuoso tools. Each member contributed to design and analysis of the project. Every challenge we faced was overcome in a collaborative manner. While one was doing the simulation work, other was doing exploration for theoretical understanding to come up with a solution for the design. Thus each member supported and collaborated with each other.

6.2Log Book of Project Implementation

Timeline	**Milestone achieved**
Week 9	Transmission gate and multiplexer design
Week 10	Observation of outputs
Week 11	Bandwidth measurement
Week 12	Ron and input capacitance measurement
Week 13	Level shifter design
Week 14	Charge injection and power dissipation measurement

7 Communication to External Stakeholders(PO(j))

7.1Executive Summary

The multiplexer project aimed to design and implement an analog 8:1 multiplexer using CMOS transmission gate logic and CMOS logic. Employing Cadence Virtuoso for schematic design and simulation, the project ensured signal integrity, bandwidth, and power consumption met specifications. Layout design and verification ensured adherence to design rules and manufacturability. The successful implementation of CMOS transmission gate logic enabled efficient signal routing, while CMOS logic facilitated precise control and selection of input channels. The project's outcomes hold implications for signal processing and data acquisition systems, offering improved functionality and performance in electronic circuit design.

8 References

[1] https://research.ijcaonline.org/volume99/number5/pxc3897911.pdf

[2] https://www.semanticscholar.org/paper/Design-Low-Power-High-Performance-8-%3A-1-MUX-using-(-Khandelwal/70f6652345fd863a5bcc083d7d5ab9d53a07ea49