WEST BENGAL STATE UNIVERSITY

B.Sc. Honours Part-I Examination, 2019

COMPUTER SCIENCE

PAPER-CMSA-I

Time Allotted: 4 Hours | Full Marks: 100

The figures in the margin indicate full marks.
Candidates should answer in their own words and adhere to the word limit as practicable.
All symbols are of usual significance.

Answer Question No. 1 and any *five* from the rest taking at least *one* from each group

1. Answer any ***ten*** questions from the following: 2×10 = 20

(a) Define Self complementary codes.

(b) What is the function of Boot Strap loader?

(c) Why decoder is called minterm generator?

(d) What is Race condition in flip flop?

(e) Find the value of y, where $(212)_y = (23)_{10}$

(f) What is 'Virtual ground'? How does it differ from actual ground?

(g) What is the replacement of D.C voltage sources in electronic equipments operating from A.C supply?

(h) How many flip-flops are required to build a mod-32 counter? What is the largest decimal number that can be stored in a mod-64 counter?

(i) Why is a JFET less temperature sensitive than a BJT?

(j) State the similarity between a multiplexer and a decoder.

(k) Show that if $xy = 0$ then $x \oplus y = x + y$

(l) Find the result of the following subtraction in the binary number system using 2's complement 1011.11 – 101.01

(m) Convert the BCD code 398 to its equivalent excess-3 code.

GROUP-A
(COMPUTER FUNDAMENTALS)

2. (a) Show that dual of the exclusive OR is equal to its complement. Prove or disprove whether it is true for the exclusive NOR. 2

(b) Convert the following Boolean expression, 3

$$Y = (A + BC)(B + \overline{C}A)$$ into standard SOP form.

(c) Design a two-input XOR gate using a two input NAND gate. 2

(d) Express (–19.750) in 2's complement representation. Use hexadecimal notation to compress the data. 3

(e) What do you mean by biased exponents in storing floating point numbers? 2

(f) Simplify the following Boolean function: 3

$$F = P\overline{Q}\,\overline{R} + \overline{P}\,\overline{Q}RS + R\overline{S} + P\overline{R}S + \overline{P}RS$$

(g) What do you mean by High-level languages? 1

3. (a) Simplify the expression $F = \Pi(1,3,5,8,9,11,15)$ using K-map and realize the optimized function using only NOR gates. 3+2

(b) Write down the pseudocode to convert a number (containing integer and fractional part) in the decimal system to any non-decimal system. 5

(c) What are the functions of BIOS in PCs? 2

(d) Point out the basic differences between software and firmware. 2

(e) What is Unicode? What is the advantage of using it? 2

GROUP-B

(INTRODUCTION TO BASIC ELECTRONICS)

4. (a) A voltage $V(t) = V_0 \sin \omega t$ is applied across a capacitance *C*. Find the expression for the value of instantaneous current *i* through *C* and hence show that the current *i* leads the voltage *V* by 90º. 4+1

(b) How can an operational amplifier be used as an integrator? 4

(c) With a neat circuit explain the operation of a bridge rectifier and also calculate its efficiency. 4+3

5. (a) Draw and explain the operation of CMOS NAND / NOR gate with an example. 5

(b) What are the differences between FET and transistor? 4

(c) Write down the operating principle of LED and its use. 3

(d) Distinguish between Zener Breakdown and Avalanche Breakdown. 4

GROUP-C

(DIGITAL SYSTEM DESIGN)

6. (a) Using J-K flip-flops draw a configuration of a 4-bit shift register. Explain how data are shifted in the configuration you have made. 3+4

(b) "74LS138 is a 3-line-to-8-line decoder" — What is the meaning of the statement? Why is such a decoder called a "binary-to-octal" decoder? 3+3

(c) Draw a logic diagram for a BCD-decimal decoder. 3

7. (a) Realize a full subtractor circuit using (4×1) MUX. Show each steps properly. 4

(b) What is Debouncer Circuit? What is the use of it? 4+1

(c) How can the problem be solved when S=R=1, in S-R Flip-flop? Design a JK flip-flop with NAND gates only. 2+3

(d) Write down the real life applications of a delay flip-flop and a seven segment display. 2

GROUP-D

8. (a) Differentiate between address bus, data bus, control bus. 3

   (b) Explain the following arithmetic expression using 3+3

   (i) Two address instruction,

   (ii) Three address instruction.

$$A = \frac{(X - Y) \times (P - Q)}{4}$$

   (c) What is Von Neumann Bottleneck? How it can be resolved? 2+2

   (d) Explain with the help of micro instruction, the instruction cycle is combination of both Fetch cycle and execute cycle. 3

9. (a) What are different addressing modes available in general purpose processor? State and justify the number of memory references that are needed for each type of addressing. 4

   (b) A computer employs RAM chips of 256×8 and ROM chips of 1024×8. The computer system needs 2 kB of RAM, 4 kB of ROM and four interface units, each with four registers. A memory mapped I/O configuration is used. The two highest order bits of the address bus are assigned 00 for RAM, 01 for ROM and 10 for interface registers. 2+4+3

   (i) How many RAM and ROM chips are needed?

   (ii) Draw a memory address map for the system.

   (iii) Give the address range in hexadecimal for RAM, ROM and interface.

   (c) Discuss the relative merits and demerits of different bus arbitration techniques. 3

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