# CS311 Lab Report
# Assignment 6 - Caches

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## 1 Introduction

We upgrade the pipelined processor model to a discrete event simulator model and add caches to make it faster.

## 2 Commands

In order to simulate the processor, we run the commands in order:

```
ant
ant make-jar
java -jar <path_to_simulator.jar> <path_to_config_file> <path_to_output_file> <path_to_object_file>
```

## 3 Results

### 3.1 Task 1

L1d cache fixed

| Benchmark | 16 Bytes | 128 Bytes | 512 Bytes | 1024 Bytes |
|---|---|---|---|---|
| fibonacci.out | 0.023 | 0.047 | 0.043 | 0.055 |
| prime.out | 0.073 | 0.044 | 0.042 | 0.040 |
| descending.out | 0.022 | 0.107 | 0.095 | 0.087 |
| evenorodd.out | 0.019 | 0.018 | 0.018 | 0.018 |
| palindrome.out | 0.119 | 0.064 | 0.060 | 0.056 |

### 3.2 Task 2

L1i cache fixed

| Benchmark | 16 Bytes | 128 Bytes | 512 Bytes | 1024 Bytes |
|---|---|---|---|---|
| fibonacci.out | 0.057 | 0.056 | 0.056 | 0.055 |
| prime.out | 0.040 | 0.040 | 0.040 | 0.040 |
| descending.out | 0.094 | 0.092 | 0.089 | 0.087 |
| evenorodd.out | 0.018 | 0.018 | 0.018 | 0.018 |
| palindrome.out | 0.057 | 0.056 | 0.056 | 0.056 |

### 3.3 Task 3

The relationship between cache size, cache latency, and perfor- mance is complex and depends on the specific characteristics of the benchmarks, as well as the access patterns of both instructions and data in the cache. Bal- ancing cache size and latency is essential to optimize overall system performance for a range of workloads.