Assignment 6

Duration: 2 weeks

We will begin developing a Monitor Synthesizer for properties written in Linear Temporal Logic. As a first step, in this assignment, we will develop a tool that

1. uses the LTL2BA to convert a given property specified in LTL to its equivalent Buchi Automaton. You can experiment with the properties from Assignment 5, as well as make up at least 3 more properties of your own.
2. employs Algorithm 1 described in [1] to determine the Finite Automata corresponding to the good and bad prefixes (if they exist). A more elaborate description of the same procedure is available in [2] (Section 3.2). Print the Finite Automata on screen.

[1] Doron Peled, Klaus Havelund, “Refining the Safety–liveness Classification of Temporal Properties According to Monitorability”, Models, Mindsets, Meta: The What, the How, and the Why Not?, 2018.
[2] Benny et al., “faRM-LTL: A Domain-Specific Architecture for Flexible and Accelerated Runtime Monitoring of LTL Properties”, Runtime Verification, 2024.