MOD 5 Counter TASK 2

Counting states:-

000

001

010

011

100

Task-2(Mod-5 Counter Physical Design)

• Designed Mod-5 Counter in the Xilinx ISE.

• Completed the netlist to layout design flow using cadence Genus and Innovus.

• All the files are uploaded in the Github with the link: https://github.com/Anirban792/mod5pd.git

• Path of the folder is: "/afs/iitd.ac.in/user/j/jv/jvl212382/AUG\_ANIRBAN\_SIM/counter"

• Verilog file: Created in the Xilinx ISE (performed its simulation and synthesis)

VERILOG Code:

`timescale 1ns / 1ps

//////////////////////////////////////////////////////////////////////////////////

// Company:

// Engineer:

//

// Create Date: 21:31:59 10/06/2021

// Design Name:

// Module Name: mod8

// Project Name:

// Target Devices:

// Tool versions:

// Description:

//

// Dependencies:

//

// Revision:

// Revision 0.01 - File Created

// Additional Comments:

//

//////////////////////////////////////////////////////////////////////////////////

module mod8(clk,rst,out

);

input clk,rst;

output [2:0]out;

reg [2:0]out;

always @(posedge clk)

begin

if(rst==0)

out <= 0;

else if(out<4)

out <= out+1;

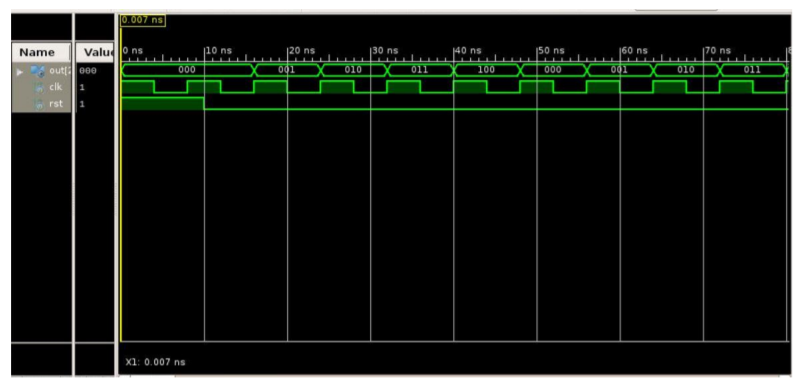
else

out <= 0;

end

endmodule

Simulation Waveform:



Netlist File: Generated in the Genus tool

// Generated by Cadence Genus(TM) Synthesis Solution 19.12-s121\_1

// Generated on: Oct 17 2021 21:27:08 IST (Oct 17 2021 15:57:08 UTC)

// Verification Directory fv/mod8

module mod8(clk, rst, out);

input clk, rst;

output [2:0] out;

wire clk, rst;

wire [2:0] out;

wire n\_0, n\_1, n\_2, n\_3;

DFQZRM2RA \out\_reg[2] (.CK (clk), .D (n\_0), .RB (out[0]), .Q

(out[2]));

DFQZRM2RA \out\_reg[1] (.CK (clk), .D (n\_3), .RB (n\_2), .Q (out[1]));

MXB2M1RA g115(.A (n\_1), .B (out[0]), .S (out[1]), .Z (n\_2));

AN2M2R g114(.A (n\_3), .B (out[1]), .Z (n\_0));

NR2B1M2R g116(.B (out[2]), .NA (rst), .Z (n\_3));

DFZRM2RA \out\_reg[0] (.CK (clk), .D (n\_3), .RB (n\_1), .Q (out[0]),

.QB (n\_1));

endmodule

TCL file used for the Synthesis in genus

set search\_path "/afs/iitd.ac.in/service/tools/public/asiclib/umcoa/L65/libraries/UMC65LLSC/synopsys/ccs"

set\_attribute lib\_search\_path "/afs/iitd.ac.in/service/tools/public/asiclib/umcoa/L65/libraries/UMC65LLSC/synopsys/ccs"

set\_attribute hdl\_search\_path "./AUG\_ANIRBAN\_SIM/counter"

set\_attribute library "uk65lscllmvbbr\_100c25\_tc\_ccs.lib"

read\_hdl mod8.v

elaborate

check\_design -unresolved

read\_sdc ./upcounter\_8bit.sdc

synthesize -to\_mapped -effort medium

write\_hdl > ./typical/counter\_netlist.v

write\_sdc > ./typical/counter.sdc

SDC file generated(timing constraints):

# ####################################################################

# Created by Genus(TM) Synthesis Solution 19.12-s121\_1 on Sun Oct 17 21:27:08 IST 2021

# ####################################################################

set sdc\_version 2.0

set\_units -capacitance 1000fF

set\_units -time 1000ps

# Set the current design

current\_design mod8

create\_clock -name "clk" -period 650.0 -waveform {0.0 390.0} [get\_ports clk]

set\_clock\_gating\_check -setup 0.0

set\_input\_delay -clock [get\_clocks clk] -add\_delay 60.0 [get\_ports rst]

set\_output\_delay -clock [get\_clocks clk] -add\_delay 95.0 [get\_ports {out[2]}]

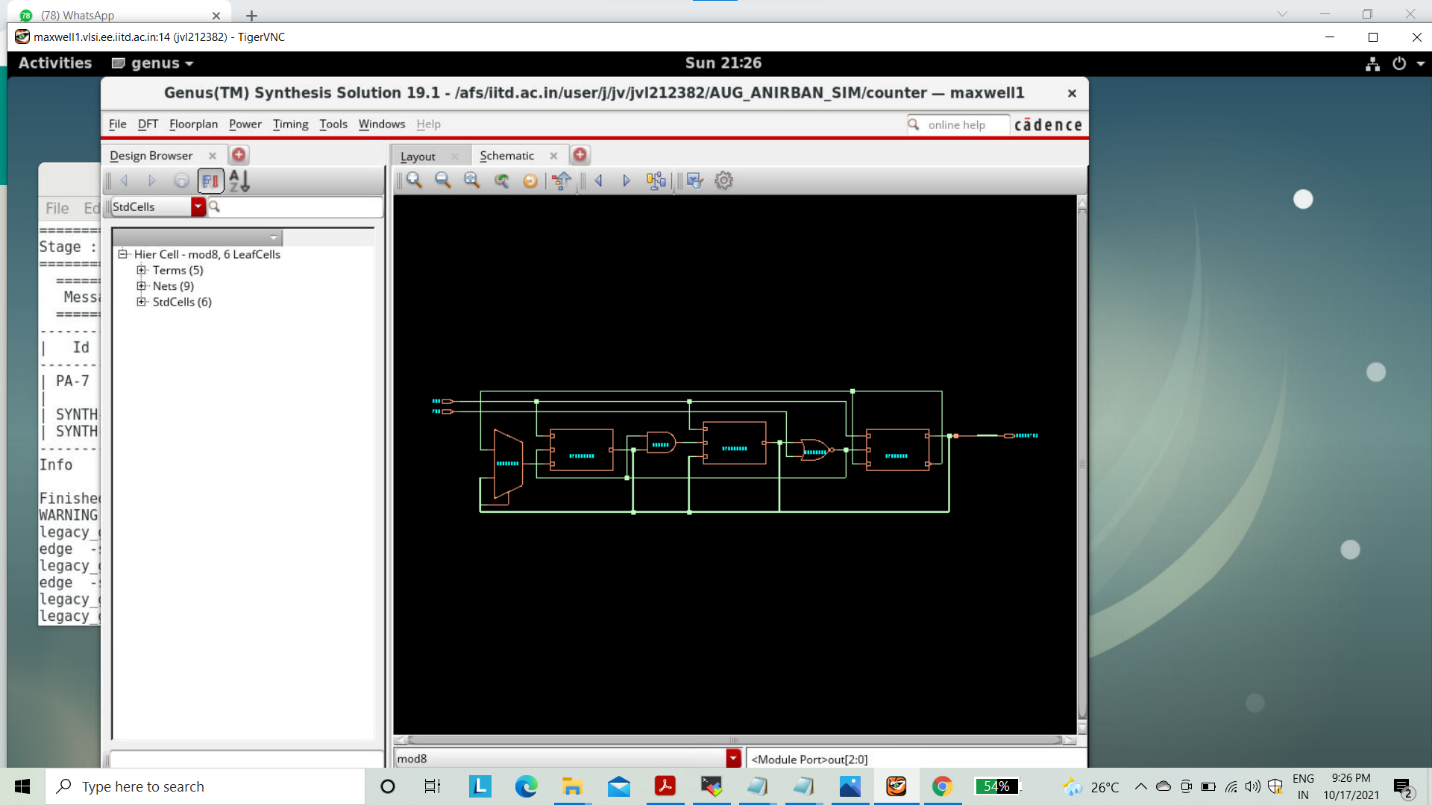
set\_output\_delay -clock [get\_clocks clk] -add\_delay 95.0 [get\_ports {out[1]}]

set\_output\_delay -clock [get\_clocks clk] -add\_delay 95.0 [get\_ports {out[0]}]

set\_wire\_load\_mode "top"

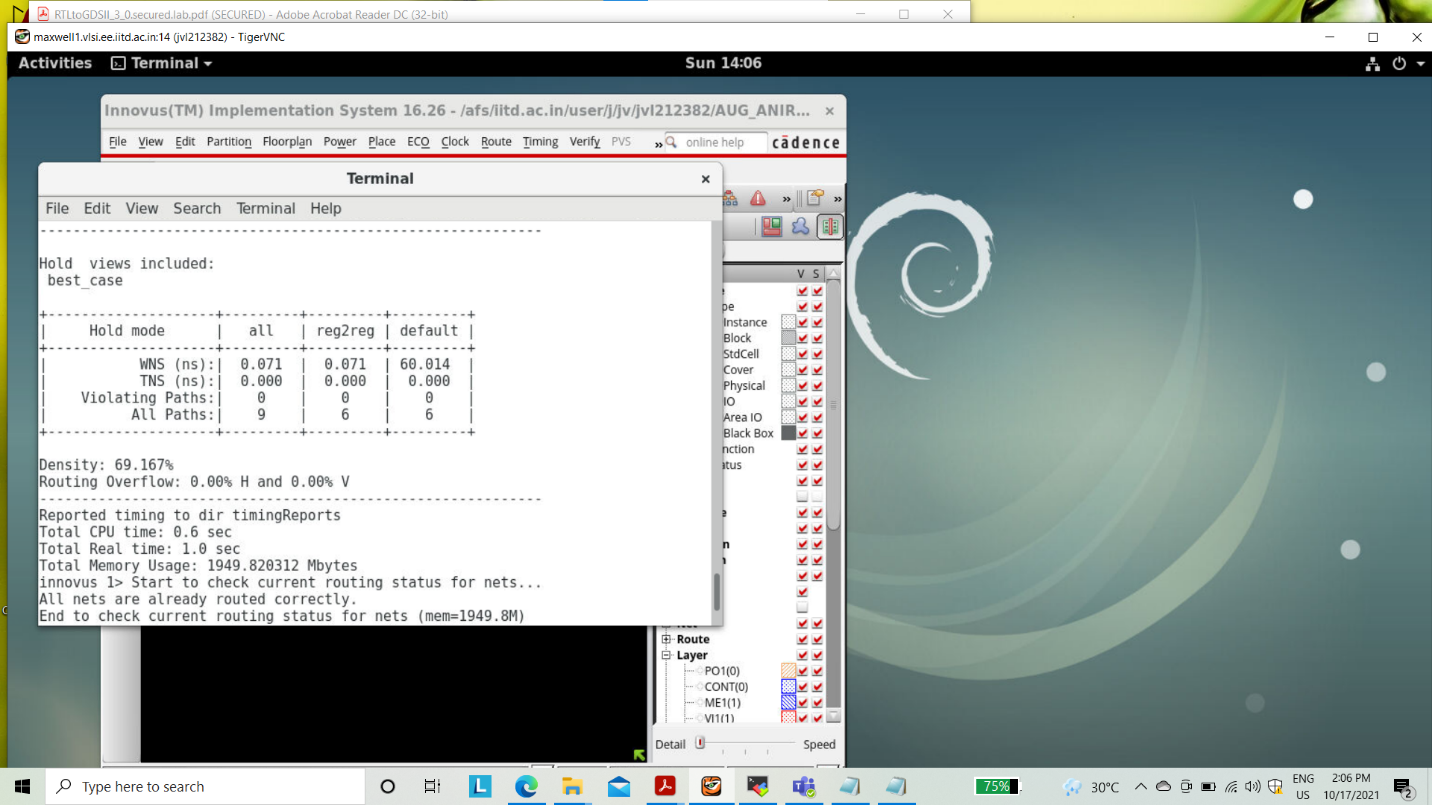
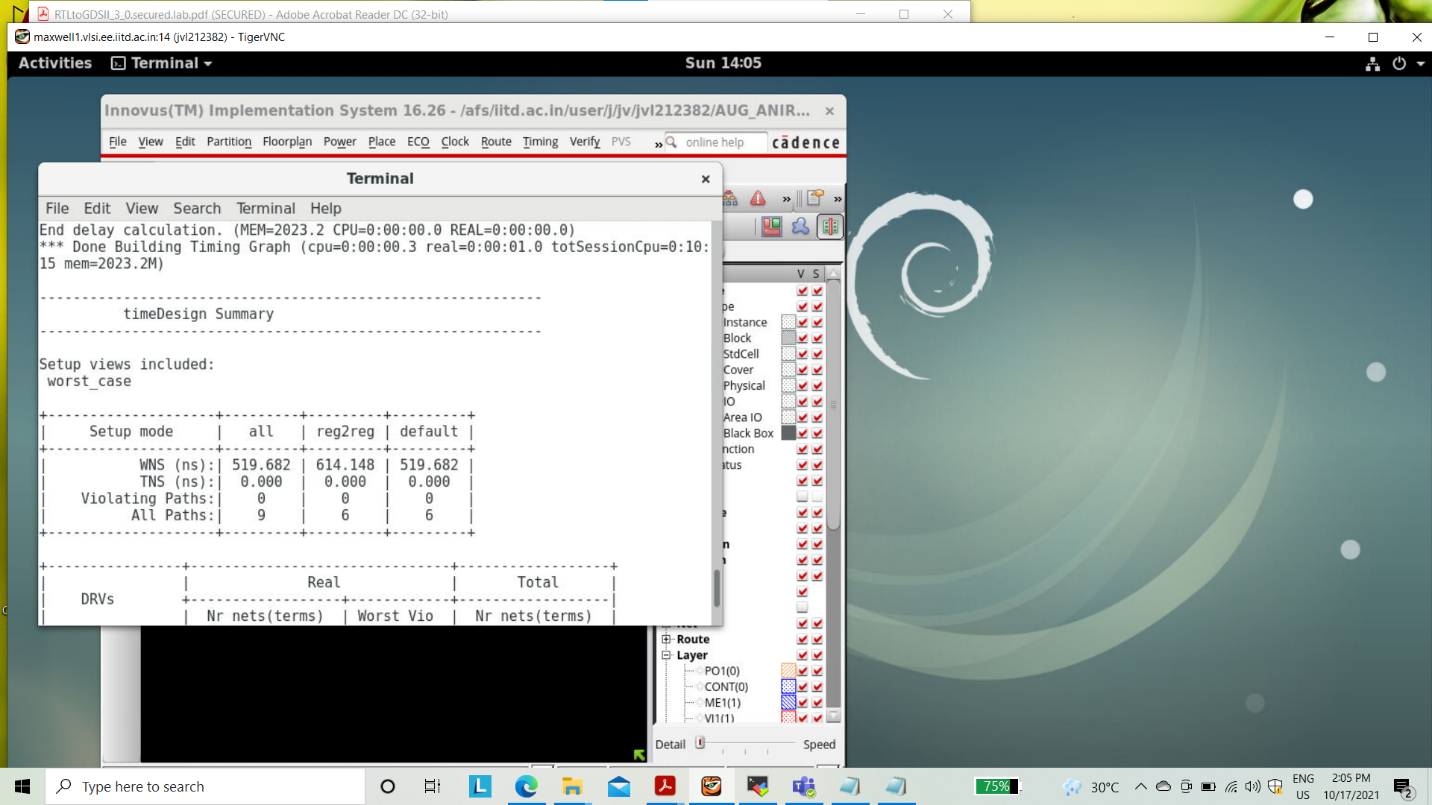
set\_clock\_uncertainty -setup 35.0 [get\_clocks clk]

set\_clock\_uncertainty -hold 0.02 [get\_clocks clk]

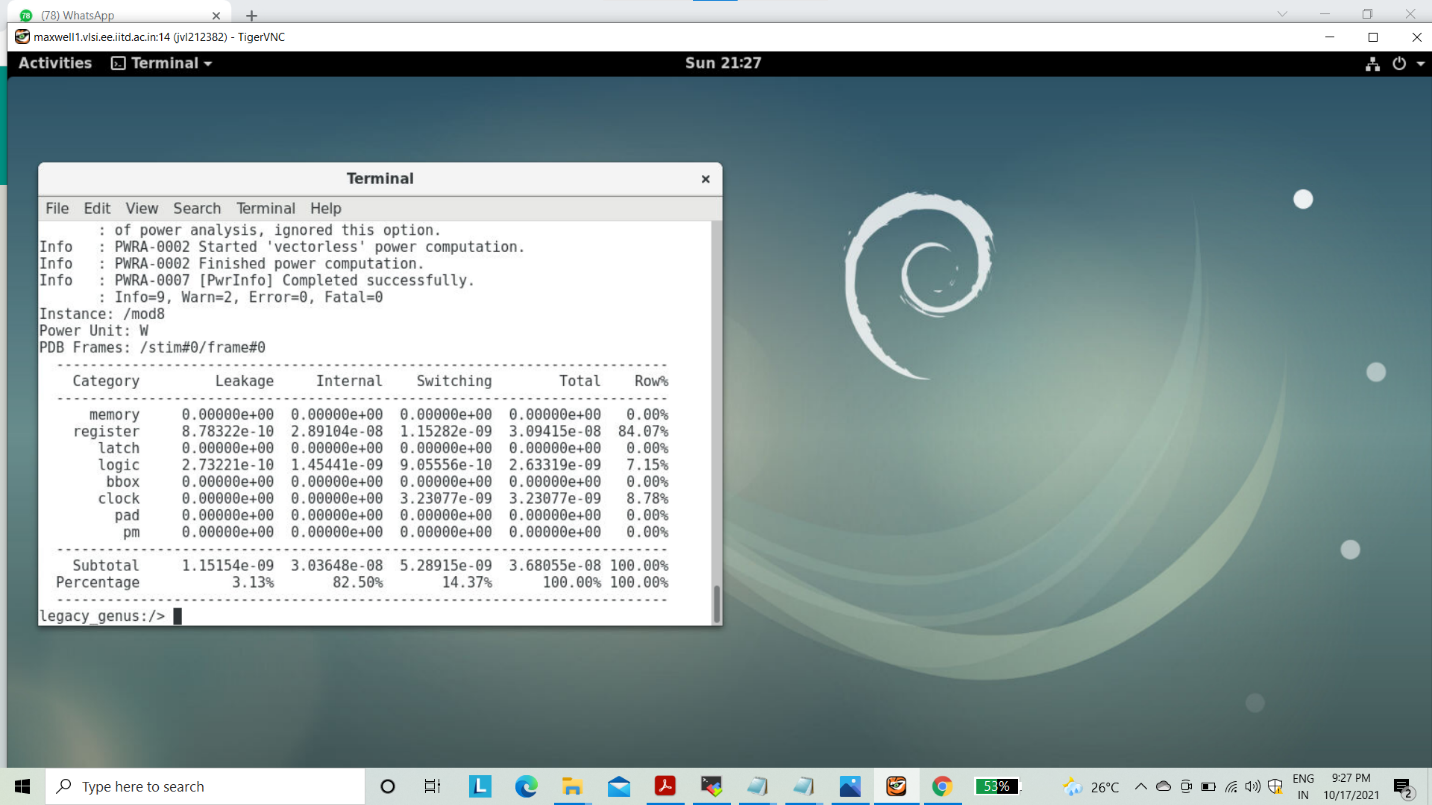
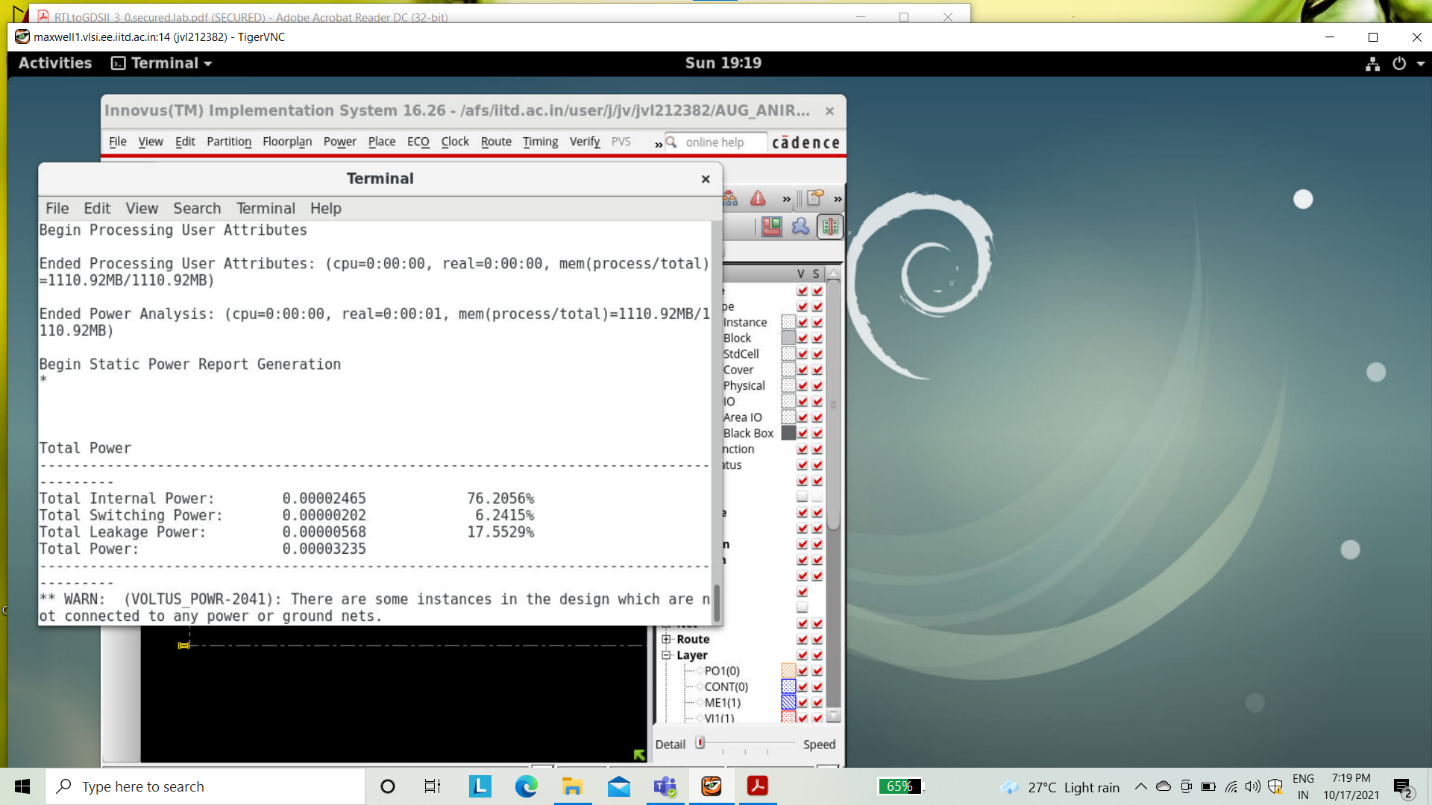
Schematic Generated in Genus GUI:

Timing Report

Report Timing (Pre-CTS) Setup and Hold timing report are generated. As there is no negative slack, so there is no timing violation.



SETUP & HOLD TIME FROM DELAY7 FILE:- 0.038, 002

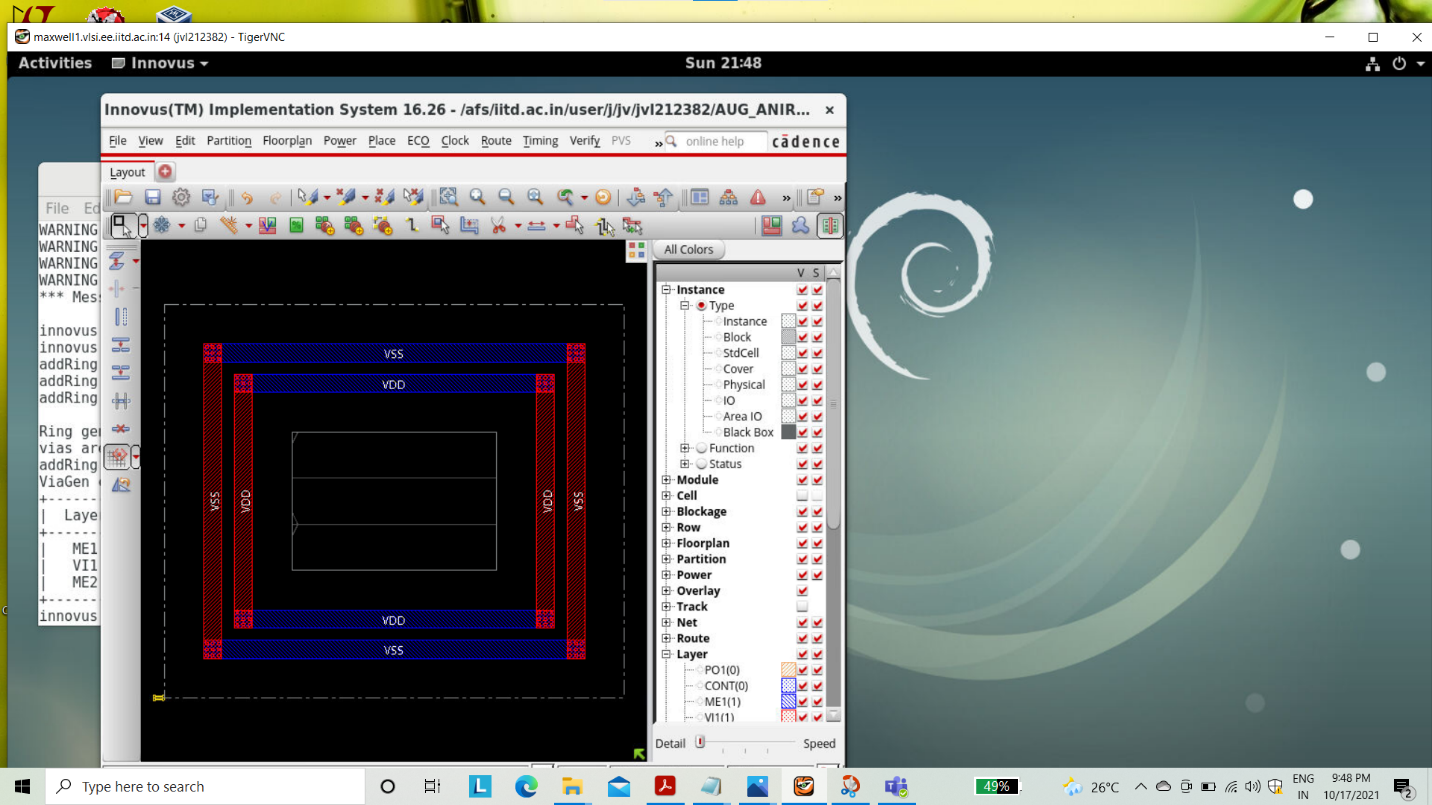
Power Report

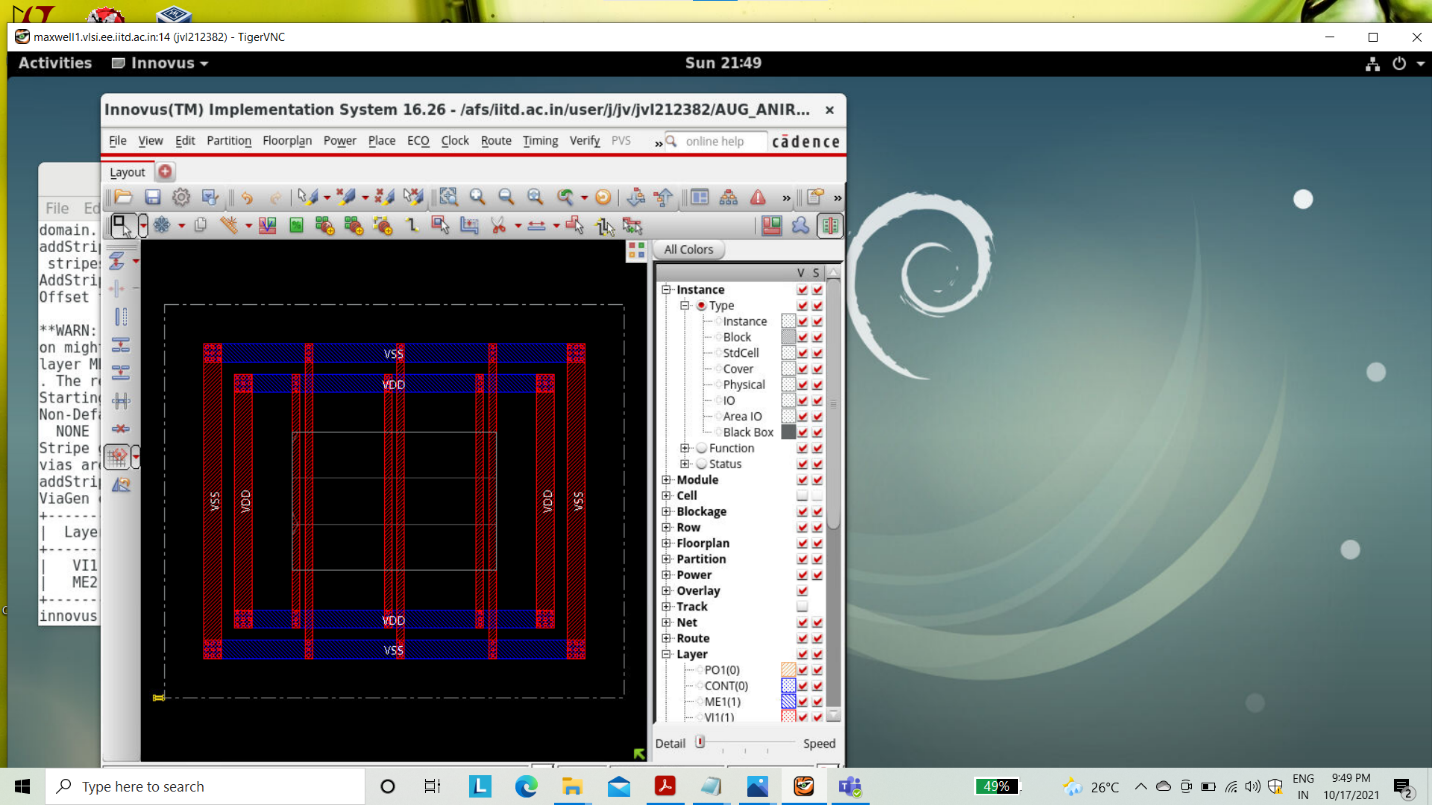
Floorplanning

Initial FloorPlan is displayed in the display area as given below

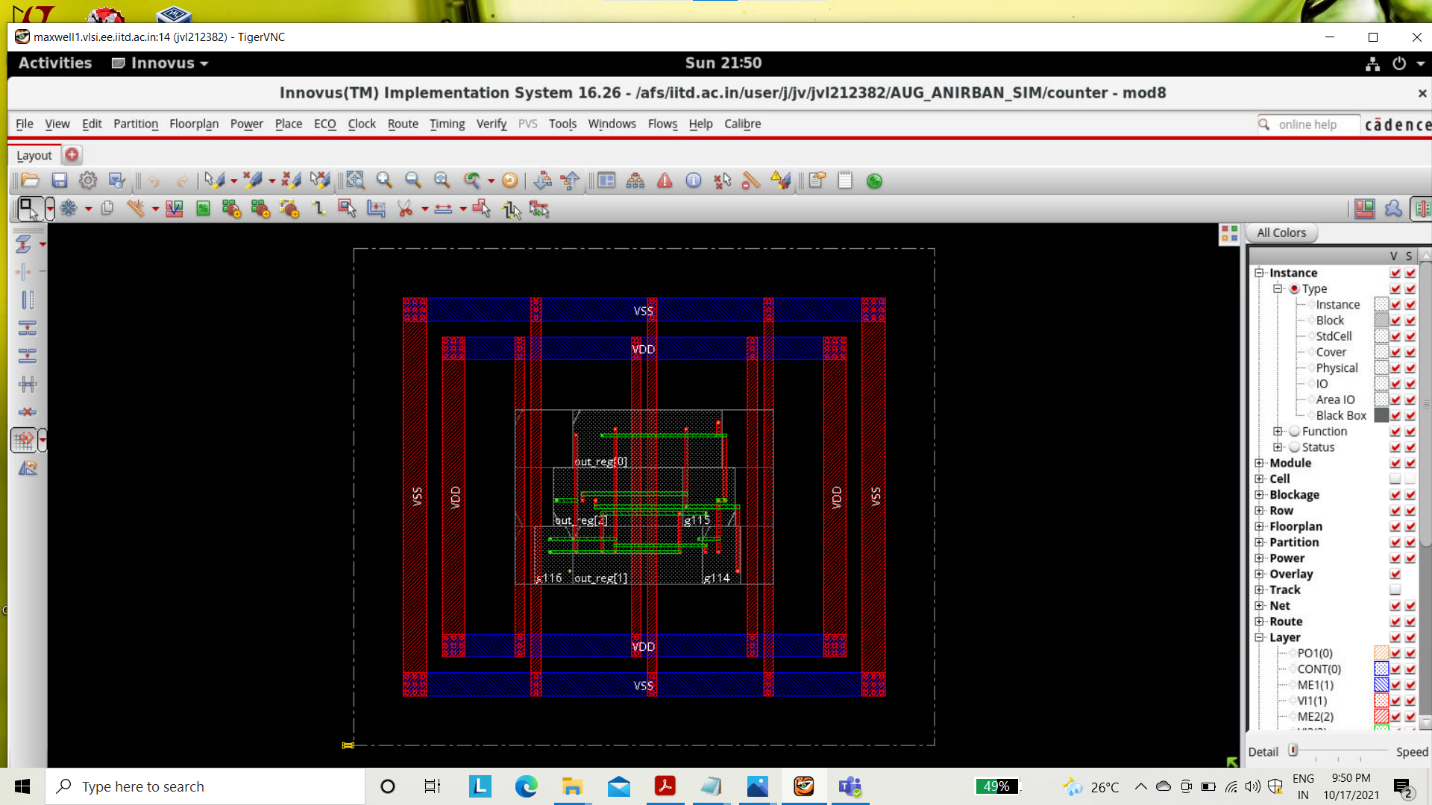
Power Planning

Power ring and power strips are included with proper spacing and width. Metal layer M1(1) and M2(2) are chosen for this.

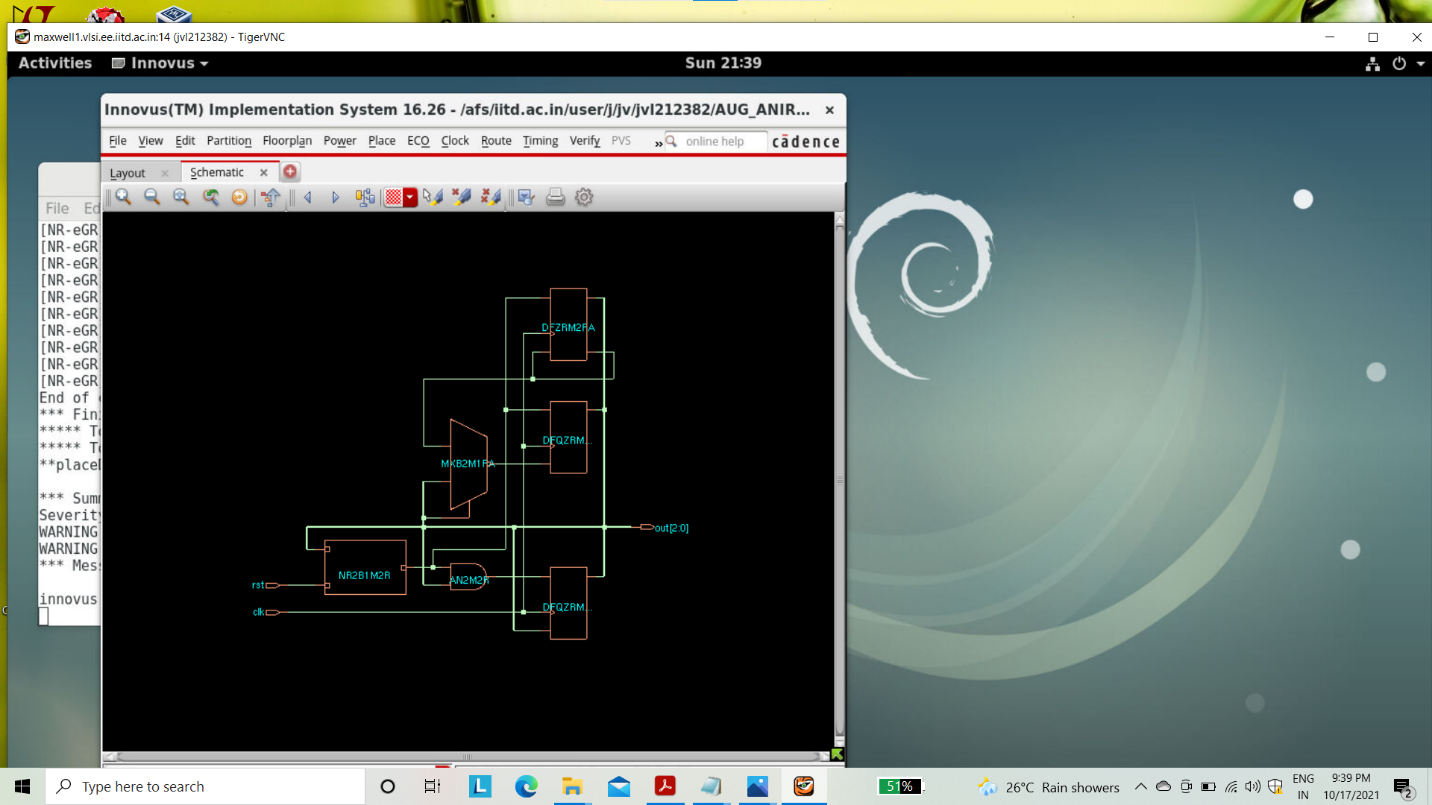




PLACEMENT OF STANDARD CELL



INNOVUS SCHEMATIC



Clock Tree Synthesis(CTS) clock tree spec file is created.

Report Timing (Post-CTS)

