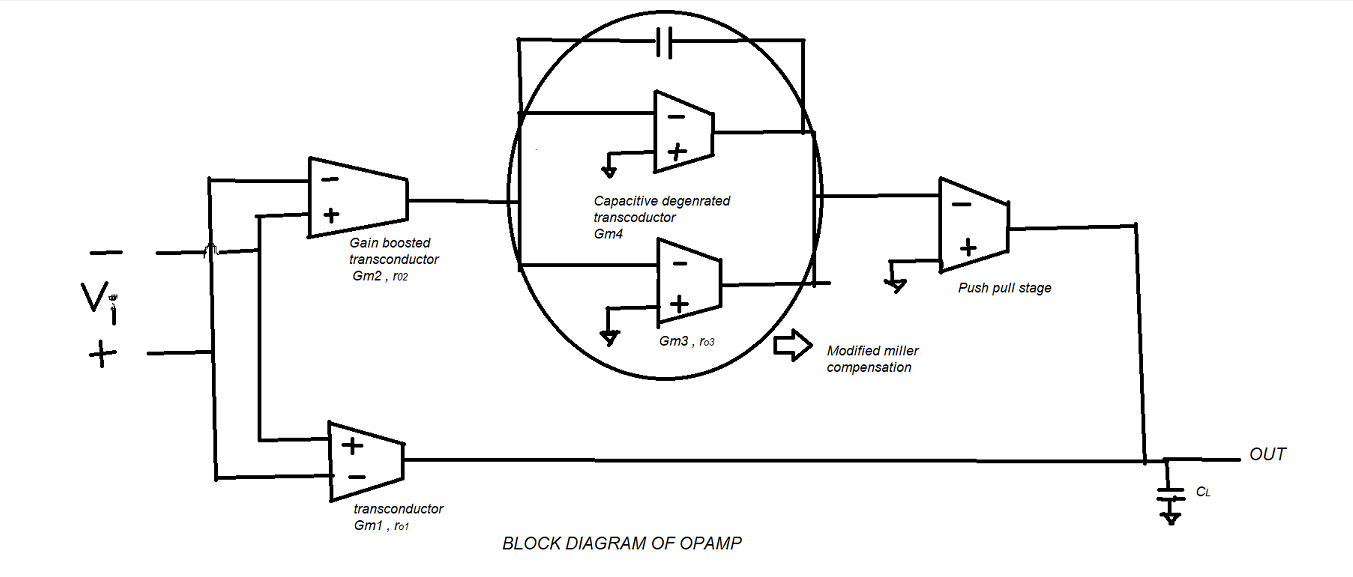
**Target specifications**

|  |  |
| --- | --- |
| UGB | 10GHz |
| DC Gain | 50dB |
| Phase Margin | >50 |
| Gain Margin | 10dB |
| Load Capacitance | 500fF |
| FOM | 450 |
| PSRR of Bandgap | 40 |
| Noise of Bandgap | 30ppm/C |
| Power of circuit | 30mW |
| Input Referred noise(till UGB) | 80uVrms |

**Opamp**



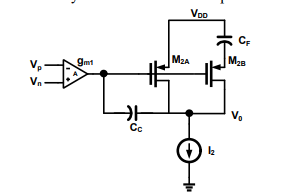
**BLOCK DESCRIPTION:**

Gm1: It is realized using a simple 5T differential pair.

Gm2: This block is realized using a gain boosted single stage OPAMP. The aim of this circuit is to touch the ceiling of 10GHz UGB. But for that we haven’t compromised blindly on gain. To get a decent gain this method has been employed. As the input to Gm1 and Gm2 are the same, The same NMOS structure of the Gm1 has been used along with PMOS connected in parallel with that of the Gm1’s. Obviously on top of this common NMOS stage a gain booster has been connected made up of NMOS.

**MODIFIED MILLER COMPENSATION NETWORK:**

In order to make the layout area efficient a degenerate capacitive PMOS has been used in parallel with a conventional PMOS. The capacitor degeneration creates a zero which can be tuned to perform the famous frequency compensation for UGB enhancement.



PUSH PULL STAGE: This stage has been realized with inverter.

**Bandgap**

Bandgap reference based on the exponential properties of the BJT devices with a moderate temperature coefficient of 65ppm/C, later this has become the golden reference circuit designed on the modern CMOS technologies. The main principle of this circuit is to generate a Proportional to Absolute temperature (PTAT) voltage, complementary to absolute voltage (CTAT) scale them and add to obtain a temperature-independent reference voltage, the traditional pnp transistor based  bandgap reference suffers from flicker noise and other noise sources of the latch-up circuitry. This gives a complete different figure from the traditional used bandgap by exploiting the sub-threshold region of the mosfet to generate golden reference for a voltage range upto < 1V by varying the resistance values of the circuit. A additional STP circuit is provided with the schematic.

