Tutorial Questions (Part 2 continued)

ASM State Machine Design

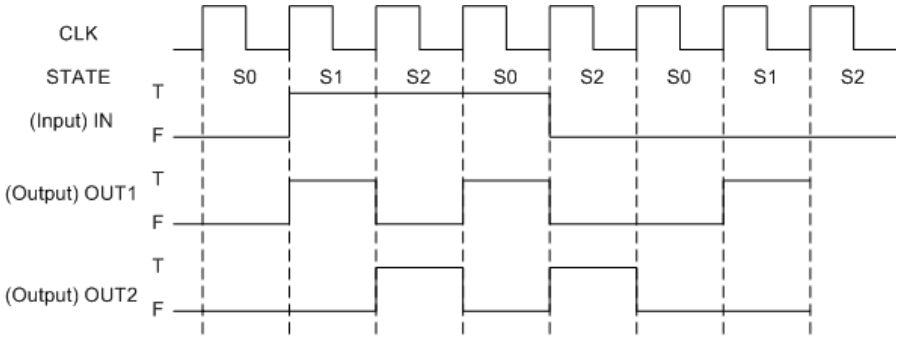
Please attempt the self-study questions (labeled "SS").

20. A state machine's output **Q** depends on the value of an input signal X in the *current* and *previous clock cycles*, i.e., $\mathbf{X_t}$ and $\mathbf{X_{t-1}}$ as specified below:

$\mathbf{X_t}$	$\mathbf{X_{t-1}}$	$\mathbf{Q^+}$
0	0	**Q**
0	1	1
1	0	0
1	1	**Q**

Design the state machine using (a) J-K flip-flops and (b) D flip-flops. Does one design need more components than the other? Why?

21. For the state machine with the timing diagram shown in the figure below:
    (a) draw its functional block diagram clearly showing the input & output signals,
    (b) construct the *ASM* chart,
    (c) determine the next state table,
    (d) draw a detailed circuit diagram showing the realization of the state machine in the traditional method using D flip-flops, and
    (e) write a *VHDL* description (i.e., program) for the state machine.



SS10. A ***3-bit synchronous counter*** counts in one of two sequences depending on a 1-bit *synchronous control input*, EVEN. When EVEN is false, the counter behaves as *a normal 3-bit mod-8 up-counter*, otherwise it counts in the sequence: .. 0, 2, 4, 6, 0, 2 …

(a) What is meant by "*synchronous input*"?
(b) Draw the *ASM* chart for the counter.
(c) If the counter's current output is "2", under what conditions will it output "3" in the next state?
(d) Implement the counter using *D-Flip-flops* and any additional logic devices. Clearly show the steps in your design and verify the correct operation of the counter.

(e) Using additional logic circuits, show how you would incorporate a "*terminal count*" output, TC, which is asserted if the state is 7 and EVEN=0, or if the state is 6 and EVEN=1.

22. Given the *ASM* chart of a state machine shown in Figure (a) below,
    (a) complete the corresponding timing diagram in Figure (b),
    (b) construct the next state table for the state machine,
    (c) draw a detailed circuit diagram showing the realization/implementation of the state machine in the **traditional method**,
    (d) draw a detailed circuit diagram showing the realization/implementation of the state machine in the **PLA method** using a PLA device with 4 inputs, 4 outputs and 8 product terms.

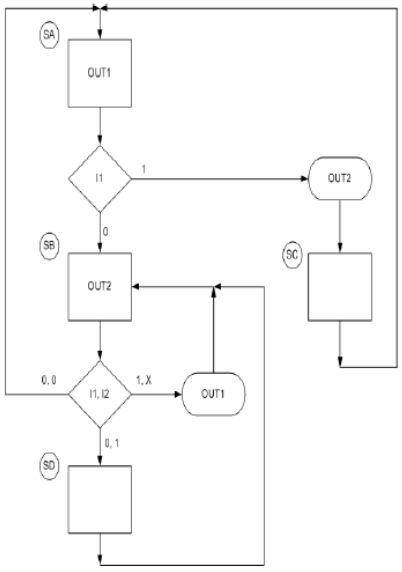


Figure (a)

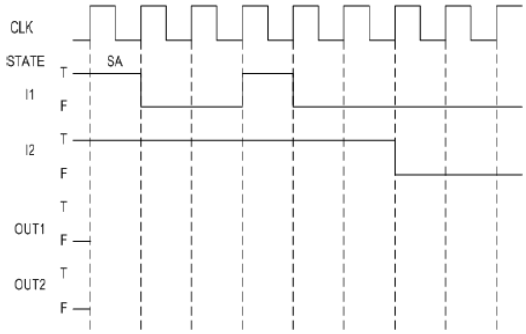
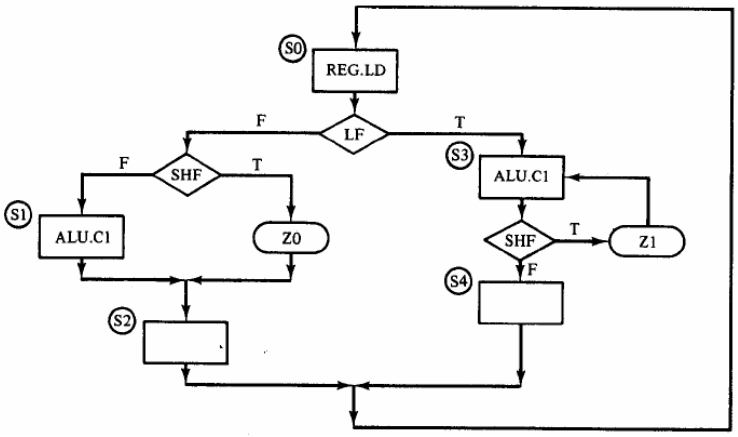


Figure (b)

23. Given the *ASM* chart below:



(a) Draw a functional block diagram of the state machine.
(b) Draw a block diagram of the state generator, clearly showing the inputs, outputs, and the state flip-flops (D-FFs).
(c) Noting that ROMs can be used to realize *combinational logic functions*, realize the state machine by using a ROM. Draw the entire circuit, clearly showing all ROM connections and the ROM contents in `hexadecimal` form.

24. A digital circuit is to be designed to implement the "*snooze*" function of an alarm clock. The circuit signals are as follows:

Synchronous Inputs: `RING, RESET`.
Output: `ALARM`

The circuit remains in the "wait" mode until input `RING` is asserted for one clock period, at which time the circuit goes into the "snooze" mode by asserting `ALARM` for 10 seconds, waiting for 5 minutes and continuously repeating this cycle until the user resets the circuit causing `RESET` to be asserted for one clock period.

Derive the *ASM* chart and *identify* the *architectural elements* (i.e, *list* the elements and their functions) required for a hardware realization of this state machine. Write a *VHDL* program which realizes this state machine. You may assume that an accurate 1Hz clock is available as input.

SS11. A digital circuit has to be designed to find the number of 1's in an 8-bit input data.

The operation of this circuit is specified as follows: When the input `START` becomes 1 (for one clock cycle), an 8-bit number is input into the circuit one-bit per consecutive clock cycle via the circuit's 1-bit input `DATA`. The circuit evaluates and outputs `X`, a 3-bit output signal which is the number of 1's received up to the current instant. After the 8-bits have been received, the circuit asserts the output signal `DONE` and clears `X`.

Derive the *ASM* chart for this circuit. Write a *VHDL* program which realizes the circuit and verify its performance using available simulation tools.

25. A synchronous state machine needs to be designed to *count people entering and leaving a room*. The room has a *separate* entrance and exit. Each is equipped with a sensor to detect people *coming in through the entrance* or *leaving through the exit*. The sensors provide signals `ENTER` (when a person enters) and `LEAVE` (when a person exits), which are **TRUE** for one clock period. The entrance and exit are each narrow enough for only one person to pass through at a time, but it is possible for one person to enter *while* another is exiting during one clock period. The machine should output an `EMPTY` signal when nobody is in the room and a `FULL` signal when there are 3 people (*the maximum allowed*) in the room. The `EMPTY` and `FULL` signals should be asserted as soon as the conditions are satisfied, i.e. before the next active clock transition. Nobody will be allowed into the room while `FULL` is asserted. Derive the *ASM* chart and write a *VHDL* program which realizes this state machine. You may assume that an accurate 1Hz clock is available as input.