EE2020

Digital Fundamentals

(L6: Logic IC families)

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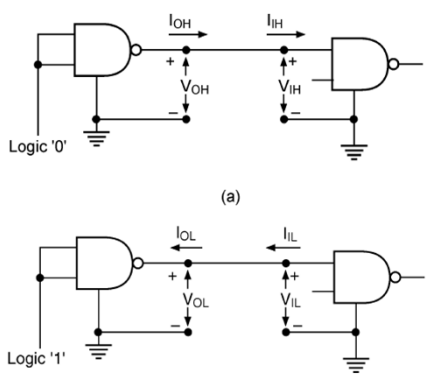
Outline

- Introduction to digital IC technologies
- Logic gate characteristics
- CMOS logic gates
- TTL logic gates
- Commercial logic families
- CMOS-TTL Interfacing

Logic gate characteristics

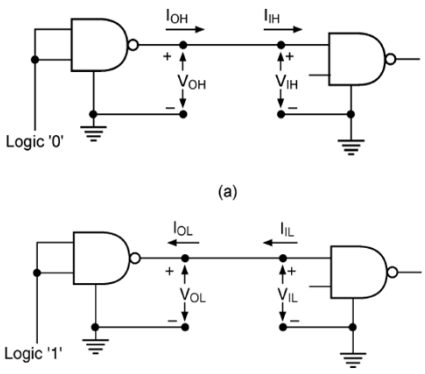
- **Static parameters**
  - V_{OL} → Maximum Logic LOW output voltage
  - V_{OH} → Minimum Logic HIGH output voltage
  - V_{IL} → Maximum Logic LOW input voltage
  - V_{IH} → Minimum Logic HIGH input voltage
  - NM_H → Noise margin high
  - NM_L → Noise margin low
  - I_{OL}/I_{OH} → Logic LOW/HIGH output currents
  - I_{IL}/I_{IH} → Logic LOW/HIGH input currents (for TTL only)
  - Power dissipation
- **Dynamic parameters**
  - Propagation delay
  - Fan-out

V_{OH}, V_{OL}, V_{IH}, V_{IL}



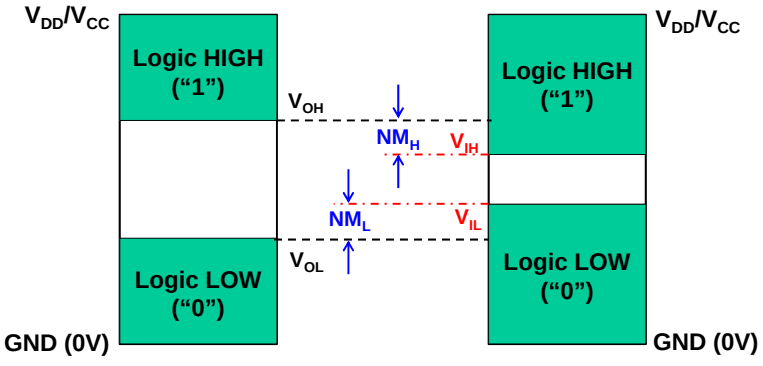
- **V_{OH}** is minimum output voltage that establishes valid logic high to the following gate
- **V_{OL}** is the maximum output voltage that established valid logic low to the following gate
- **V_{IH}** is the minimum valid logic high input voltage
- **V_{IL}** is the maximum valid logic low input voltage

I_{OH}, I_{OL}, I_{IH}, I_{IL}



- I_{OH} is maximum current that can flow out of an output when output voltage maintains a valid logic high
- I_{OL} is the maximum current that can flow into an output when output voltage maintains a valid logic low
- I_{IH} is the current flowing into or out of an input when the input voltage is a valid logic high
- I_{IL} is the current flowing into or output an input when the input voltage is a valid logic low

Noise margin (NM_H, NM_L)

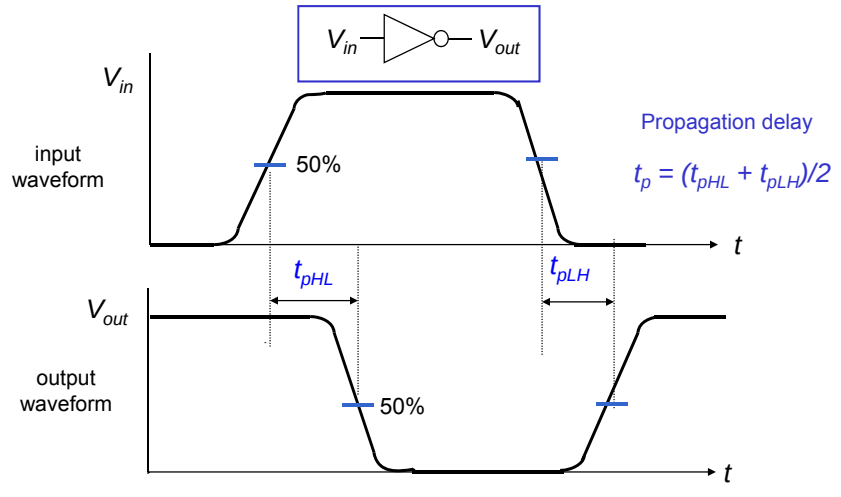


$$NM_H = V_{OH} - V_{IH}$$
$$NM_L = V_{IL} - V_{OL}$$

Power Dissipation

- Represents the amount of power needed by the gate. Often expressed in mW (milliwatts).
- Calculated from the supply voltage V_{CC} and the current I_{CC} that is drawn by the circuit.
- Power dissipation $P_D = V_{CC} * I_{CC}$
- Current drawn depends on the logic state of gate.

Propagation delay

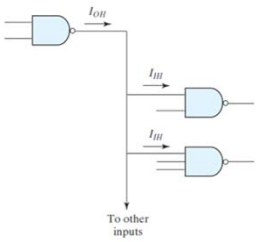


Fan-Out

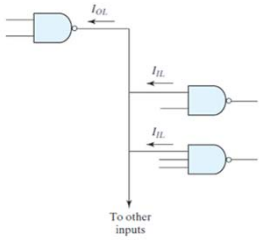
- Determines how many standard loads can be connected to the output of a gate
  - A standard load is defined as the amount of current needed by an input of another gate in the same logic family
  - Loading is also used to indicate fan-out.
- The output of a gate can supply a limited amount of current. Above that it is said to be overloaded.
- Each input of a gate also requires current
- Each additional connection adds to the gate load
- Exceeding the maximum load may cause malfunction

Fan-Out

Output is logic HIGH:



Output is logic LOW:



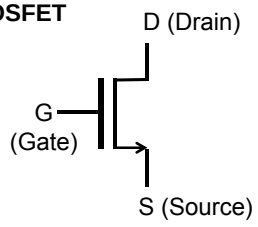
- Calculated from the amount of current available in the gate-output to that is needed in the input.
- Fan-out = min(I_{OH}/I_{IH}, I_{OL}/I_{IL})
- Example: standard TTL gates
  I_{OH} = 400 μA, I_{IH} = 40 μA, I_{OL} = 16 mA, I_{IL} = 1.6 mA
  - Fan-out = min(400/40, 16/1.6) = 10
  - The maximum number of gates that can be connected (or driven) is 10

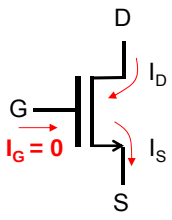
Digital IC technologies

- Digital integrated circuits can be designed in different technologies
- Technology will impact on the performance of ICs
- The two mainstream technologies are
  - CMOS IC technology
  - Bipolar IC technology
- CMOS IC technology is based metal-oxide-semiconductor field-effect transistors (MOSFET)
- Bipolar IC technology is based on bipolar junction transistors (BJT)

MOSFET

***n*-MOSFET**

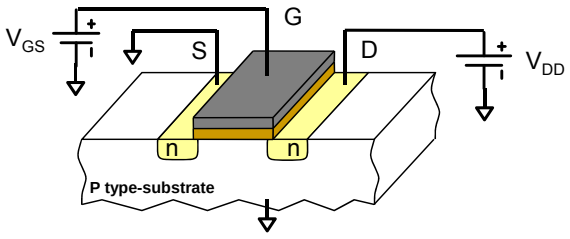




$$I_D = IS$$
$$I_D = f(VGS)$$
$$\Delta I_D = \frac{df(VGS)}{dV_{GS}} \Delta V_{GS}$$

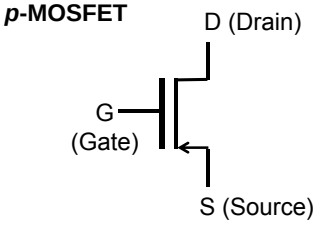
Small V_{GS} change can induce large I_D change → amplification

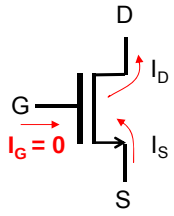
MOSFET is a voltage-controlled device



MOSFET

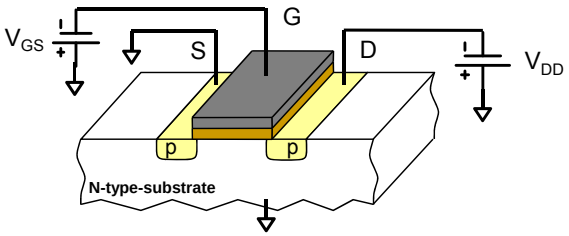
***p*-MOSFET**





$$I_D = IS$$
$$I_D = f(VGS)$$
$$\Delta I_D = \frac{df(VGS)}{dV_{GS}} \Delta V_{GS}$$

Small V_{GS} change can induce large I_D change → amplification



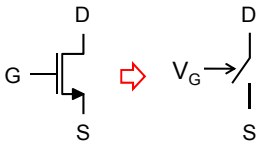
Logic ICs based on MOS technology

- **PMOS or NMOS**
  - The early MOS technology was based on either PMOS or NMOS only. It was later replaced by CMOS technology.
- **CMOS (Complementary MOS)**
  - Both NMOS and PMOS are used in the technology
  - CMOS static logic is used to implement logic gates
  - The advantages of CMOS static logic are
    - Full output swing from ground to supply voltage → high noise margin;
    - There is always a low impedance path from the output to ground or supply voltage
    - No static power dissipation (only one transistor is on)
    - No static input current → very high input impedance (input is capacitive)

Transistor as a switch

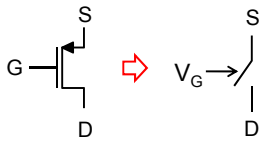
- In this part, we consider an MOS transistor (MOSFET) as a switch
- MOS transistors can be either NMOS or PMOS transistors
- We view a 3-terminal MOSFET as a blackbox whose drain and source terminals are equivalent to the two terminals of an ordinary switch and the gate controls the switch

NMOS transistor:



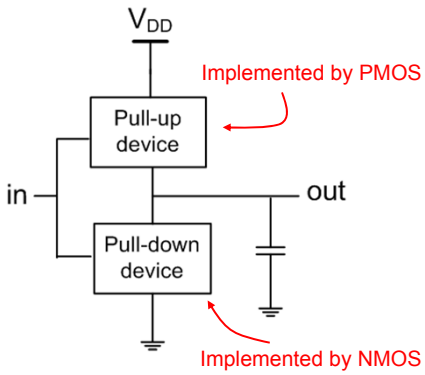
$V_G = V_{DD}$ ("1") → NMOS is **on** (switch closed)
$V_G =$ 0V ("0") → NMOS is **off** (switch open)

PMOS transistor:



V_G = 0V ("0") → PMOS is **on** (switch closed)
$V_G = V_{DD}$ ("1") → PMOS is **off** (switch open)

CMOS logic gates

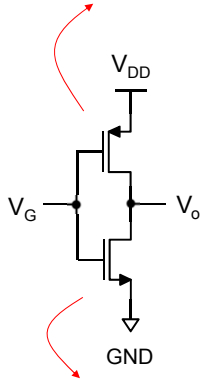


Recall → Features of CMOS static logic:

- Full output swing from ground to supply voltage → high noise margin;
- There is always a low impedance path from the output to ground or supply voltage
- No static power dissipation (only one transistor is on)
- No static input current → very high input impedance (input is capacitive)

CMOS *NOT* Gate (Inverter) and Buffer

$V_G = V_{DD}$ ("1") → PMOS turns OFF (D and S open circuit) → equivalent to an open switch
$V_G = 0V$ ("0") → PMOS turns ON (D and S short circuit) → equivalent to a closed switch



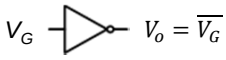
Physical truth table:

V_G	V_o
0V	V_{DD}
V_{DD}	0V

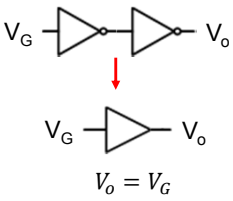
Logic truth table:

V_G	V_o
0	1
1	0

Inverter:



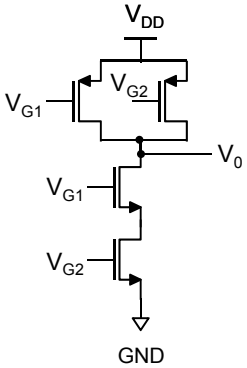
Buffer:



$V_G = V_{DD}$ ("1") → NMOS turns ON (D and S short) → equivalent to a closed switch
$V_G = 0V$ ("0") → NMOS turns OFF (D and S open circuit) → equivalent to an open switch

CMOS *NAND* gate

$V_G = V_{DD}$ ("1") → PMOS turns OFF (D and S open circuit) → equivalent to an open switch
$V_G = 0V$ ("0") → PMOS turns ON (D and S short circuit) → equivalent to a closed switch



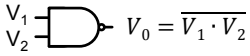
Physical truth Table:

V_{G1}	V_{G2}	V_o
0V	0V	V_{DD}
V_{DD}	0V	V_{DD}
0V	V_{DD}	V_{DD}
V_{DD}	V_{DD}	0

Logic truth Table:

V_{G1}	V_{G2}	V_o
0	0	1
1	0	1
0	1	1
1	1	0

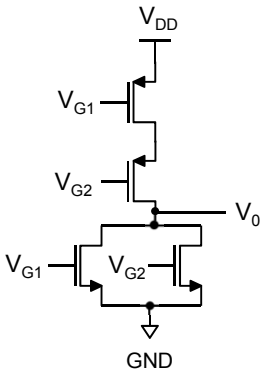
NAND gate:



$V_G = V_{DD}$ ("1") → NMOS turns ON (D and S short) → equivalent to a closed switch
$V_G = 0V$ ("0") → NMOS turns OFF (D and S open circuit) → equivalent to an open switch

CMOS *NOR* gate

$V_G = V_{DD}$ ("1") → PMOS turns OFF (D and S open circuit) → equivalent to an open switch
$V_G = 0V$ ("0") → PMOS turns ON (D and S short circuit) → equivalent to a closed switch

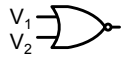


Physical truth Table:

V_{G1}	V_{G2}	V_o
0V	0V	V_{DD}
V_{DD}	0V	0
0V	V_{DD}	0
V_{DD}	V_{DD}	0

Logic truth Table:

V_{G1}	V_{G2}	V_o
0	0	1
1	0	0
0	1	0
1	1	0

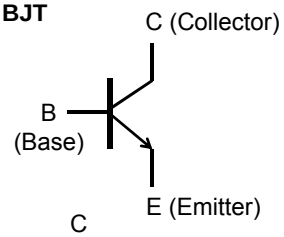
NOR gate: 

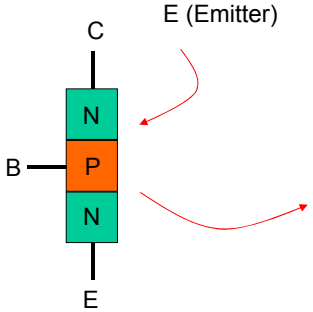
$V_0 = \overline{V_1 + V_2}$

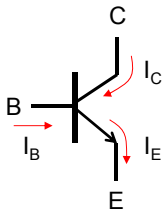
$V_G = V_{DD}$ ("1") → NMOS turns ON (D and S short) → equivalent to a closed switch
$V_G = 0V$ ("0") → NMOS turns OFF (D and S open circuit) → equivalent to an open switch

Bipolar Junction transistor (BJT)

NPN BJT





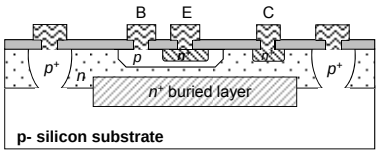


$I_B + IC = IE$
$I_C = \beta IB$

$\Delta I_C = \beta \Delta I_B$

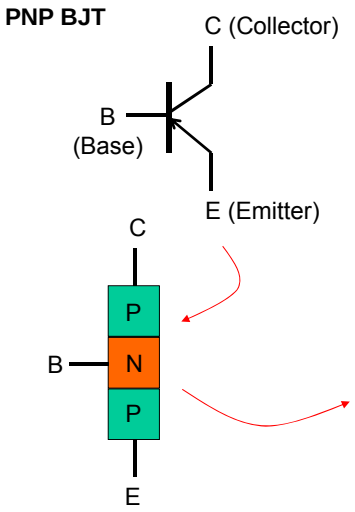
Small I_B change can induce large I_C change → amplification

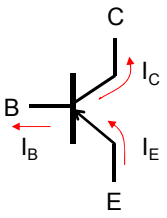
BJT is a current-controlled device



Cross section of BJT IC technology

Bipolar Junction transistor – cont.



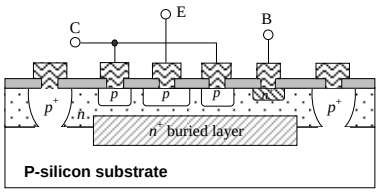


$I_B + IC = IE$

$I_C = \beta IB$

$\Delta I_C = \beta \Delta I_B$

Small I_B change can induce large I_C change → amplification



Cross section of BJT IC technology

Logic ICs based on BJT IC technology

- **TTL** (Transistor-Transistor Logic)
  - Invented by *TRW Inc.* in US, first commercial TTL logic IC was introduced by Sylvania in 1963 and became popular with *Texas Instrument*'s 5400 and 7400 series
- **ECL** (Emitter-Coupled Logic)
  - Invented by IBM, first commercial integrated-circuit ECL family was introduced by *Motorola* in 1962
  - Suitable for high-speed logic circuits

TTL logic gates

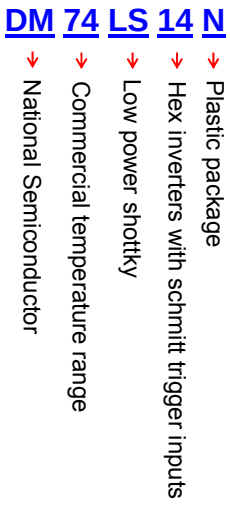
Features of TTL logic gates

- Based on BJTs
- Most widely used logic ICs at gate or MSI level
- Typically operated under 5V supply voltage
- Having different series that optimized for low power, high speed, etc
- Inputs of the gate draw static current

- Due to lack of prerequisite, we'll not discuss circuit details of TTL logic gates

Commercial logic families

- 74xxx Series
  - **TTL** family (**T**ransistor-**T**ransistor **L**ogic)
  - Use Bipolar or CMOS technology
- Name convention
  - 1st field: 2 or 3 letters → Manufacturer (sometimes omitted)
  - 2nd field: 74 → Commercial temperature range (54 → Military)
  - 3rd field: 4 letters → Logic sub-family
  - 4th field: 2 or more digits → Type of device
  - 5th field: Type of package or other information (sometimes omitted)

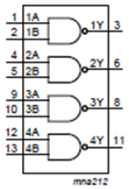


74 series Logic Sub-families (3rd field)

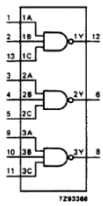
- TTL (Bipolar)
  - 74L → Low power
  - 74H → High speed
  - 74LS → Low power Schotty
  - 74AS → Advanced low power schotty
  - 74ALS → Advanced low power schotty
  - .....
- CMOS (not TTL, but retains some compatibility)
  (same part numbers as bipolar are retained to identify the function)
  - 74C → CMOS 4-15V
  - 74HC → High speed
  - 74AC → Advanced CMOS
  - 74LVC → Low voltage, 1.65 to 3.3V
  - 74LVX → 3.3V with 5V tolerant inputs
  - ……

Some 74 series Logic gates

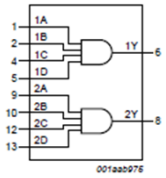
7400 (74HC00)
(Quad 2-input NAND gate)



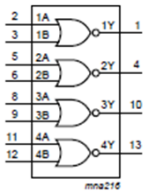
7410(74HC10)
(Dual 3-input AND gate)



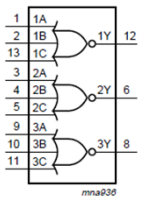
7421(74HC21)
(Dual 4-input AND gate)



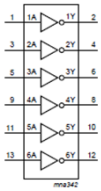
7402(74HC02)
(Quad 2-input NOR gate)



7427(74HC27)
(Quad 3-input NOR gate)



7404(74HC04)
(Hex inverters)



CMOS logic family

- **4000(RCA)/14000 (Motorola)**
  - Very low power dissipation.
  - Operate over wide power supply range (3 to 15V).
  - Slow compared to TTL and other CMOS series.
  - Very low output current capability.
  - Not pin compatible with TTL
  - This very first series of CMOS is rarely used now.
- **74C**
  - Pin compatible & functionally equivalent to TTL devices with same number.
  - Many TTL functions are available in this series.
  - Same performance as 4000 series.

CMOS logic family (cont.)

- **74HC/HCT (High speed CMOS)**
  - Improved version of 74C series. Its speed about same as TTL 74LS series, much higher current capability than 74C series.
  - 74HCT devices are voltage compatible with TTL but 74HC devices are not.
- **74AC/ACT (Advanced CMOS)**
  - Functionally equivalent to various TTL series, but not pin compatible.
  - Pin incompatibility because pin placements chosen for better noise immunity.
  - ACT series offers better noise immunity, less propagation delay, and higher maximum clock speed.
- **74AHC (Advanced high-speed CMOS)**
  - Newest CMOS series, replacement for HC devices.
  - For faster, lower power applications.

CMOS/TTL Comparison (static)

Input/output voltage levels (in volts) with $V_{DD} = V_{CC} = +5$ V.

	CMOS							TTL			
Parameter	4000B	74HC	74HCT	74AC	74ACT	74AHC	74AHCT	74	74LS	74AS	74ALS
V_{IH} (*min*)	3.5	3.5	2.0	3.5	2.0	3.85	2.0	2.0	2.0	2.0	2.0
V_{IL} (*max*)	1.5	1.0	0.8	1.5	0.8	1.65	0.8	0.8	0.8	0.8	0.8
V_{OH} (*min*)	4.95	4.9	4.9	4.9	4.9	4.4	3.15	2.4	2.7	2.7	2.7
V_{OL} (*max*)	0.05	0.1	0.1	0.1	0.1	0.44	0.1	0.4	0.5	0.5	0.4
V_{NH}	1.45	1.4	2.9	1.4	2.9	0.55	1.15	0.4	0.7	0.7	0.7
V_{NL}	1.45	0.9	0.7	1.4	0.7	1.21	0.7	0.4	0.3	0.3	0.4

Noise margin H and L

CMOS/TTL Comparison (Dynamic)

Parameter	4000B	74HC/HCT	74AC/ACT	74AHC/T	74	74LS	74AS	74ALS	ECL
Power dissipation Per gate (mW)									
Static	1.0×10^{-3}	2.5×10^{-3}	5.0×10^{-3}	9.0×10^{-3}	10	2	8	1.2	25
at 100 kHz	0.1	0.17	0.08	0.006	10	2	8	1.2	25
Propagation delay (ns)	50	8	4.7	3.7	9	9.5	1.7	4	1
Speed-power (at 100 kHz) (pJ)	5	1.4	0.37	0.02	90	19	13.6	4.8	25
Maximum clock rate (MHz)	12	40	100	130	35	45	200	70	300
Worst-case noise margin (V)	1.5	0.9	0.7	0.55	0.4	0.3	0.3	0.4	0.25

Summary

- Digital IC technology
  - BJT and MOSFET
  - BJT and CMOS technology
- CMOS logic gates
  - Implementation of NOT, NAND, NOR, AND and OR gates
- Commercial logic families
  - TTL and CMOS
- Logic gate characteristics
  - Static parameters (V_{OH}, V_{OL}, V_{IH}, V_{IL}, I_{OH}, I_{OL}, I_{IH}, I_{IL}, NM_H, NM_L and P_D)
  - Dynamic parameters (t_p and fan-out)
  - CMOS/TTL comparison
- Logic family interfacing (TTL driving CMOS, CMOS driving TTL)