NATIONAL UNIVERSITY OF SINGAPORE

Department of Electrical and Computer Engineering

Department of Electrical and Computer Engineering

EE2020 Laboratory

D1 Manual II

Session: Semester I, 2014/15

I. **D1 Intro Details** are applicable for D1 Intro session where you will gain familiarity with implementing TTL circuits on breadboard.

II. **D1 Project Details** give you more details regarding the D1 project, which you will be implementing progressively through D1A, D1B and D1C sessions.

A. D1 PROJECT DETAILS

I. Project Guidelines and Grading Information

- You will progressively be building an application through the rest of your D1 sessions (D1A, D1B, and D1C).

- You need to be familiar with the list of ICs given in Section II.

- Please follow the considerations given in Section III while designing your circuit.

- The **30%** weight carried by D1 project is split as **5%**, **15%** and **10%** for D1A, D1B and D1C sessions respectively.

- The tasks for D1A, D1B and D1C are given in Section IV.

- If the absence is due to *valid reasons*, please submit your **original** medical certificate / excuse letter / other documented evidence the very next day after the last day you are excused for by the document. Late submission will not be entertained. **It is noted that hall activities and extra curriculum activities are not considered as valid reasons**. Please verify with Teaching Assistant (TA) first if you are not sure.

- An appropriate penalty applies on absentee's final grade unless you were *absent with valid reasons*. There will not be any make-up sessions per se for absentees.

- The final D1 Assessment will be carried in week 13 (**10-14 Nov 2014**). Each student has 10 minutes to present and demonstrate their D1 project. GAs will test students' understanding of the design during the presentation.

- The rubrics used for assessment are
  (i). Ability to execute a design process.
  (ii). Ability to verify that a design achieves desired needs.
  (iii). Neatness of your circuit and observance of wiring rules.

- (i) and (ii) are assessed based on the correctness of your design, your understanding of the design process and the requisite background knowledge (as can be inferred from your response to the questions asked by GAs), as well as the functionality of your circuit.

- Students are also required to submit a ONE-page progress report to the assigned GA at the end of each D1 Lab sessions (D1A, D1B). No extension is allowed.

- Students' performance during D1A, D1B and D1C and the progress reports will be used in their D1 Assessment. Attendance and learning attitude will also be considered especially those who are unable to demonstrate the assigned task during the final D1 Assessment. In addition to the above, there is a small discretionary component, awarded by GAs based on your motivation, elegance of design, extra features implemented (if any) etc.

- A 5-page report will be handed in to the assigned GA before the presentation is started.

- The report (maximum of 5 pages) covering the whole project. There is no specific format for the report, but as is with the report of a small project, it may have a brief introduction, design methodology, parts used and justification for their use, neat & labeled schematic(s), brief explanation of sub-circuits, experiment results (state clearly if the result matches the design requirements – if it doesn't, explain why not), understanding/experience gained from this project, possible improvements, etc.

- We will perform necessary normalizations to ensure that *no student is at a disadvantage because of being assigned a specific project or being under a particular GA.*

II. List of ICs

- A list of popular TTL integrated circuits is given below.
- Make sure that you understand the working of *all of them very well* ***before*** coming for the lab sessions.
- You are encouraged to remember *or* bring printouts/e-copies of relevant parts of the datasheet (pinouts, function table/timing diagram) for all of the ICs for D1 sessions.
- Datasheets can be obtained from the lab or from the manufacturers' websites (you can simply Google part number+datasheet).
- You can use devices which are not listed below if they are available in the lab - please check the availability with the lab staff.

Sl.No.	Description	Part Number
1	Quad 2-input NAND gates	7400
2	Quad 2-input NOR gates	7402
3	Hex inverters	7404
4	Quad 2-input AND gates	7408
5	Dual 4-input NAND gates	7420
6	Dual 4-input AND gates	7421
7	Quad 2-input OR gates	7432
8	Quad 2-input XOR gates	7486
9	Triple 3-input AND gates	7411
10	Dual 4-input NAND gates	7420
11	Dual 4-input AND gates	7421
12	Triple 3-input NOR gates	7427
13	BCD to 7-segment Decoder	7447/7448
14	4 bit magnitude comparator	7485
15	3 to 8 Line decoder / demultiplexer	74138
16	Dual 2 to 4 line decoder / demultiplexer	74139
17	Quad 2 to 1 line data selector/multiplexer	74157
18	Hex D-type flip flop	74174
19	Quad D-type flip flop	74175
20	Synchronous 4-bit up/down counter with mode control	74191
21	Synchronous 4-bit up/down counter with dual clock	74193

22	Dual D-type flip flop with preset and clear	7474
23	4 bit universal bi-directional shift register	74194
24	4 bit binary adder	74283

III. Design Considerations and Hints

1. You may use a single pulser circuit (implemented in D1Intro) to clean up the signal from a push-button to obtain a pulse that is high for exactly one clock cycle.

2. The clock inputs of **all** your sequential devices should be connected to a single free running clock signal; example shown in Fig. 6.

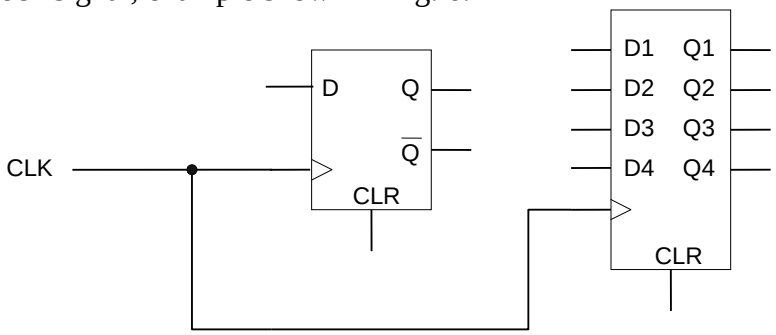

Figure 6: The same clock signal must be used for all sequential device clock inputs.

3. Do **not** connect the inputs (DIP and push button switches) to the clock inputs of sequential devices. Clock inputs must be connected to the clock signal only (Fig. 7).

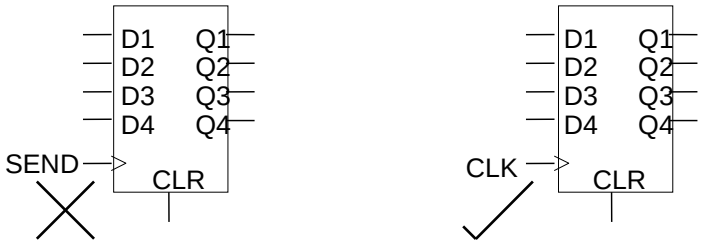

Figure 7: A clock pulse should be connected to the clock inputs of all the sequential devices.

4. Do not gate the clock input (Fig. 8).

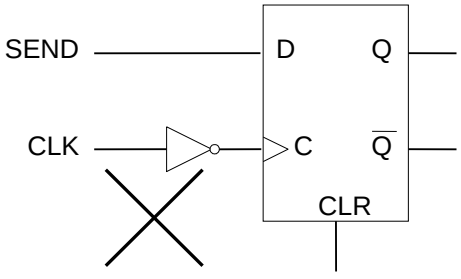

Figure 8: Clock signals must go directly into sequential device clock inputs.

[Hint : To inhibit counting, use *enable* function rather than gating the clock.]

5. Design your circuit **on your own**, after building up a good knowledge on the basic building blocks of digital circuits i.e. flip-flops, counters, registers, multiplexers, decoders etc. Identify the functional units you need, and find the most appropriate IC/combination of ICs to map it to.

6. Depending on your design, using **MSI chips** (such as decoders, comparators etc.) may dramatically reduce the number of components required for the circuit compared to using only basic gates such as NAND's, NOR's and inverters. MSI chips tend to yield clearer and more efficient designs.

7. You are encouraged to use **simulation software** such as Xilinx ISE's schematic option or Circuitlogix (free student version) or Multisim (30 day evaluation version or free Analog devices edition) to gain better understanding of the working of various components/ICs through simulation.

8. Your **design** has to be implemented on the **2 strips of breadboard** provided to you. You may not be able to accommodate more than 12 ICs on them.

9. From our experience, **7416x ICs** might have problems clocking from 555 timer. If you design using 7416x and experience problems, you might want to use the TTL clock from the Function Generator instead of the 555-based clock. However, this will limit your ability to work on your circuit outside the designated lab sessions.

10. Good luck and have fun!

IV. Project Descriptions

The project descriptions are given below. You will be doing only one project, corresponding to the day of your lab.

MON: Queueing System

From telecommunications, traffic engineering to the design of production lines, queueing theory plays an important role in making decision about the resource distribution. In this project, a queueing system is designed for three production lines. A push button is used to indicate the arrival of each item to one of the production lines. The items will distribute to each production line in order (first item goes to first line, second item goes to second line etc.). When there are nine items in the production lines (three item in each line), the system will stop accepting the new items for five seconds and then the system will be automatically reset. A RESET button is used to reset the system. A seven segment display shows the total number of items in the all three production lines.

D1 Project Guideline:

D1A: Implement two push buttons (one for item arrival and reset) and a counter to count the total number of items in the production lines

D1B: Design the queueing system to evenly distribute the items to each production line

D1C: Implement the seven segment display and the system reset part

TUE: Encryption Counter with Parity Check

In cryptography, encryption is the process of encoding information such that only authorized people can read it. After data transmission, a parity check is used for detecting errors. In this project, an encryption counter with parity check is designed. Let **T** denote the input signal (using the output of a counter) and **T'** denote the encrypted output. A 4-bit DIP switch is used as the key, **K**. The input is encrypted as follows:

$$T' = T \text{ XOR } K$$

When the key is changed, K should be synchronously updated and T reset to 0000.
The parity bit is defined as 0 if the sum of the bits of the input signal is odd. Otherwise 1 is assigned.
Decryption is the reverse process of encryption. Design a decryption circuit follow by a seven segment display to show the count only when the parity bit is 1.

D1 Project Guideline:

D1A: Implement the 4-bit DIP switches (key for encryption and key for decryption), a push button for start/reset and a counter. It is noted that there are two DIP switches (one is for the encryption and the other is for the decryption.

D1B: Implement the encryption, decryption and parity check

D1C: Implement the seven segment display.

THU: Traffic Light Controller

A traffic light controller produces five output signals. Three output signals named Veh_Red, Veh_Amber, Veh_Green control the flow of vehicles while the other two signals named Man_Red, Man_Green control the flow of pedestrians. Veh_Red and Man_Green are always asserted at the same time. Similarly, it applied on Veh_Green and Man_Red. Each traffic light indicator will last for seven seconds in the following steps:

1) 7 seconds for Veh_Red and Man_Green
2) 7 seconds for Veh_Green and Man_Red
3) 7 seconds for Veh_Amber

The process is repeated. A push button is used for pedestrians to cross the road. Three seconds after pressing the push button, the traffic light controller will trigger to the step (3), 7 seconds for Veh_Amber. So the pedestrians can cross the road after ten seconds pressing the button. A seven segment display is used to show the remaining time for pedestrians to cross the road. It only works in Step (1). It is noted that push button should not work during Step (1) and the 3-second waiting time.

D1 Project Guideline:

D1A: Implement the push button and a three second counter

D1B: Implement the main controller part

D1C: Implement the seven segment display

Fri: Weighted Timing Controller

A simple microwave oven has two cooking modes: a “Slow Cooking” mode that operates on low power and a “Fast Cooking” mode that operates on high power. Cooking time for these cycles depends on the weight of items being cooked and is determined as follows.

Fast cooking cycle: 2* Weight seconds
Slow cooking cycle: 3* Weight seconds

The system will not be functioned if the cooking cycle is more than 15. The weight is indicated by a 4-bit DIP switch. A 1-bit DIP switch is used to indicate the cooking mode (fast or slow). A push button is used as START button for starting the cooking process. A seven segment display and a LED are used to indicate the count in decimal format and only odd number count is showed during the cooking process. For example, if the count is 15, the LED is asserted and seven segment shows ‘5’. If the count is 9, only the seven segment display show ‘9’.

D1 Project Guideline:

D1A: Implement the 4-bit weight DIP switch, 1-bit DIP switch for mode selection and cycle calculation

D1B: Implement the counter and hexadecimal to decimal conversion circuit

D1C: Implement the seven segment