Tutorial Questions (Part 2)

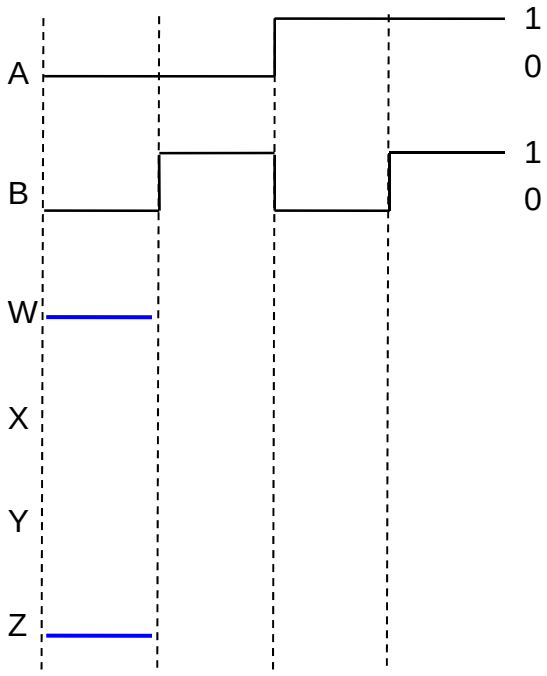
VHDL introduction

Please try out these self-study questions (labeled "SS"). These will not be discussed in class and solutions will be provided later.

SS1. For the VHDL program below, complete the timing diagram shown for output signals **W** & **Z,** and variables **X** & **Y** given that the input signals **A** & **B** are as shown.

```
entity q1_vhd is
port (A, B : in std_logic;
      W, Z : buffer std_logic);
end q1_vhd;

architecture SEQUENTIAL of q1_vhd is
begin
process( B )
  variable X, Y: std_logic;
  begin
      W <= A xor B;
      X := not W; -- old or new value of W?
      Y := A and B;
      Z <= Y;     -- old or new value of Y?
  end process;
end SEQUENTIAL;
```



SS2. Write separate VHDL programs to describe the circuits of Question 2 of *Tutorial 3 (Part 1)* and the following boolean expressions of Question 3 & 4 of *Tutorial 3 (Part 1)*.

$$X = A \oplus B \oplus C$$
$$Z = \overline{A}B + \overline{B}\overline{C}D + \overline{B}\overline{D}$$

VHDL Modeling

1. A combinational circuit has a four-bit input **A** and a one-bit output **Z**. Output Z is 1 if the 4-bit **A** is a non-prime number, and Z = 0, otherwise. Write a VHDL program to describe the circuit. (*Note that there is no need to simplify the logic expressions. See also Question 4 of Tutorial 4 Part 1*)

2. A *multiplexer* needs to select one of five 4-bit input words **A**, **B**, **C**, **D** or **E**, and output it via the 4-bit output signal **T**. The selection must be done according to the selection control inputs S_0–S_2 (see table below). Write a VHDL description (i.e.,program) for the multiplexer.

$S_2S_1S_0$	000	001	010	011	100	101	110	111
T	**ÿ**	**B**	**A**	**C**	**A**	**D**	**A**	**E**

3. Write a VHDL description of the 74138 decoder in the ***behavioural style of modeling***. (*Refer to the lecture materials for the functional table of the 74138.*)

4. A machine receives two 3-bit inputs **X**, **Y** and outputs a 6-bit output **Z**. **Z** is the product of **X** and **Y**. Write a VHDL program that implements this machine.

Hint: Use the shift and add method to perform multiplication i.e.,

```
        1 0 1
X       0 1 1
-------------
        1 0 1
      1 0 1
    0 0 0
-------------
  0 0 1 1 1 1
```

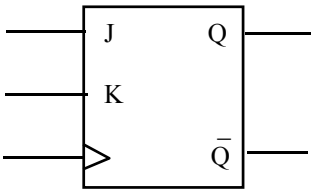
Note that the addition operation is performed as follows:
c <= a + b; *where a, b & c are standard logic vectors of the same length.*

5. Data encryption schemes are commonly used to secure data privacy. Write a VHDL program for a *digital decrypter* which has a 5-bit input, DATA_IN of the form "$C_2O_1C_1O_0C_0$" where the operation applied to the three bit data "$C_2C_1C_0$" to produce the 3-bit output DATA_OUT depends on the two bits "O_1O_0"as shown in the table below.

"O_1O_0"	**DATA_OUT**
"00"	"$C_2C_1C_0$"
"01"	"$C_0C_2C_1$"
"10"	"$C_1C_0C_2$"
"11"	"$\overline{C}_2\overline{C}_1\overline{C}_0$"

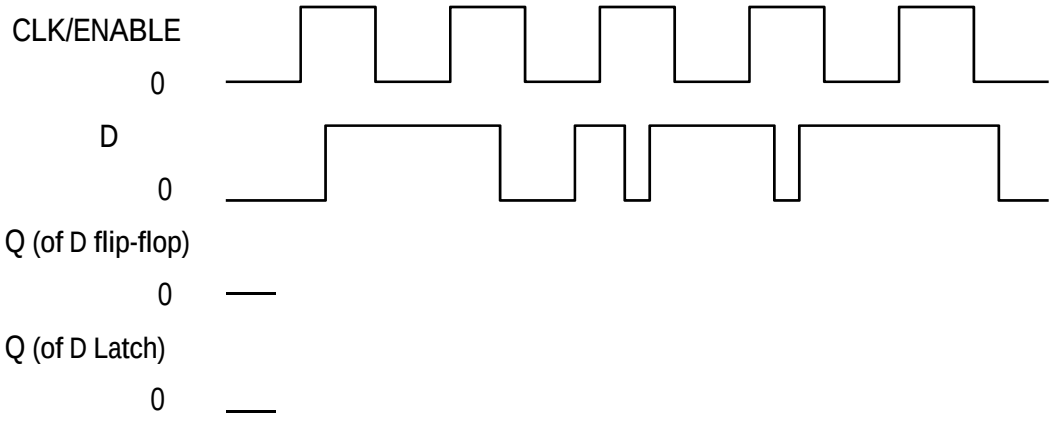
SS3. Write a VHDL program to realize the circuit of Question 5 of *Tutorial 5 (Part 1)*.

Flip Flops

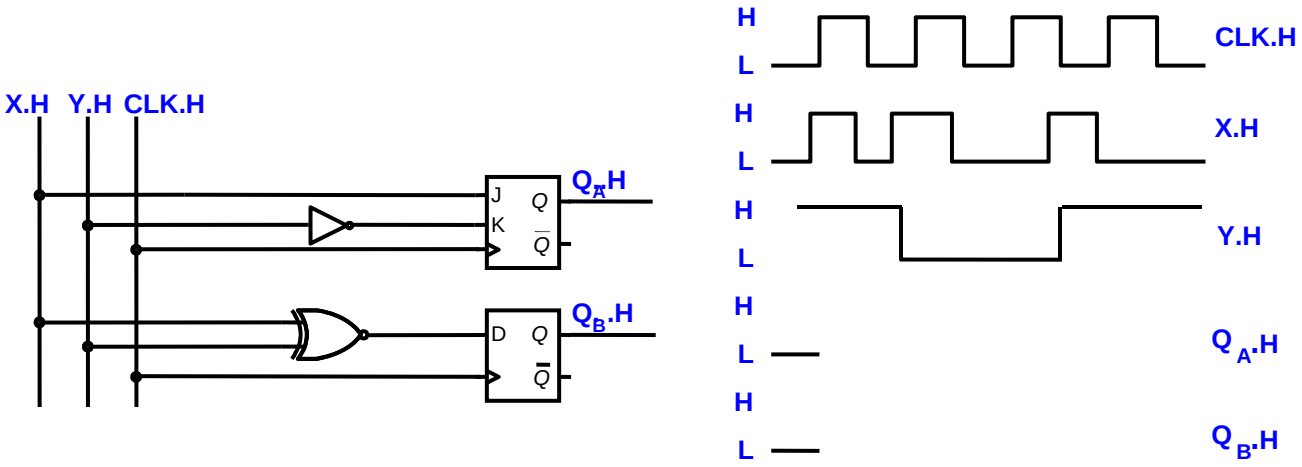


6. Using additional logic gates show how a JK flip-flop be modified to operate as a D flip-flop.

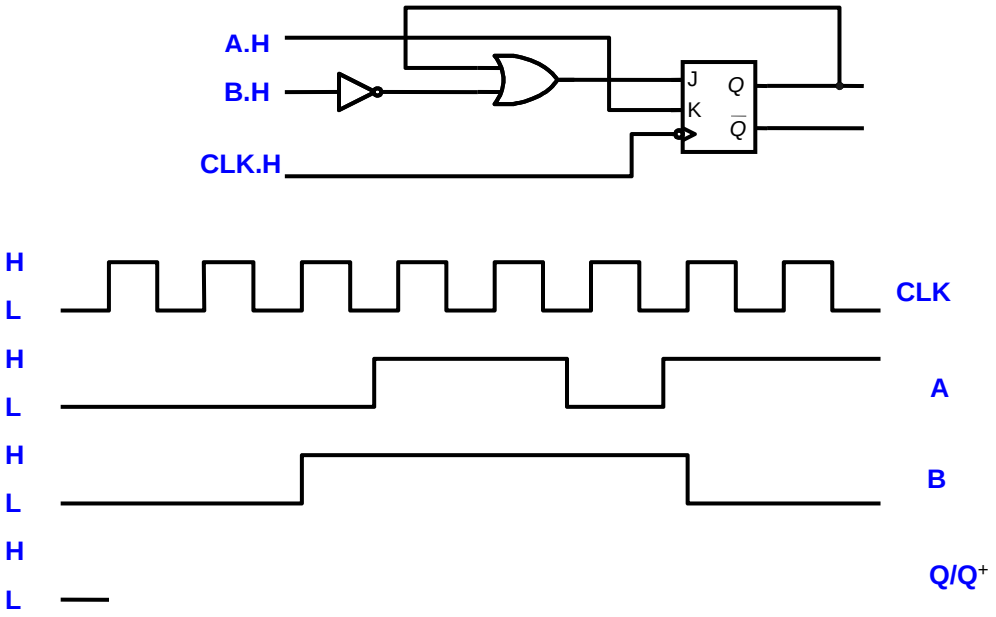
SS4. The **D** and **CLK/ENABLE** input waveforms shown below are applied to a *negative-edge triggered D flip-flop* & a *D Latch*. Clearly draw the output Q waveforms of the devices.



SS5. Given the circuit diagram below, complete the corresponding timing diagram below for each of the flip flop outputs. Show the propagation delays t_{pHL} and t_{pLH}.

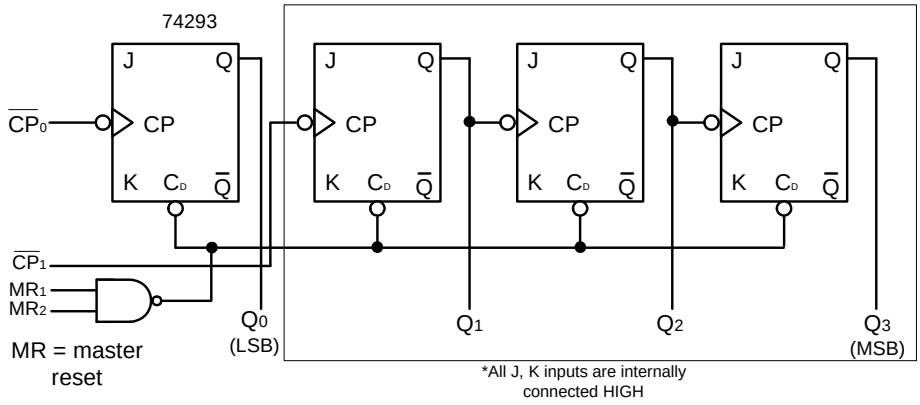


7. (a) Analyze the circuit below and complete the timing diagram.
   (b) Assuming that the circuit represents a type of flip flop, derive its characteristic table, its condensed characteristic table and its excitation table.



Counters

8. The figure below the functional circuitry of the 74'293 counter IC. Show how you would use one 74'293 IC, one J-K flip-flop and other logic gates to realize a Mod-29 counter. Draw your circuit for the Mod-29 counter using the figure below. Give a brief explanation of the circuit operation.



9. A 2-bit counter counts has four modes of operation depending an two-bit control input **X**, as shown in the table below:

X	**Modes**
00	Hold
01	Count in forward sequence
10	Count in reverse sequence
11	Clear

Carry out the following to implement the 2-bit counter noting that changes in the value of **X** can affect the operation at any point during the sequence:

(i) Construct the functional block diagram of this counter
(ii) Determine the next state table of this counter
(iii) Design & implement the counter using D FFs (using excitation table of D FFs).

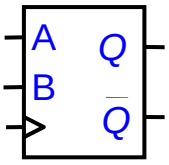
SS6. Implement the counter in the question above in VHDL. Test your solution using the Xilinx tools.

10. A counter machine has input **X**, clock input **CLK**, asynchronous reset input **RST** and output **Y**. When **X** is '0', the "*zeros count*" increments by 1, while when X is '1' the "*ones count*" increments by 1 at the rising clock edge. Output **Y** becomes 1 and remains 1 thereafter when the "*zeros count*" & "*ones count*" are both at least three ("*zeros count*"≥3 & "*ones count*" ≥3). The counts (*ones* & *zeros*) and the output **Y** are reset to zero when **RST** is asserted. Write a VHDL description of this machine.

SS7. Implement a 3-bit Johnson in VHDL using the "*states*" approach to modeling counters in VHDL. Test your solution using the Xilinx tools.

FF Designs

11. Design the A-B flip-flop shown below (left) using a J-K flip-flop plus any gates that are needed. A-B flip-flop's condensed characteristic table is also shown below (right).



A	B	Q+
0	0	**1**
0	1	**Q**
1	0	$\overline{Q}$
1	**1**	**0**

12. A unique flip-flop has a clock input CLK, a 1-bit input X which controls its mode of operation and a 1-bit output Q. The flip-flop behaves as shown in the table below. Write and compile a VHDL program that implements this flip-flop.

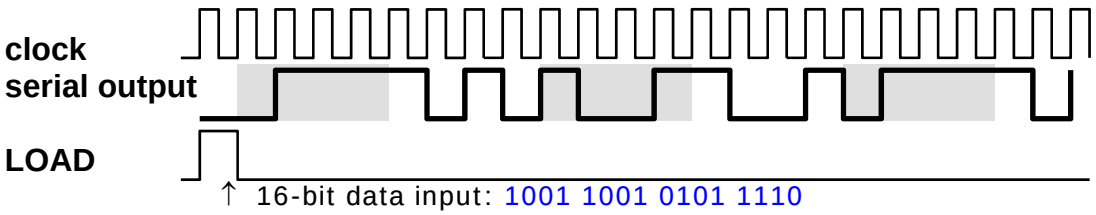
Previous value of X	Current value of X	Q+
0	0	Q
0	1	0
1	0	1
1	1	$\overline{Q}$

Registers

13. A barrel shifter is a shift register in which the data can be shifted either by one-bit position, as in a normal shift register, or by multiple shift positions. Write a VHDL code for a four-bit barrel shifter that can shift to the right by 0, 1, 2 or 3 positions.
(***Self-study exercise**: extend the capability of shifter to be able to either shift left or right!*)

SS8. Extend the capability of the shifter in the question above to be able to *either* shift left or right. Test your solution using the Xilinx tools.

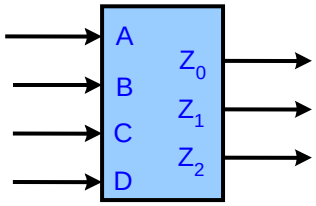
14. A *16-bit digital pulse generator* whereby the digital output serial stream is programmed by a 16-bit data input synchronously when LOAD=1. Operating like a shift register, the output of this generator cycles through the input data in synchronization with an input clock to generate the pulses. An input binary data of "1010 1010 1010 1010" will generate a square pulse having a period of two clock pulses. Similarly an input binary data of "1111 0000 1111 0000" will generate a square pulse having a period of eight clock pulses. Fig below shows the timing diagram of the generator's output for an input value of "1001 1001 0101 1110". Write a VHDL program that implements this 16-bit digital pulse generator.



PLD

15. A synchronous counter counts in the following sequence: …0,2,6,7,5,0,2,6,7,5…. Realize the counter using the PLD device (PAL16R8) shown in the following page. Show the systematic steps in your design procedure.

16. Given the block diagram of a combinational circuit below (*left*) and its truth table (*right*), realize the combinational circuit with a PLA that has 4 inputs, 4 outputs and supports 8 product terms.

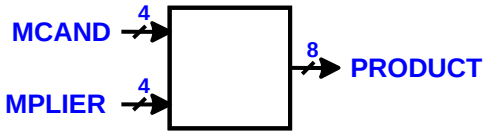


A	B	C	D	Z_0	Z_1	Z_2
0	0	0	0	1	1	0
0	0	0	1	0	0	0
0	0	1	0	0	0	0
0	0	1	1	0	0	0
0	1	0	0	0	0	0
0	1	0	1	0	1	1
0	1	1	0	1	1	0
0	1	1	1	1	0	1
1	0	0	0	0	1	1
1	0	0	1	0	0	0
1	0	1	0	1	1	0
1	0	1	1	0	0	0
1	1	0	0	0	0	0
1	1	0	1	0	1	1
1	1	1	0	0	0	0
1	1	1	1	1	0	1

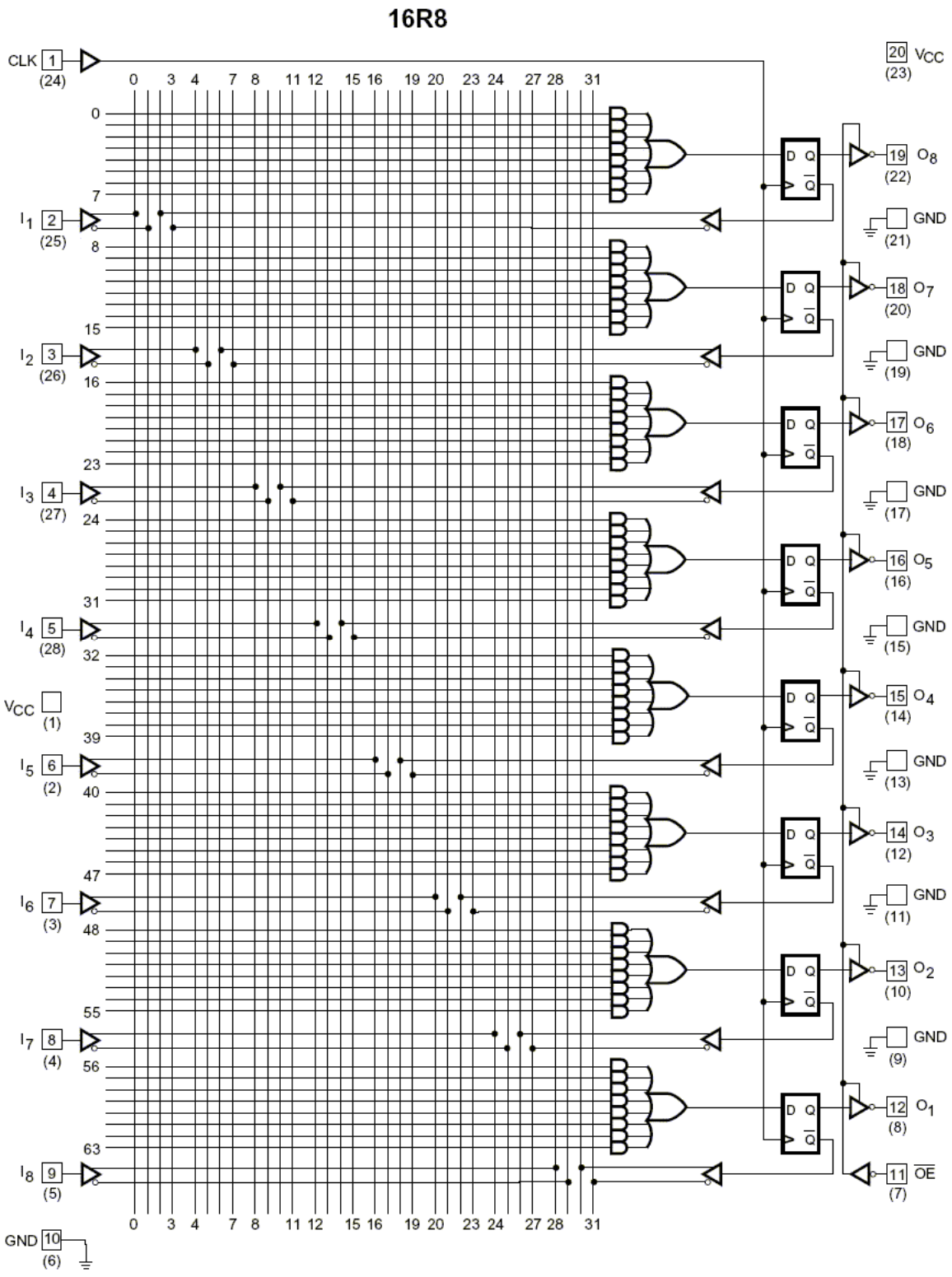
ROM and RAM

17. Draw a memory map that starts from 8000H and is allocated a 2K × 8 RAM followed by a 1K × 8 RAM.
    (a) What is the capacity of the memory map?
    (b) What is the memory range occupied by the two devices in hexadecimal notation?
    (c) Are there any unused memory? If so, specify the unused memory range.

18. The multiplier shown below can multiply two 4-bit numbers (**MCAND** & **MPLIER**) and produce an 8-bit product (**PRODUCT**).
    (a) If a ROM is used to realize this circuit, what must be the ROM capacity?
    (b) Draw a block diagram of the ROM realization, specifying all connections to the address and data lines.
    (c) What are the contents of the ROM? Explain in words.



19. Realize a 4K × 4 RAM module by using four 1K × 4 RAMs and a 2-to-4 decoder. The RAM memory address begins at 8000H. Assume that the RAM devices have an active low chip-select input and an active low write-enable input. Draw a memory map of the memory module (use hexadecimal notation), clearly showing the memory ranges occupied by the different RAM devices. Draw a labeled block diagram of the memory module, which clearly shows the interconnections of the RAMs and logic devices used for address decoding, and all necessary address, data and control signals.


16R8
CLK 1 (24)
I1 2 (25)
I2 3 (26)
I3 4 (27)
I4 5 (28)
VCC (1)
I5 6 (2)
I6 7 (3)
I7 8 (4)
I8 9 (5)
GND 10 (6)
20 VCC (23)
19 O8 (22)
GND (21)
18 O7 (20)
GND (19)
17 O6 (18)
GND (17)
16 O5 (16)
GND (15)
15 O4 (14)
GND (13)
14 O3 (12)
GND (11)
13 O2 (10)
GND (9)
12 O1 (8)
11 OE (7)
0 3 4 7 8 11 12 15 16 19 20 23 24 27 28 31
0
7
8
15
16
23
24
31
32
39
40
47
48
55
56
63
D Q
Q