EE2020 / EE2020E

Digital Fundamentals (1)

(L0 - Introduction)

Massimo ALIOTO

Dept of Electrical and Computer Engineering
Email: ***massimo.alioto@nus.edu.sg***

Modified from original slides by Prof. XU Yong Ping

1

Instructors

- **Massimo ALIOTO (Part 1)**
  - Email: massimo.alioto@nus.edu.sg
  - Office: E4-05-25
- **Ashraf KASSIM (Part 2)**
  - Email: ashraf@nus.edu.sg
  - Office: EA-04-10

- Teaching Assistants
  - Mr **LOKE Yuan Ren**, eleloke@nus.edu.sg
  - Mr **YANG Hong Choo (Daniel)**, elehcy@nus.edu.sg

2

Module introduction

Contents

- **Part 1**
  - Number systems
  - Boolean Algebra and logic gates
  - Gate-level design and minimization
  - Combinational logic circuits and design
  - Logic IC family
- **Part 2**
  - VHDL introduction and modeling
  - Sequential logic circuits
  - VHDL behavioral and structural modeling
  - Programmable logic devices
  - Digital state machine design, including using VHDL

3

Course Description

- First course on digital systems
- Introduces fundamental digital logic, digital circuits, and programmable devices
- The course also provides an overview of computer systems.
- This course provides students with an understanding of the building blocks of modern digital systems and methods of designing, simulating and realizing such systems.
- The emphasis of this module is on understanding the fundamentals of digital design across different levels of abstraction using hardware description languages.

4

Expected Learning Outcomes

- **Expected learning outcome (Part 1)**
  - *Be able to perform conversion* between binary, octal, hexadecimal and decimal number systems, and *solve simple problems;*
  - *Understand* Boolean Algebra, and *manipulate and simplify* Boolean functions using theorems and postulates;
  - *Be able to design simple combinational logic circuits* based on Truth table and Karnaugh Map
  - *Be able to design logic circuits* using appropriate elements from basic gates to flip-flops and MSI (Medium Scale Integration) circuits.
  - *Be able to design logic circuits* for practical problems/applications

5

Expected Learning Outcomes

- **Expected learning outcome (Part-2)**
  - *Describe* a digital circuit in VHDL and *confirm* the functionality through behavioural simulation
  - *Develop an ASM chart* for a digital system, *and choose appropriate circuit elements* from commercially available devices for implementation. Compare various implementation approaches
  - *Design* a circuit for a given problem in the lab, *explain design rationale orally*, and *recommend* various enhancements

6

Module organization

- **Part-1**
  - 10 lectures (2+1 hours/week)
  - 5 tutorial sessions starting in Week 2 (Check your group and venue)
  - 5 Laboratory sessions, including 2 introduction lab, starting in Week 4
- **Part-2**
  - 12 lectures (2+1 hours/week)
  - 6 tutorial sessions (Check your group and venue)
  - 3 Laboratory sessions, including one introduction lab, starting in Week 6

7

Module Assessment

- **Part 1 (50%)**
  - Project D1 (D1B&C): 30%
  - Mid-term quiz: 20%
- **Part 2 (50%)**
  - Project D2 (D2A&B): 30%
  - Final quiz: 20%
- **No final exam ☺**

8

EE2020 Part I Topics

Week	Lectures	Remark
Week 1	Introduction/ Number systems	Module introduction, Position number systems, number system conversion, signed numbers. Arithmetic using signed numbers, BCD, addition using BCD. Postulates and theorems, Boolean functions, truth table, SOP and POS forms, Truth table to SOP or POS, minterm and maxterm, canonical form. Gates & truth table, positive/negative logics and conversion, mixed logics.
Week 2	Number systems/Boolean Algebra/Logic gates	
Week 3	Gate-level design & simplification	Karnaugh map, gate-level simplificaton and implementation
Week 4	Combinational logic circuits	Combination logic MSI and design using MS
Week 5	(quick recap, clarifications, tutorials)	
Week 6	Logic ICs	Physical gates and implementation, TTL and CMOS, logic IC families
Recess week		

9

EE2020 Part II

MAJOR TOPICS	DETAILS
Using VHDL to model digital systems	Introduction to VHDL. Major Capabilities of VHDL. Concurrent and Sequential Statements. Basic VHDL Terminology. Entity. Architecture. Styles of Modeling VHDL Elements: Data Objects, Types & Operators
Sequential Circuits Design	Basic Flip-flops: Fundamental building blocks of sequential circuits. Applications of Flip-flops. Asynchronous & Synchronous counters. Counter & Flip-flop design. Registers, Register-based counter. Clocks.
State Machine Design	Clocked synchronous state machines. State machine structures : Mealy & Moore types. Analysis of state machines. Algorithmic state machine (ASM) chart notation. Synthesis of state machines from ASM Charts. Top-Down Design examples.
Programmable Logic devices (PLDs)	Description, internal architecture and notations of various PLDs: Programmable Array Logic (PAL), Programmable Logic Array (PLAs), and Programmable Read Only Memory (PROM). Introduction to CPLDs, FPGA and design flow process.
Memory Devices	Memory devices: fundamental building blocks of computer systems. RAMs, ROMs, Applications of Memory Devices. Design of Memory Modules.

10

EE2020 CA Schedule (might change a bit): Labs, Projects, Assignments & Quizzes

Date: Mon – Wed, Lab venue: Digital Electronics (E4-03-07)

Week	Lab (Part 1)	Lab (Part 2)	Quizzes
Week 3	Project D1_intro1	-	
Week 4	Project D1_intro2		
Week 5		-	
Week 6	Project D1A		
Recess Week	No lab	No lab	mid-term quiz (March 1)
Week 7		Project D2_intro	
Week 8			
Week 9	Project D1B		
Week 10		Project D2A	
Week 11	Project D1C		
Week 12	-	Project D2B	Final Quiz
Week 13	lab assessment		

11

EE2020 Tutorial Schedule (Part I)

Week	Tutorials	Assignment
WK1	**No tutorial**	
WK2	Tutorial - 1	
WK3	Tutorial - 2	
WK4	Tutorial - 3	
WK5	Tutorial - 4	
WK6	Tutorial - 5	
Recess Week		

- For each tutorial, questions will be posted on IVLE the week before, the solutions will be published the same week

12

Module information

- **Course materials**
  - IVLE (Everything about the course)
- **Need help**
  - Discussion Forum under IVLE (Preferred)
  - Tutors (tutorial questions)
  - TAs and GAs (Labs and projects)
    - during lab sessions
  - Face-to-face consultation with lecturer:
    - by appointment, to be taken at the end of each lecture
    - then, the date/time of the appointment is publicized on IVLE, so that any student can join
- **Reference books**

- D. Harris, S. Harris, Digital Design and Computer Architecture (1st or 2nd ed.), Morgan Kaufmann (AVAILABLE IN THE LIBRARY)
- Mano/Ciletti, *Digital Design, Fifth Edition, Pearson*
- Brown/Vranesis, *Fundamentals of Digital Logic with VHDL Design*, Third Edition, McGraw Hill.

13

Before Getting Started...

14

Before Getting Started...

15

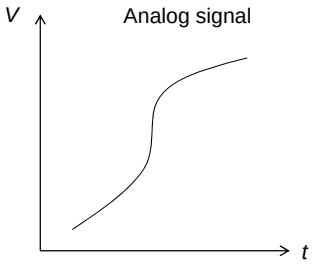
Introduction

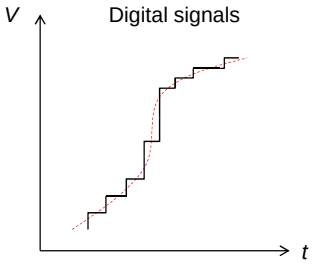
1. Analog vs. digital circuit
2. Why digital?
3. Why study this module?

16

Analog vs. Digital Circuit

- Analog circuit deals with continuous signals
- Digital circuit deals with signals having discrete levels



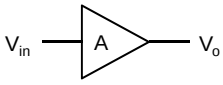


17

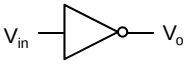
Analog vs. Digital Circuit (cont.)

- Analog circuit is more susceptible to noise
- Digital circuit is a binary system which is much more robust

Analog amplifier



Inverter



18

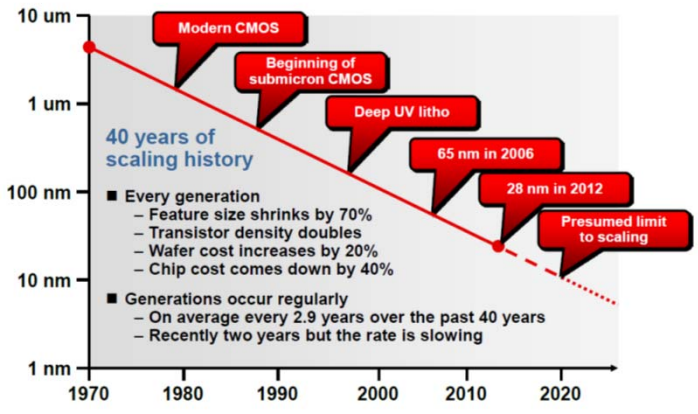
Why digital?

- Robustness (reliability)
- Programmability
- Scalability (in integrated circuit technology)
- Cost

19

Technology Scaling

Semiconductor Technology Scaling

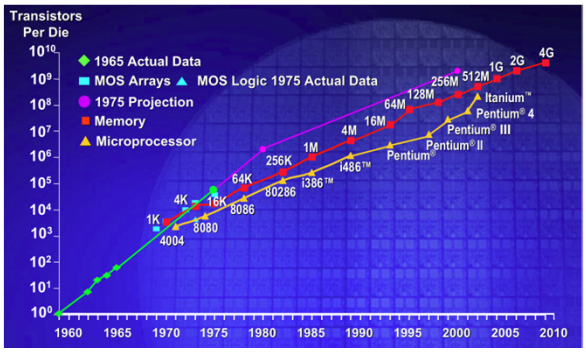


*Dennis Buss, Texas Instrument, USA

20

Technology Scaling (cont.)

Number of transistors per chip

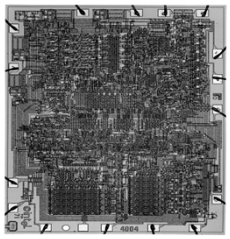


Moore's law

As more and more transistors can be integrated on a single chip,
- the functionality is increased
- Or for the same functionality, the chip area is reduced → Cost per transistor is reduced.

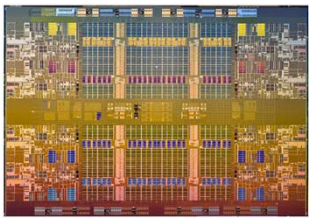
21

Technology Scaling (cont.)



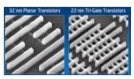
1971:

- Intel 4-bit processor in 10 μm PMOS process with 2300 transistors
- Initial clock speed of 108 kHz
- 10μm pMOS technology



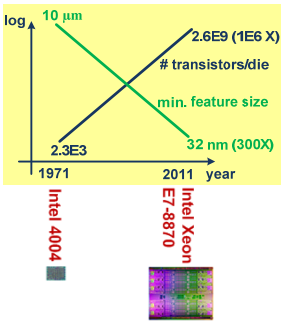
2013:

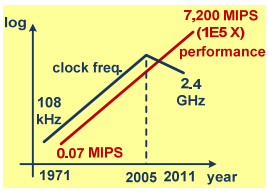
- Intel Xeon E7-8870 processor (10 cores) 2.6 billion transistors
- IBM zEC12 5.5 GHz clock freq., MCM with 6 X 6 cores in 32 nm SOI, 6 X 300W power (liquid cooling!), 2.75 billion transistors for each core, single-thread high performance
- Intel Core i7-4960X (6 cores) in 22nm trigate CMOS



22

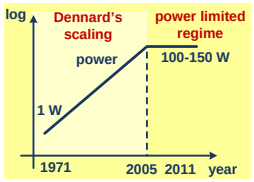
Technology Scaling (cont.)

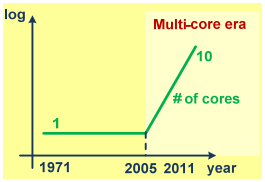




Intel 4004

Intel Xeon E7-8870





23

Digital Revolution and Information Age

- 1947 – Invention of transistor
- 1971 – First microprocessor

***Rapid development of digital computing and communication technology brought about the digital revolution and information age**

- 1980s – Personal computers
- 1990s – World Wide Web, digital cameras
- 2000s – Mobile phones, digital TVs, ipod
- circa 2010 – Smart phones, xPad, cloud computing (accessible everywhere), social networking (constantly connected)
- 2013 and beyond – Cloud computing, Internet of things, ultra-low power high-performance mobile computing, ubiquitous computing, immersive computing/augmented reality, gesture recognition...

24

Why studying this module?

- The module is about the fundamentals of digital systems, which is important if you are interested in the design of digital circuits and systems, especially if you plan to specialize in the following areas:
  - Digital integrated circuits (very important)
  - Embedded systems (very important)
- It's the first module about Hardware Description Language (HDL), which is widely used for digital system design and modeling
- You will also learn analytical and problem solving skills through the projects (practical design problems)
- It also serves as prerequisite for other modules at senior levels.

25