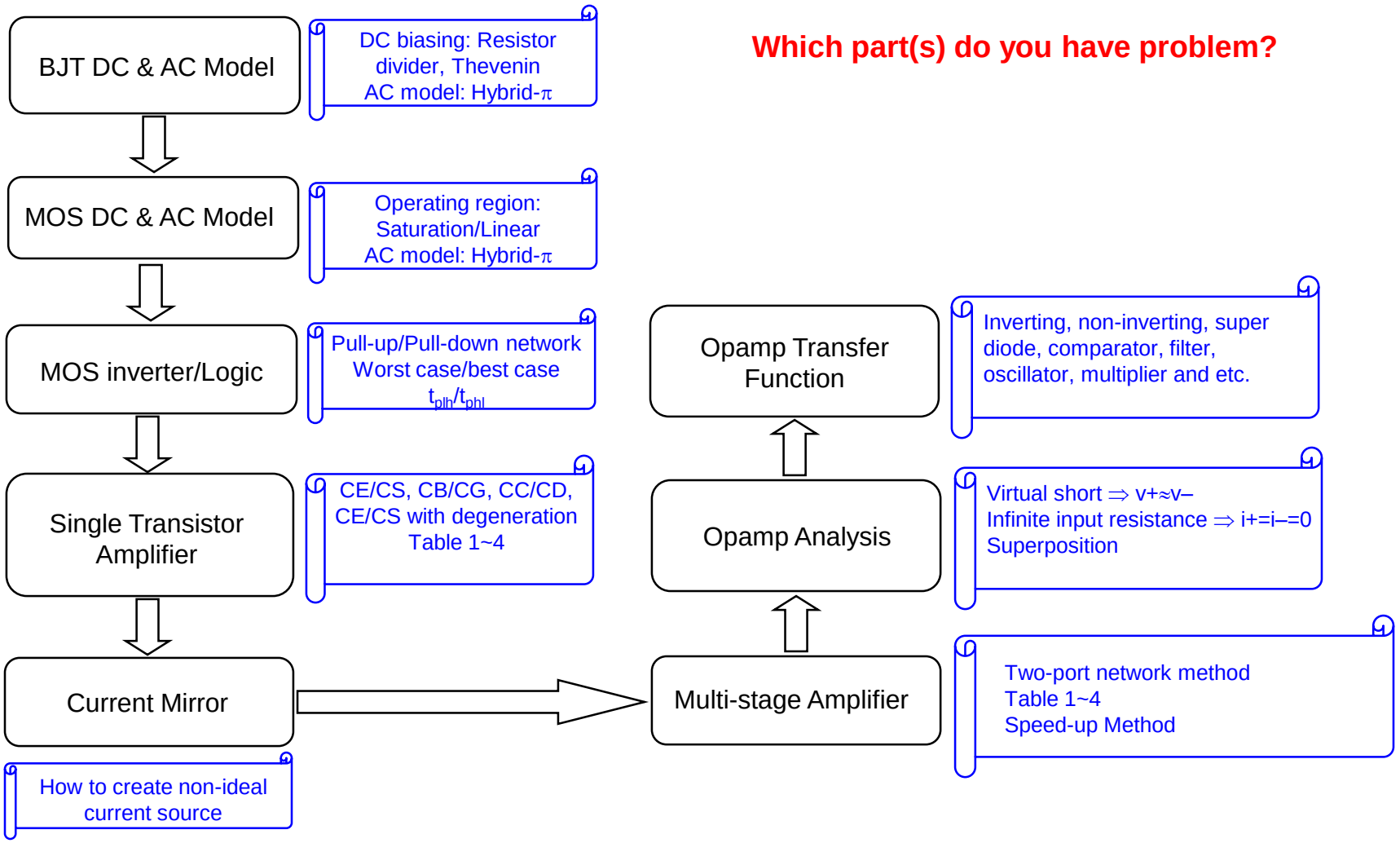
EE2021
Devices and Circuits

Revision

Summary on Materials Covered



Which part(s) do you have problem?

Logic Synthesis

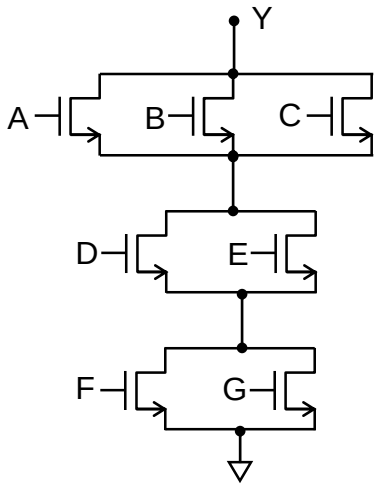
$$Y = \overline{(A+B+C)\cdot(D+E)\cdot(F+G)}$$

$$= \overline{(A+B+C)} + \overline{(D+E)} + \overline{(F+G)}$$

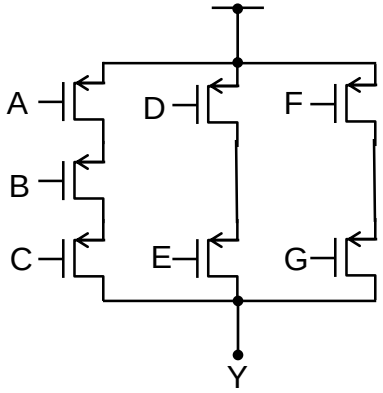
Hint: Demorgan Theorem

$$= (\overline{A}\cdot\overline{B}\cdot\overline{C}) + (\overline{D}\cdot\overline{E}) + (\overline{F}\cdot\overline{G})$$

Pull Down Network

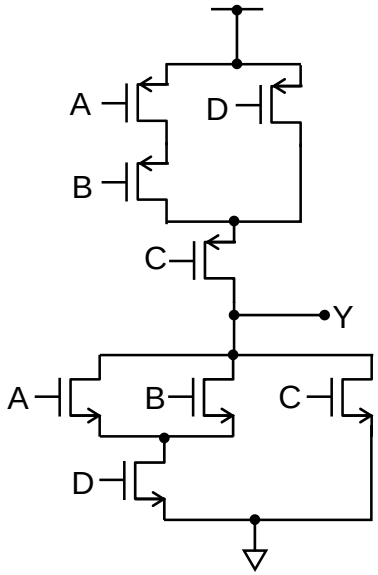


Pull Up Network (Duality)



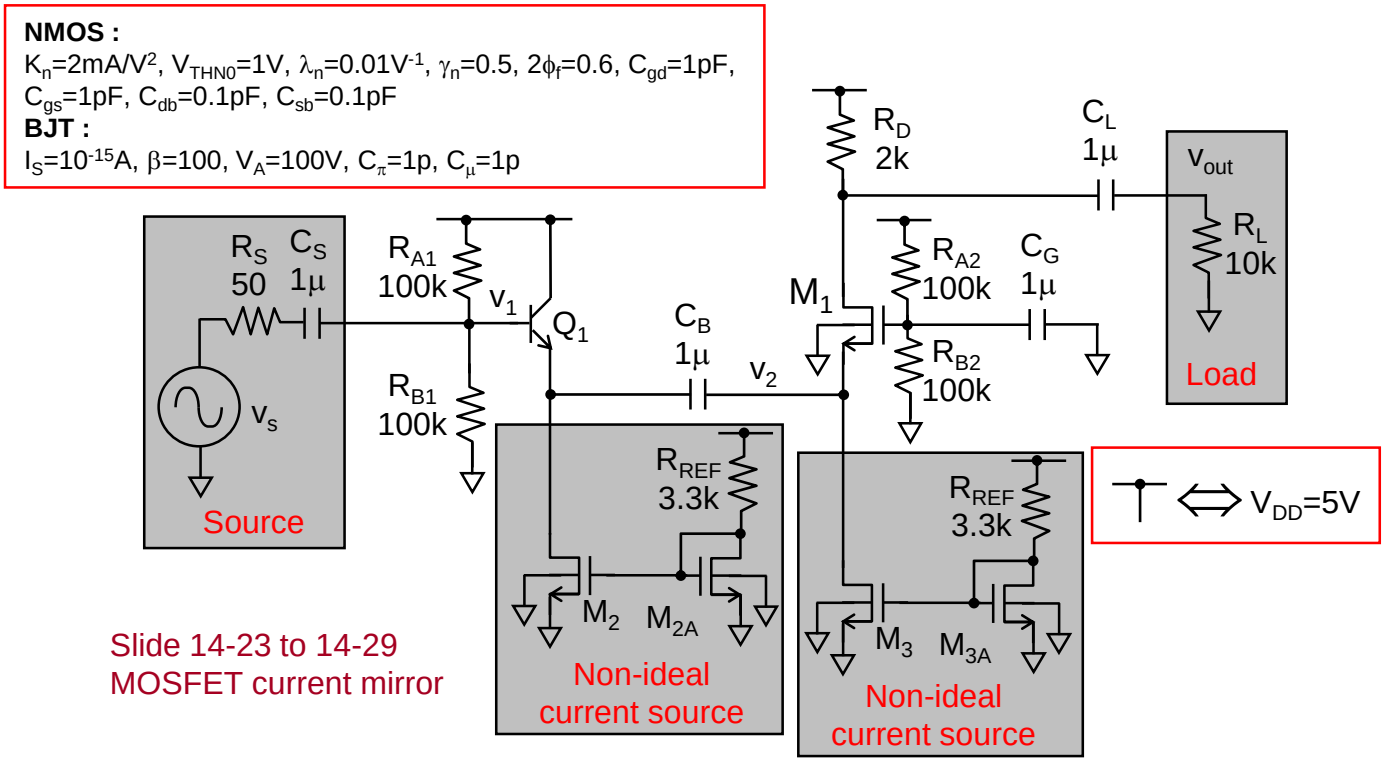
Rev-3

Logic Function



$$
\begin{aligned}
Y &= \overline{(A+B)\cdot D + C} \\
&= \overline{(A+B)\cdot D}\cdot\overline{C} \\
&= \left(\overline{(A+B)}+\overline{D}\right)\cdot\overline{C} \\
&= \left(\overline{A}\cdot\overline{B}+\overline{D}\right)\cdot\overline{C}
\end{aligned}
$$

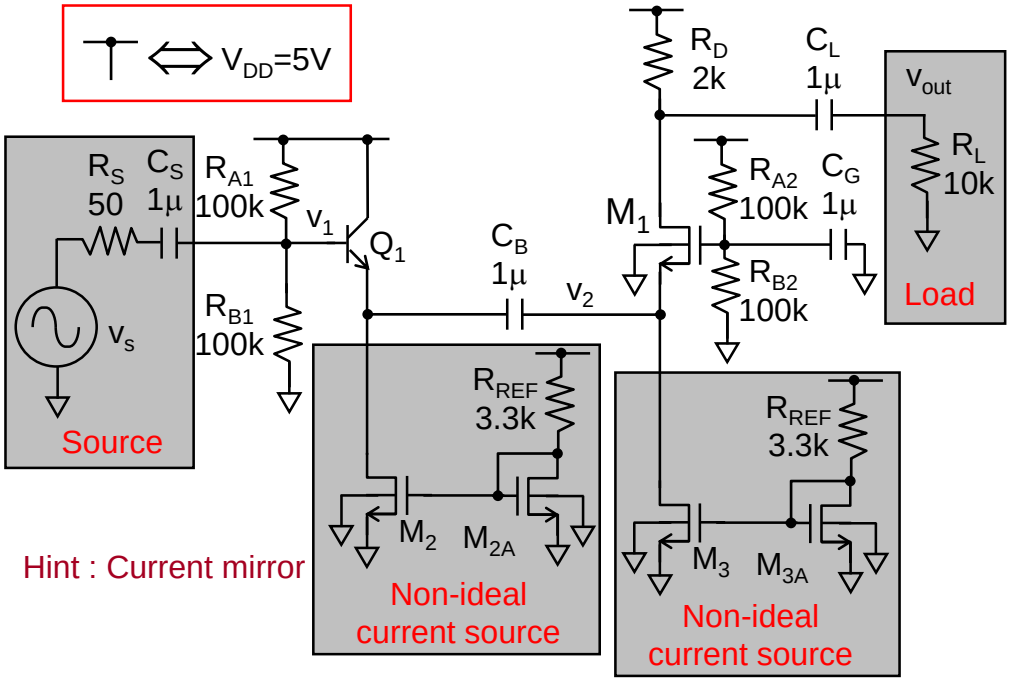
DC Analysis : Identifying



- Identify AC source, load and non-ideal current source

DC Analysis : DC Biasing

NMOS :
K_n=2mA/V^2, V_{THN0}=1V, λ_n=0.01V^{-1}, γ_n=0.5, $2\phi_f$=0.6, C_{gd}=1pF, C_{gs}=1pF, C_{db}=0.1pF, C_{sb}=0.1pF
BJT :
I_S=10^{-15}A, β=100, V_A=100V, C_π=1p, C_μ=1p



Hint : Current mirror

- Find the DC biasing current for Q_1 and M_1

Determine DC Biasing

$$I_{D,M2A} = K_n\left(V_{GS,M2A} - V_{THN0}\right)^2 \cdots\cdots(1)$$

$$I_{D,M2A} = \frac{V_{DD} - V_{GS,M2A}}{R_{REF}} \cdots\cdots(2)$$

$$\Rightarrow 6.6V_{GS,M2A}^2 - 13.2V_{GS,M2A} + 6.6 = 5 - V_{GS,M2A}$$

$$\Rightarrow 6.6V_{GS,M2A}^2 - 12.2V_{GS,M2A} + 1.6 = 0$$

$$\Rightarrow V_{GS,M2A} = \frac{-(-12.2) \pm \sqrt{(12.2)^2 - 4(6.6)(1.6)}}{2(6.6)}$$

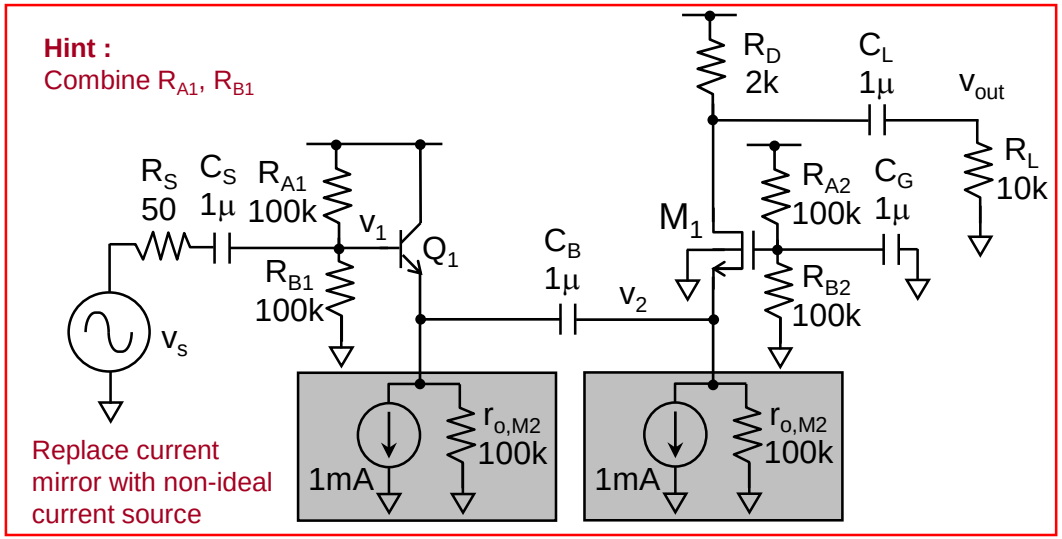
$$= 1.71 \quad or \quad 0.142 \left(< V_{THN0} \Rightarrow invalid\right)$$

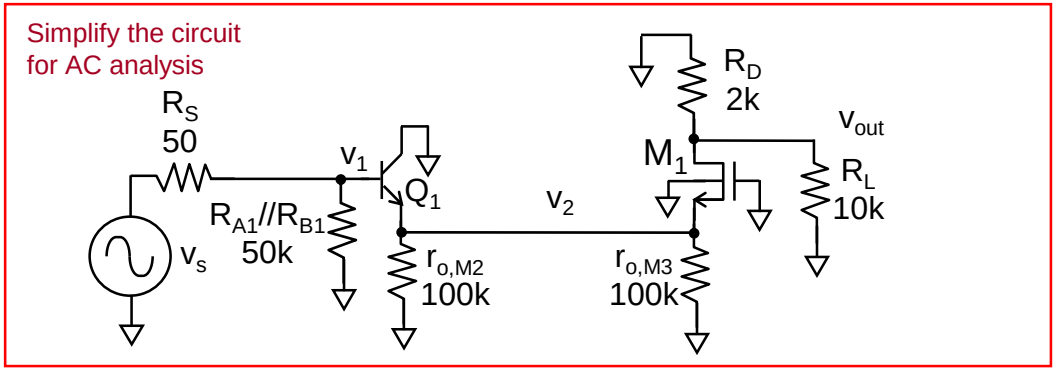
$$\Rightarrow I_{C,Q1} \approx I_{D,M2A} = I_{D,M2} = 1mA$$

Similarly

$$\Rightarrow I_{D,M1} = I_{D,M3} = I_{D,M3A} = 1mA$$

AC Analysis : Simplify the Circuit and Find Out AC Small Signal Parameter





Determine AC small signal parameter

$$g_{m,M1} = \sqrt{4K_n I_{D,M1}} = 2.83mA/V$$

$$g_{mb,M1} = -\frac{g_{m,M1}}{4} = -0.71mA/V$$

$$r_{o,M1} = r_{o,M3} = r_{o,M2} = \frac{1}{\lambda_n I_{D,M1}} = 100k$$

$$g_{m,Q1} = \frac{I_C}{V_T} = 40mA/V$$

$$r_{\pi,Q1} = \frac{\beta}{g_{m,Q1}} = 2.5k$$

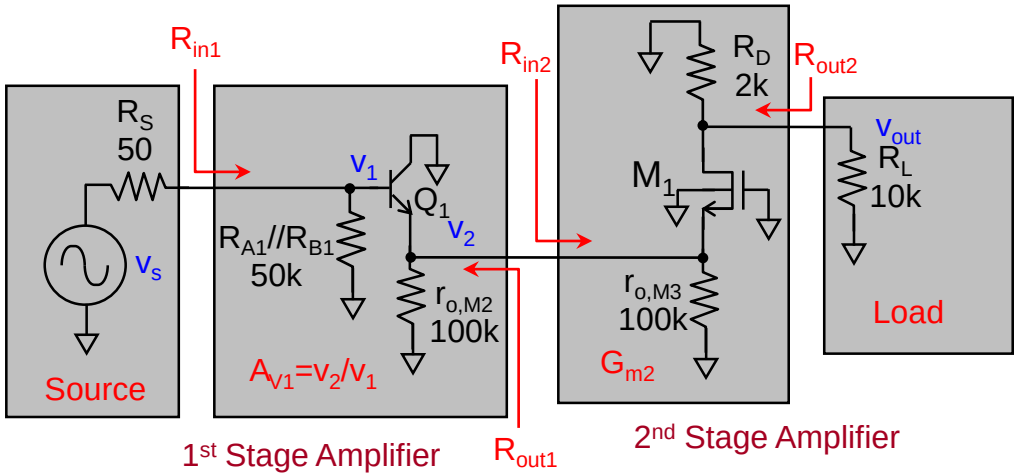
$$r_{o,Q1} = \frac{V_A}{I_{C,Q1}} = 100k$$

Hint :

1) DC voltage source→AC ground
2) DC current source→Open circuit
3) DC block/bypass capacitor→AC short circuit

- Simplify the circuit for AC analysis by replacing current mirror with non-ideal current source
- Find out the AC small signal parameters (g_m, r_π, r_o) for transistors Q_1, M_1, M_2, M_3

AC Analysis : Identify Amplifier



1st stage amplifier configuration :
Common Collector (CC)

2nd stage amplifier configuration :
Common Gate (CG)

1st stage amplifier G_{m1} :
Not applicable
Table 3 Configuration C

2nd stage amplifier G_{m2} :
$-(g_{m,M1}-g_{mb,M1})=-3.54$mA/V
Table 4 Configuration B

- Identify the 1st and 2nd stage amplifiers by drawing rectangular box surrounding them
- Write down the corresponding two ports-network parameters

AC Analysis : Identify Two-ports Network Parameters (R_{in2}, R_{out1})

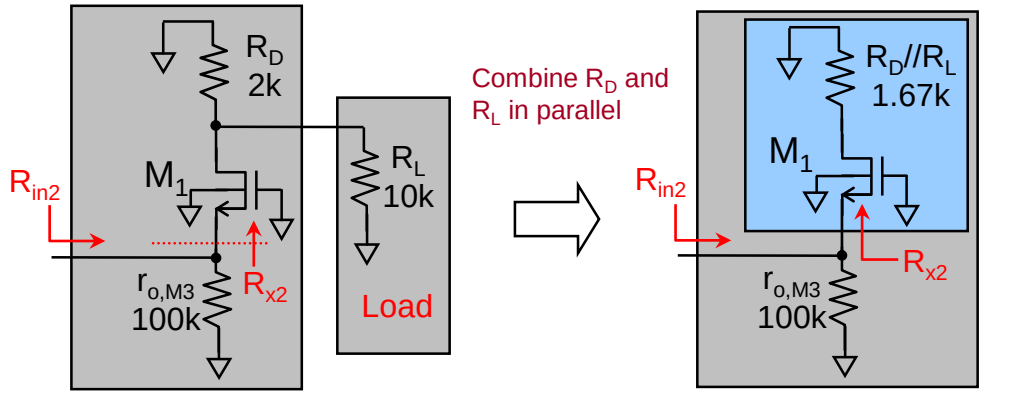


Table 2 Configuration D

$$R_{x2} = \frac{1}{g_{m,M1} - g_{mb,M1}} \frac{r_{o,M1} + (R_D \,//\, R_L)}{r_{o,M1}}$$

$$\approx \frac{1}{g_{m,M1} - g_{mb,M1}} = 283$$

$$R_{in2} = R_{x2} \,//\, r_{o,M3} \approx R_{x2} = \frac{1}{g_{m,M1} - g_{mb,M1}} = 283$$

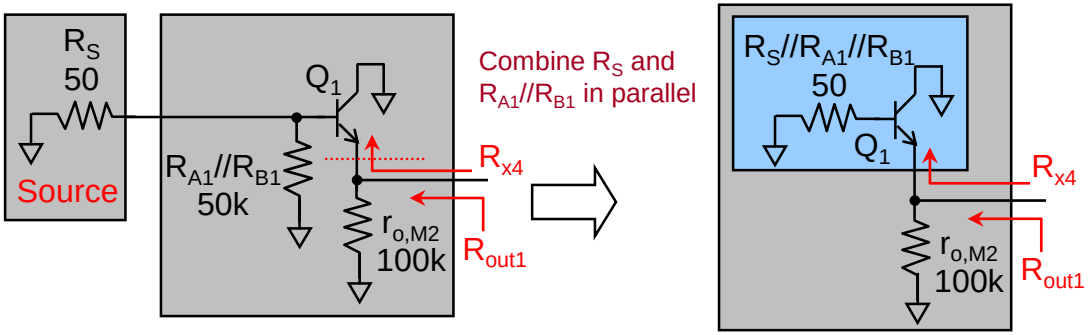


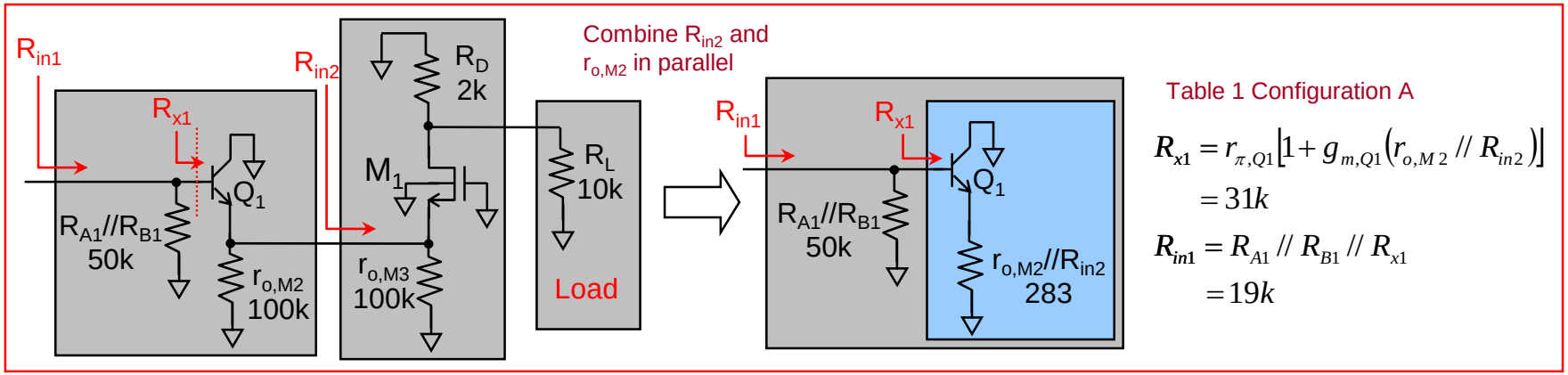
Table 1 Configuration C

$$R_{x4} = \frac{R_S \,//\, R_{A1} \,//\, R_{B1}}{\beta + 1} + \frac{1}{g_{m,Q1}} \approx \frac{1}{g_{m,Q1}} = 25$$

$$R_{out1} = R_{x4} \,//\, r_{o,M2} \approx \frac{1}{g_{m,Q1}} = 25$$

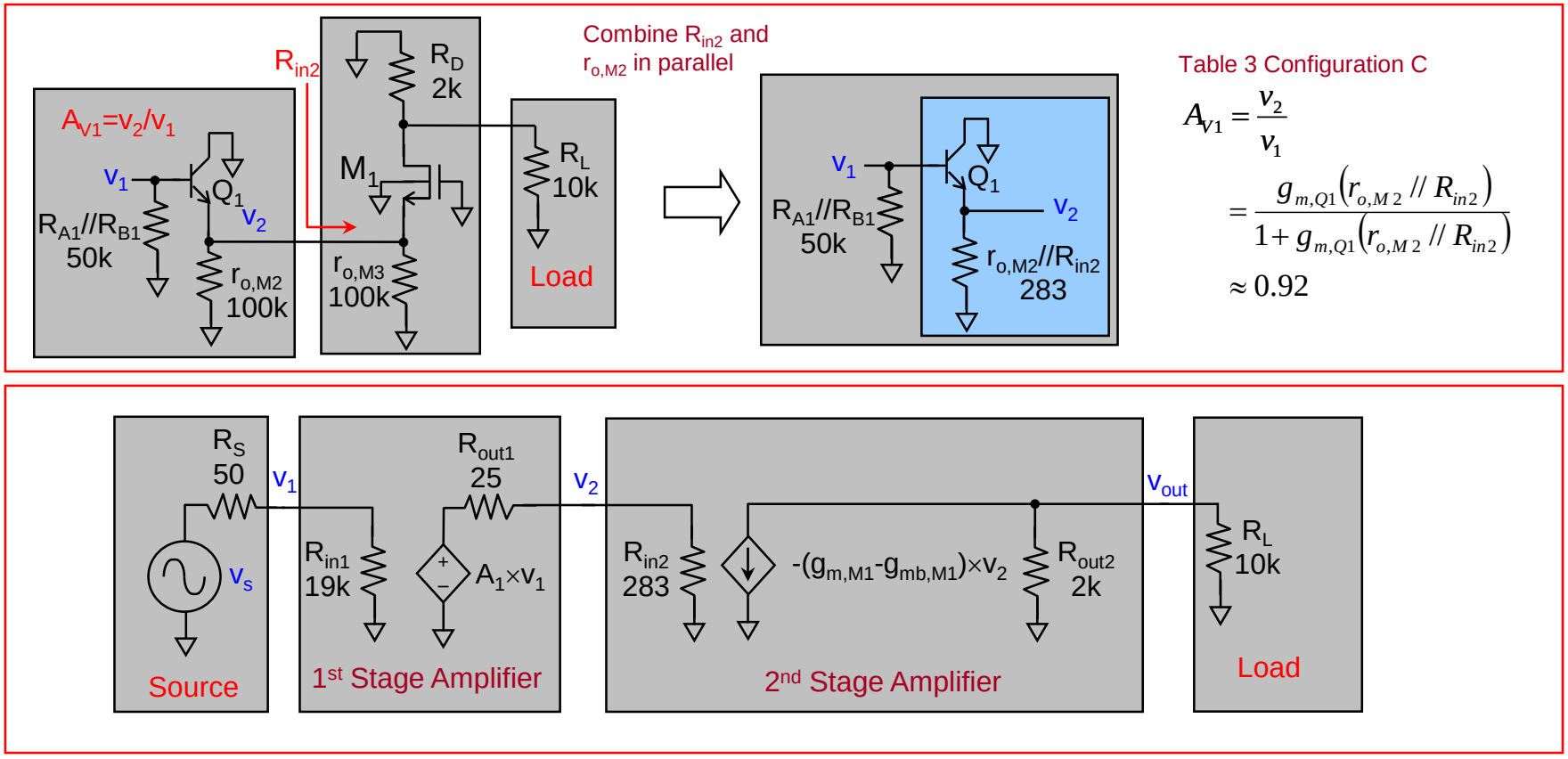
- Estimate R_{in2} and R_{out1} (Throw away half the circuit)

AC Analysis : Identify Two-ports Network Parameters (R_{in1}, R_{out2})



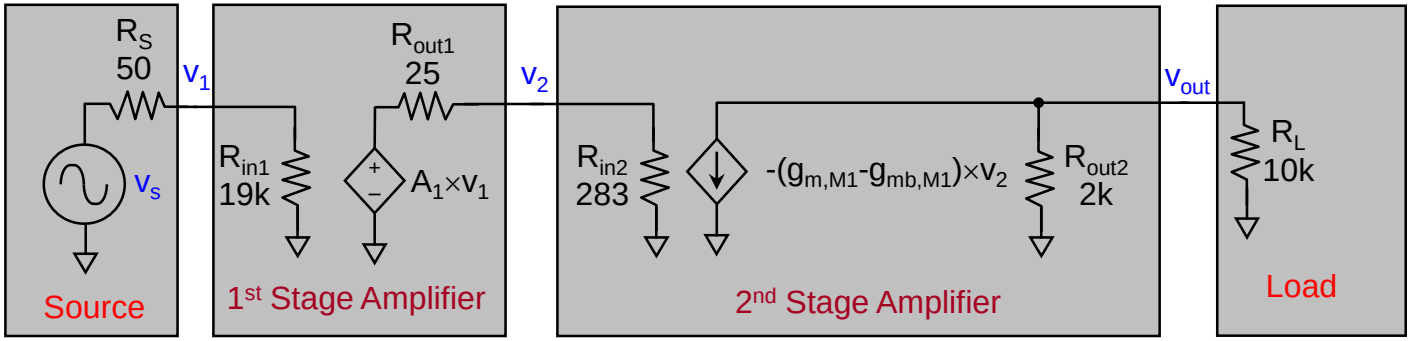
- Estimate R_{in1} and R_{out2}

AC Analysis : Identify $A_{V1}=v_2/v_1$



- Estimate $A_{V1}=v_2/v_1$
- Draw out two-ports network equivalent

AC Analysis : Overall Gain $A_V=v_{out}/v_s$



$$v_1 = \frac{R_{in1}}{R_{in1}+R_S} \times v_s \approx v_s$$

$$v_2 = \frac{g_{m,Q1}\left(r_{o,M2} \,//\, R_{in2}\right)}{1+g_{m,Q1}\left(r_{o,M2} \,//\, R_{in2}\right)} \times v_1 \approx 0.92 \times v_1 \approx 0.92 \times v_s$$

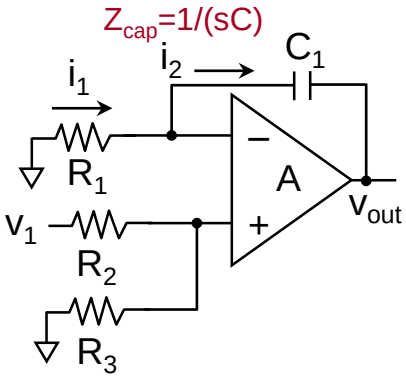
$$v_{out} = \left(g_{m,M1}-g_{mb,M1}\right)\left(v_2\right) \times \left(R_{out2} \,//\, R_L\right) \approx 5.91 \times v_2 \approx 5.43 \times v_s$$

$$A_V = \frac{v_{out}}{v_s} = \underbrace{\frac{R_{in1}}{R_{in1}+R_S}}_{Resistor\ Divider} \times \underbrace{A_{V1}}_{CC} \times \underbrace{G_{m2}\left(R_{out2} \,//\, R_L\right)}_{CG}$$

$$= \underbrace{\frac{R_{in1}}{R_{in1}+R_S}}_{Resistor\ Divider} \times \underbrace{\frac{g_{m,Q1}\left(r_{o,M2} \,//\, R_{in2}\right)}{1+g_{m,Q1}\left(r_{o,M2} \,//\, R_{in2}\right)}}_{CC} \times \underbrace{\left(g_{m,M1}-g_{mb,M1}\right)\left(R_{out2} \,//\, R_L\right)}_{CG} = 5.43$$

- Estimate overall gain $A_V=v_{out}/v_s$

Opamp Circuit Analysis



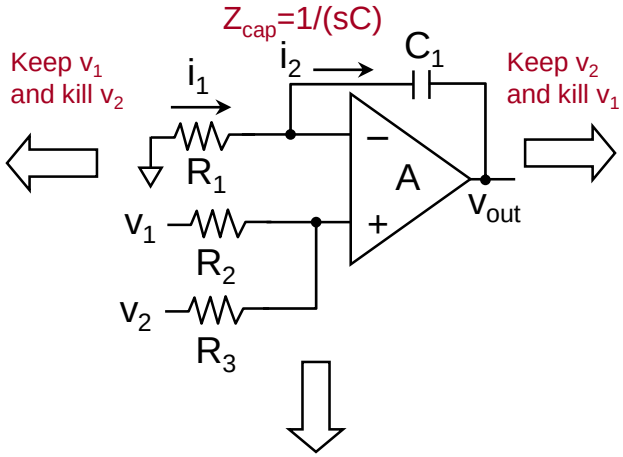
$$v_+ = v_1 \times \frac{R_3}{R_2 + R_3} \approx v_- \left[\because Virtual \quad short\right]$$

$$i_1 = i_2 \left[\because i_- = i_+ = 0\right]$$

$$\Rightarrow \frac{0 - v_-}{R_1} = \frac{v_- - v_{out}}{\frac{1}{sC_1}}$$

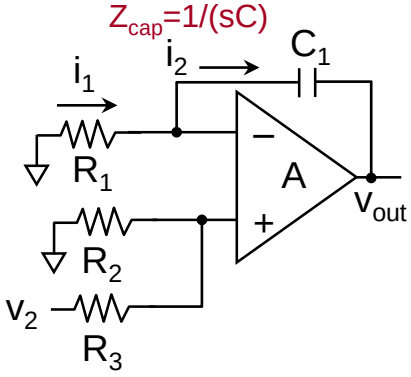
$$\Rightarrow v_{out} = v_- \times \left(1 + \frac{1}{sC_1R_1}\right)$$

$$= v_1 \times \frac{R_3}{R_2 + R_3} \times \left(1 + \frac{1}{sC_1R_1}\right)$$



Superposition :

$$v_{out} = \left(\frac{v_1 \times R_3 + v_2 \times R_2}{R_2 + R_3}\right)\left(1 + \frac{1}{sC_1R_1}\right)$$



$$v_+ = v_2 \times \frac{R_2}{R_3 + R_2} \approx v_- \left[\because Virtual \quad short\right]$$

$$i_1 = i_2 \left[\because i_- = i_+ = 0\right]$$

$$\Rightarrow \frac{0 - v_-}{R_1} = \frac{v_- - v_{out}}{\frac{1}{sC_1}}$$

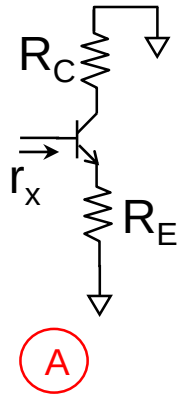
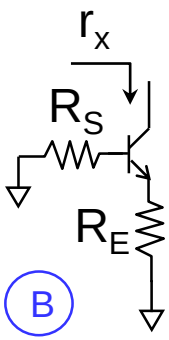
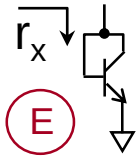
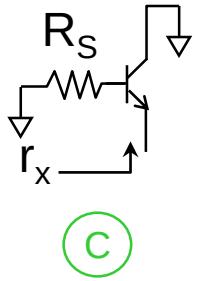
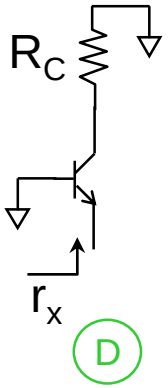
$$\Rightarrow v_{out} = v_- \times \left(1 + \frac{1}{sC_1R_1}\right)$$

$$= v_2 \times \frac{R_2}{R_3 + R_2} \times \left(1 + \frac{1}{sC_1R_1}\right)$$

- Virtual short ($v_+ \approx v_-$)
- Infinite input resistance ($i_+ = i_- = 0$)
- Superposition

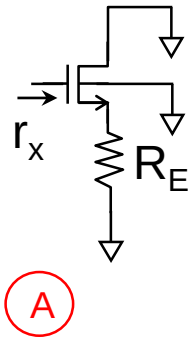
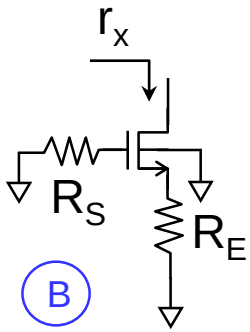
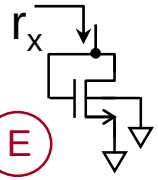
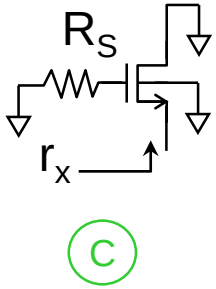
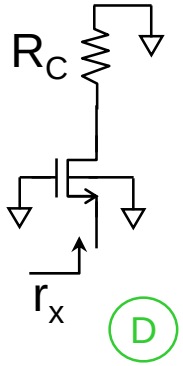
BJT Equivalent Resistance Summary (Table 1)

Blue: look into collector terminal Red: look into base terminal Green: look into emitter terminal

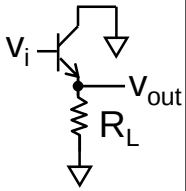
Conf	r_x	Conf	r_x	Conf	r_x
	$r_\pi + (1+\beta)R_E$ $\approx r_\pi(1+g_m R_E)$		$r_o\left\{1+g_m\left[(r_\pi+R_S)\,//\,R_E\right]\left(\frac{r_\pi}{r_\pi+R_S}\right)\right\}$ $If\ \ R_S=0\ \ and\ \ r_\pi << R_E$ $\Rightarrow r_{x,\max}=r_o(\beta+1)$		$\frac{1}{g_m}$
	$\frac{R_S+r_\pi}{1+\beta}\,//\,r_o$ $\approx \frac{R_S}{1+\beta}+\frac{1}{g_m}$		$\frac{1}{g_m}\times\frac{r_o+R_C}{r_o+R_C/\beta}$		

MOS Equivalent Resistance Summary (Table 2)

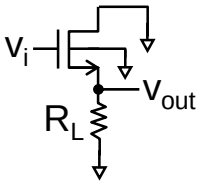
Blue: look into drain terminal Red: look into gate terminal Green: look into source terminal

Conf	r_x	Conf	r_x	Conf	r_x
	∞		$r_o\left[1+\left(g_m-g_{mb}\right)R_E\right]$		$\frac{1}{g_m}$
	$\frac{1}{g_m-g_{mb}}$		$\frac{1}{g_m-g_{mb}}\times\frac{r_o+R_C}{r_o}$		

BJT Summary (Table 3)

BJT	G_m	A_V
CE A	g_m	Derive Based on 2-ports Network
CB B	$-g_m$	Derive Based on 2-ports Network
CC C 	Not Applicable	$\frac{g_m R_L}{1+g_m R_L}$
CE with Emitter Degeneration D	$\frac{g_m}{1+g_m R_E}$	Derive Based on 2-ports Network

MOS Summary (Table 4)

MOS	G_m	A_V
CS A	g_m	Derive Based on 2-ports Network
CG B	$-(g_m - g_{mb})$ $Drop\ \ g_{mb}\ \ if\ \ no\ \ body\ \ effect$	Derive Based on 2-ports Network
CD C 	Not Applicable	$\frac{g_m R_L}{1+(g_m - g_{mb})R_L} \approx \frac{g_m}{g_m - g_{mb}}$ $Drop\ \ g_{mb}\ \ if\ \ no\ \ body\ \ effect$
CS with R_E D	$\frac{g_m}{1+(g_m - g_{mb})R_E}$ $Drop\ \ g_{mb}\ \ if\ \ no\ \ body\ \ effect$	Derive Based on 2-ports Network