NATIONAL UNIVERSITY OF SINGAPORE

Department of Electrical and Computer Engineering

EE2021: Tutorial 2 (*pn* Junction) - Solutions

<u>Homework 1</u>:

Homework 1 is Question 2 of Tutorial 2 and you will need to submit a hand-written, hardcopy in class <u>on Wednesday, 11 Feb 2015.</u>

- Unless otherwise stated, you may assume temperature, $T = 300$ K, $V_T = 0.025$V, and make use of the equations given in the lecture notes directly, without having to derive them. Assume that all the symbols are as defined in the lecture notes.

1. Calculate the parameters in the table below for the following 3 silicon *pn* junction diodes (junction area, $A = 1$ mm^2) under no applied external voltage condition, at $T = 300$K. N_A is the net acceptor doping on the p-type side, and N_D is the net donor doping on the n-type side. It is given that $n_i = 1.5 \times 10^{10}$ cm^{-3} for silicon at 300 K.

Diode	N_A / cm^{-3}	N_D / cm^{-3}	V_o / V	W_{dep} / µm	x_p / µm	x_n / µm
A	5 x 10^{15}	5 x 10^{15}				
B	5 x 10^{15}	5 x 10^{17}				
C	5 x 10^{17}	5 x 10^{17}				

Comment on how the above answers vary with the net doping concentrations of the *p* and *n* regions, N_A and N_D, respectively.

---

1. The relevant equations are:

- $V_0 = V_T \times \ln\left(\frac{p_{p0} n_{n0}}{n_i^2}\right)$, where, in this case, $p_{p0} = N_A$, $n_{n0} = N_D$.
- $W_{dep} = \sqrt{\frac{2\varepsilon_S}{q}\left(\frac{1}{N_A} + \frac{1}{N_D}\right)V_0}$
- $\frac{x_p}{x_n} = \frac{N_D}{N_A}$
- $x_p = \left(\frac{N_D}{N_A + N_D}\right)W_{dep}$ and $x_n = \left(\frac{N_A}{N_A + N_D}\right)W_{dep}$

For Diode A :

$p_{p0} = N_A = 5\times 10^{15}$ cm^{-3}, $n_{n0} = N_D = 5\times 10^{15}$ cm^{-3}.

$$V_0 = V_T = \ln\left(\frac{p_{p0}n_{n0}}{n_i^2}\right) = 0.025\times\ln\left[\frac{5\times10^{15}\times5\times10^{15}}{\left(1.5\times10^{10}\right)^2}\right] = 0.636\ \text{V}.$$

$$W_{dep} = \sqrt{\frac{2\varepsilon_S}{q}\left(\frac{1}{N_A}+\frac{1}{N_D}\right)V_0} = \sqrt{\frac{2\times11.7\times8.854\times10^{-14}}{1.602\times10^{-19}}\left(\frac{1}{5\times10^{15}}+\frac{1}{5\times10^{15}}\right)\times0.636}$$
$$= 5.74\times10^{-5}\ \text{cm} = 0.574\ \mu\text{m}.$$

$$x_p = \left(\frac{N_D}{N_A+N_D}\right)W_{dep} = \left(\frac{5\times10^{15}}{5\times10^{15}+5\times10^{15}}\right)\times0.574 = 0.287\mu\text{m}.$$

$$x_n = \left(\frac{N_A}{N_A+N_D}\right)W_{dep} = \left(\frac{5\times10^{15}}{5\times10^{15}+5\times10^{15}}\right)\times0.574 = 0.287\mu\text{m}.$$

The answers are :

Diode	N_A / cm^{-3}	N_D / cm^{-3}	V_o / V	W_{dep} / µm	x_p / µm	x_n / µm
A	5 x 10^{15}	5 x 10^{15}	**0.636**	**0.574**	**0.287**	**0.287**
B	5 x 10^{15}	5 x 10^{17}	**0.751**	**0.443**	**0.439**	**0.0044**
C	5 x 10^{17}	5 x 10^{17}	**0.866**	**0.067**	**0.033**	**0.033**

Comments :

- The built-in voltage, V_o, increases with increasing doping concentration, but the rate of increase is small because the functional dependence is logarithmic.
- The width of the depletion region, W_{dep}, decreases with increasing doping concentration (of either one side of *pn*-junction, or both), since it is almost inversely proportional to the square root of the doping concentration. The proportionality is not exact because W_{dep} also depends on V_o.
- The extensions of the depletion regions into the *p*-region and *n*-region, x_p and x_n, respectively, depend not only on N_A and N_D, but also the ratio of N_A/N_D. Between diodes A and C, where $N_A/N_D = 1$, x_p and x_n follow the same trend as W_{dep}, i.e., decrease with increasing doping concentration. As for diode B, where $N_A/N_D \neq 1$, $x_p >> x_n$ as a result of $N_A << N_D$. In general, the higher the doping concentration on one side of the junction, the narrower is the width of the depletion region in that region.

2. Consider a Si substrate with an initial doping of 3×10^{15} cm^{-3} of donors (Region 1). A pn junction is made in the Si substrate by doping a selected region (Region 2) with an additional 8×10^{15} cm^{-3} of acceptors, as shown in Fig. Q2.1. The temperature, $T = 300$ K, the intrinsic carrier concentration in Si, $n_i = 1.5\times10^{10}$ cm^{-3} and the thermal voltage, $V_T = 0.025$ V.

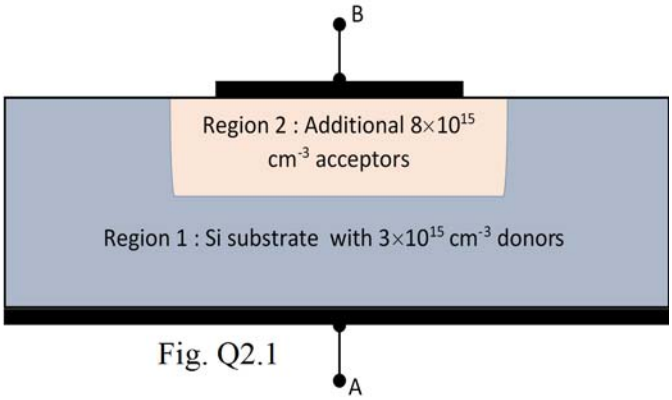


Fig. Q2.1

(a) In the Si substrate (Region 1), what are the majority carriers (i.e., electrons or holes?) and what are the minority carriers? What are the respective concentrations of the majority carriers and the minority carriers?

(b) In Region 2, what are the majority carriers and the minority carriers ? What are their respective concentrations?

(c) What is the built-in voltage V_0 of the pn junction?

(d) Under the reverse bias condition, which of the two terminals (A and B) is at s higher voltage with respect to the other?

(e) In Fig Q2.2 below, sketch the respective minority carrier distributions in the neutral p-region and n-region of the pn junction (i.e., where $x < -x_p$ and $x > x_n$) under a reverse bias of 1 V and indicate their concentrations at the boundaries of the neutral regions. The depletion region of the pn junction extends from $x = -x_p$ to $x = x_n$). You can assume that the neutral regions in the pn junction to be much longer than the respective minority carrier diffusion lengths.

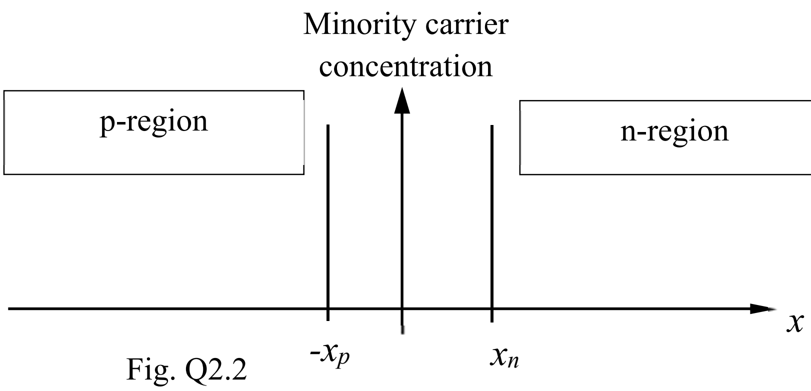


Fig. Q2.2

2. (a) The substrate is doped only with donors ($N_D = 3\times10^{15}$ cm^{-3} >> n_i), which contribute to electrons, hence majority carriers in the substrate are <u>electrons.</u> [1 mark]

The minority carriers are <u>holes</u>. [1 mark]

Majority carrier concentration, $\underline{n_{n0} \approx N_D = 3\times10^{15}\text{ cm}^{-3}}$. [1 mark]

Minority carrier concentration,

$p_{n0} = n_i^2/n_{n0} = (1.5\times10^{10})^2/(3\times10^{15}) = \underline{7.5\times10^4\text{ cm}^{-3}}$. [1 mark]

(b) Region 2 contains both the original donors ($N_D = 3\times10^{15}$ cm^{-3}) as well as additional acceptors of concentration $N_A = 8\times10^{15}$ cm^{-3}. There is thus compensation doping. As $N_A > N_D$, Region 2 is p-type. The majority carriers are <u>holes</u>. [1 mark]

The minority carriers are <u>electrons</u>. [1 mark]

Majority carrier concentration ≈ Net acceptor doping, i.e.,

$p_{p0} \approx N_A - N_D = 8\times10^{15} - 3\times10^{15} = \underline{5\times10^{15}\text{cm}^{-3}}$. [2 marks]

Minority carrier concentration,

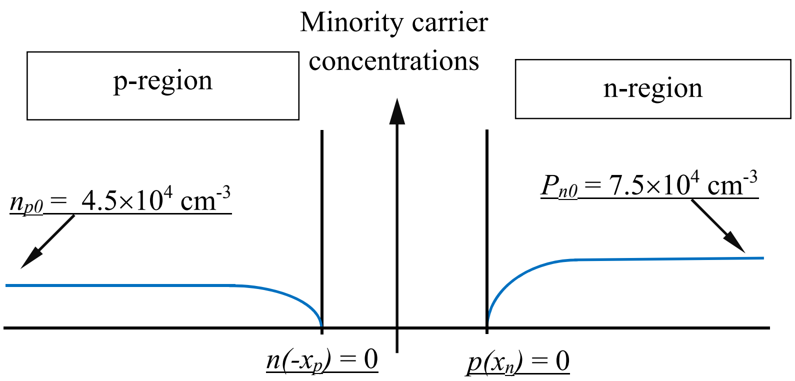
$n_{p0} = n_i^2/p_{p0} = (1.5\times10^{10})^2/(5\times10^{15}) = \underline{4.5\times10^4\text{ cm}^{-3}}$. [2 marks]

(c) The built-in voltage of the pn junction

$$\underline{V_0 = V_T \ln\left(\frac{p_{p0}n_{no}}{n_i^2}\right) = 0.025\times\ln\left[\frac{5\times10^{15}\times3\times10^{15}}{\left(1.5\times10^{10}\right)^2}\right] = 0.623\text{ V}}.$$ [2 marks]

(d) Under reverse bias, A is at a higher voltage with respect to B. [2 marks]

(e)



For each concentration indicated (answer underlined) - 1 mark [total 4 marks]

For each minority carrier distribution indicated (blue line) - 1 mark. [total 2marks]

3. Figure Q3 shows a circuit consisting of a voltage source V_{DD}, two resistors R_1, R_2 and a Zener diode, which breaks down at a reverse voltage $V_Z = 6$ V. For reverse voltages less than V_Z, the reverse saturation current of the diode is negligible.

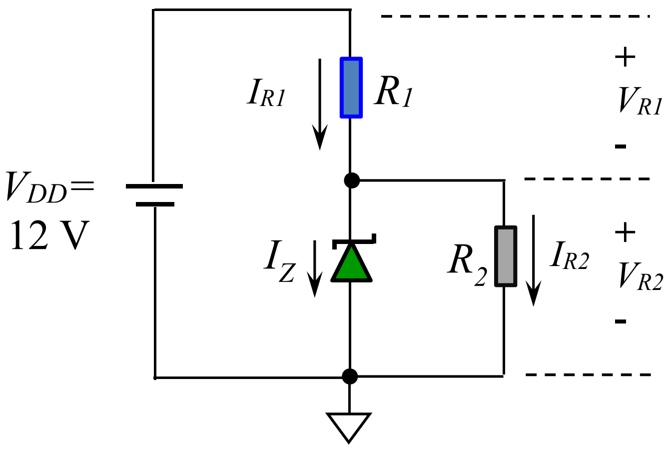


Fig. Q3

(a) Consider the case where $R_1 = 10$ kΩ and $R_2 = 2$ kΩ. *Assume* that the Zener diode is NOT operating in the breakdown region.

(i) Calculate the voltage V_{R2} across the Zener diode. Hence check whether the assumption that the Zener diode is NOT operating in the breakdown region is correct.

(ii) Calculate the voltage V_{R1} and the currents I_{R1}, I_{R2}, I_Z.

(b) Consider the case where $R_1 = 2$ kΩ and $R_2 = 4$ kΩ. Is the assumption that the Zener diode is NOT operating in the breakdown region valid in this case?

Determine the voltages V_{R1}, V_{R2} and the currents I_{R1}, I_{R2}, I_Z.

3. (a) If it is assumed that the Zener diode in NOT operating in the breakdown region, then it behaves like an open circuit since its reverse current is negligible. R_1 and R_2 are therefore in series.

(i) $V_{R2} = V_{DD} \times \dfrac{R_2}{R_1 + R_2} = 12 \times \dfrac{2\text{ k}}{10\text{ k} + 2\text{ k}} = 2\text{ V}.$

As V_{R2} is also the voltage across the Zener diode, and it is less than the breakdown voltage of V_Z (= 6V), the assumption that the Zener diode is not operating in the breakdown region is valid.

(ii) $V_{R1} = V_{DD} - V_{R2} = 10\text{ V}.$

As it is given that the reverse saturation current of the Zener diode when it is not operating in the breakdown region is negligible, $I_Z \approx 0$.

$$I_{R1} = I_{R2} = \frac{V_{DD}}{R_1 + R_2} = \frac{12\text{ V}}{10\text{ k} + 2\text{ k}} = 1\text{ mA}.$$

(b) First, we <u>assume</u> initially that the Zener diode is <u>not</u> operating in the breakdown region, and calculate the voltage across it.

$$V_{R2} = V_{DD} \times \frac{R_2}{R_1 + R_2} = 12 \times \frac{4\text{ k}}{2\text{ k} + 4\text{ k}} = 8\text{ V}.$$

As this voltage is greater than the breakdown voltage of the Zener diode (V_Z = 6V), the initial <u>assumption</u> that the Zener diode is not operating in the breakdown region is <u>not correct</u>. It is in fact operating in the breakdown region. In this case, the voltage across the Zener diode, and also R_2, is clamped to the breakdown voltage, i.e.,

$$V_{R2} = V_Z = 6\text{ V}.$$

$$V_{R1} = V_{DD} - V_{R2} = 6\text{ V}.$$

$$I_{R2} = \frac{V_{R2}}{R_2} = \frac{6\text{ V}}{4\text{ k}} = 1.5\text{ mA}.$$

$$I_{R1} = \frac{V_{R1}}{R_1} = \frac{6\text{ V}}{2\text{ k}} = 3\text{ mA}.$$

$$I_Z = I_{R1} - I_{R2} = 1.5\text{ mA}.$$

4. The current (I) flowing through a semiconductor pn junction diode at various forward bias voltages (V) are measured and tabulated as follows:

V (V)	I (A)
0.00	0.00
0.10	~0.00
0.20	~0.00
0.30	~0.00
0.40	~0.00
0.50	4.70×10^{-5}
0.55	3.70×10^{-4}
0.60	2.52×10^{-3}
0.62	5.91×10^{-3}
0.64	1.38×10^{-2}
0.66	2.73×10^{-2}
0.68	6.40×10^{-2}
0.70	1.51×10^{-1}

(a) Plot the I-V characteristic of the diode from V = 0 to 0.7 V, and estimate the cut-in voltage of the diode.

(b) The I-V characteristic of the semiconductor diode is given as follows:

$$I = I_S\left(e^{V/V_T} - 1\right), \text{ where } V_T = 0.025\text{V}.$$

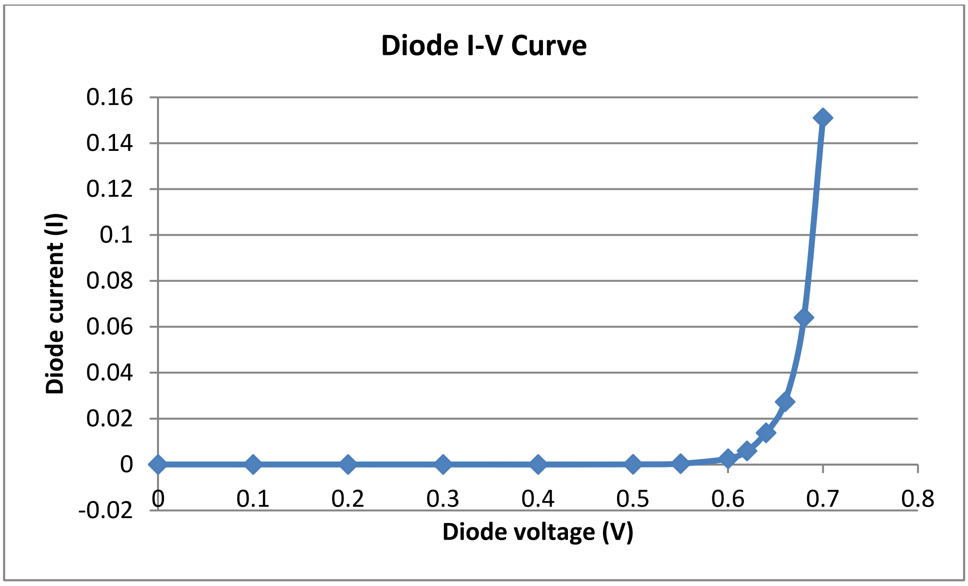
Estimate the value of the reverse saturation current (I_S) by devising a suitable plot between I and V in forward bias.

Take note that the values of I in the above table are measured, and are therefore likely to have experimental errors. Hence, one will not estimate I_S by applying a single set of I versus V values from the table to the above equation, as that will not be accurate. Also, different sets of I versus V values are likely to give different I_S.
[Hint: The range of voltage (V) of the plot to be devised is an important consideration, and you need to transform the above equation into the form of $y = mx + C$, i.e., a linear relation between y and x, where m and C are constants.]

(c) Consider the above diode where there is the series resistance, r_s, of the neutral p and n neutral regions. If, in a practical diode, r_s is 10 Ω, find the voltage drops across r_s using the currents at various voltages given in the table in part (a) when the voltage across the pn junction is 0.5, 0.6 and 0.7 V. Comment on your results. What are the actual voltages that would need to be applied to the real diode with r_s to have the same currents?

(d) Based on your calculations in part (c), discuss the effect on the I-V characteristic of the diode due to r_s.

4. (a) Plot of the I-V characteristic of the diode from $V = 0$ to 0.7 V is shown below.



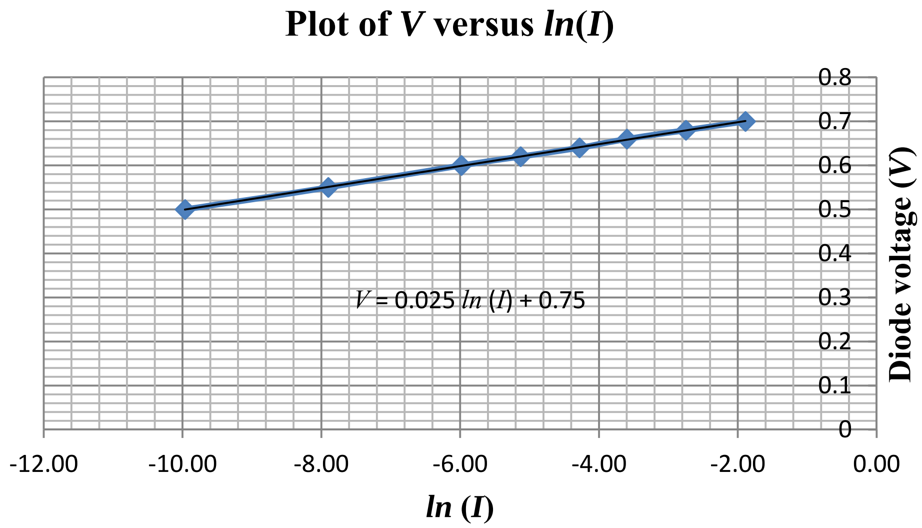
Cut-in voltage is ~0.6 V.

(b) For $V >> V_T$, $e^{V/V_T} \gg 1$, $\quad I = I_S\left(e^{V/V_T} - 1\right) \cong I_S e^{V/V_T}$

Hence, $\quad I/I_S = e^{V/V_T} \Rightarrow V = V_T[ln(I) - ln(I_S)]$

So, V is seen as a ***linear*** function of $ln(I)$. By plotting V against $ln(I)$ for $V >> V_T$ (e.g., $V \geq 0.5$ V), a straight line is obtained and its intercept with $ln(I)$-axis gives the value of $ln(I_S)$.

***V*(v)**	***ln* (*I*)**
0.5	-9.97
0.55	-7.90
0.6	-5.98
0.62	-5.13
0.64	-4.28
0.66	-3.60
0.68	-2.75
0.7	-1.89



From the above plot of V versus $ln(I)$ curve, the best-fit straight line is found (using EXCEL) to be -

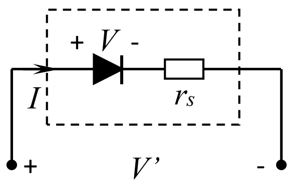
$$V = 0.025\ ln\ (\mathrm{I}) + 0.75.$$

By means of a best-fit plot, the experimental errors are average out. It is also seen in the above plot that it is **not** practical to extrapolate the best-fit straight line to find the intercept with the $ln(I)$-axis, so as to estimate I_S. Instead, we can compare the best-fit equation with $V = V_T[ln(I) - ln(I_S)]$, which yields

$$-V_T\ ln\ (I_S) = 0.75 \Rightarrow I_S = e^{-0.75/V_T} = e^{-30} = 9.36 \times 10^{-14}\ \mathrm{A}.$$

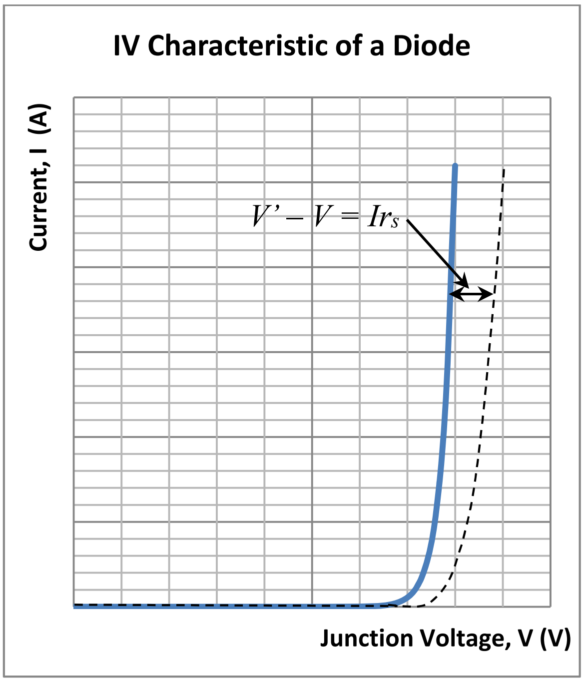
(c) The voltage drops across the resistor are 0.47 mV, 25.2 mV, 1.51 V at 0.5, 0.6 and 0.7 V, respectively. The diode current will be significantly reduced at 0.7 V, owing to the large voltage drop across r_s of 1.51 V, but the effect will be much reduced at 0.5 V. To maintain the diode current, we need to apply 0.6252 V and 2.21 V, respectively, instead of 0.6 V and 0.7V. There is practically no need to change the voltage at 0.5 V.

(d) Effectively, with substantial r_s, V in the equation: $I = I_S\left(e^{V/V_T} - 1\right)$ is reduced with respect to the voltage applied to the two ends (ohmic contacts) of the *pn* junction, $V' \cong V + Ir_s$, as shown in the figure below, where the dashed box represents a diode with substantial r_s. Note that V is now an ***internal*** voltage of the *pn* junction (across a region close to the space charge region).



$$I = I_S\left(e^{V/V_T} - 1\right) = I_S\left(e^{[V' - Ir_S]/V_T} - 1\right)$$

For the same I, owing to the additional voltage Ir_s, a higher voltage V' must be applied across the ohmic contacts of the pn junction. The higher the I, the higher is the difference between V' and V. Hence, with respect to the IV plot of part (a), a plot of I versus V' (dotted line) is shifted to the right and with a higher right shift for higher I, as shown below.



---

5. For the circuit shown in Fig. Q5, V_{DD} = 7 V and R = 3.3 kΩ, while the diode has parameters of I_s = 57.8 pA, and n = 1.56.

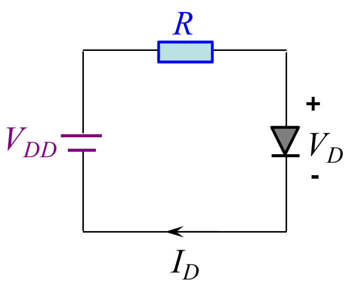


Fig. Q5

(a) Using the iteration method, find the values of I_D and V_D.

(b) In order to simplify the calculation, it is suggested to replace the diode in the circuit by a piecewise linear model which has parameters V_{DO} and r_D. Find appropriate values for V_{DO} and r_D if we wish the model to be accurate over the range of I_D from 1 mA to 3 mA.

[Hint: Use equation (2.41) of the pn-junction lecture notes, solve for 2 unknowns using 2 sets of (*I*,*V*) data.]

(c) Repeat the calculation for I_D and V_D in the circuit using the piecewise-linear model instead of the iteration method.

(d) Reflection:

(i) What is the error incurred in using the piecewise linear model?

(ii) How does the current range we use to determine V_{DO} and r_D influence the accuracy of the model?

(iii) The value of V_{DD} in the circuit is now changed to 1 V. If the model with the same parameter values is used to calculate I_D and V_D, would you expect the accuracy of the model to change? And why?

---

5. (a) Initially, we make a guess and assume V_{D1} = 0.7 V and apply Kirchhoff's Voltage Law (KVL) to the circuit to obtain an estimate for I_D –

$$I_{D1} = \frac{V_{DD}-V_{D1}}{R} = \frac{7-0.7}{3.3\text{k}} = 1.909 \text{ mA}$$

For the next iteration, better estimate of V_{D2} is given by solving the diode equation

$$1.909\ 10^{-3} = 57.8\ 10^{-12} \exp\left(\frac{V_{D2}}{1.56 \times 0.025}\right) \quad \Rightarrow V_{D2} = 0.6752 \text{ V}$$

With a better estimate V_{D2} = 0.6752 V, we obtain another estimate I_{D2} -

$$I_{D2} = \frac{V_{DD}-V_{D2}}{R} = \frac{7-0.6752}{3.3\text{k}} = 1.917 \text{ mA.}$$

For the next iteration, better estimate,V_{D3} is given by solving the diode equation

$$1.917\ 10^{-3} = 57.8\ 10^{-12} \exp\left(\frac{V_{D3}}{1.56 \times 0.025}\right) \quad \Rightarrow V_{D3} = 0.6753 \text{ V}$$

With a better estimate V_{D3} = 0.6753 V, we obtain another estimate I_{D3} -

$$I_{D3} = \frac{V_{DD}-V_{D3}}{R} = \frac{7-0.6753}{3.3\text{k}} = 1.917 \text{ mA.}$$

which is not changed much from the previous estimate.

Hence, V_D = **0.6753 V** and I_D = **1.917 mA** for the circuit.

(b) From the pn-junction lecture notes,

$$i_D = (v_D - V_{D0}) / r_D, \qquad v_D \geq V_{D0}. \qquad (2.41)$$

Using the diode equation, we can compute the diode voltage for diode currents at either end of the range:

$I = 1\text{mA}$, $V = 0.65$ V; and $I = 3\text{mA}$, $V = 0.6928$ V.

Substituting both sets of data into Eq (2.41), we have 2 equations

$$1 \text{ x } 10^{-3} = (0.65 - V_{DO})/r_D,$$

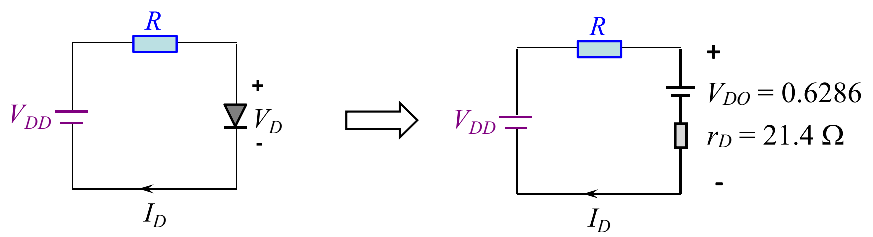
and

$$3 \text{ x } 10^{-3} = (0.6928 - V_{DO})/r_D.$$

Solving for V_{DO} and r_D, we have

V_{DO} = 0.6286 V; r_D = 21.42Ω .

(c)



Applying the piecewise linear model to replace the diode in the circuit, we can use KVL,

$$I_D = \frac{V_{DD} - V_{DO}}{R + r_D} = \frac{7 - 0.6286}{3.3\text{k} + 21.42} \cong \mathbf{1.918\ mA} \quad \text{(close to answer of (a))}$$

$V_D = V_{DO} + I_D r_D = 0.6286\,V + 1.918m \times 21.42\Omega = \mathbf{0.670\ V}$ (0.8% lower than answer of (a))

(d) Reflection:

(i) The piecewise linear model gives 0.8% lower value for V_D. It is accurate enough for most purposes.

(ii) The value of $\boldsymbol{r_D}$ is determined by the slope of the line joining the two (I, V) points used in computing the model parameters, and the value of V_{DO} is the intercept of the line with the x-axis. The choice of the 2 points is important and, for greatest accuracy, the 2 points should be chosen to straddle the region of interest in the I_D

– V_D characteristic, and the 2 points should not be too far apart. Otherwise, the model may not give accurate results.

(iii) If V_{DD} is reduced to 1.0 V, we would expect significantly decreased accuracy, as the diode voltage is now close to or less than V_{DO}, where the piece wise model is not so accurate. (Students are not expected to calculate the following, but for information the accurate solution: V_D = 0.5703 V, I_D = 0.130 mA. Using Piecewise model: V_D = 0.631 V, I_D = 0.1118 mA, > 10% out)

---

6. For the circuit shown in Fig. Q6, there are two current sources that supply currents of 101I and I, respectively, and two diodes D1 and D2. The I-V characteristics of D1 and D2 are given as follows:

$$I_{D1} \cong I_S e^{V_{D1}/V_T} \quad \text{and} \quad I_{D2} \cong 5 \times I_S e^{V_{D2}/V_T}, \text{ respectively.}$$

(a) In the context of the circuit of Fig. Q6, what are the assumptions made to obtain the above 2 approximate diode equations?

(b) Note that the saturation current of D2 is 5 times that of D1. Suggest possible ways to achieve that.

(c) Obtain an expression for V_{OUT} in terms of I, $R1$ and V_T.

(d) If $R1=R0\times(1+0.02\times T)$, where T is the absolute temperature, specify the $R0$ and I relationship such that V_{OUT} is temperature independent, i.e. V_{OUT} remains constant while temperature changes.

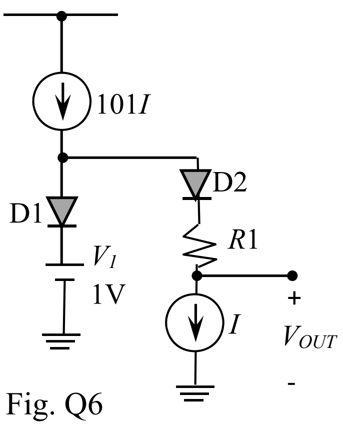


Fig. Q6

---

6. (a) Current flowing through D2 is I in the forward bias direction, and through D1 is $100\times I$ (= $101I - I$, by means of Kirchhoff Current Law), which is also in the forward bias direction. For the two approximate equations to be valid, the forward bias voltages of D1and D2 must be >> V_T.

(b) One can make the (junction) area of D2 5 times that of D1. Alternatively, one can adjust the doping concentrations of the pn junction diode, however, it may not be as straightforward as changing the junction area, because doping concentration will affect the mobility of carriers, and hence diffusion coefficients, diffusion length, etc., that will also affect the saturation current.

(c) Applying Kirchhoff Current Law (KCL):

Diode D2: $I_{D2} = 5 \times I_S e^{V_{D2}/V_T} = I \quad \Rightarrow \quad V_{D2} = V_T \ln\left(\frac{I}{5I_S}\right)$

Diode D1:

$$I_{D1} = I_S e^{V_{D1}/V_T} = 101I - I_{D2} = 101I - I = 100I \ \Rightarrow \ V_{D1} = V_T \ln\left(\frac{100I}{I_S}\right)$$

Hence, by means of Kirchhoff Voltage Law (KVL):

$$V_{OUT} = 1 + V_{D1} - V_{D2} - I \times R1 = 1 + \ V_T \ln\left(\frac{100I}{I_S}\right) - V_T \ln\left(\frac{I}{5I_S}\right) - I \times R1$$

$$= 1 + \frac{kT}{q}\ln(500) - I \times R1$$

(e)

$$V_{OUT} = 1 + \frac{kT}{q}\ln(500) - I \times R1$$

$$= 1 + \frac{kT}{q}\ln(500) - I \times R0(1 + 0.02T)$$

For temperature independence

$$\frac{kT}{q}\ln(500) - I \times R0 \times 0.02T = 0$$

$$I \times R0 = \frac{50 \times k}{q}\ln(500)$$