EE2021
Devices and Circuits

Multi-Stage Amplifier Analysis, Speed up method

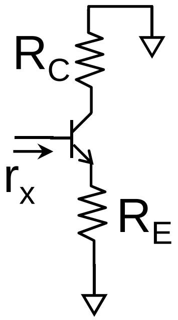
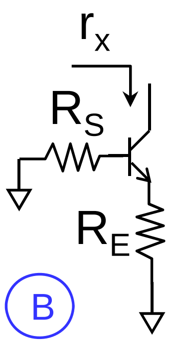
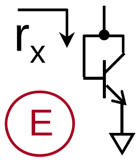
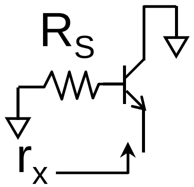
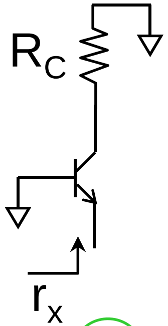
Lecture Outline

- **PMOS Multi-Stage Amplifier,**
- **BJT Multi-Stage Amplifier,**
- **NMOS Multi-Stage Amplifier,**

Not all transistors are equally important (serve different roles) in multi-stage amplifier

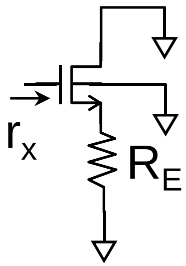
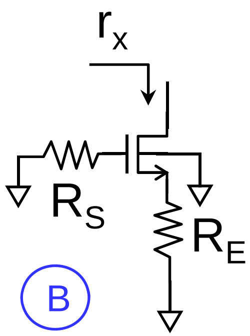
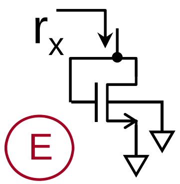
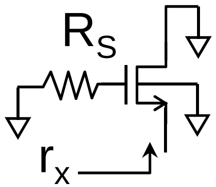
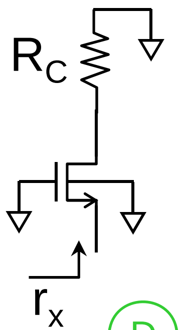
BJT Equivalent Resistance Summary (Table 1)

Blue: look into collector terminal | Red: look into base terminal | Green: look into emitter terminal

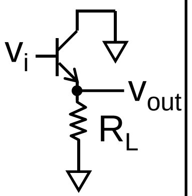
Conf	r_x	Conf	r_x	Conf	r_x
 A	$r_\pi + (1+\beta)R_E$ $\approx r_\pi(1+g_m R_E)$	 B	$r_o\left\{1+g_m[(r_\pi+R_S)//R_E]\left(\frac{r_\pi}{r_\pi+R_S}\right)\right\}$ *If* $R_S=0$ *and* $r_\pi \ll R_E$ $\Rightarrow r_{x,\max}=r_o(\beta+1)$	 E	$\frac{1}{g_m}$
 C	$\frac{R_S+r_\pi}{1+\beta}//r_o$ $\approx \frac{R_S}{1+\beta}+\frac{1}{g_m}$	 D	$\frac{1}{g_m}\times\frac{r_o+R_C}{r_o+R_C/\beta}$		

MOS Equivalent Resistance Summary (Table 2)

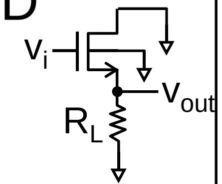
Blue: look into drain terminal   Red: look into gate terminal   Green: look into source terminal

Conf	r_x	Conf	r_x	Conf	r_x
 A	∞	 B	$r_o\left[1+(g_m-g_{mb})R_E\right]$	 E	$\frac{1}{g_m}$
 C	$\frac{1}{g_m-g_{mb}}$	 D	$\frac{1}{g_m-g_{mb}}\times\frac{r_o+R_C}{r_o}$		

BJT Amplifier Configurations (Table 3)

BJT	G_m	A_V
CE A	g_m	Derive Based on 2-port Network
CB B	$-g_m$	Derive Based on 2-port Network
CC C 	Too Complex To Be Useful	$\dfrac{g_m R_L}{1+g_m R_L}$
CE with Emitter Degeneration D	$\dfrac{g_m}{1+g_m R_E}$	Derive Based on 2-port Network

MOS Amplifier Configurations (Table 4)

MOS	G_m	A_V
CS A	g_m	Derive Based on 2-port Network
CG B	$-(g_m - g_{mb})$ $Drop \;\; g_{mb} \;\; if \;\; no \;\; body \;\; effect$	Derive Based on 2-port Network
CD C 	Too Complex To Be Useful	$\dfrac{g_m R_L}{1+(g_m - g_{mb})R_L} \approx \dfrac{g_m}{g_m - g_{mb}}$ $Drop \;\; g_{mb} \;\; if \;\; no \;\; body \;\; effect$
CS with R_E D	$\dfrac{g_m}{1+(g_m - g_{mb})R_E}$ $Drop \;\; g_{mb} \;\; if \;\; no \;\; body \;\; effect$	Derive Based on 2-port Network

Similarity of Circuit AC Analysis to Differentiation

$$\frac{\partial\left(x^2\right)}{\partial x}=\lim_{\Delta x\to 0}\frac{\left(x+\Delta x\right)^2-x^2}{\Delta x}$$
$$=2x$$

$$\frac{\partial\left(e^x\right)}{\partial x}=\lim_{\Delta x\to 0}\frac{e^{x+\Delta x}-e^x}{\Delta x}$$
$$=e^x$$

$$\frac{\partial\left(\sin x\right)}{\partial x}=\lim_{\Delta x\to 0}\frac{\sin\left(x+\Delta x\right)-\sin x}{\Delta x}$$
$$=\cos x$$

$$f\left(x\right)=x^2+e^x+\sin x$$

$$\boxed{f'\left(x\right)=2x+e^x+\cos x}$$

Find out the derivative directly using differentiation table

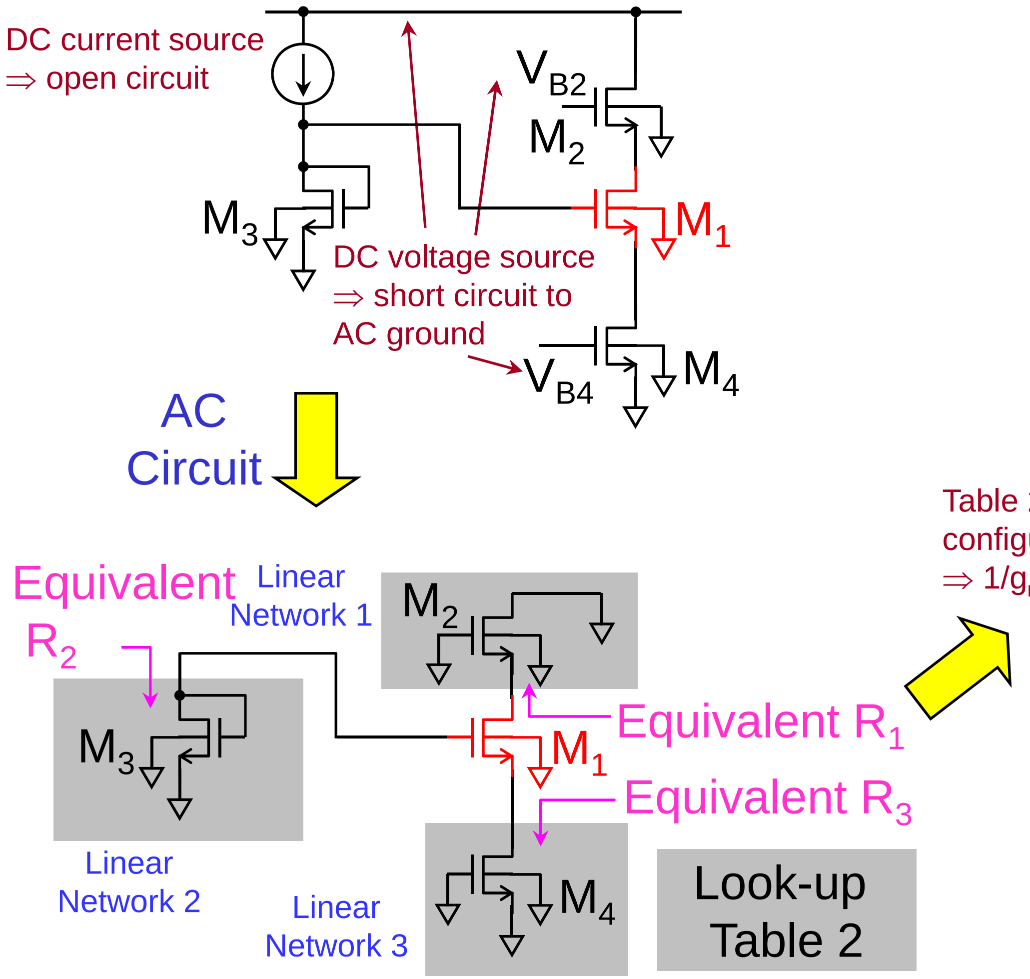
Differentiation Table

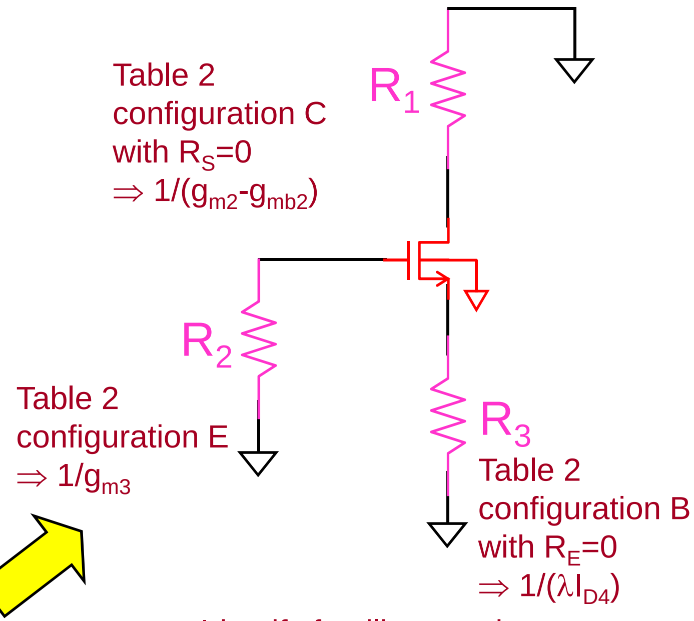
f(x)	f'(x)
x^n	$n \cdot x^{n-1}$
sin(x)	cos(x)
e^x	e^x

Differentiation

- Find derivative for important functions
- Group all these derivatives into a so-called differentiation table
- To derive derivative for more complex function, use the table to write down the individual derivatives directly

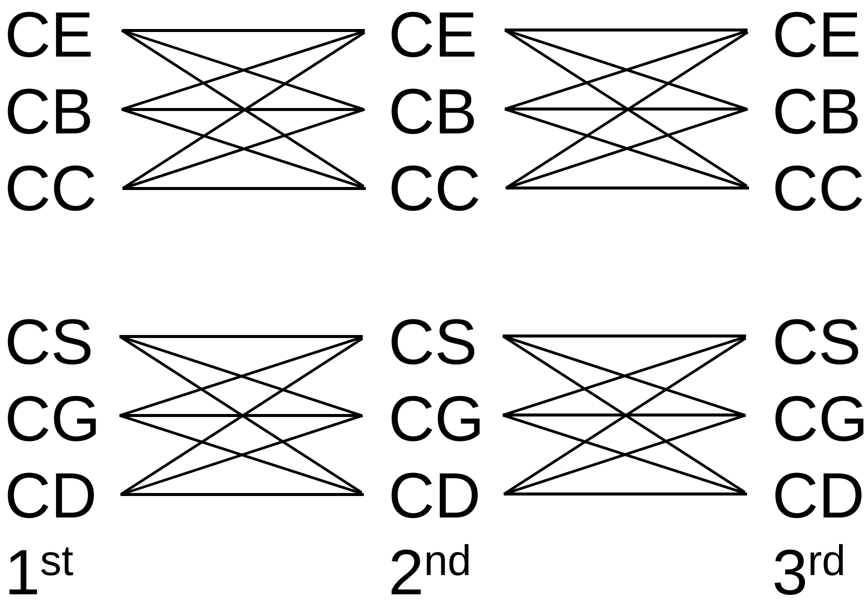
AC Analysis of Complicated Circuit





Identify familiar transistor configurations and apply formula directly for the equivalent resistance

Multi-Stage Amplifier



Why multi-stage?

- To modify R_{in}, R_{out} or the overall gain

Steps for Multi-stage Amplifier Analysis

DC Analysis

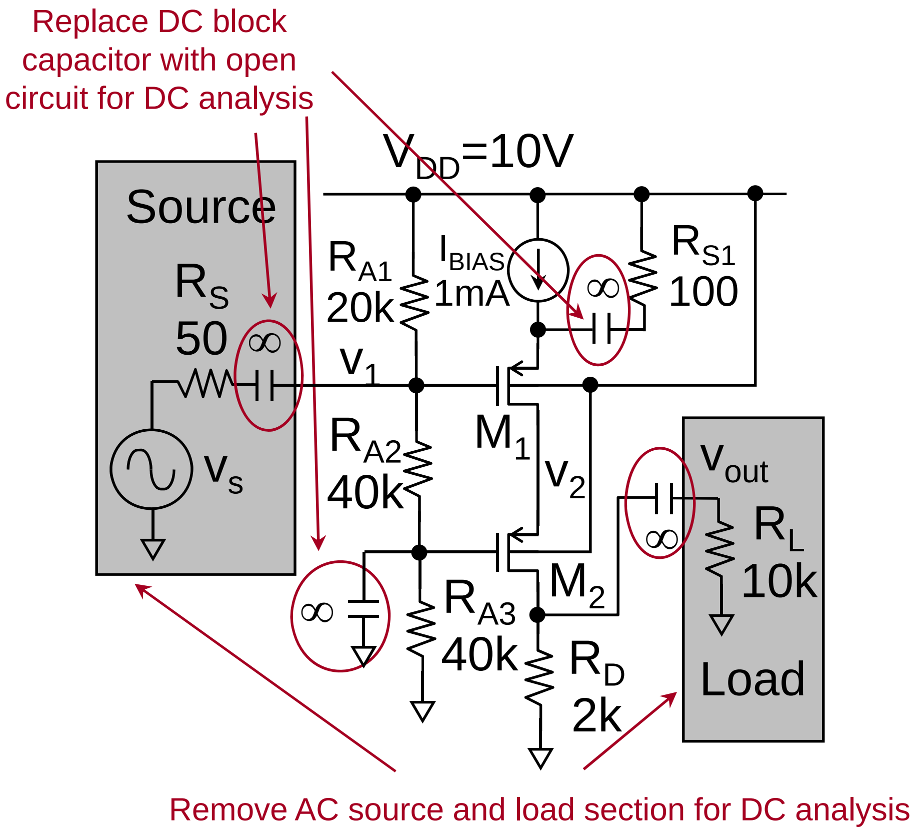
1. Remove AC source and load section
2. Replace capacitor with open circuit
3. Obtain DC biasing
4. Obtain AC small signal parameters, such as g_m, r_π, r_o

AC Analysis

1. DC voltage source $\Rightarrow$ short circuit to AC ground
   DC current source $\Rightarrow$ open circuit
2. Replace DC block capacitor with short circuit
3. Identify source, load and different single stage amplifiers within the multi-stage amplifier
4. Finding the two-port parameter equivalent associated with each single stage amplifier, such as R_{in}, R_{out}, G_m
5. Replace each single stage amplifier with the corresponding two-port network and find the A_V

Different from single stage

PMOS Example (DC Analysis)

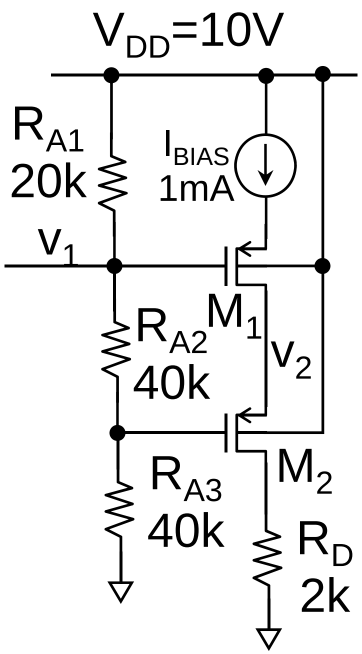


K_p=2mA/V^2
V_{THP}=-1V
λ_p=0.01V^{-1}

$V_{G,M1}$=Gate voltage of M_1
$V_{S,M1}$=Source voltage of M_1
$V_{G,M2}$=Gate voltage of M_2
$V_{S,M2}$=Source voltage of M_2

- Identify Source and Load

PMOS Example (DC Analysis)



Determine DC biasing

$$I_{D,M2} = I_{D,M1} = I_{S,M1} = I_{BIAS} = 1mA$$

Determine AC small signal parameter

$$g_{m,M1} = g_{m,M2} = \sqrt{4K_p I_{D,M1}}$$
$$= 2.8mA/V$$

$$\boxed{g_{mb} \approx -\frac{g_m}{4} = -0.71mA/V}$$

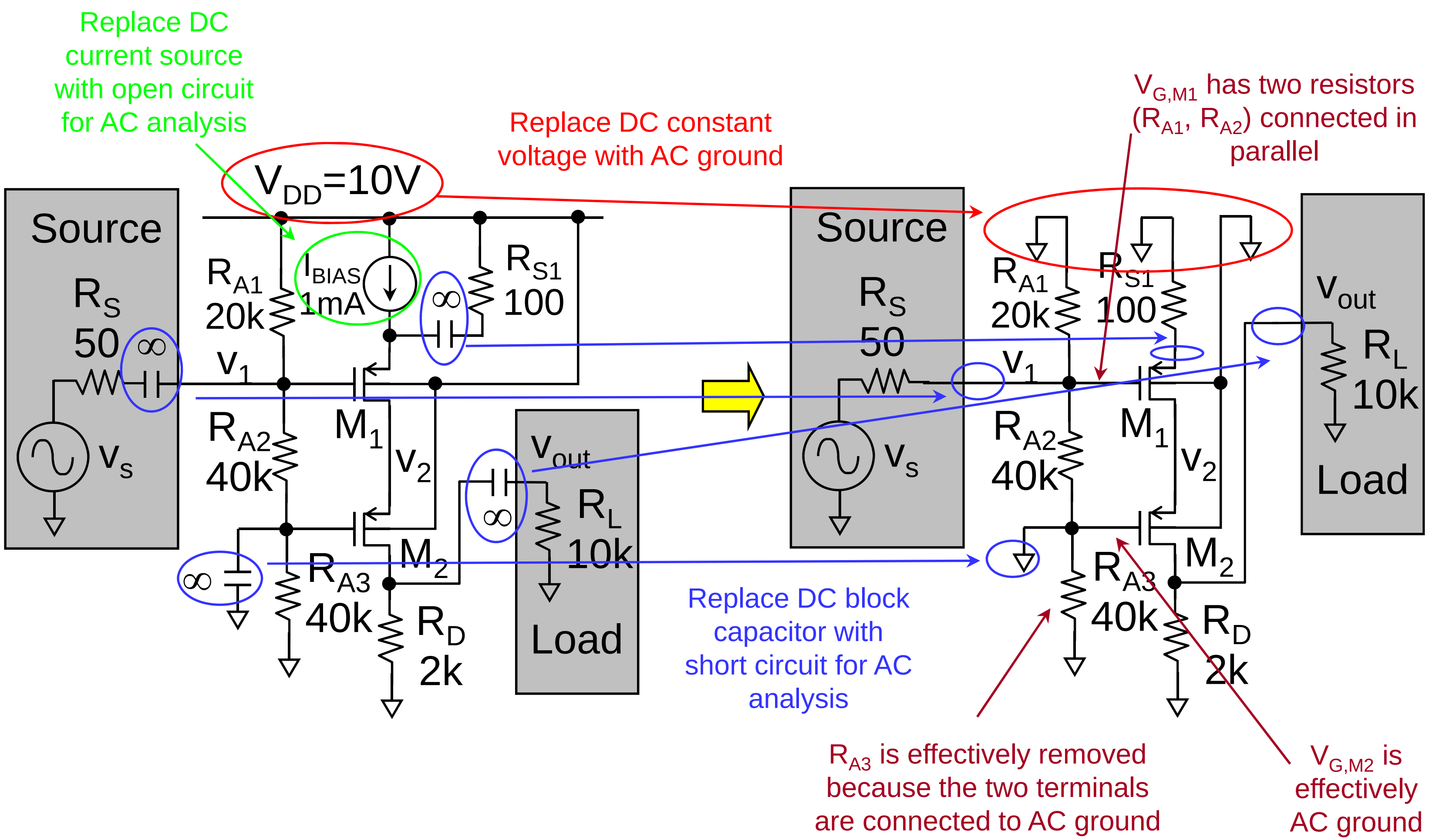
Good approximation, no need to go through detailed calculations

$$r_i = \infty$$

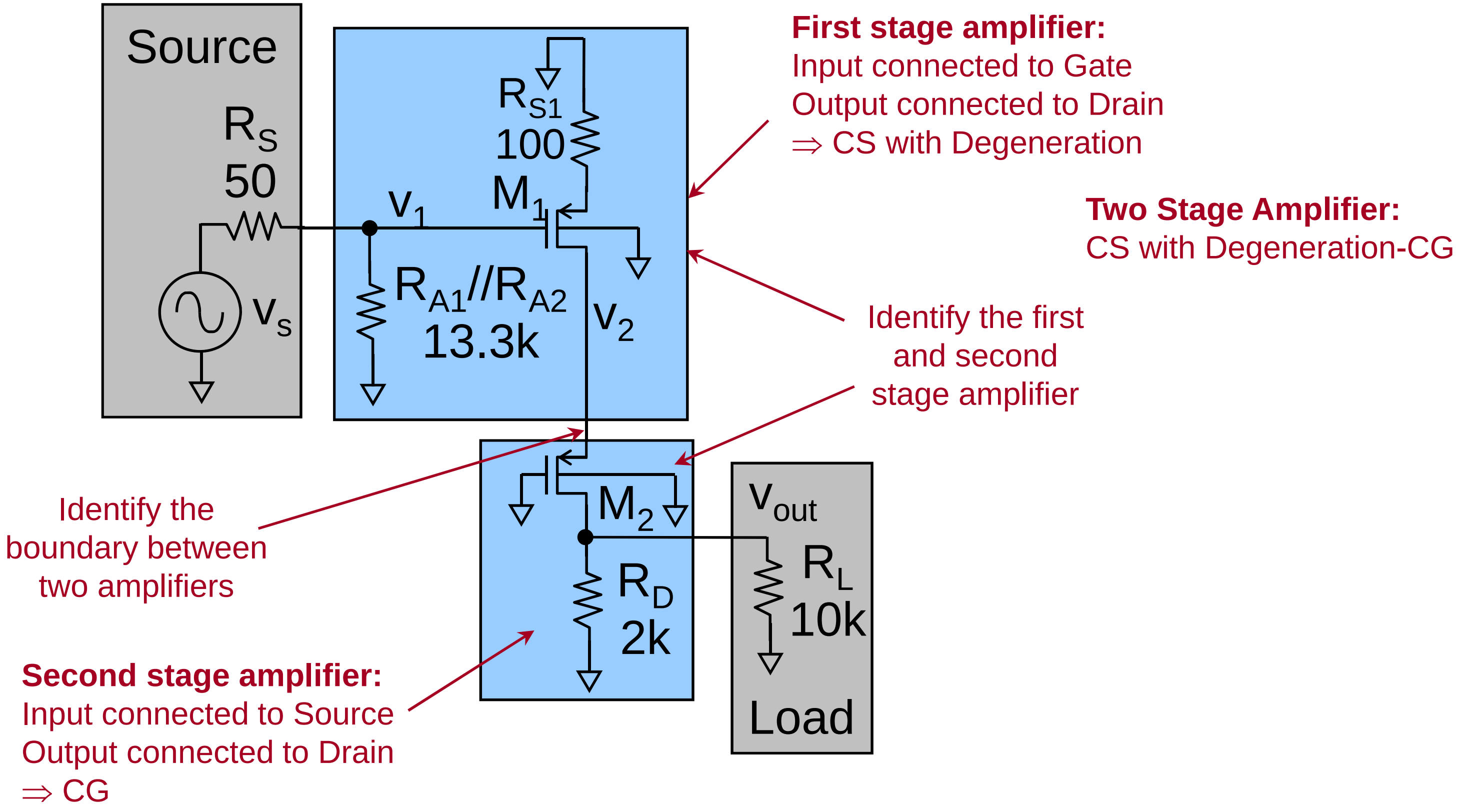
$$r_o = \frac{1}{\lambda_p I_D} = 100k\Omega$$

K_p=2mA/V^2
V_{THP}=-1V
λ_p=0.01V^{-1}

PMOS Example (AC Analysis)



PMOS Example (Identify Single Stage)



- Each single stage amplifier can be replaced with its two-port network equivalent consisting of R_{in}, R_{out} and G_m

PMOS Example (Identify 2-Port Parameters)

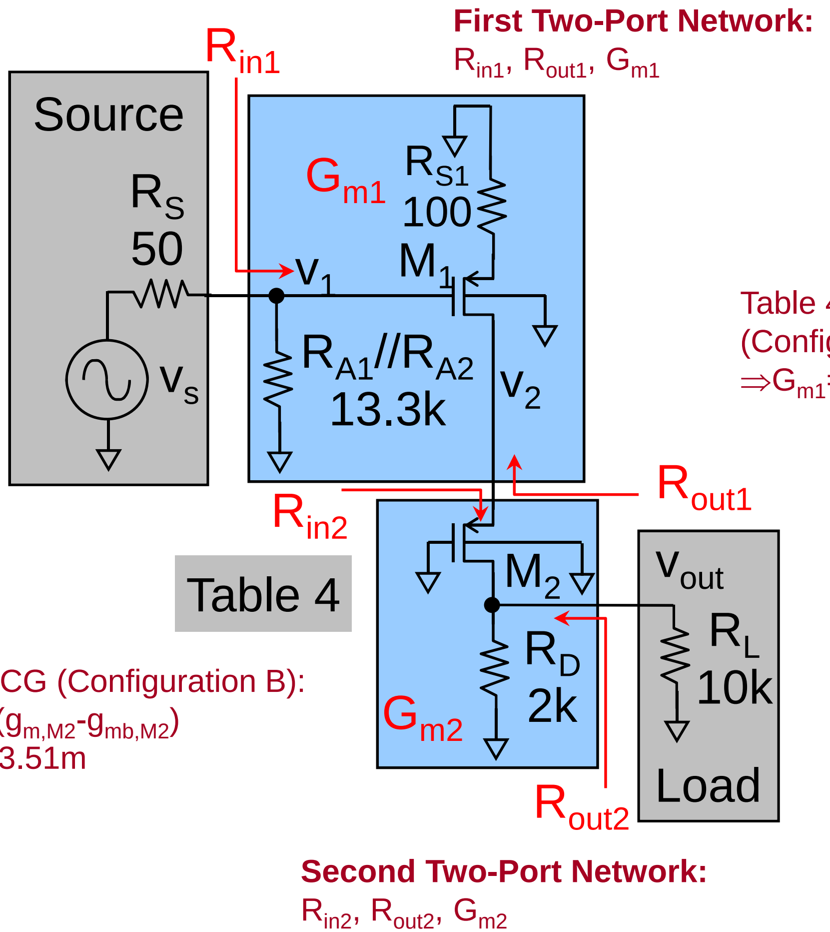


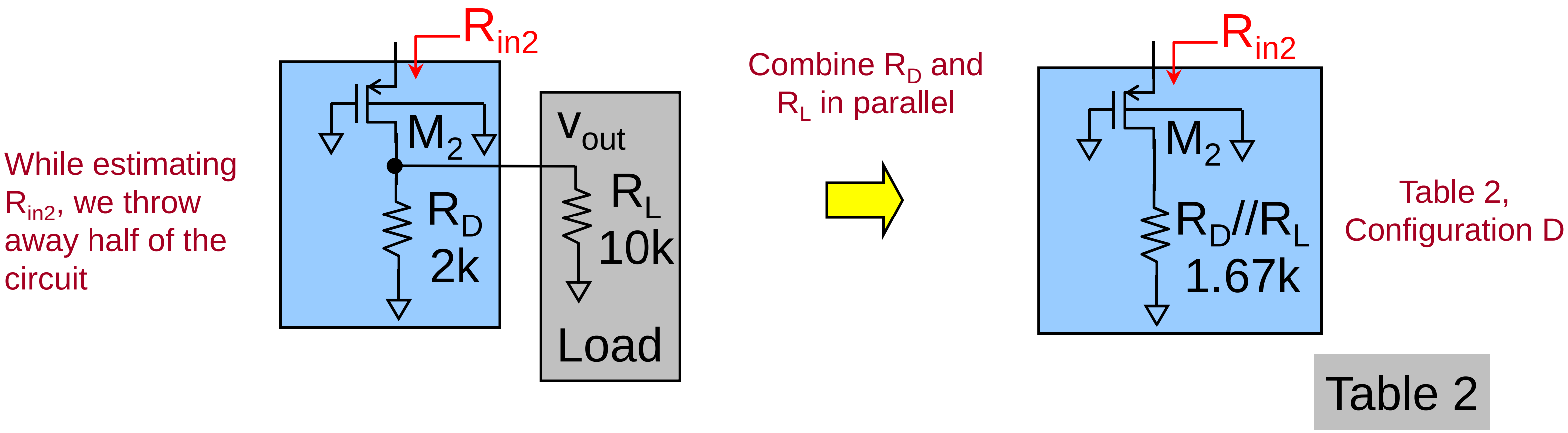
Table 4, CS with Degeneration (Configuration D):
$\Rightarrow G_{m1}=g_{m,M1}/[1+(g_{m,M1}-g_{mb,M1})R_{S1}]$
$=2.08m$

Table 4, CG (Configuration B):
$\Rightarrow G_{m2}=-(g_{m,M2}-g_{mb,M2})$
$=-3.51m$

R_{in1}, R_{in2}, R_{out1}, R_{out2}: Which one to be solved first?

- Identify the 2-port network and the corresponding R_{in}, R_{out} and G_m

PMOS Example (Finding R_{in2})



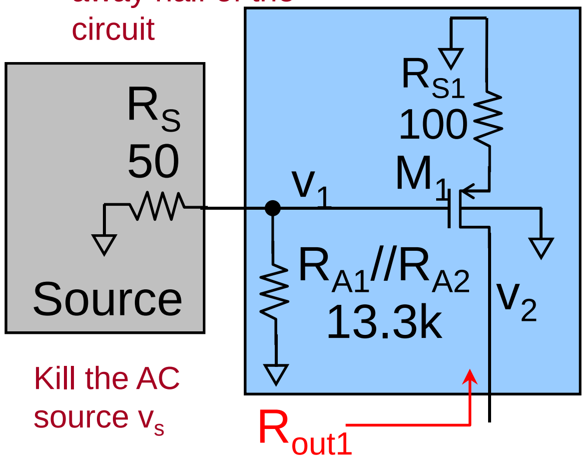
$$\textit{Configurat ion} \quad D$$

$$\Rightarrow R_{in2} = \frac{1}{g_{m,M2} - g_{mb,M2}} \frac{r_{o,M2} + (R_L // R_D)}{r_{o,M2}} \approx \frac{1}{g_{m,M2} - g_{mb,M2}} = 285$$

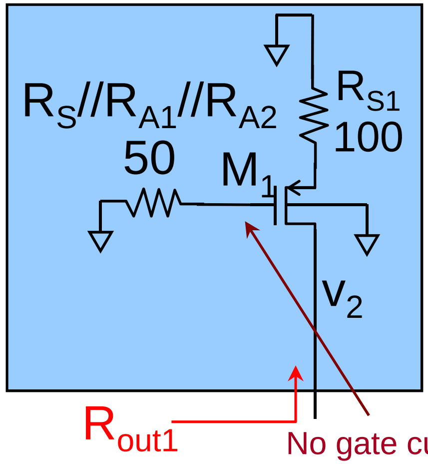
PMOS Example (Finding R_{out1})

Combine R_S and $R_{A1}//R_{A2}$ in parallel

While estimating R_{out1}, we throw away half of the circuit



Kill the AC source v_s



No gate current $\Rightarrow v_g$ is AC ground

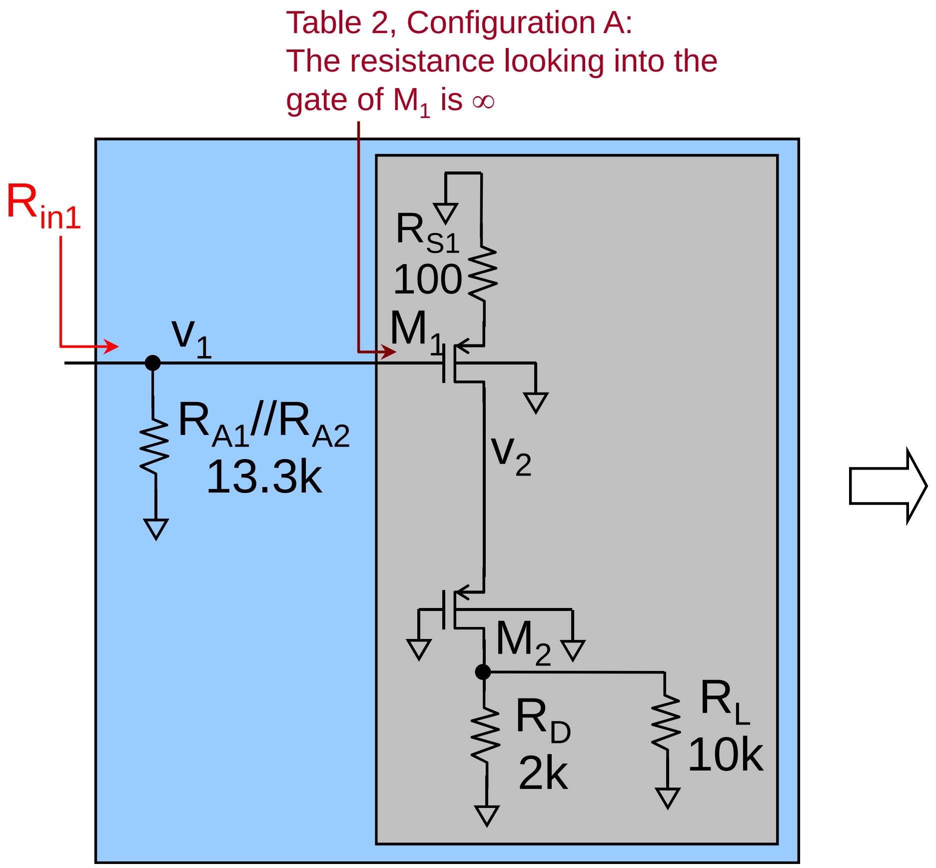
Table 2, Configuration B

Table 2

Configurat ion B

$$\Rightarrow R_{out1} = r_{o,M1}\left[1 + \left(g_{m,M1} - g_{mb,M1}\right)R_{S1}\right] = 135k$$

PMOS Example (Finding R_{in1})



$$R_{in1} = R_{A1} // R_{A2}$$
$$= 13.3k$$

PMOS Example (Finding R_{out2})

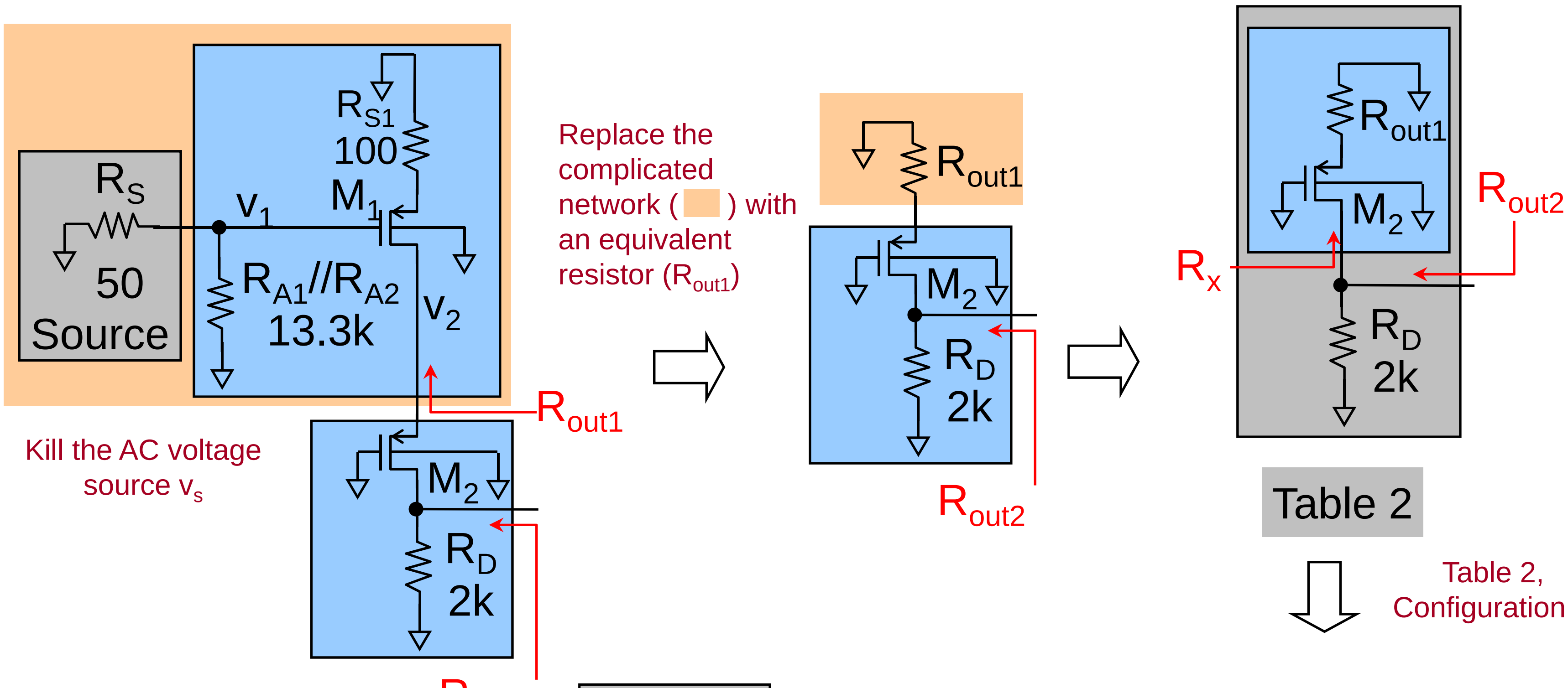
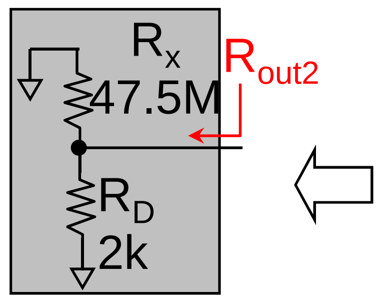


Table 2, Configuration B

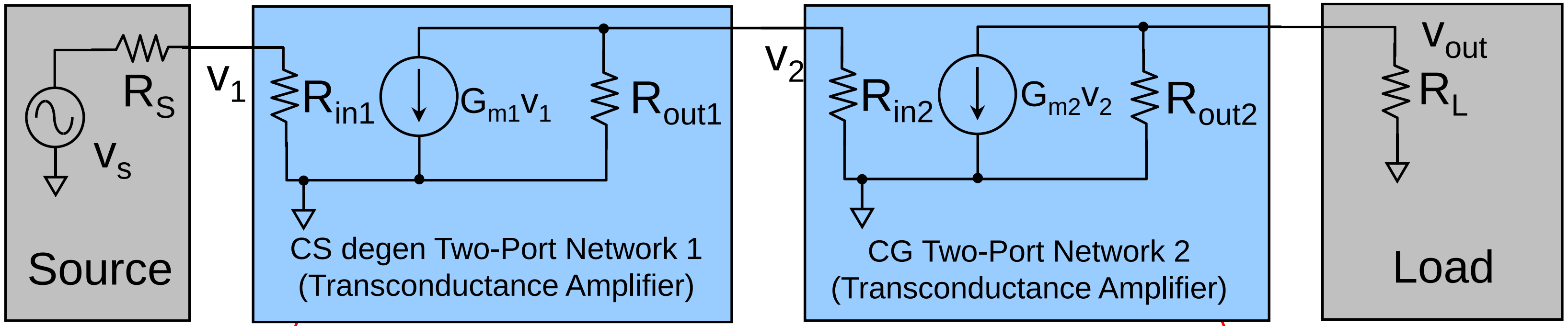


Configurat ion B

$$\Rightarrow R_x = r_{o,M2}\left[1+\left(g_{m,M2}-g_{mb,M2}\right)R_{out1}\right]$$
$$\approx 47.5M$$

$$R_{out2} = R_D \,//\, R_x \approx 2k$$

PMOS Example (2-Port)

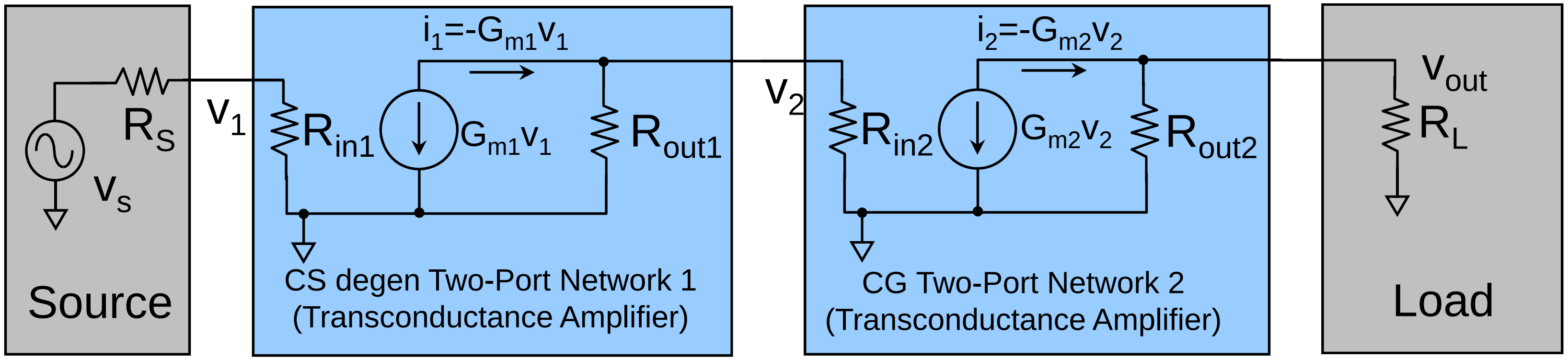


Replace each single stage amplifier with their two-port network equivalent

$$R_{in1} = R_{A1} // R_{A2}$$
$$= 13.3k$$
$$R_{out1} = r_{o,M1}\left[1 + \left(g_{m,M1} - g_{mb,M1}\right)R_{S1}\right]$$
$$= 135k$$
$$G_{m1} = \frac{g_{m,M1}}{1 + \left(g_{m,M1} - g_{mb,M1}\right)R_{S1}}$$
$$= 2.08m$$

$$R_{in2} = \frac{1}{g_{m,M2} - g_{mb,M2}} \frac{r_{o,M2} + R_D // R_L}{r_{o,M2}}$$
$$\approx 285$$
$$R_{out2} = R_D // \left\{r_{o,M2}\left[1 + \left(g_{m,M2} - g_{mb,M2}\right)R_{out1}\right]\right\}$$
$$\approx 2k$$
$$G_{m2} = -\left(g_{m,M2} - g_{mb,M2}\right)$$
$$= -3.51m$$

PMOS Example (2-Port)



$$v_1 = v_s \times \frac{R_{in1}}{R_{in1} + R_S}$$

$$\approx v_s$$

$$v_2 = i_1 \times \left(R_{out1} // R_{in2}\right)$$

$$= -G_{m1} v_1 \left(R_{out1} // R_{in2}\right)$$

$$\approx -0.59 v_1 \approx -0.59 v_s$$

$$v_{out} = i_2 \times \left(R_{out2} // R_L\right)$$

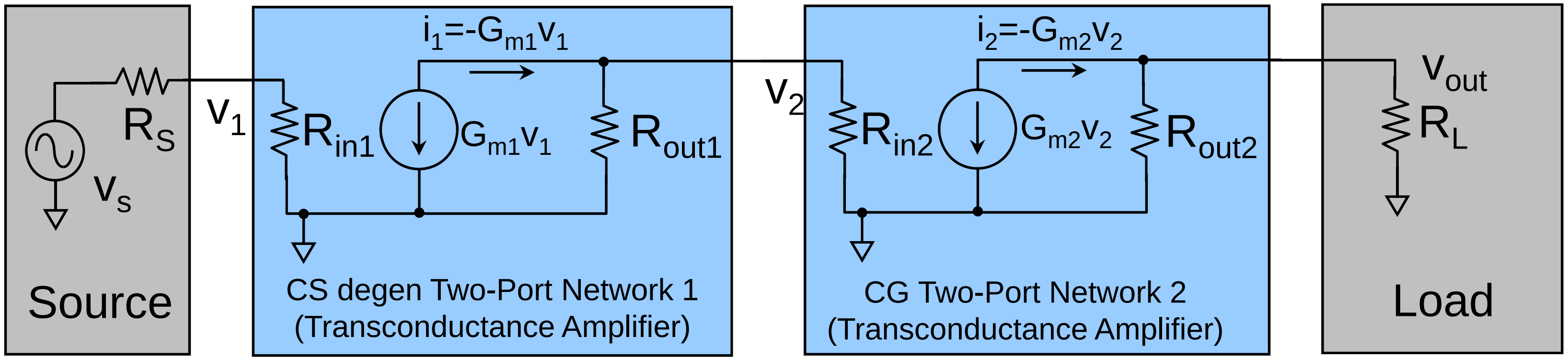
$$= -G_{m2} v_2 \left(R_{out2} // R_L\right)$$

$$\approx 5.86 v_2$$

$$= -3.46 v_s$$

$$A_V = \frac{v_{out}}{v_s} = -3.46$$

PMOS Example (2-Port)



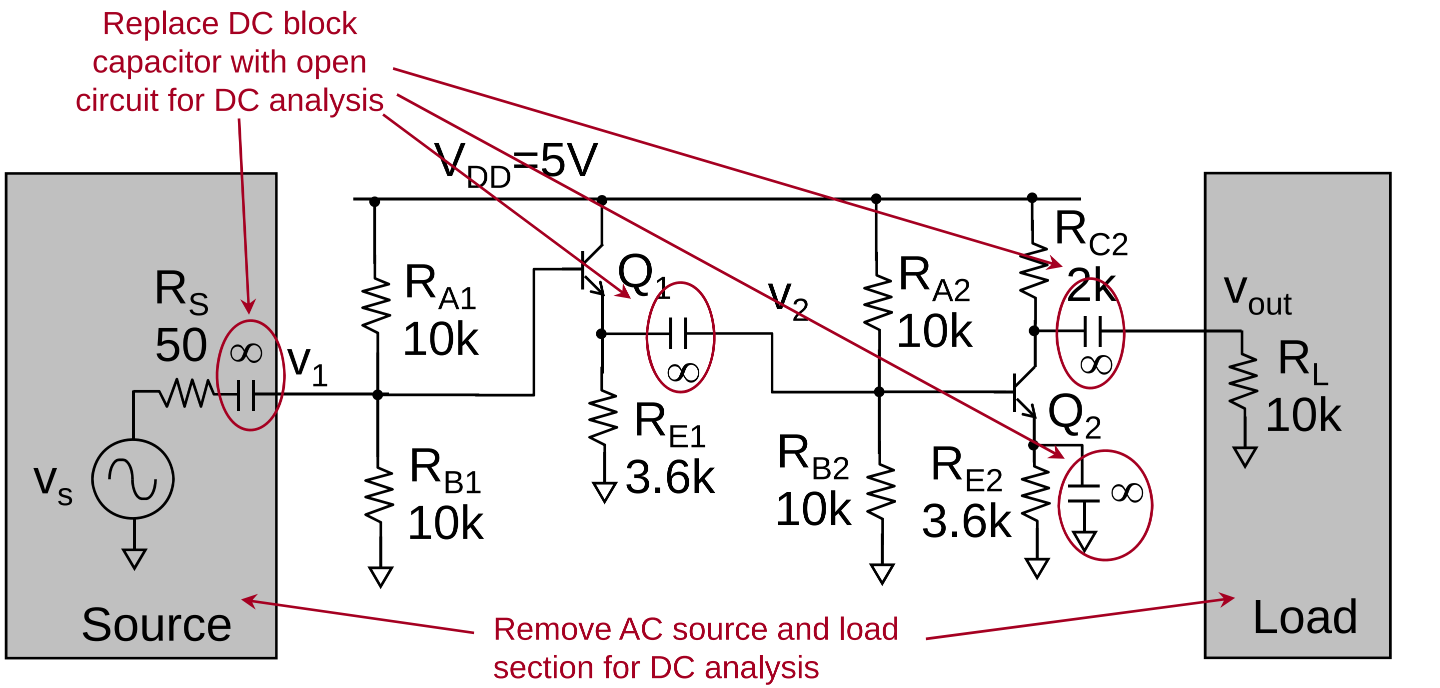
$$A_V = \frac{v_{out}}{v_s} = \frac{v_1}{v_s} \times \frac{v_2}{v_1} \times \frac{v_{out}}{v_2}$$

$$= \underbrace{\frac{(R_{A1} // R_{A2})}{R_S + (R_{A1} // R_{A2})}}_{Resistor\ \ Divider} \times \underbrace{\left[-G_{m1}(R_{out1} // R_{in2})\right]}_{1st\ \ Stage\ \ CS\ with\ \ Degeneration} \underbrace{\left[-G_{m2}(R_{out2} // R_L)\right]}_{2nd\ \ Stage\ \ CG}$$

$$= \underbrace{\frac{(R_{A1} // R_{A2})}{R_S + (R_{A1} // R_{A2})}}_{Resistor\ \ Divider} \times \underbrace{\frac{-g_{m,M1}}{1 + (g_{m,M1} - g_{mb,M1})R_{S1}} \frac{1}{g_{m,M2} - g_{mb,M2}}}_{1st\ \ Stage\ \ CS\ with\ \ Degeneration} \underbrace{(g_{m,M2} - g_{mb,M2})(R_D // R_L)}_{2nd\ \ Stage\ \ CG}$$

$$= -3.46$$

BJT Example (DC Analysis)

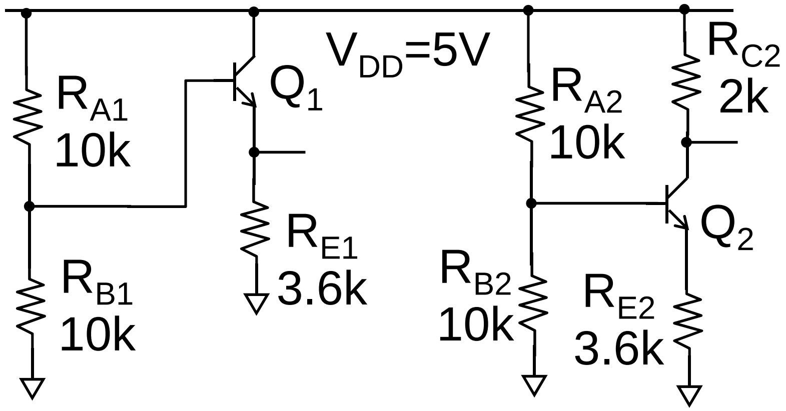


$V_{B,Q1}$=Base voltage of Q_1
$V_{E,Q1}$=Emitter voltage of Q_1
$V_{B,Q2}$=Base voltage of Q_2
$V_{C,Q2}$=Collector voltage of Q_2

$I_S=10^{-15}A$
$\beta=100$
$V_A=100V$

- Identify Source and Load

BJT Example (DC Analysis)



$I_S=10^{-15}$A
β=100
V_A=100V

The goal of DC analysis is to find the collector current flowing through Q_1 and Q_2 (I_{C1}, I_{C2}). To find the collector current, we can assume $V_{BE,Q1}$ and $V_{BE,Q2}$ equal to 0.7V, and obtain the current through KCL and KVL.

Never do the following:

$$\cancel{\because V_{BE,Q1} = V_{BE,Q2} \approx 0.7}$$

$$\cancel{\Rightarrow I_{C1} \approx I_{C2} \approx I_S e^{\frac{V_{BE,Q1}}{V_T}}}$$

Determine DC Biasing

$$\boxed{V_{B,Q1} = \frac{R_{B1}}{R_{A1}+R_{B1}} \times V_{DD} = 2.5V}$$

Simple resistor divider

$$\boxed{V_{E,Q1} = V_{B,Q1} - 0.7 = 1.8V}$$

Using the approximation $V_{BE,Q1}$=0.7V

$$\Rightarrow I_{C,Q1} \approx I_{E,Q1} = \frac{V_{E,Q1}}{R_{E1}} = 500\,\mu A$$

$$\Rightarrow I_{B,Q1} = \frac{I_{C,Q1}}{\beta} = 5\,\mu A$$

$$\boxed{V_{B,Q2} = \frac{R_{B2}}{R_{A2}+R_{B2}} \times V_{DD} = 2.5V}$$

Simple resistor divider

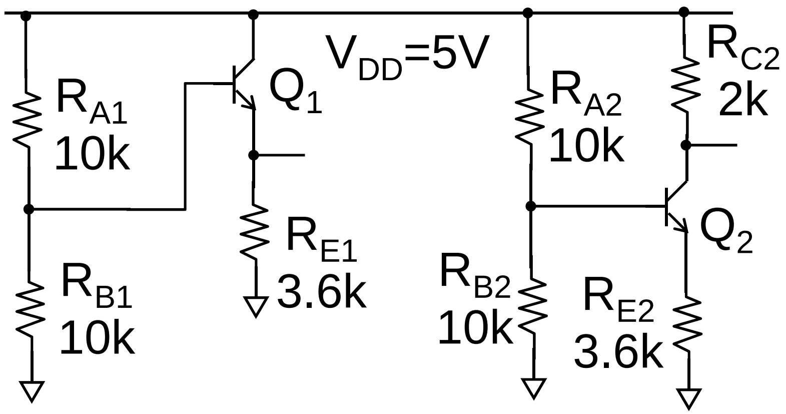
$$\boxed{V_{E,Q2} = V_{B,Q2} - 0.7 = 1.8V}$$

Using the approximation $V_{BE,Q2}$=0.7V

$$\Rightarrow I_{C,Q2} \approx I_{E,Q2} = \frac{V_{E,Q2}}{R_{E2}} = 500\,\mu A$$

$$\Rightarrow I_{B,Q2} = \frac{I_{C,Q2}}{\beta} = 5\,\mu A$$

BJT Example (Small Signal AC Equivalent)



Determine AC small signal parameter

$$\because I_{C,Q1} = I_{C,Q2} = 500\mu \quad and \quad V_T = 25mV$$

$$\Rightarrow g_{m,Q1} = g_{m,Q2} = \frac{I_{C,Q1}}{V_T} = 20mA/V$$

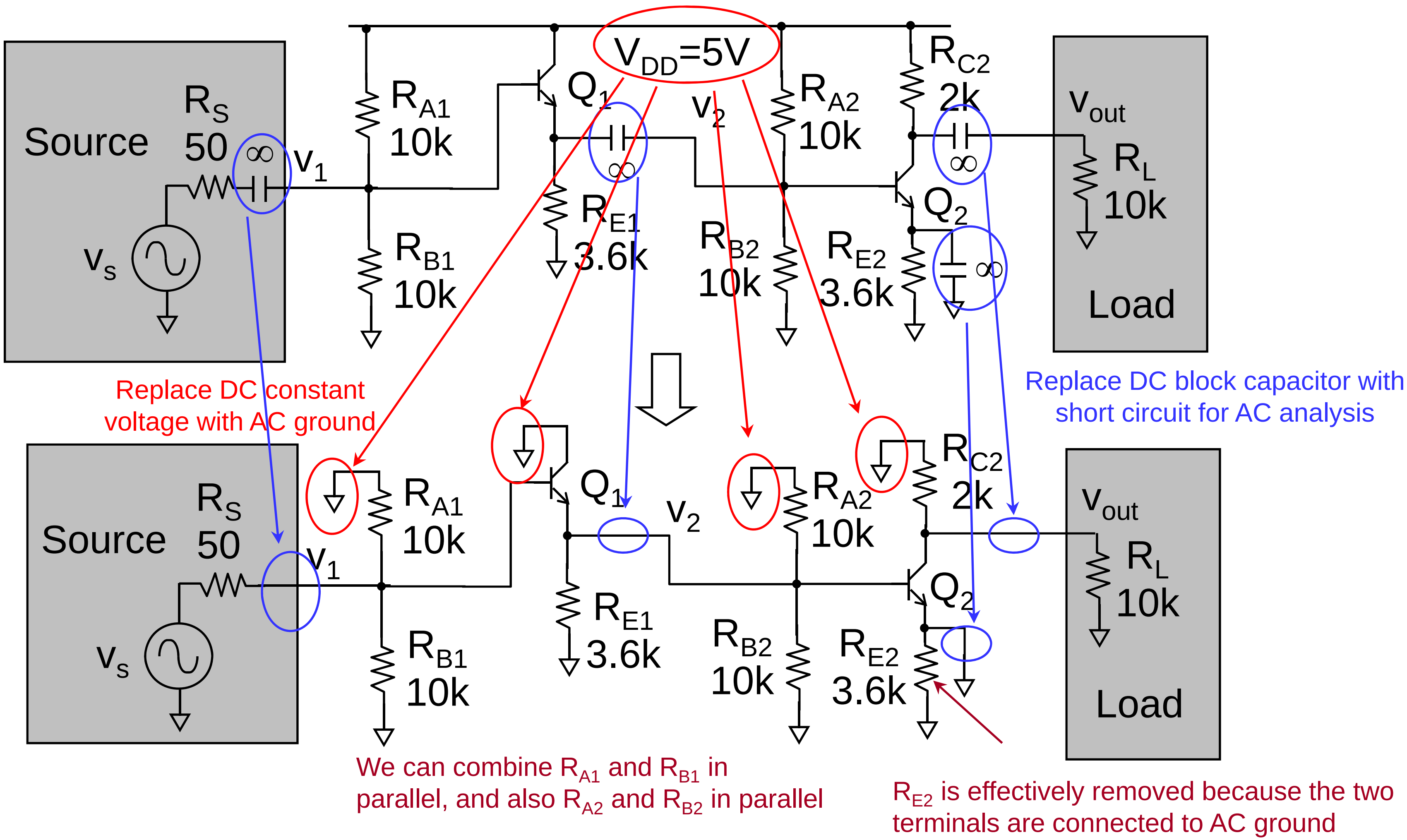
$$\Rightarrow r_{\pi,Q1} = r_{\pi,Q2} = \frac{\beta}{g_{m,Q1}} = 5k$$

$$r_{o,Q1} = r_{o,Q2} = \frac{V_A}{I_{C,Q1}} \approx 200k$$

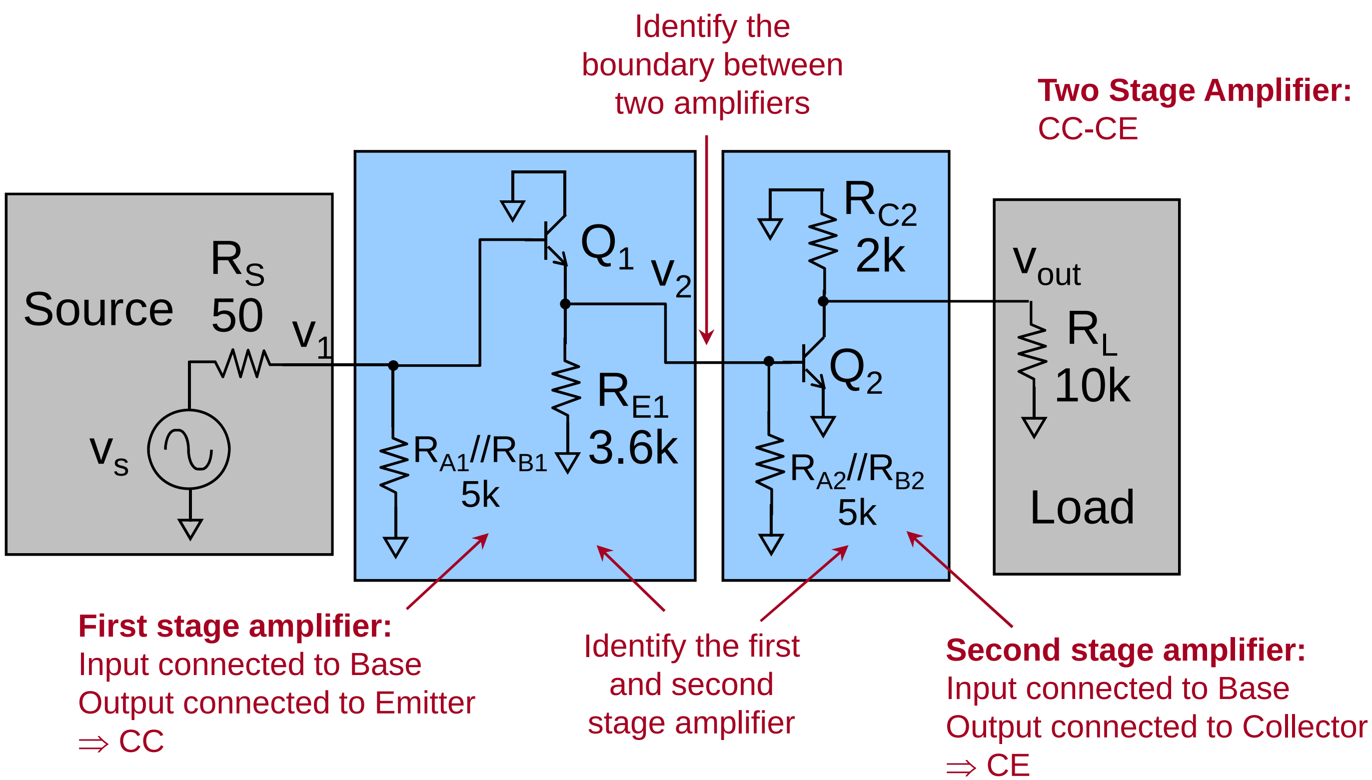
Notice that all AC small signal parameters depend on collector current

Find g_m, r_π and r_o

BJT Example (AC Analysis)



BJT Example (Identify Single Stage)



- Each single stage amplifier can be replaced with its two-port network equivalent consists of R_{in}, R_{out} and G_m

BJT Example (Identify 2-Port Parameters)

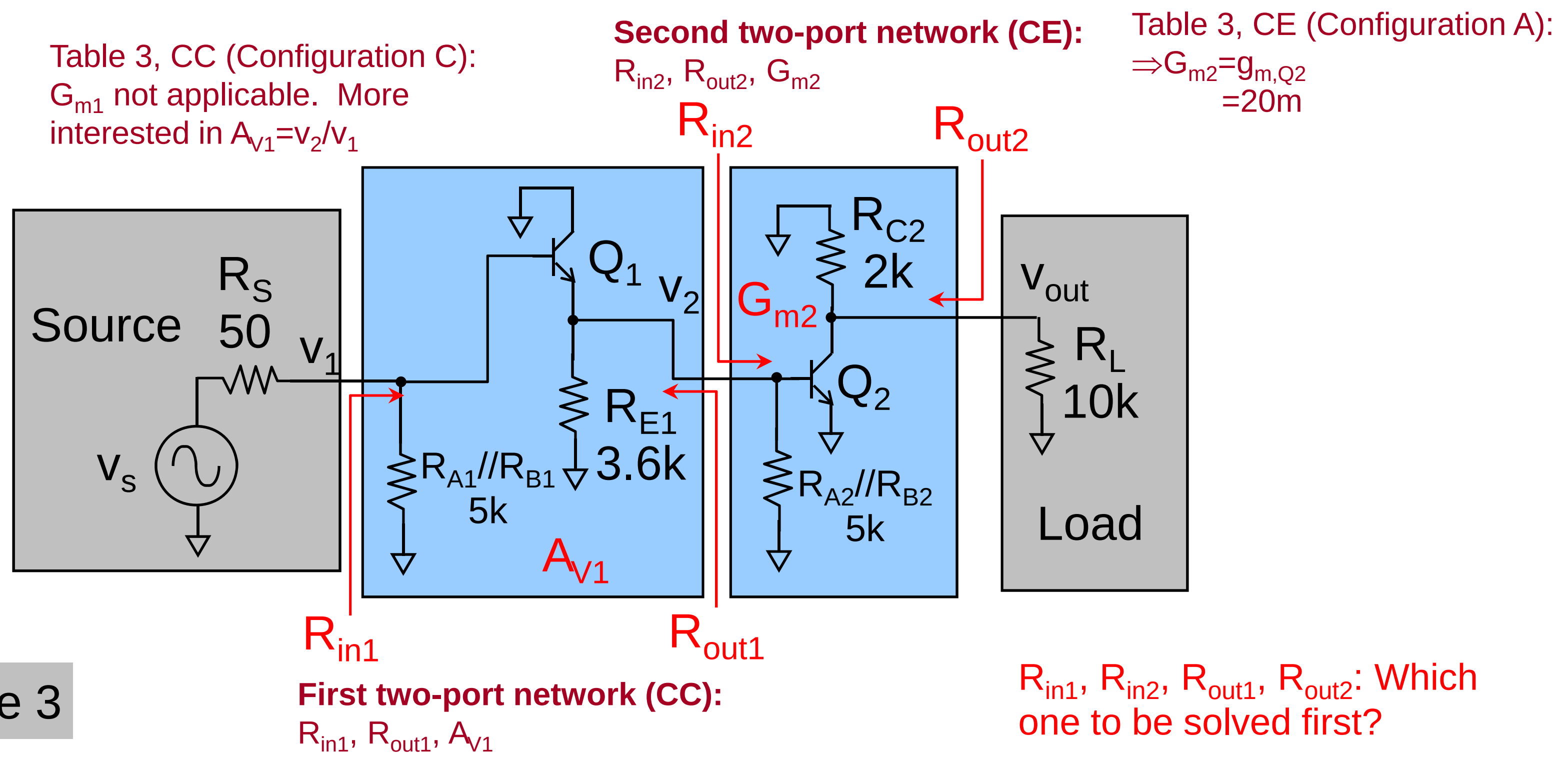
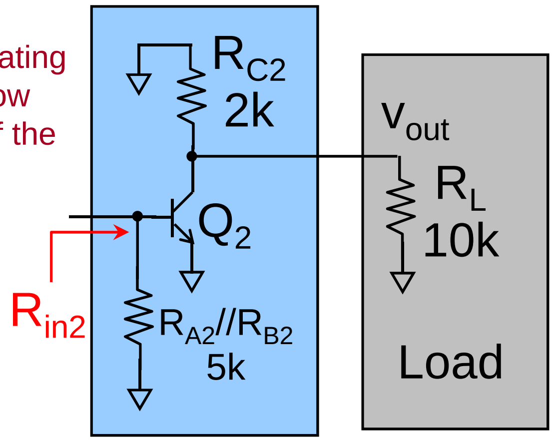


Table 3

- Identify the 2-port network and the corresponding R_{in}, R_{out}, G_m, and A_V

BJT Example (Finding R_{in2})

While estimating R_{in2}, we throw away half of the circuit



Combine R_{C2} and R_L in parallel

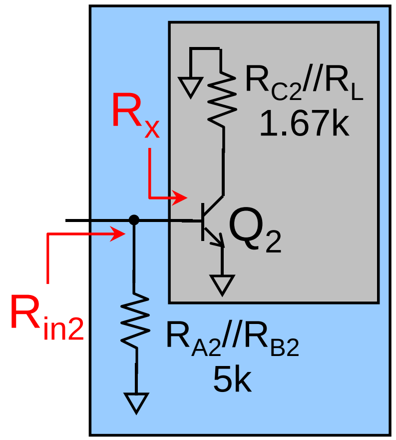
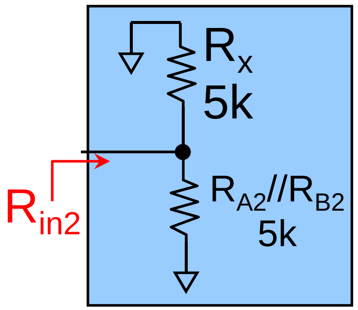


Table 1

Table 1, Configuration A with R_E=0

$$Configuration \text{ (A)}$$

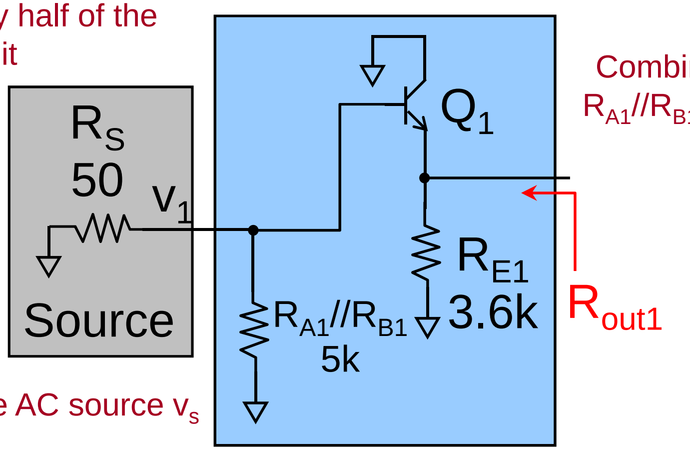
$$\Rightarrow R_x = r_{\pi,Q2} = 5k$$



$$\Rightarrow R_{in2} = R_{A2} // R_{B2} // R_x$$
$$= R_{A2} // R_{B2} // r_{\pi,Q2}$$
$$= 2.5k$$

BJT Example (Finding R_{out1})

While estimating R_{out1}, we throw away half of the circuit



Kill the AC source v_s

Combine R_S and $R_{A1}//R_{B1}$ in parallel

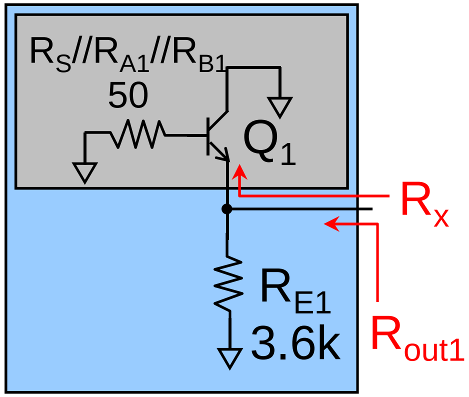


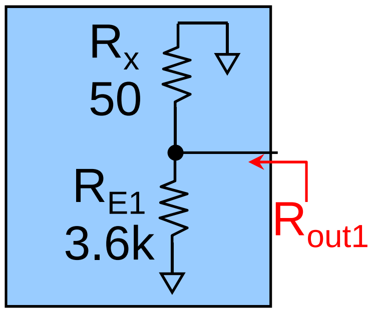
Table 1

Table 1, Configuration C

Configuration C

$$\Rightarrow R_x = \frac{R_S // R_{A1} // R_{B1}}{\beta + 1} + \frac{1}{g_{m,Q1}}$$

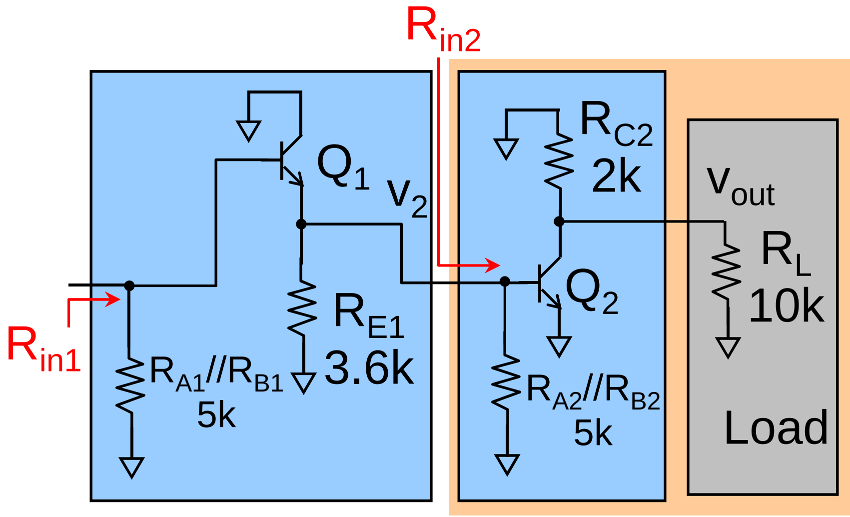
$$\approx 50$$



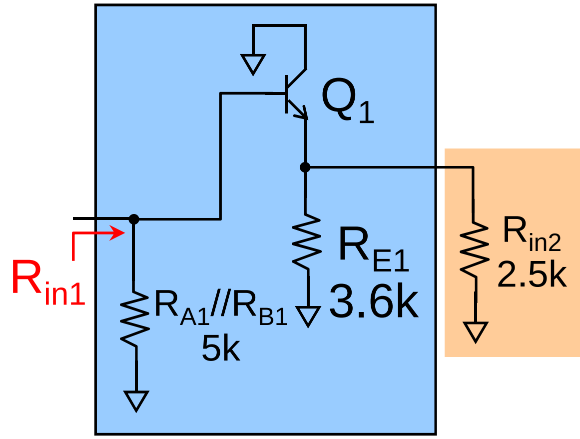
$$\Rightarrow R_{out1} = R_x // R_{E1}$$

$$\approx 50$$

BJT Example (Finding R_{in1})



Replace the complicated network ( ) with an equivalent resistor (R_{in2})



Any complicated network can be replaced with an equivalent resistor

Combine R_{in2} and R_{E1} in parallel

Table 1, Configuration A

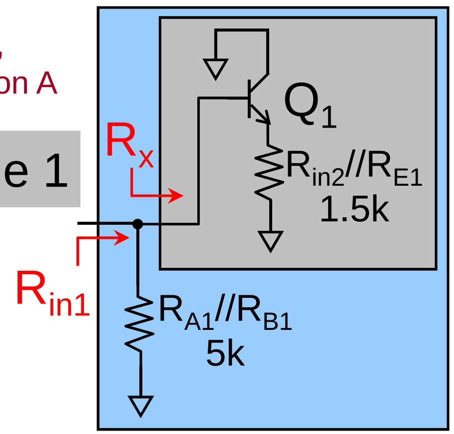
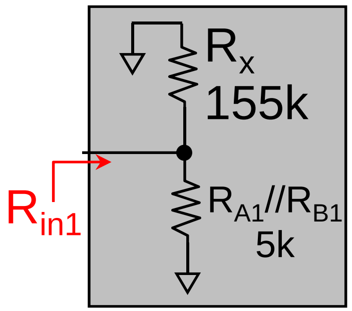


Table 1

Configurat ion A

$$\Rightarrow R_x = r_{\pi,Q1}\left[1 + g_{m,Q1}\left(R_{in2} // R_{E1}\right)\right]$$

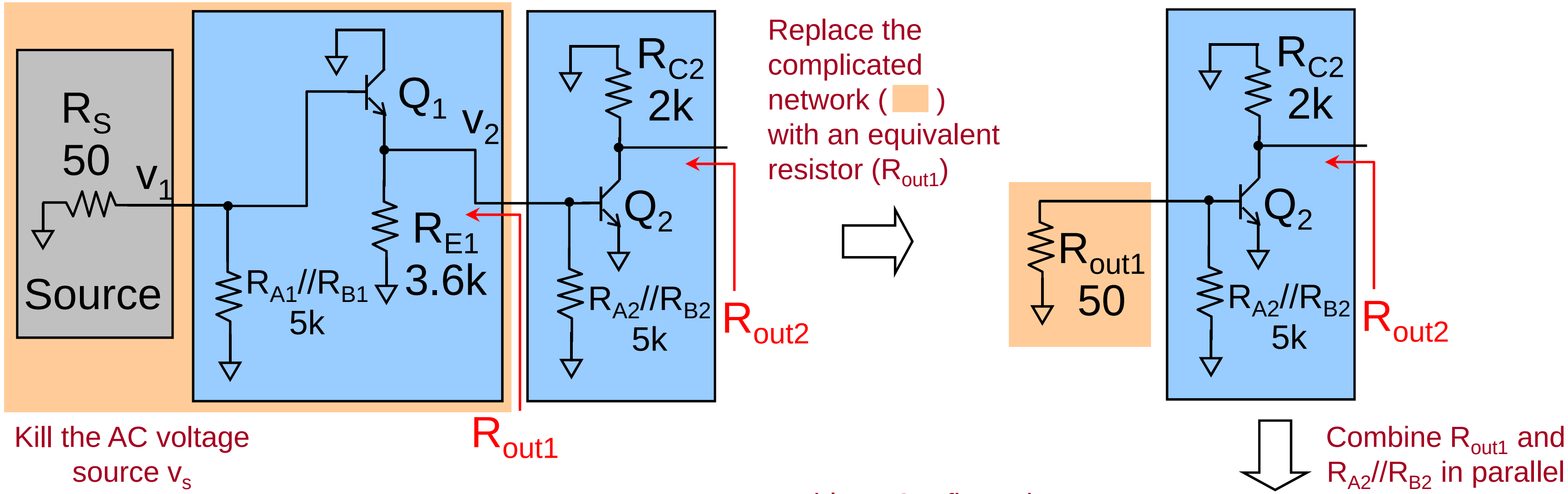
$$\approx 155k$$

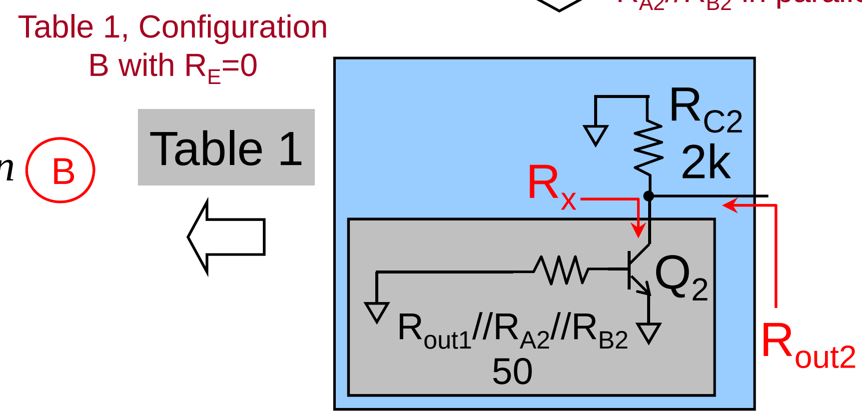


$$\Rightarrow R_{in1} = R_x // R_{A1} // R_{B1}$$

$$= 4.8k$$

BJT Example (Finding R_{out2})

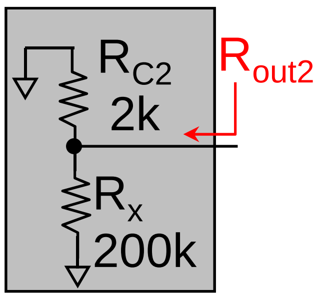




$$\text{Configurat ion (B) with } R_E = 0$$

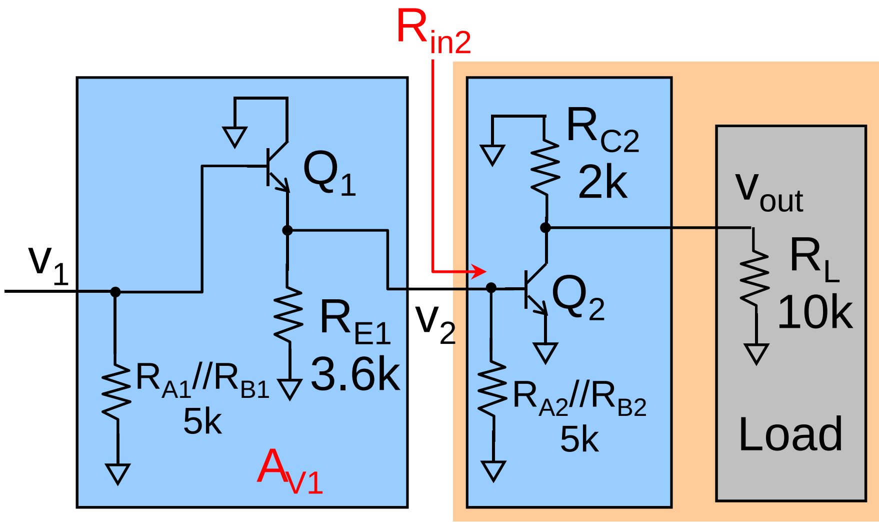
$$\Rightarrow R_x = r_{o,Q2}$$

$$\approx 200k$$

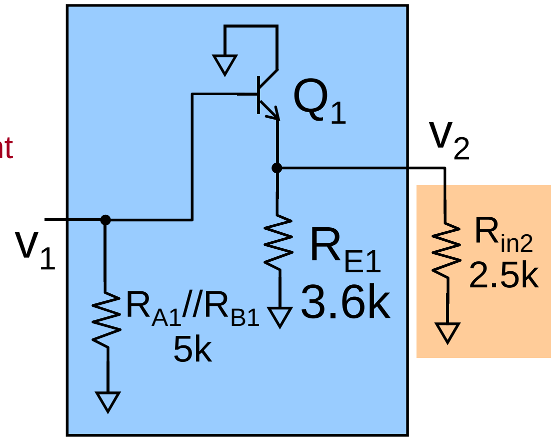


$$R_{out2} = R_{C2} // R_x \approx 2k$$

BJT Example (Finding $A_{V1}=v_2/v_1$)



Replace the complicated network ( ) with an equivalent resistor (R_{in2})



Combine R_{in2} and R_{E1} in parallel

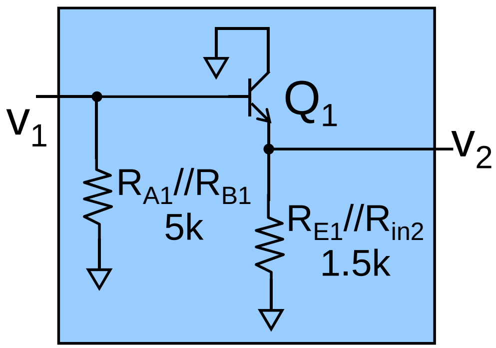


Table 3

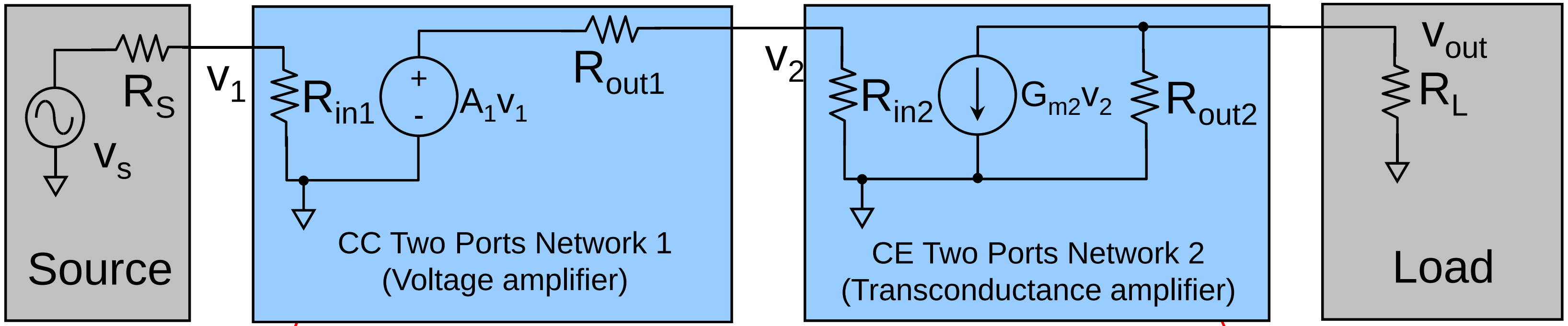
Table 3, Configuration C

Configurat ion C

$$A_{V1}=\frac{v_2}{v_1}=\frac{g_{m,Q1}\left(R_{E1}//R_{in2}\right)}{1+g_{m,Q1}\left(R_{E1}//R_{in2}\right)}$$

$$\approx 1$$

BJT Example (2-Port)



Replace each single stage amplifier with their two-port network equivalent

$$R_{in1} = R_{A1} // R_{B1} // \{r_{\pi,Q1}[1+g_{m,Q1}(R_{E1} // R_{in2})]\}$$
$$= 4.8k$$

$$R_{out1} = R_{E1} // \left[\frac{R_S // R_{A1} // R_{B1}}{\beta+1} + \frac{1}{g_{m,Q1}}\right]$$
$$= 50$$

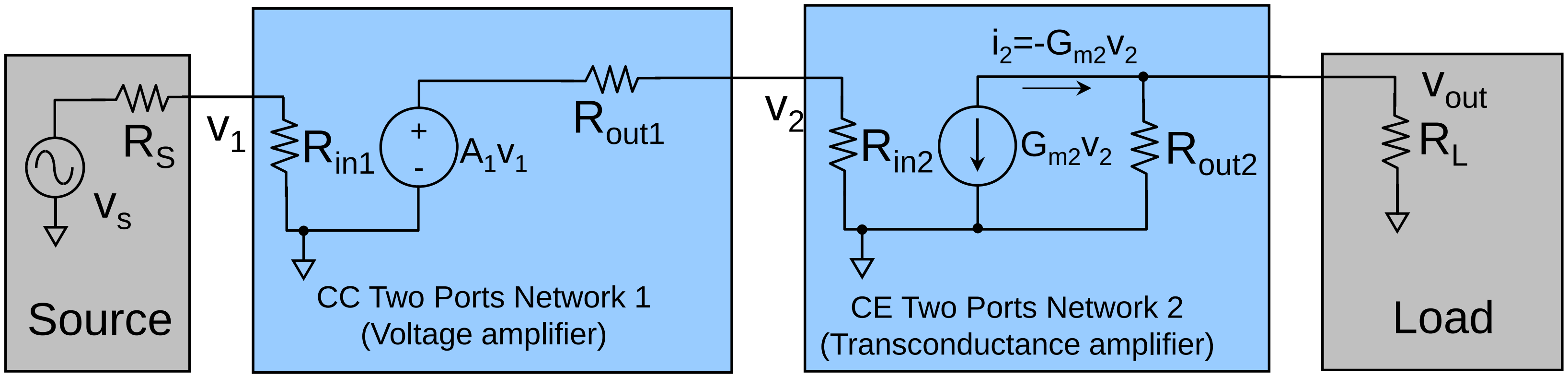
$$A_{V1} = \frac{v_2}{v_1} = \frac{g_{m,Q1}(R_{E1} // R_{in2})}{1+g_{m,Q1}(R_{E1} // R_{in2})}$$
$$\approx 1$$

$$R_{in2} = R_{A2} // R_{B2} // r_{\pi,Q2}$$
$$= 2.5k$$

$$R_{out2} = R_{C2} // r_{o,Q2}$$
$$\approx 2k$$

$$G_{m2} = g_{m,Q2}$$
$$= 20m$$

BJT Example (2-Port)



$$v_1 = v_s \times \frac{R_{in1}}{R_{in1} + R_S}$$

$$\approx v_s$$

$$v_2 = v_1 \times \frac{g_{m,Q1}\left(R_{E1} // R_{in2}\right)}{1 + g_{m,Q1}\left(R_{E1} // R_{in2}\right)}$$

$$\approx v_1$$

$$v_{out} = i_2 \times \left(R_{out2} // R_L\right)$$

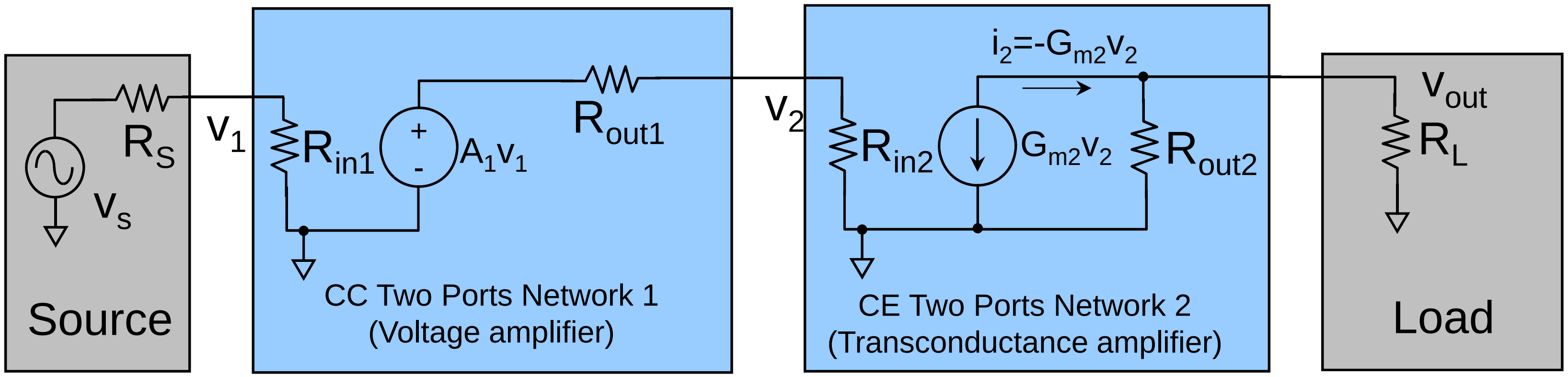
$$= -G_{m2} v_2 \left(R_{out2} // R_L\right)$$

$$\approx -33 v_2$$

$$= -33 v_s$$

$$A_V = \frac{v_{out}}{v_s} = -33$$

BJT Example (2-Port)



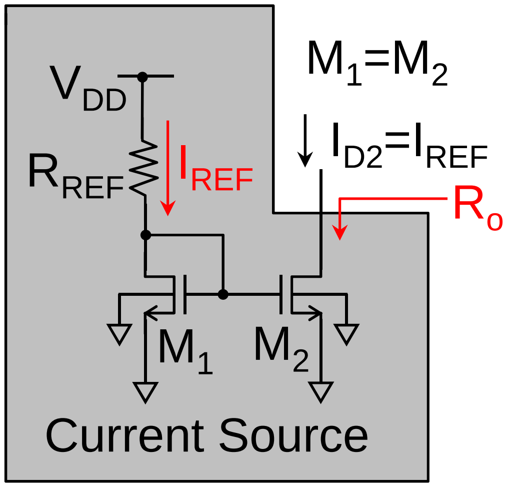
$$A_V = \frac{v_{out}}{v_s} = \frac{v_1}{v_s} \times \frac{v_2}{v_1} \times \frac{v_{out}}{v_2}$$

$$= \underbrace{\frac{R_{in1}}{R_S + R_{in1}}}_{Resistor\ \ Divider} \quad 1st \ \ \underbrace{A_{V1}}_{Stage \ \ CC} \quad \underbrace{\left[-G_{m2}\left(R_{out2} // R_L\right)\right]}_{2nd \ \ Stage \ \ CE}$$

$$= \underbrace{\frac{R_{in1}}{R_S + R_{in1}}}_{Resistor\ \ Divider} \underbrace{\frac{g_{m,Q1}\left(R_{E1} // R_{in2}\right)}{1 + g_{m,Q1}\left(R_{E1} // R_{in2}\right)}}_{1st \ \ Stage \ \ CC} \underbrace{\left(-g_{m,Q2}\right)\left(R_{C2} // r_{o,Q2} // R_L\right)}_{2nd \ \ Stage \ \ CE}$$

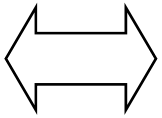
$$= -33.33$$

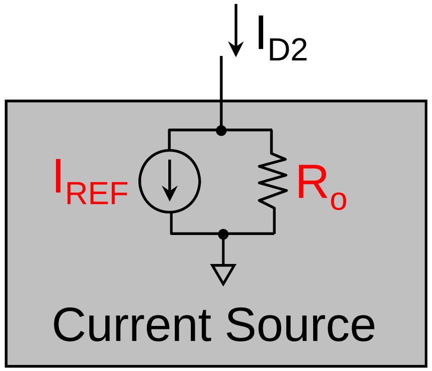
Current Source



Identify transistors used as current source

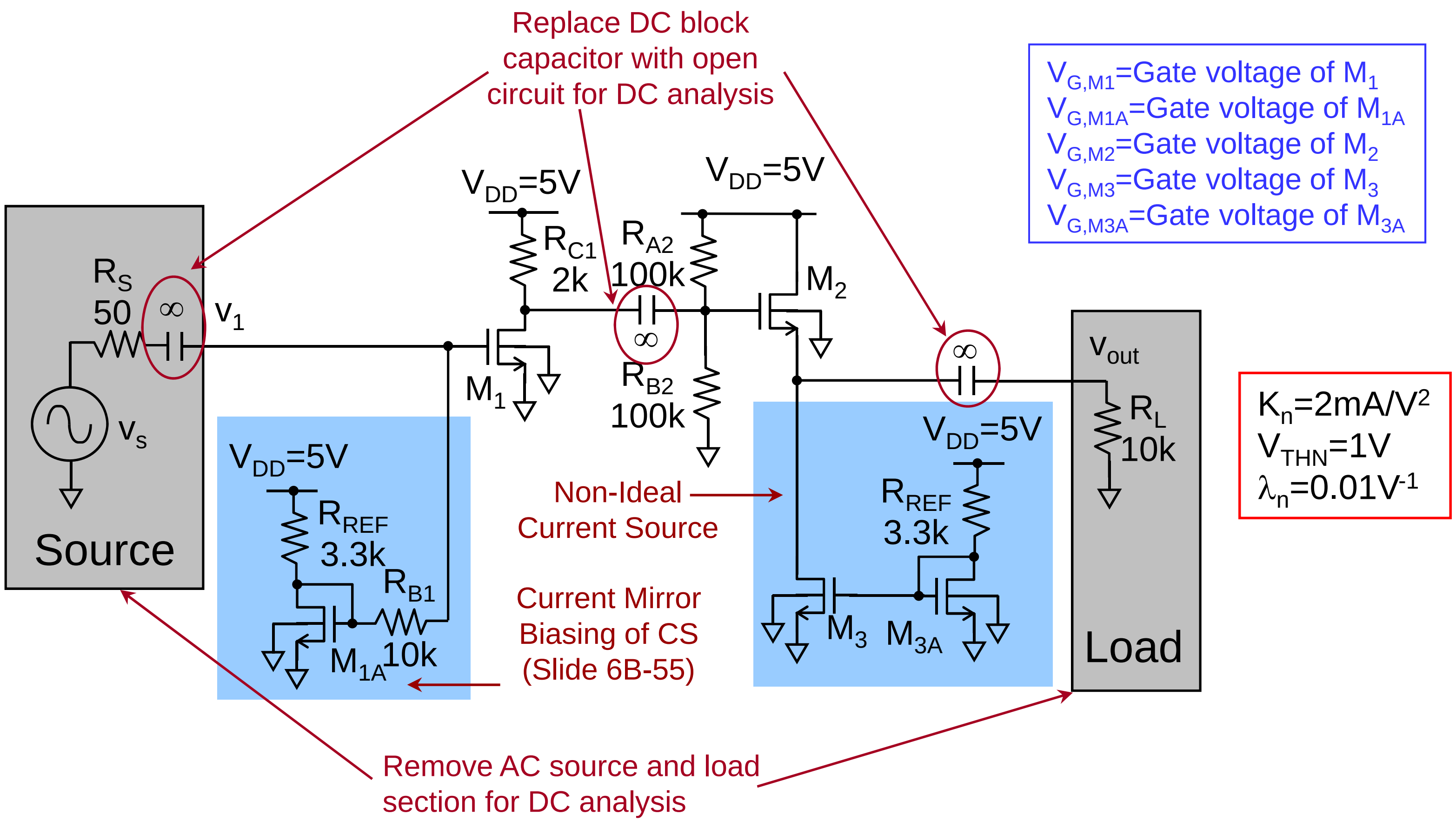
Replace those transistors with a non-ideal current source equivalent





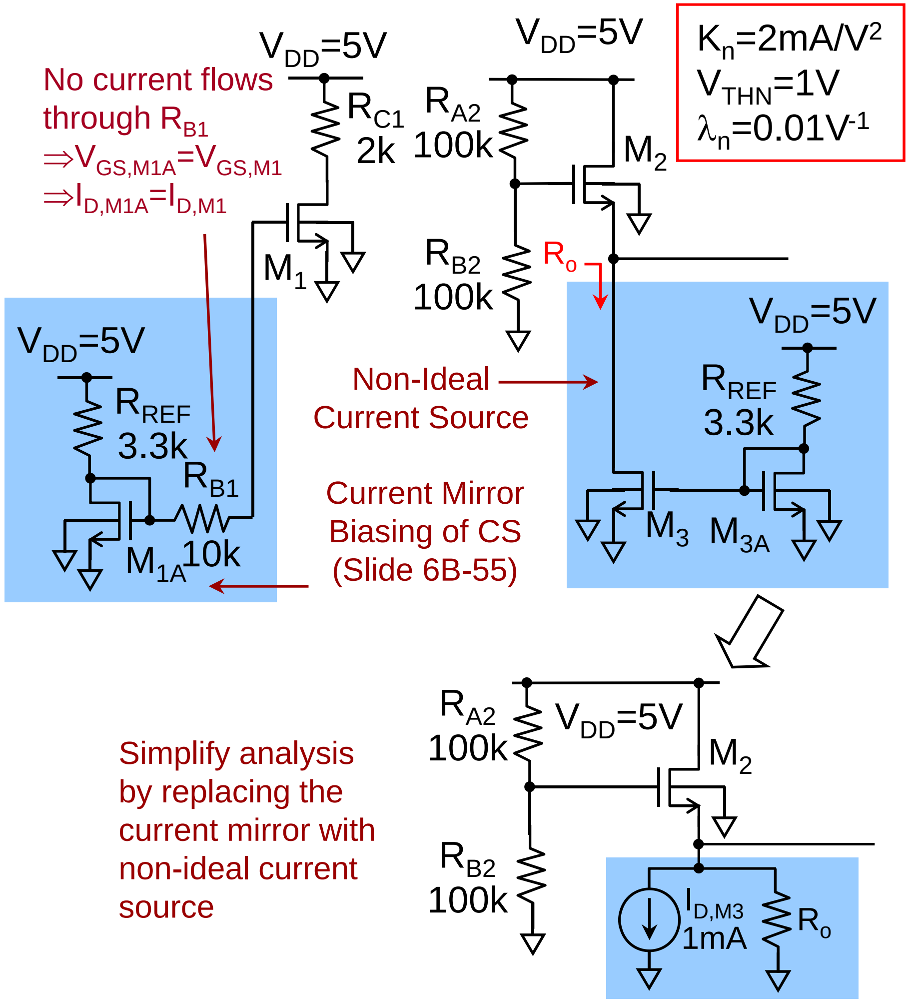
- Not all transistors are amplifiers
- Some transistors are used as non-ideal current source

Two Stage Amplifier Example (DC Analysis)



- Identify Source and Load

Two Stage Amplifier Example (Current Mirror Biasing)



K_n=2mA/V²
V_{THN}=1V
λ_n=0.01V⁻¹

Determine DC Biasing

$$I_{D,M1A} = K_n\left(V_{GS,M1A} - V_{THN0}\right)^2 \cdots\cdots (1)$$

$$I_{D,M1A} = \frac{V_{DD} - V_{GS,M1A}}{R_{REF}} \cdots\cdots (2)$$

$$\Rightarrow 6.6V_{GS,M1A}^2 - 13.2V_{GS,M1A} + 6.6 = 5 - V_{GS,M1A}$$

$$\Rightarrow 6.6V_{GS,M1A}^2 - 12.2V_{GS,M1A} + 1.6 = 0$$

$$\Rightarrow V_{GS,M1A} = \frac{-(-12.2) \pm \sqrt{(12.2)^2 - 4(6.6)(1.6)}}{2(6.6)}$$

$$= 1.71 \quad or \quad 0.142$$

$$\because V_{GS,M1A} = 0.142 \Rightarrow M_{1A} \quad turns \quad off$$

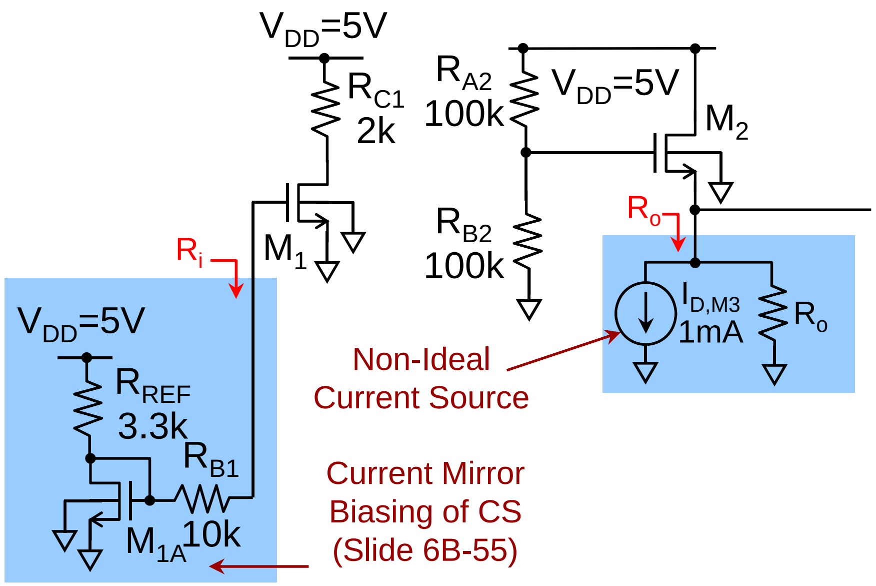
$$\Rightarrow V_{GS,M1A} = 1.71$$

$$\Rightarrow I_{D,M1A} = I_{D,M1} = 1mA$$

Similarly

$$I_{D,M2} = I_{D,M3} = I_{D,M3A} = 1mA$$

Two Stage Amplifier Example (Small Signal AC Equivalent)



Notice that all AC small signal parameters depend on drain current

Find g_m, r_π and r_o

Determine AC small signal parameters

$$\because I_{D,M1A} = I_{D,M1} = I_{D,M2} = 1mA$$

$$\Rightarrow g_{m,M1A} = g_{m,M1} = g_{m,M2} = \sqrt{4K_n I_{D,M1A}} = 2.83mA/V$$

$$\Rightarrow g_{mb,M1A} = g_{mb,M1} = 0$$

$$\Rightarrow g_{mb,M2} = -\frac{g_{m,M1A}}{4} = -0.71m$$

$$r_{o,M1} = r_{o,M2} = \frac{1}{\lambda_n I_{D,M1}} \approx 100k$$

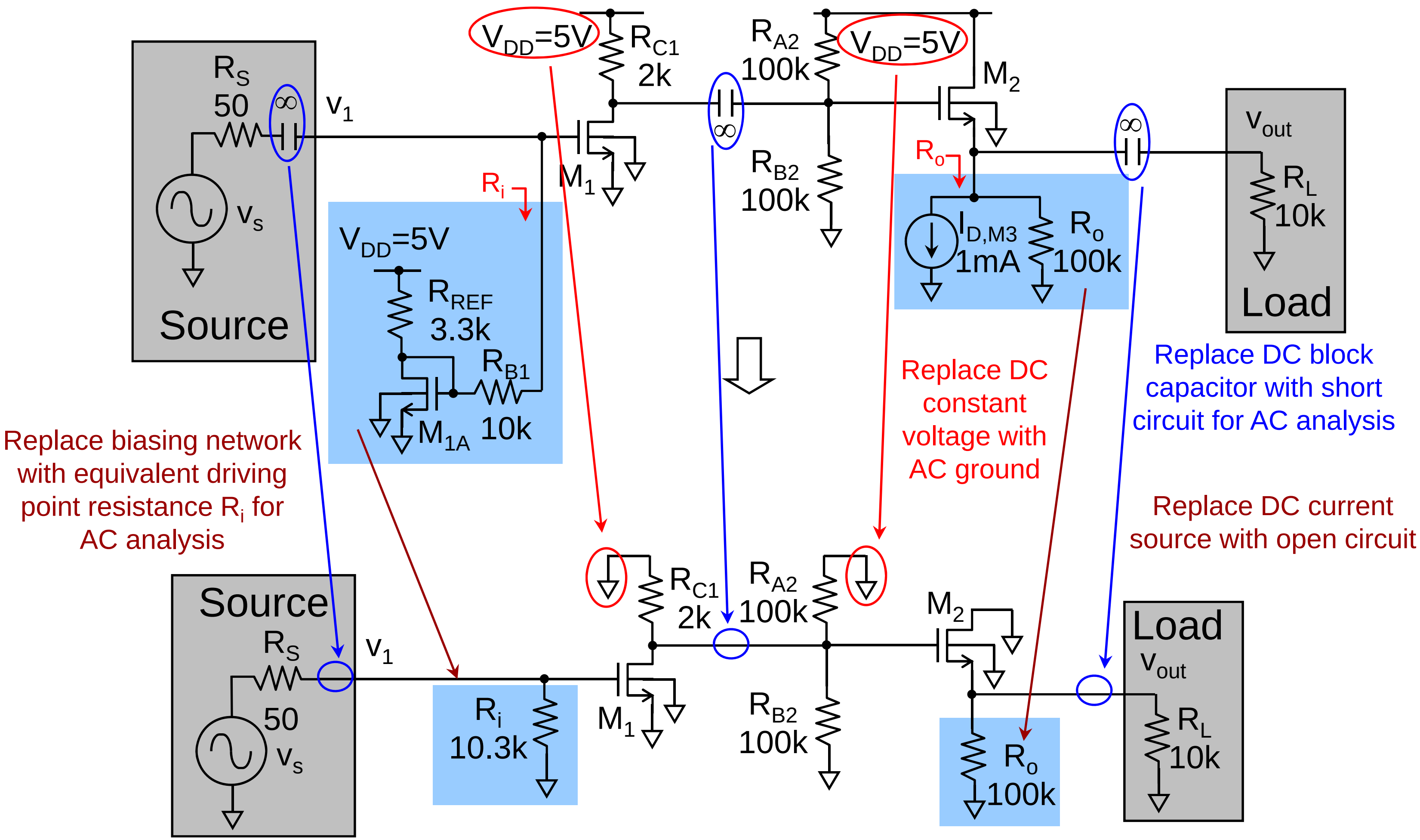
$$\boxed{R_o = r_{o,M3} = \frac{1}{\lambda_n I_{D,M3}} \approx 100k}$$

Table 2, Configuration B

$$\boxed{R_i = R_{B1} + \left(R_{REF} \,//\, \frac{1}{g_{m,M1A}}\right) = 10.3k}$$

Slide 6B-55

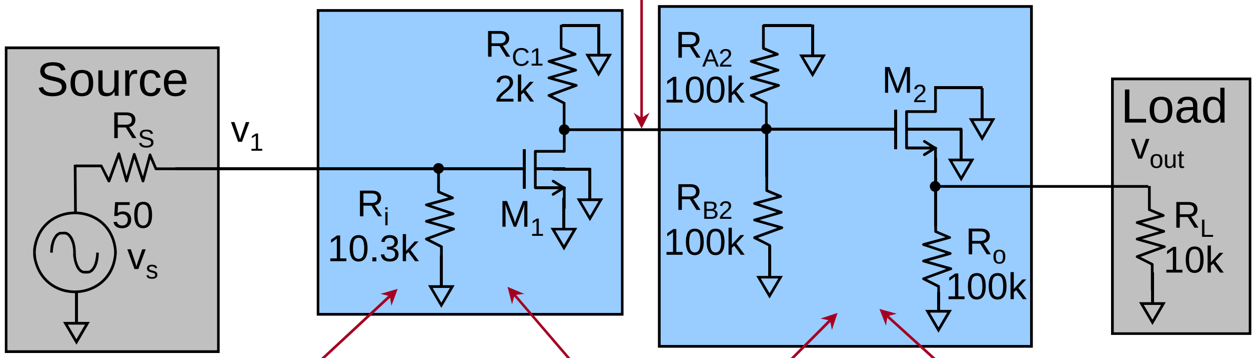
Two Stage Amplifier Example (AC Analysis)



Two Stage Amplifier Example (Identify Single Stage)

Identify the boundary between two amplifiers

Two Stage Amplifier:
CS-CD



First stage amplifier:
Input connected to Gate
Output connected to Drain
⇒ CS

Identify the first and second stage amplifier

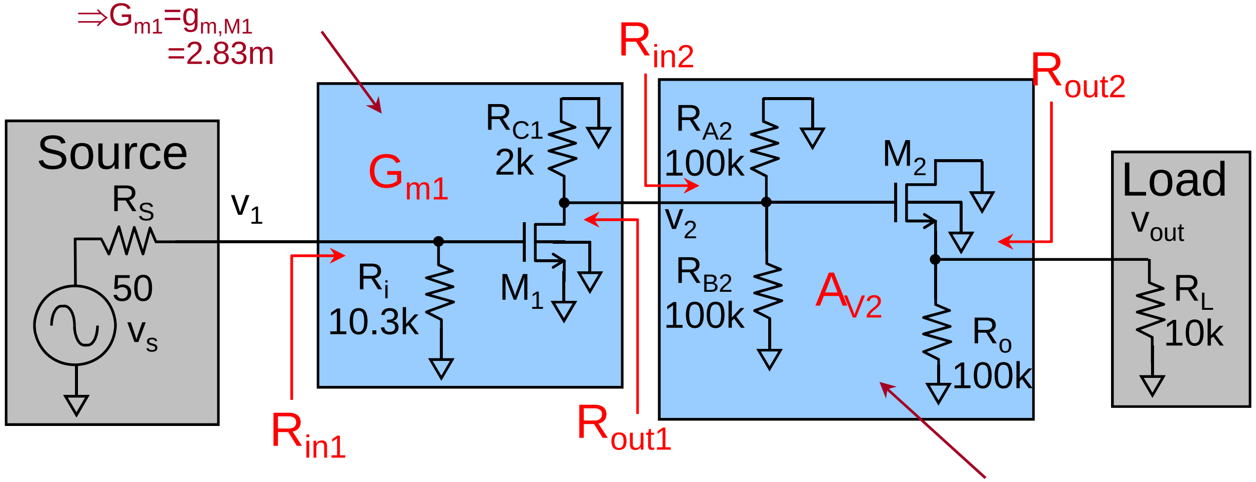
Second stage amplifier:
Input connected to Gate
Output connected to Source
⇒ CD

- Each single stage amplifier can be replaced with its two-port network equivalent consists of R_{in}, R_{out} and G_m

Two Stage Amplifier Example (Identify 2-Port Parameters)

Table 4, CS (Configuration A):
$\Rightarrow G_{m1}=g_{m,M1}$
$=2.83m$

Second two-port network (CD):
R_{in2}, R_{out2}, A_{V2}



First two-port network (CS):
R_{in1}, R_{out1}, G_{m1}

Table 3, CD (Configuration C):
G_{m2} not applicable. More interested in $A_{V2}=v_{out}/v_2$

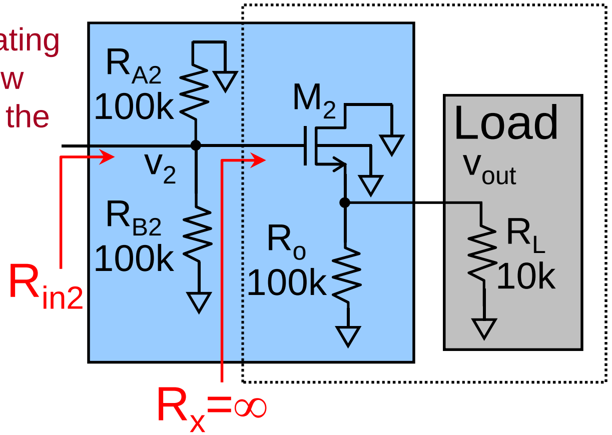
Table 4

R_{in1}, R_{in2}, R_{out1}, R_{out2}: Which one to be solve first?

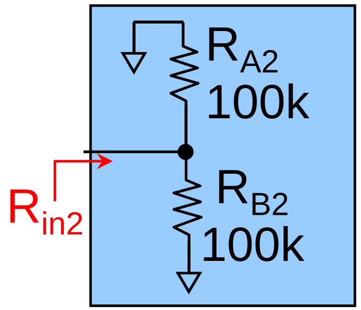
- Identify the 2-port network and the corresponding R_{in}, R_{out}, G_m, and A_V

Two Stage Amplifier Example (Finding R_{in2} and R_{in1})

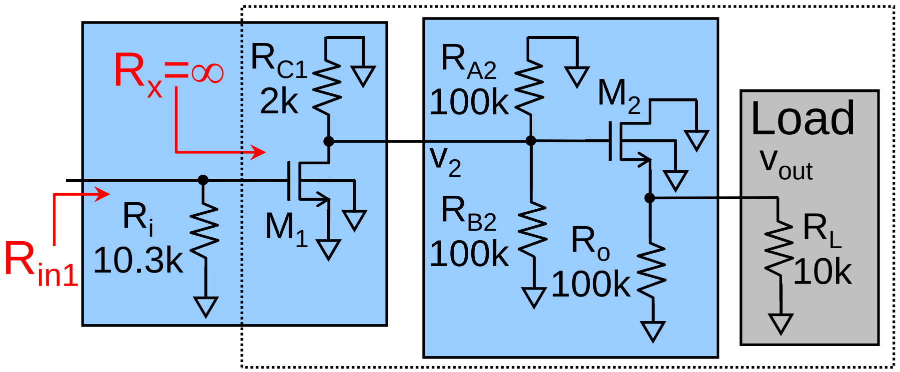
While estimating R_{in2}, we throw away half of the circuit



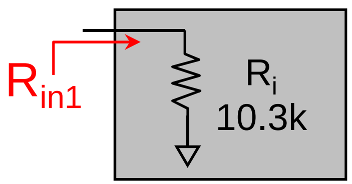
Equivalent resistance (R_x) looking into the gate is infinite



$$\Rightarrow R_{in2} = R_{A2} // R_{B2}$$
$$= 50k$$



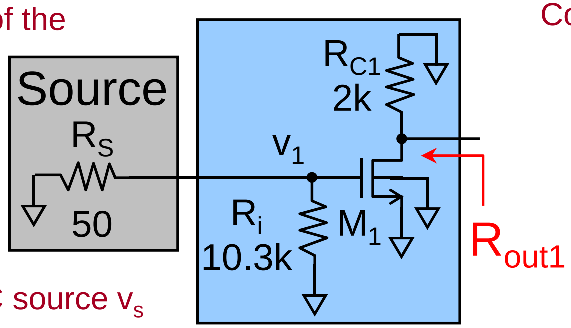
Equivalent resistance (R_x) looking into the gate is infinite



$$\Rightarrow R_{in1} = R_i$$
$$= 10.3k$$

Two Stage Amplifier Example (Finding R_{out1})

While estimating R_{out1}, we throw away half of the circuit



Kill the AC source v_s

Combine R_S and R_i in parallel

No current flows through the gate $\Rightarrow v_1=0$

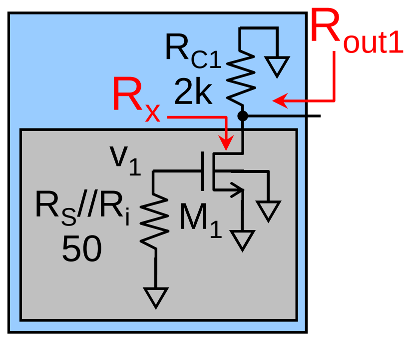
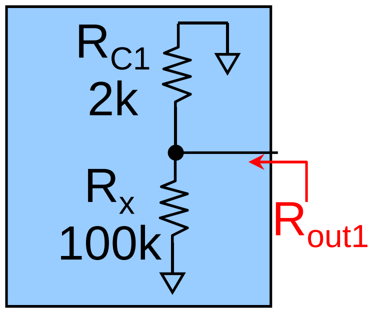


Table 2

Table 2, Configuration B with $R_E=0$

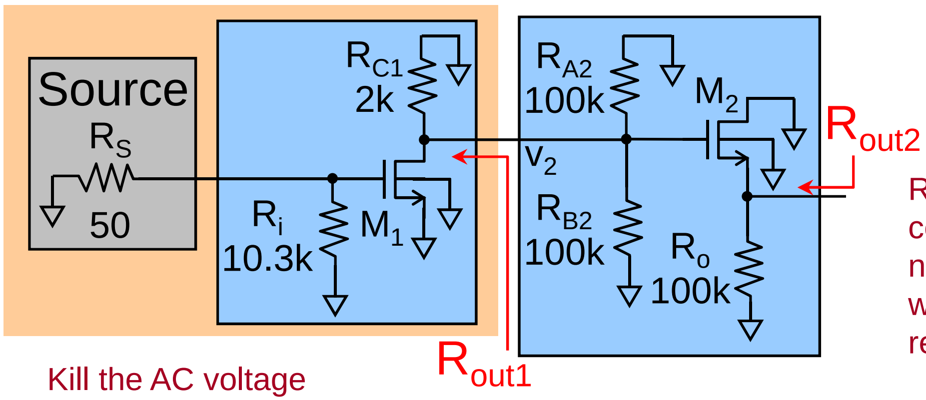
Configurat ion B

$$\Rightarrow R_x = r_{o,M1}$$
$$= 100k$$



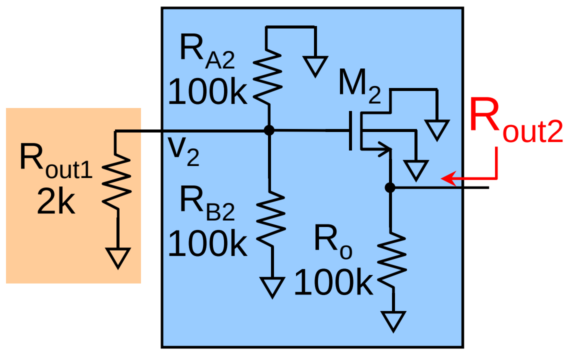
$$\Rightarrow R_{out1} = R_x // R_{C1}$$
$$\approx 2k$$

Two Stage Amplifier Example (Finding R_{out2})



Kill the AC voltage source v_s

Replace the complicated network ( ) with an equivalent resistor (R_{out1})



Combine R_{out1} and $R_{A2}//R_{B2}$ in parallel

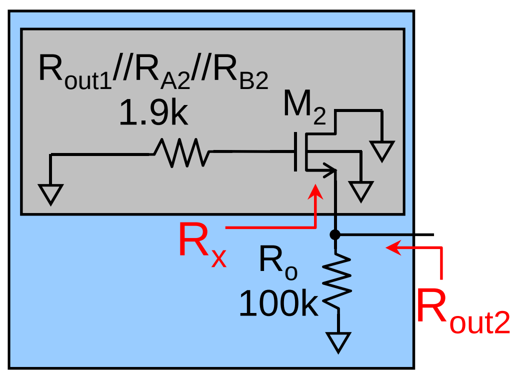


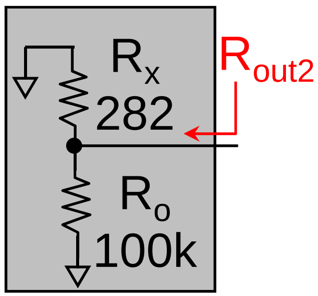
Table 2, Configuration C

Table 2

Configuration C

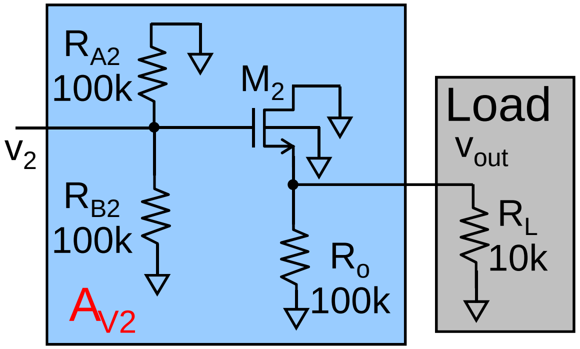
$$\Rightarrow R_x = \frac{1}{g_{m,M2} - g_{mb,M2}}$$

$$\approx 282$$



$$R_{out2} = R_o \,//\, R_x \approx 282$$

Two Stage Amplifier Example (Finding $A_{V2}=v_{out}/v_2$)



Combine R_L and R_o in parallel

Combine R_{A2} and R_{B2} in parallel

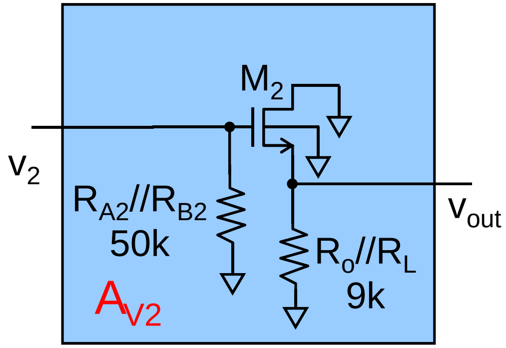


Table 4

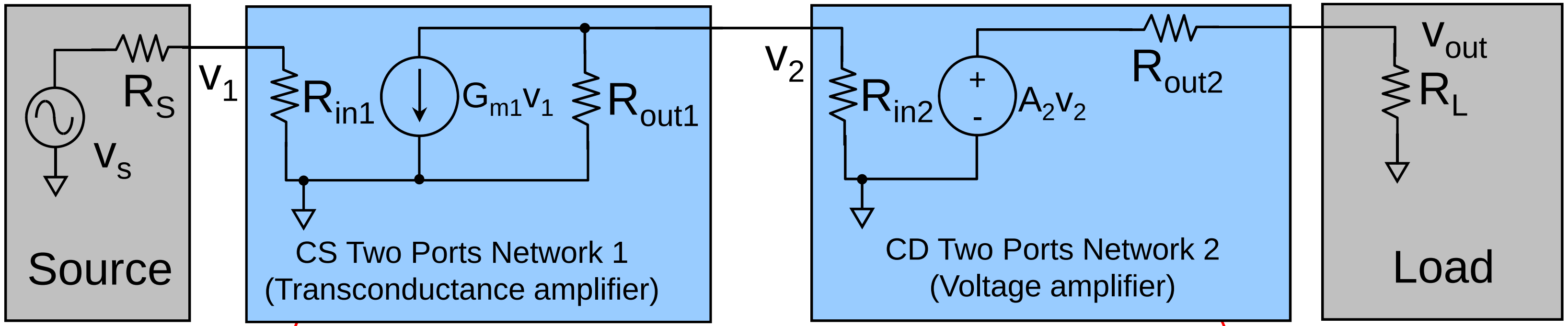
Table 3, Configuration C

Configuration C

$$A_{V2}=\frac{v_{out}}{v_2}=\frac{g_{m,M2}\left(R_o//R_L\right)}{1+\left(g_{m,M2}-g_{mb,M2}\right)\left(R_o//R_L\right)}$$

$$\approx 0.78$$

Two Stage Amplifier Example (2-Port)



Replace each single stage amplifier with their two-port network equivalent

$$R_{in1} = R_i = R_{B1} + \left(R_{REF} // \frac{1}{g_{m,M1A}} \right)$$

$$= 10.3k$$

$$R_{out1} = R_{C1} // r_{o,M1}$$

$$\approx 2k$$

$$G_{m1} = g_{m,M1}$$

$$= 2.83mA/V$$

$$R_{in2} = R_{A2} // R_{B2}$$

$$= 50k$$

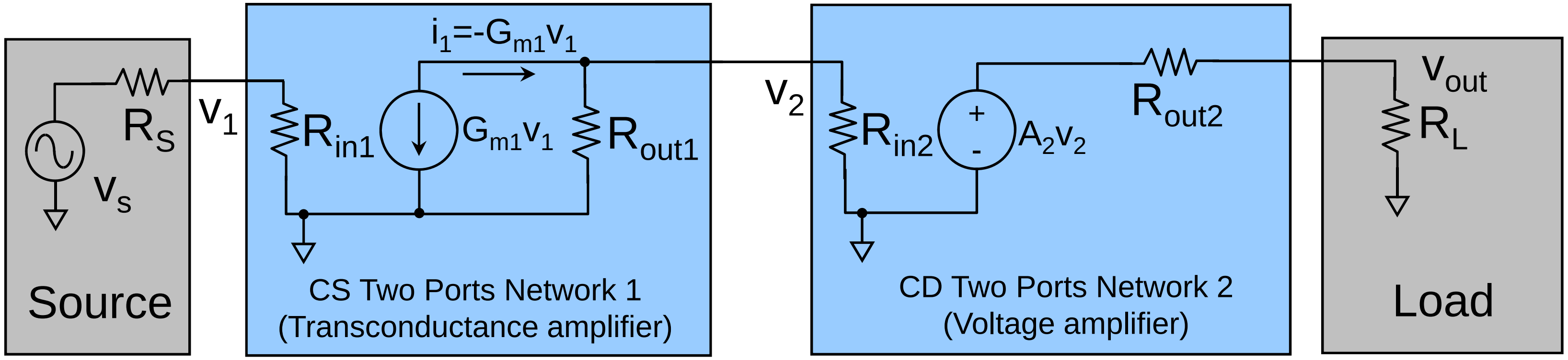
$$R_{out2} = \frac{1}{g_{m,M2} - g_{mb,M2}} // R_o$$

$$\approx 282$$

$$A_{V2} = \frac{v_{out}}{v_2} = \frac{g_{m,M2}(R_o // R_L)}{1 + (g_{m,M2} - g_{mb,M2})(R_o // R_L)}$$

$$= 0.78$$

Two Stage Amplifier Example (2-Port)



$$v_1 = v_s \times \frac{R_{in1}}{R_{in1} + R_S}$$

$$\approx v_s$$

$$v_2 = i_1 \times \left(R_{out1} // R_{in2}\right)$$

$$= -G_{m1} v_1 \times \left(R_{out1} // R_{in2}\right)$$

$$\approx -5.4 v_s$$

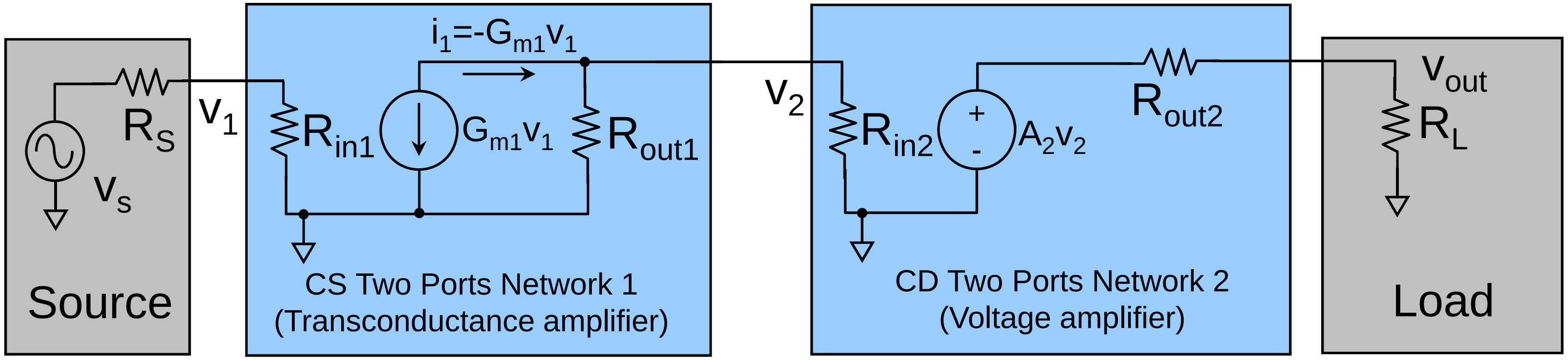
$$v_{out} = v_2 \times \frac{g_{m,M2}\left(R_o // R_L\right)}{1 + \left(g_{m,M2} - g_{mb,M2}\right)\left(R_o // R_L\right)}$$

$$= 0.78 v_2$$

$$\approx -4.2 v_s$$

$$A_V = \frac{v_{out}}{v_s} = -4.2$$

Two Stage Amplifier Example (2-Port)



$$A_V = \frac{v_{out}}{v_s} = \frac{v_1}{v_s} \times \frac{v_2}{v_1} \times \frac{v_{out}}{v_2}$$

$$= \underbrace{\frac{R_{in1}}{R_S + R_{in1}}}_{Resistor\ \ Divider} \underbrace{\left[-G_{m1}\left(R_{out1} // R_{in2}\right)\right]}_{1st\ \ Stage\ \ CS} \underbrace{A_{V2}}_{2nd\ \ Stage\ \ CD}$$

$$= \underbrace{\frac{R_{in1}}{R_S + R_{in1}}}_{Resistor\ \ Divider} \underbrace{\left(-g_{m,M1}\right)\left(R_{C1} // R_{in2}\right)}_{1st\ \ Stage\ \ CS} \underbrace{\frac{g_{m,M2}\left(R_L // r_{o,M3}\right)}{1 + \left(g_{m,M2} - g_{mb,M2}\right)\left(R_L // r_{o,M3}\right)}}_{2nd\ \ Stage\ \ CD}$$

$$= -4.2$$

How about Amplifier Design?

Amplifier Analysis

1. Resistors, capacitors and transistors are all given
2. Perform DC Analysis using Large Signal Model
3. Determine transistor small signal AC parameters, i.e. g_m, g_{mb}, r_o, r_π
4. Determine amplifier configuration and 2-port network parameters, i.e. R_{in}, R_{out}, G_m, A_V
5. Determine the overall gain of amplifier

Amplifier Design

1. The overall gain of amplifier is specified
2. Determine suitable amplifier configuration and corresponding 2-port network parameters, i.e. R_{in}, R_{out}, G_m, A_V to give the desired gain
3. Determine transistor small signal AC parameters, i.e. g_m, g_{mb}, r_o, r_π, to give the desired 2-port network parameters
4. Determine the DC biasing required to give the desired g_m, g_{mb}, r_o, r_π.
5. Choose the resistors, capacitors, transistors and proper voltage or current source to give the desired DC biasing

Lecture Summary

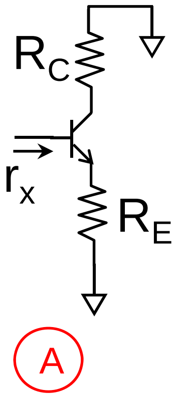
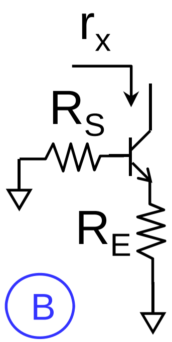
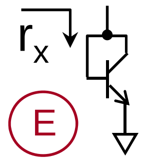
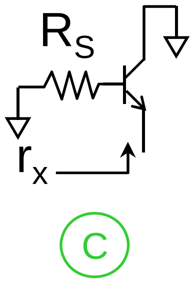
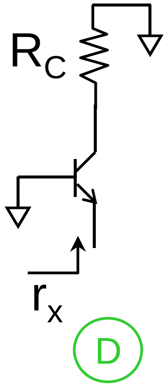
- **Conceptually explain the analysis of multi-stage amplifier.**
- **Multi-stage amplifier analysis for 2-stage PMOS amplifiers.**
- **Multi-stage amplifier analysis for 2-stage BJT amplifiers.**
- **Multi-stage amplifier analysis for 2-stage NMOS amplifiers.**

Reading Assignment

- **Reading: Reference Book (Sedra & Smith)**
  Chapter 6, pp. 666 – 673. (Multi-stage amplifier)

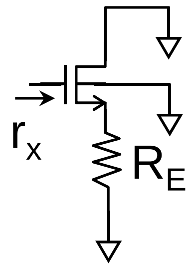
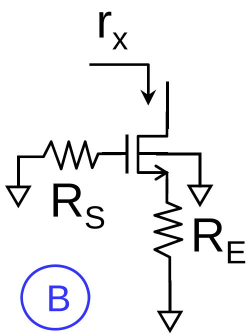
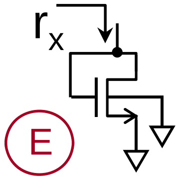
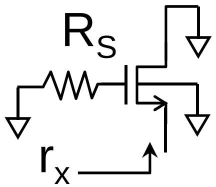
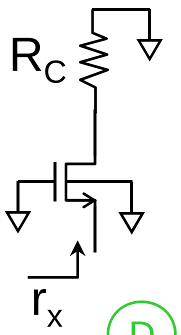
BJT Equivalent Resistance Summary (Table 1)

Blue: look into collector terminal Red: look into base terminal Green: look into emitter terminal

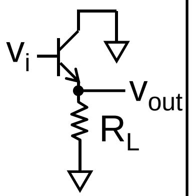
Conf	r_x	Conf	r_x	Conf	r_x
	$r_\pi + (1+\beta)R_E$ $\approx r_\pi(1+g_m R_E)$		$r_o\left\{1+g_m\left[(r_\pi+R_S)//R_E\right]\left(\frac{r_\pi}{r_\pi+R_S}\right)\right\}$ *If* $R_S=0$ *and* $r_\pi << R_E$ $\Rightarrow r_{x,\max}=r_o(\beta+1)$		$\frac{1}{g_m}$
	$\frac{R_S+r_\pi}{1+\beta}//r_o$ $\approx \frac{R_S}{1+\beta}+\frac{1}{g_m}$		$\frac{1}{g_m}\times\frac{r_o+R_C}{r_o+R_C/\beta}$		

MOS Equivalent Resistance Summary (Table 2)

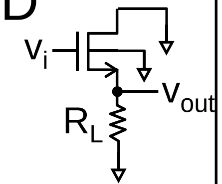
Blue: look into drain terminal Red: look into gate terminal Green: look into source terminal

Conf	r_x	Conf	r_x	Conf	r_x
 A	∞	 B	$r_o\left[1+\left(g_m-g_{mb}\right)R_E\right]$	 E	$\frac{1}{g_m}$
 C	$\frac{1}{g_m-g_{mb}}$	 D	$\frac{1}{g_m-g_{mb}}\times\frac{r_o+R_C}{r_o}$		

BJT Amplifier Configurations (Table 3)

BJT	G_m	A_V
CE A	g_m	Derive Based on 2-port Network
CB B	$-g_m$	Derive Based on 2-port Network
CC C 	Too Complex To Be Useful	$\dfrac{g_m R_L}{1+g_m R_L}$
CE with Emitter Degeneration D	$\dfrac{g_m}{1+g_m R_E}$	Derive Based on 2-port Network

MOS Amplifier Configurations (Table 4)

MOS	G_m	A_V
CS A	g_m	Derive Based on 2-port Network
CG B	$-(g_m - g_{mb})$ $Drop\ \ g_{mb}\ \ if\ \ no\ \ body\ \ effect$	Derive Based on 2-port Network
CD C 	Too Complex To Be Useful	$\frac{g_m R_L}{1+(g_m - g_{mb})R_L} \approx \frac{g_m}{g_m - g_{mb}}$ $Drop\ \ g_{mb}\ \ if\ \ no\ \ body\ \ effect$
CS with R_E D	$\frac{g_m}{1+(g_m - g_{mb})R_E}$ $Drop\ \ g_{mb}\ \ if\ \ no\ \ body\ \ effect$	Derive Based on 2-port Network