NATIONAL UNIVERSITY *of* SINGAPORE

Department of Electrical and Computer Engineering

EE2021 – Devices and Circuits

Tutorial 4

Homework 3:

Homework 3 is Question 2 and Question 6 of Tutorial 4. You have to submit the homework assignment in hardcopy in class on Wednesday 1 April 2015.

Unless otherwise stated, you may use the tables of the amplifier configurations and equivalent resistances in your lecture notes in your solutions to the questions.

Q1. Draw the pull down network (PDN) and pull up network (PUN) of the following logic function:

$$Y = \overline{\{[(A.B) + C].D\} + (E.F)}\ .$$

Determine also the best case propagation delay of the above PUN, $t_{pLH,best}$, in terms of that of an inverter, $t_{pLH,inv}$. All NMOS and PMOS transistors in the above logic networks and the inverter have sizing of $(W/L)_n = n$ and $(W/L)_p = p$, respectively.

Q2. (i) Design the pull down network of the following logic function :

$$Y = \overline{(A+B)\cdot C\cdot (D+E)}.$$

[5 marks]

(ii) Assume that all the transistors have a sizing of $(W/L)_{min}$. Compare the worst case t_{pHL} of the logic circuit with the t_{pHL} of an inverter with the same transistor sizing.

[4 marks]

(iii) Suggest one way of sizing the transistors of the logic circuit such that its worst case t_{pHL} equals the t_{pHL} of an inverter with a sizing of $(W/L)_{min}$.

[3 marks]

Q3. Figure Q3 shows a pull-down network (PDN) for a logic function Y.

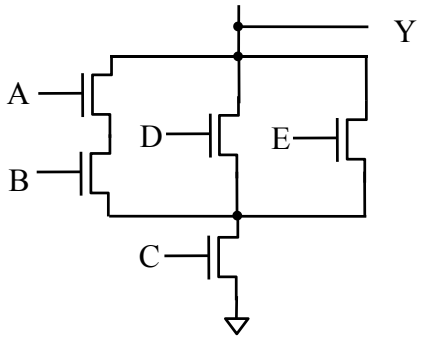

Fig. Q3

(i) Express Y in terms of A, B, C, D and E.

(ii) Draw the pull-up network (PUN) corresponding to the PDN in Fig. Q3.

(iii) All NMOS and PMOS transistors in the above logic circuit have a sizing of $(W/L)_{\text{min}}$. We shall compare the dynamic performance of the logic circuit with respect to a symmetric inverter where the sizing of NMOS transistor, $(W/L)_{NMOS} = (W/L)_{\text{min}}$, and the sizing of PMOS transistor, $(W/L)_{PMOS} = (\mu_n/\mu_p)(W/L)_{NMOS} = 2.5(W/L)_{\text{min}}$.

How many times is t_{PHL} of the above logic circuit compared to that of the symmetric inverter? Give the best and worst case values.

(iv) Repeat the calculations in part (iii) for t_{PLH} of the above logic circuit.

[Ans. (iii) Best = 1.4, Worst = 3; (iv) Best = 1.79, Worst = 7.5]

Q4. Assume that the AC small signal parameters of the BJTs are $g_{m,Qi}$, $r_{\pi,Qi}$, $r_{o,Qi}$, and the AC small signal parameters of the MOSFETs are $g_{m,Mj}$, $g_{mb,Mj}$, $r_{i,Mj}$, $r_{o,Mj}$, where i (i = 1, 2) and j (j = 1, 2, 3) are the corresponding device indices. Using the equivalent resistance tables in your lecture notes, write down the expressions for the small signal AC equivalent resistances, R_{x1}, R_{x2} and R_{x3} in the circuit in Fig. Q4.

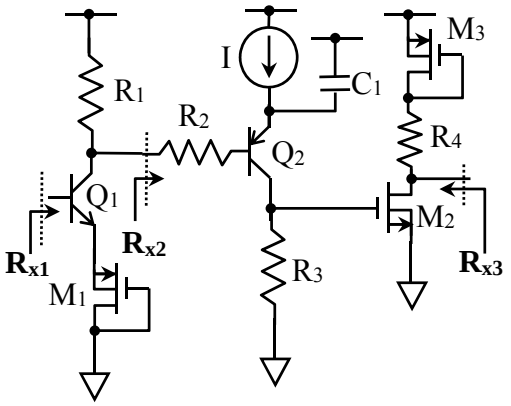

Fig. Q4

Q5. Design a voltage amplifier that provides 0.25 W of signal output power to a 100 Ω load resistor. The signal source provides a 25 mV root-mean-square (RMS) voltage signal and has a source resistance of 0.5 MΩ.

(i) Using the specifications given above, calculate the required voltage gain v_o/v_s. [Hint: You need to calculate the signal voltage v_o (RMS value) across the load, and compare it with the source voltage signal v_s (RMS value)].

[Ans: 200]

(ii) Design a multi-stage amplifier to meet the required voltage gain using chips given below. You may use a chip more than once. Please keep the number of stages in the multi-stage amplifier to a maximum of 3. The voltage gain of the multi-stage amplifier you design can be slightly higher (e.g. up to 20% higher) than the required voltage gain.

Three voltage amplifier chips are available:

Chip 1: Input resistance r_{i1} = 1 MΩ; Gain a_{v1} = 10; Output resistance r_{o1} = 10 kΩ.
Chip 2: Input resistance r_{i2} = 10 kΩ; Gain a_{v2} = 75; Output resistance r_{o2} = 1 kΩ.
Chip 3: Input resistance r_{i3} = 10 kΩ; Gain a_{v3} = 1; Output resistance r_{o3} = 10 Ω.

Q6. Figure Q6 below shows a single stage amplifier with current mirror biasing.

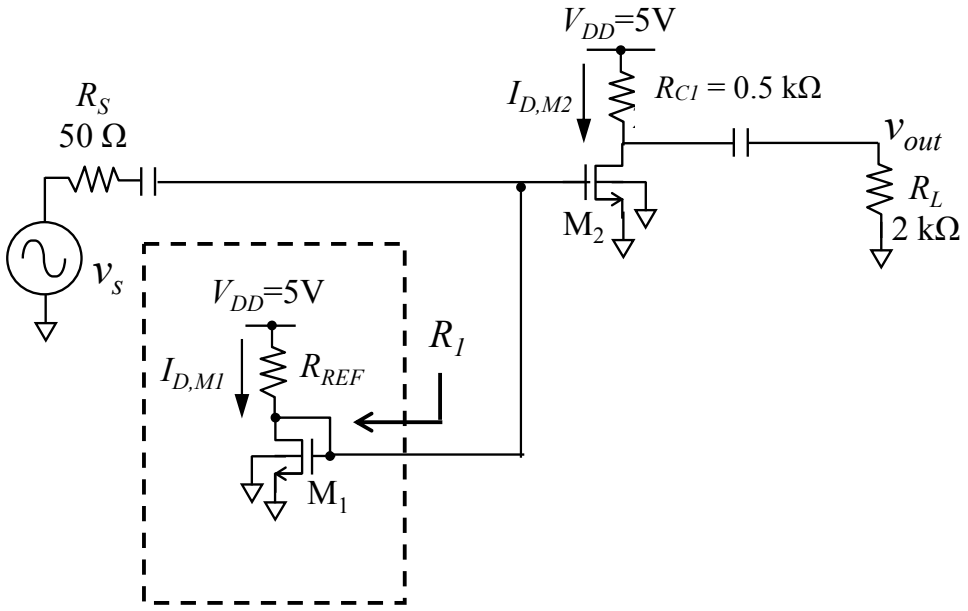

Fig. Q6

For the two n-channel MOSFETs, $V_{THN1} = V_{THN2} = 1$ V, $\lambda_{M1} = \lambda_{M2} = 0$, $K_{n,M1} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_{M1} =$ 2 mA V^{-2}, $K_{n,M2} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_{M2} = 4$ mA V^{-2}, where $\left(\frac{W}{L}\right)_{M2} = 2\left(\frac{W}{L}\right)_{M1}$.

(i) Design R_{REF} such that $I_{D,M1} = 2$ mA.

[5 marks]

(ii) What is the value of $I_{D,M2}$?

[2 marks]

(iii) Calculate the small signal parameters of the two MOSFETs, i.e., $g_{m,M1}$, $r_{o,M1}$, $g_{m,M2}$, $r_{o,M2}$.

[4 marks]

(iv) Calculate the value of the a.c. equivalent resistance, R_1, of the circuit enclosed in the dashed box in Fig. Q6.

[3 marks]

(v) Identify the configuration of the single stage amplifier.

[1 mark]

(vi) Determine the parameters, G_m, R_{in} and R_{out} of the two-port network of the amplifier.

[3 marks]

Q7. [This question will not be discussed during tutorial class.]

This is a new amplifier circuit that we have not analyzed in the lectures. It is not among the amplifier configurations listed in the tables in the lecture notes. Hence, the two-port network parameters of this amplifier has to be derived from first principles.

For the amplifier circuit shown in Fig. Q7, the transistor Q_1 has the following parameter values: $I_S = 10^{-15}$ A, $\beta = 100$, $V_A = 100$ V.

(i) What are the values of the small signal parameters, $g_{m,Q1}$, $r_{\pi,Q1}$ and $r_{o,Q1}$ of Q_1?

[Ans. 20 mA/V, 5 k, 200k]

(ii) Transform the circuit for AC analysis and replace the transistor with its small signal equivalent.

(iii) Assuming that the amplifier can be transformed into a 2-port transconductance amplifier, find the three parameters (G_m, R_{in}, R_{out}) of the 2-port network.

[Ans. 18 mA/V, 45 Ω, 268 Ω]

(iv) Derive the overall gain $A_V = v_{out}/v_s$.

[-2.6]

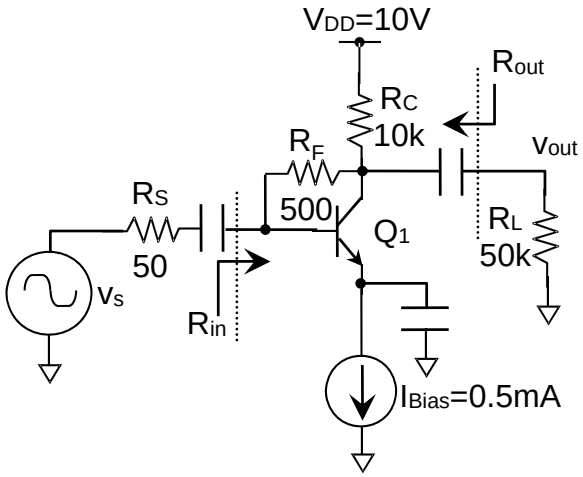

Fig. Q7