NATIONAL UNIVERSITY OF SINGAPORE

EXAMINATION FOR

(Semester II: 2011/2012)

EE2021 –DEVICES AND CIRCUITS

April/May 2011 - Time Allowed: 2.5 Hours

INSTRUCTIONS TO CANDIDATES:

1. This paper contains **FOUR (4)** questions and comprises **FIFTEEN(15)** printed pages.
2. Answer all questions. **Start each question on a new page.**
3. All questions carry equal marks.
4. This is a **CLOSED BOOK** examination.
5. Programmable calculators are allowed in this examination.
6. The following information can be used where applicable:

Elementary charge	e	=	1.602×10^{-19} C
Boltzmann constant	k	=	1.381×10^{-23} J K^{-1}
		=	8.618×10^{-5} eV K^{-1}
Thermal energy (T = 300 K)	kT	=	0.0259 eV
Thermal voltage (T = 300 K)	V_t	=	0.0259 V
Permittivity of free space	ε_0	=	8.854×10^{-14} F cm^{-1}

For silicon at 300 K:

Intrinsic carrier concentration	n_i	=	1.5×10^{10} cm^{-3}
Relative permittivity of silicon	ε_r (Si)	=	11.7
Relative permittivity of silicon dioxide	ε_r (SiO_2)	=	3.9

7. A set of formulas and tables is given in the APPENDIX for your reference.

Q.1 The schematic cross-sectional view of a silicon device is shown in Figure Q.1.1 and its parameters are shown in Table Q.1.1.

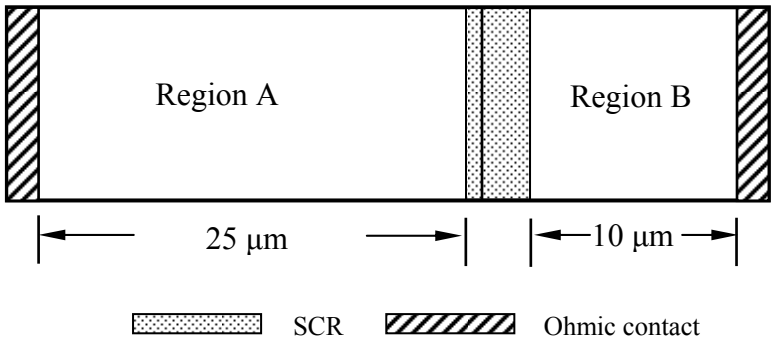


Figure Q.1.1 : Schematic cross-sectional view of a silicon device (not to scale).

Table Q.1.1 : Parameters of the silicon device.

	Region A	Region B
Donor concentration, N_D (cm^{-3})	1.8×10^{17}	0
Acceptor concentration, N_A (cm^{-3})	2.0×10^{16}	2.0×10^{16}
Minority carrier lifetime, τ (s)	1×10^{-8}	5×10^{-6}
Length of neutral region, excluding SCR, (cm)	25×10^{-4}	10×10^{-4}
Cross-sectional area, A (cm^2)	1×10^{-4}	1×10^{-4}

(a) Determine the resistances of the neutral regions A and B, respectively, of the silicon device. You may make use of the graph of the carrier mobilities versus total dopant concentration given in Figure Q.1.2.

[6 marks]

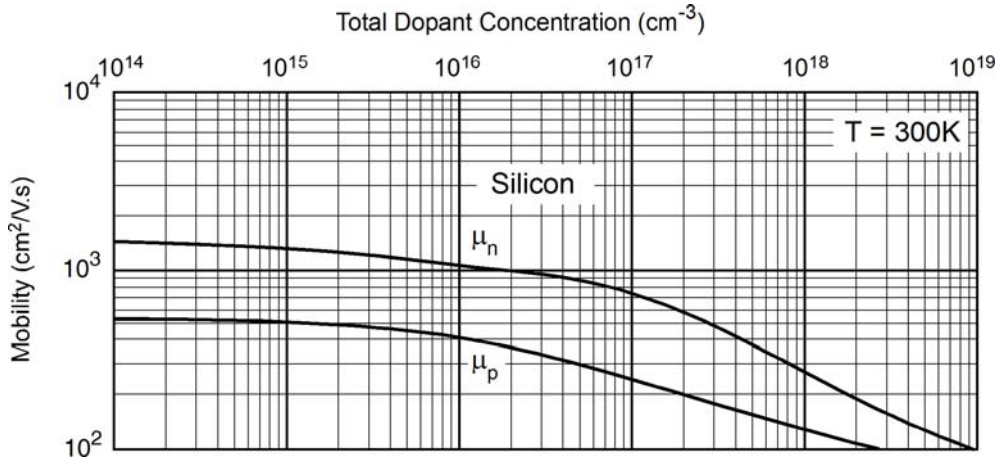


Figure Q.1.2: Electron (μ_n) and hole (μ_p) mobilities in silicon at 300 K, as a function of total dopant concentration.

Question Q.1 continues on Page 3

(b) The current-voltage (*I-V*) characteristics of the p-n junction is given by the ideal diode equation :

$I = I_S\left[\exp\left(\left[\frac{eV}{kT}\right]\right) - 1\right]$ where I_S is the reverse saturation current.

For the given device, determine I_S.

[8 marks]

(c) The device is connected in the circuit shown in Figure Q.1.3, where it is represented as a diode in series with a resistance R_S, as indicated within the dotted rectangle. R_S represents the resistance of the neutral regions of the device. The input voltage V_i is 3 V and it is found that the current I is 2.83 mA. Calculate the voltage V_o and the resistance R_L.

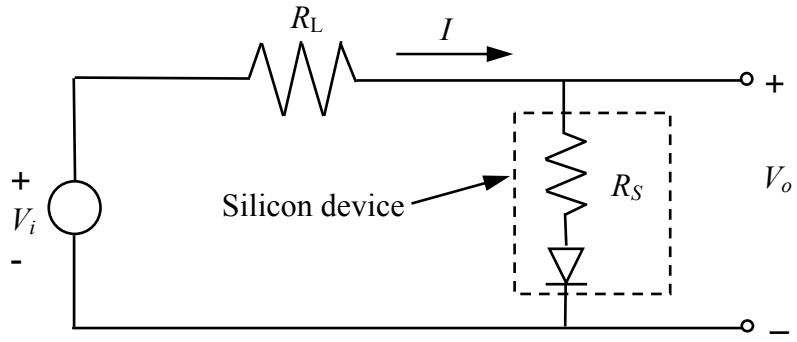


Figure Q.1.3

[6 marks]

(d) The input voltage changes by a small amount ΔV_i, where ΔV_i = 50 mV. Draw a small signal equivalent of the above circuit, and calculate the change in the output voltage, ΔV_o. In your calculations, you may neglect the capacitances in the diode.

[5 marks]

Q.2 (a) An n-p-n bipolar junction transistor has the following parameters:

Emitter doping, $N_{DE} = 10^{19}$ cm^{-3},
Base doping, $N_{AB} = 10^{17}$ cm^{-3},
Minority carrier diffusivity in the base, $D_{nB} = 10$ cm^2 s^{-1},
Minority carrier diffusion length in the base, $L_{nB} = 2 \times 10^{-3}$ cm,
Cross-sectional area, $A = 0.01$ cm^2.

The bipolar transistor is biased in the forward active mode, with an base-emitter voltage, $V_{BE} =$ 0.65 V, and a base-collector voltage, $V_{BC} =$ -5 V. Under these conditions, the width of the neutral region in the base, x_B, is equal to 1×10^{-4} cm.

(i) Calculate the concentrations of the electrons (minority carriers) in the base, at the edges of the space-charges regions.

[3 marks]

(ii) Calculate the magnitude of the collector current.

[3 marks]

(iii) Calculate the total minority carrier charge in the neutral region of the base.

[2 marks]

(iv) The base-emitter voltage is changed to 0.66 V. Calculate the *change* in the total minority carrier charge in the neutral region of the base. Hence explain (no calculation is needed) why there is a diffusion capacitance in the base of the bipolar transistor.

[5 marks]

(b) The threshold voltage of a p-channel MOSFET, V_{THP}, is -1.2 V. The voltage applied to the gate, with respect to the source, V_{GS}, is -2 V. State, and explain briefly, whether the device is operating in the saturation region when the drain-to-source voltage,

(i) $V_{DS} =$ -0.4 V, **[2 marks]**

(ii) $V_{DS} =$ -1 V. **[2 marks]**

Question Q.2 continues on Page 5

(c) The drain current versus drain voltage (I_D - V_{DS}) characteristics of an n-channel MOSFET is shown in Figure Q.2.1.

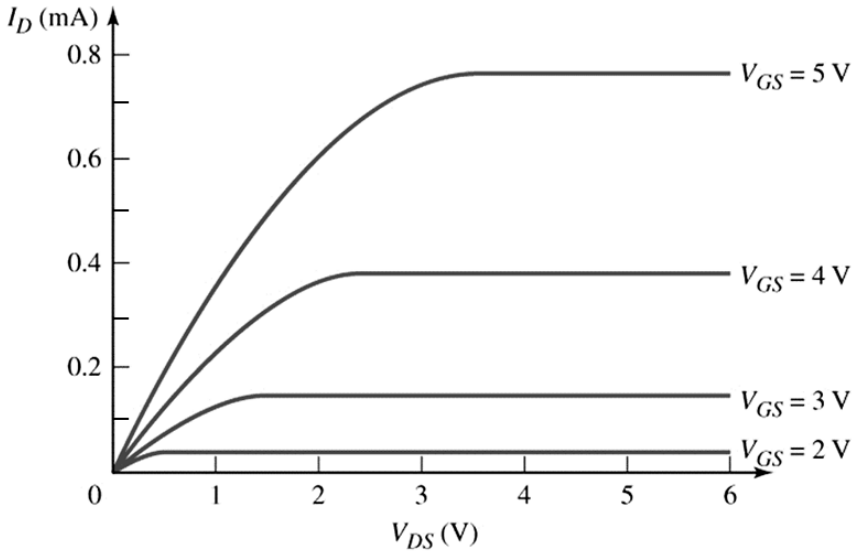


Figure Q.2.1 : I_D - V_{DS} characteristics of an n-channel MOSFET.

(i) For the given MOSFET, calculate the threshold voltage, V_{THN}, and the conductance parameter K_n.

[6 marks]

(ii) Calculate the saturation drain current when V_{GS} = 3.5 V.

[2 marks]

Q.3

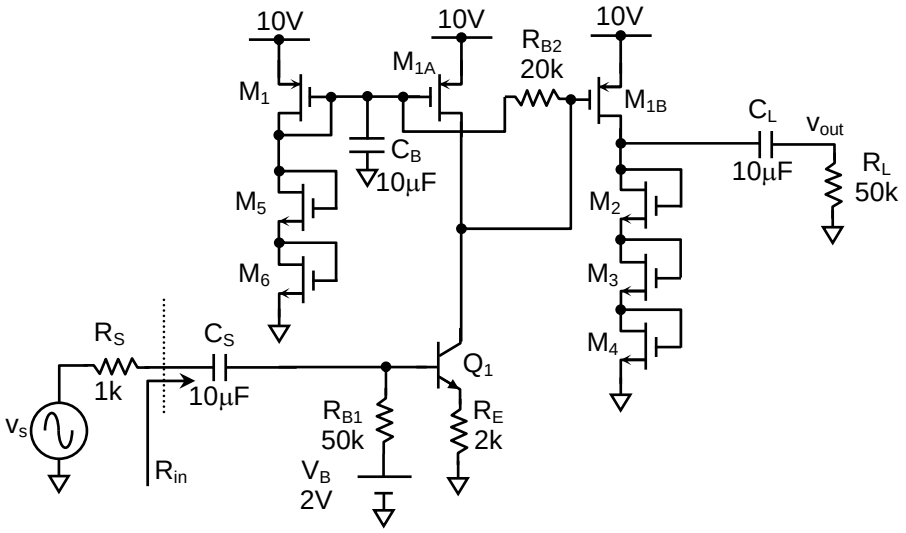


Figure Q.3

A multistage amplifier circuit is shown in Figure Q.3. You may assume that the body and the source terminals of the NMOS and PMOS are connected together, i.e., no body effect for NMOS and PMOS. You may also assume the following device parameters, and that all npn BJT, NMOS and PMOS devices are identical:

- β=100, V_A=500,
- K_n=2mA/V^2, V_{THN}= 3V, λ_p=0.001V^{-1},
- K_p=2mA/V^2, V_{THP}= −1V, λ_p=0.001V^{-1}.

(a) Determine $I_{D,M1A}$. Work out the small signal AC parameters of Q_1, M_2 and M_{1B}.

[6 marks]

(b) Identify the two stage amplifier configuration.

[2 marks]

(c) Obtain the small signal gain (v_{out}/v_s) of the amplifier.

[8 marks]

(d) If M_2, M_3 and M_4 are replaced with diode-connected PMOS transistors, discuss the impact on overall gain.

[4 marks]

(e) The engineer designing the circuit realizes that actual measured gain differs significantly from (c). Identify the reason.

[5 marks]

Q.4 (a) (i) Write down the logic function of the pull-down network shown in Figure Q.4.

[5 marks]

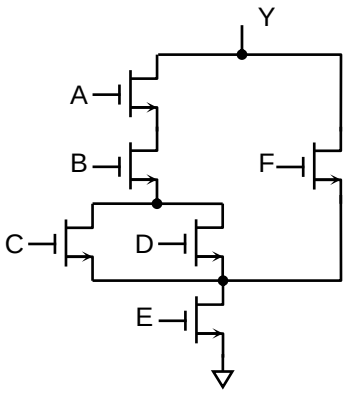


Figure Q.4

(ii) Draw the corresponding pull-up network.

[5 marks]

(iii) Assume that all NMOS transistors in the designed pull-down network have a sizing of $2n$, and the NMOS transistor in the symmetric inverter has a sizing of n. Find the relationship between worst case $t_{pHL,logic}$ and $t_{pHL,inv}$.

[3 marks]

(b)

(i) Propose an opamp-based circuit that can produce cos(ωt) given the input signal as sin(ωt).

[4 marks]

(ii) Propose an opamp-based circuit that will rectify cos(ωt) or sin(ωt).

[4 marks]

(iii) Based on (i) and (ii), propose an opamp-based circuit that can produce a square wave with duty cycle of 0.75, i.e., the positive pulse width is $0.75 \times T_{period}$.

[4 marks]

END OF QUESTIONS

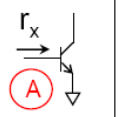
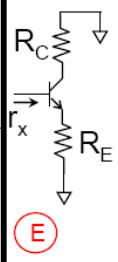
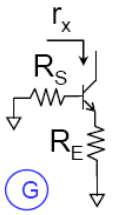
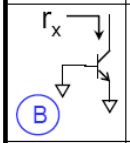
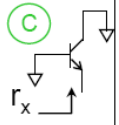
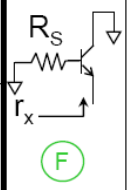
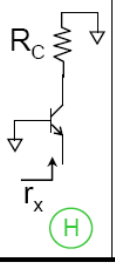
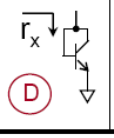
APPENDIX

1. Law of mass action	$p_0 n_0 = n_i^2$
2. Space-charge density	$\rho = e\left(p + N_D^+ - n - N_A^-\right)$
3. Conductivity	$\sigma = e\left(n\mu_n + p\mu_p\right)$
4. Current densities	$J_n = en\mu_n E + eD_n \frac{dn}{dx}$ $J_p = ep\mu_p E - eD_p \frac{dp}{dx}$
5. Einstein Relation	$\frac{D_n}{\mu_n} = \frac{D_p}{\mu_p} = \frac{kT}{e}$
6. Decay of excess minority carrier concentration as a function of time, under low-level injection conditions, where τ is the minority carrier lifetime.	$\delta n(t) = \delta n(0)\exp\left(\frac{-t}{\tau}\right)$ $\delta p(t) = \delta p(0)\exp\left(\frac{-t}{\tau}\right)$
7. Poisson's equation (Gauss's Law)	$\frac{dE}{dx} = -\frac{d^2\phi}{dx^2} = \frac{\rho(x)}{\varepsilon_r \varepsilon_0}$
8. Built-in potential of an abrupt p-n junction diode.	$V_{bi} = \frac{kT}{e}\ln\left(\frac{n_{n0}}{n_{p0}}\right) = \frac{kT}{e}\ln\left(\frac{p_{p0}}{p_{n0}}\right)$ $= \frac{kT}{e}\ln\left(\frac{N_A N_D}{{n_i}^2}\right)$
9. Space-charge region width of an unbiased abrupt pn junction diode.	$W = \left[\frac{2\varepsilon_r \varepsilon_0 V_{bi}}{e}\left(\frac{N_A + N_D}{N_A N_D}\right)\right]^{\frac{1}{2}}$
10. Magnitude of the maximum electric field in an abrupt pn junction diode.	$E_{\max} = \frac{eN_A N_D}{\varepsilon_r \varepsilon_0 (N_A + N_D)} W$

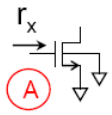
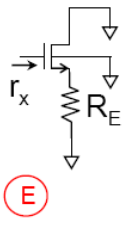
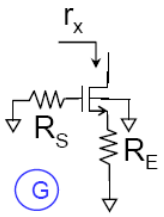
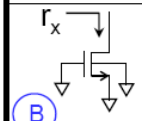
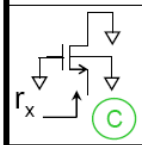
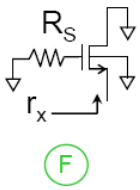
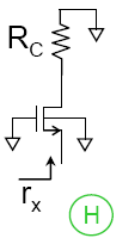
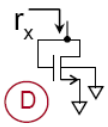
11. Excess carrier concentration with respect to <u>position</u> for a long-base abrupt pn junction diode under low-level injection conditions	$\delta n_p(x') = \delta n_p(0) \cdot \exp\left(-\frac{x'}{L_n}\right)$ $\delta p_n(x'') = \delta p_n(0) \cdot \exp\left(-\frac{x''}{L_p}\right)$
12. Excess carrier concentration at the edges of the space-charge region of an abrupt pn junction diode under low-level injection conditions.	$\delta n_p(0) = n_{p0}\left[\exp\left(\frac{e\,V}{k\,T}\right)-1\right]$ $\delta p_n(0) = p_{n0}\left[\exp\left(\frac{e\,V}{k\,T}\right)-1\right]$
13. Minority carrier diffusion lengths.	$L_n = \sqrt{D_n \tau_n}$ $L_p = \sqrt{D_p \tau_p}$
14. Ideal diode current density-voltage equation for an abrupt, pn junction diode.	$J = J_s\left[\exp\left(\frac{eV_a}{k\,T}\right)-1\right]$, where V_a is the applied voltage, and $J_s = J_{s,p} + J_{s,n}$
14a. For "long" n-type neutral region	$J_{s,p} = e\,\frac{D_p}{L_p}\,p_{n0}$
14b. For "short" n-type neutral region	$J_{s,p} = e\,\frac{D_p}{W_n}\,p_{n0}$
14c. For "long" p-type neutral region	$J_{s,n} = e\,\frac{D_n}{L_n}\,n_{p0}$
14d. For "short" p-type neutral region	$J_{s,n} = e\,\frac{D_n}{W_p}\,n_{p0}$
15. Junction capacitance of an abrupt pn junction diode.	$C_j = \frac{\varepsilon_0 \varepsilon_{r(Si)} A}{W}$
16. Incremental resistance of a pn junction diode	$r_d = \frac{V_t}{I_Q}$
17a. Emitter injection efficiency of an **npn** bipolar junction transistor (short base and long emitter)	$\gamma = \frac{I_{En}}{I_E} = \frac{1}{1 + \frac{D_E}{D_B}\frac{x_B}{L_E}\frac{N_B}{N_E}}$

17b. Emitter injection efficiency of an **npn** bipolar junction transistor (short base and short emitter)	$\gamma = \frac{I_{En}}{I_E} = \frac{1}{1+\frac{D_E}{D_B}\frac{x_B}{x_E}\frac{N_B}{N_E}}$
18a. Base transport factor of an **npn** bipolar transistor (general definition)	$\alpha_T = \frac{I_{Cn}}{I_{En}}$
18b. Base transport factor of an **npn** bipolar transistor (short base)	$\alpha_T = 1 - \frac{1}{2}\left(\frac{x_B}{L_n}\right)^2$
Note : For **pnp** bipolar transistors, interchange the roles of the electrons and holes.	
19. Common base current gain of a bipolar junction transistor	$\alpha = \frac{I_C}{I_E}$
20. Common emitter current gain of a bipolar junction transistor.	$\beta = \frac{I_C}{I_B} = \frac{\alpha}{1-\alpha}$
21. Gate oxide capacitance of a MOSFET (per unit area of the capacitor)	$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}} = \frac{\varepsilon_o \times \varepsilon_{r(SiO_2)}}{t_{ox}}$
22. Drain current in the linear region of an n-channel MOSFET	$I_D = 2K_n\left[(V_G - V_{TH})V_D - \frac{1}{2}V_D^2\right]$
23. Drain current in the saturation region of an n-channel MOSFET	$I_D = K_n(V_G - V_{TH})^2$
24. Transconductance of a MOSFET	$g_m \equiv \frac{dI_D}{dV_G}$

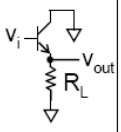
BJT DP Summary (Table 1)

Conf	DP r_x	Conf	DP r_x	Conf	DP r_x
	$\frac{\beta}{g_m}$		$r_\pi + (1+\beta)R_E$ $\approx r_\pi(1+g_m R_E)$		$r_o\left\{1+g_m\left[(r_\pi+R_S)\,//\,R_E\right]\left(\frac{r_\pi}{r_\pi+R_S}\right)\right\}$ *If* $R_S=0$ *and* $r_\pi \ll R_E$ $\Rightarrow r_{x,\max}=r_o(\beta+1)$
	$\frac{V_A}{I_C}$				
	$\frac{1}{g_m}$		$\frac{R_S+r_\pi}{1+\beta}\,//\,r_o$ $\approx \frac{R_S}{1+\beta}+\frac{1}{g_m}$		$\frac{1}{g_m}\times\frac{r_o+R_C}{r_o+R_C/\beta}$
	$\frac{1}{g_m}$				

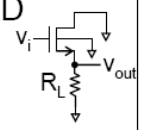
MOS DP Summary (Table 2)

Conf	DP r_x	Conf	DP r_x	Conf	DP r_x
	∞		∞		$r_o\left[1+(g_m-g_{mb})R_E\right]$
	$\frac{1}{\lambda I_D}$				
	$\frac{1}{g_m-g_{mb}}$		$\frac{1}{g_m-g_{mb}}$		$\frac{1}{g_m-g_{mb}}\times\frac{r_o+R_C}{r_o}$
	$\frac{1}{g_m}$				

BJT Summary (Table 3)

BJT	G_m	A_V
CE (A)	g_m	Derive Based on 2-ports Network
CB (B)	$-g_m$	Derive Based on 2-ports Network
CC (C) 	Not Applicable	$\frac{g_m R_L}{1+g_m R_L}$
CE with Emitter Degeneration (D)	$\frac{g_m}{1+g_m R_E}$	Derive Based on 2-ports Network

MOS Summary (Table 4)

MOS	G_m	A_V
CS (A)	g_m	Derive Based on 2-ports Network
CG (B)	$-(g_m - g_{mb})$ *Drop g_{mb} if no body effect*	Derive Based on 2-ports Network
CD (C) 	Not Applicable	$\frac{g_m R_L}{1+(g_m - g_{mb})R_L} \approx \frac{g_m}{g_m - g_{mb}}$ *Drop g_{mb} if no body effect*
CS with R_E (D)	$\frac{g_m}{1+(g_m - g_{mb})R_E}$ *Drop g_{mb} if no body effect*	Derive Based on 2-ports Network

1) Logic Gates:

For K transistor in series:

$$\left(\frac{W}{L}\right)_{eq} = \left[\left(\frac{W}{L}\right)_1^{-1} + \left(\frac{W}{L}\right)_2^{-1} + \cdots + \left(\frac{W}{L}\right)_K^{-1}\right]^{-1}$$

For K transistor in parallel:

$$\left(\frac{W}{L}\right)_{eq} = \left(\frac{W}{L}\right)_1 + \left(\frac{W}{L}\right)_2 + \cdots + \left(\frac{W}{L}\right)_K$$

2) MOSFET Equation:

$$I_{DN} = K_N\left(V_{GS} - V_{THN}\right)^2 = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_N\left(V_{GS} - V_{THN}\right)^2 \qquad if \qquad V_{DS} > V_{GS} - V_{THN}$$

$$I_{DN} = 2K_N\left[\left(V_{GS} - V_{THN}\right)V_{DS} - \frac{V_{DS}^2}{2}\right] \quad if \qquad V_{DS} > V_{GS} - V_{THN}$$

$$I_{DP} = K_P\left(\left|V_{GS}\right| - \left|V_{THP}\right|\right)^2 = \frac{1}{2}\mu_p C_{ox}\left(\frac{W}{L}\right)_P\left(\left|V_{GS}\right| - \left|V_{THP}\right|\right)^2 \qquad if \qquad \left|V_{DS}\right| > \left|V_{GS}\right| - \left|V_{THP}\right|$$

$$I_{DP} = 2K_P\left[\left(\left|V_{GS}\right| - \left|V_{THP}\right|\right)\left|V_{DS}\right| - \frac{V_{DS}^2}{2}\right] \quad if \qquad \left|V_{DS}\right| > \left|V_{GS}\right| - \left|V_{THP}\right|$$

$$g_{mn} = \sqrt{4K_N I_{DN}} \qquad r_{on} = \frac{1}{\lambda_n I_{DN}} \qquad g_{mp} = \sqrt{4K_P I_{DP}} \qquad r_{op} = \frac{1}{\lambda_p I_{DP}}$$

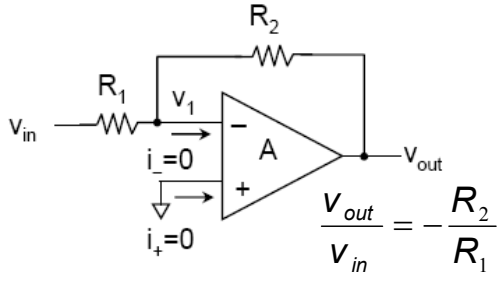
2) BJT Equation:

$$I_C = \beta I_B = \frac{\beta I_E}{\beta + 1} \qquad I_C = I_S e^{\frac{V_{BE}}{V_T}}$$

$$g_m = \frac{I_C}{V_T} \qquad r_o = \frac{V_A}{I_C}$$

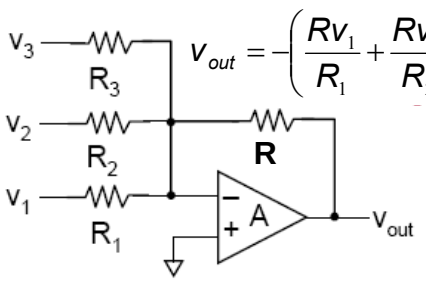
3) Opamp Circuits:

Inverting Amplifier



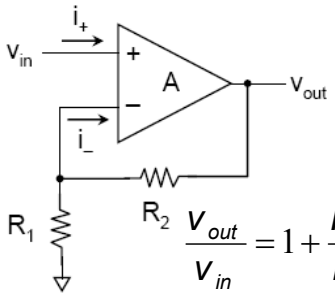
$$\frac{v_{out}}{v_{in}} = -\frac{R_2}{R_1}$$

Summing Amplifier



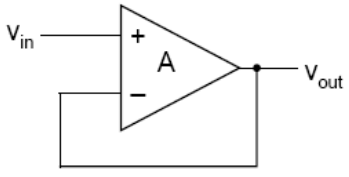
$$v_{out} = -\left(\frac{Rv_1}{R_1} + \frac{Rv_2}{R_2} + \frac{Rv_3}{R_3}\right)$$

Non-inverting Amplifier



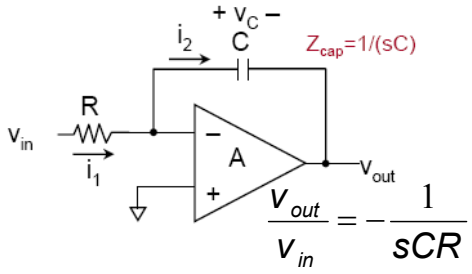
$$\frac{v_{out}}{v_{in}} = 1 + \frac{R_2}{R_1}$$

Buffer



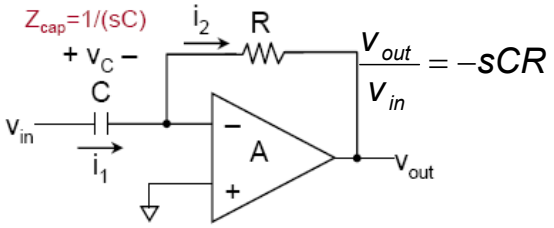
$$\frac{v_{out}}{v_{in}} = 1$$

Integrator



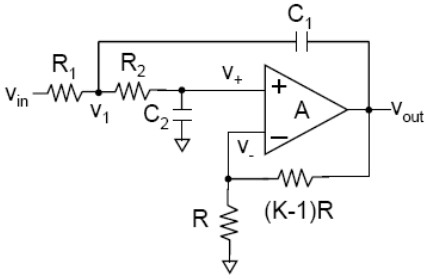
$$\frac{v_{out}}{v_{in}} = -\frac{1}{sCR}$$

Differentiator



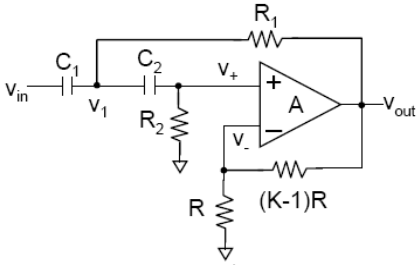
$$\frac{v_{out}}{v_{in}} = -sCR$$

SK Lowpass Filter



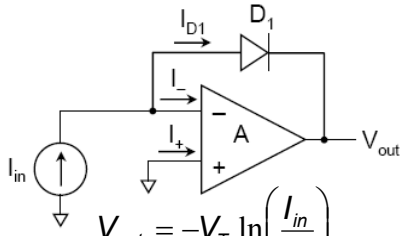
$$\frac{v_{out}}{v_{in}} = \frac{\frac{K}{C_1C_2R_1R_2}}{s^2 + s\left(\frac{1}{C_1R_1} + \frac{1}{C_2R_2} + \frac{1}{C_1R_2} - \frac{K}{C_2R_2}\right) + \frac{1}{C_1C_2R_1R_2}} = \frac{H_o\omega_o^2}{s^2 + \frac{\omega_o}{Q}s + \omega_o^2}$$

SK Highpass Filter



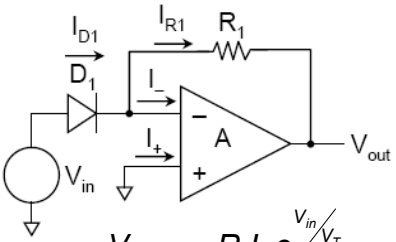
$$\frac{v_{out}}{v_{in}} = \frac{Ks^2}{s^2 + s\left(\frac{1}{C_2R_2} + \frac{1}{C_1R_2} + \frac{1}{C_1R_1} - \frac{K}{C_1R_1}\right) + \frac{1}{C_1C_2R_1R_2}} = \frac{H_os^2}{s^2 + \frac{\omega_o}{Q}s + \omega_o^2}$$

Logarithm Amplifier



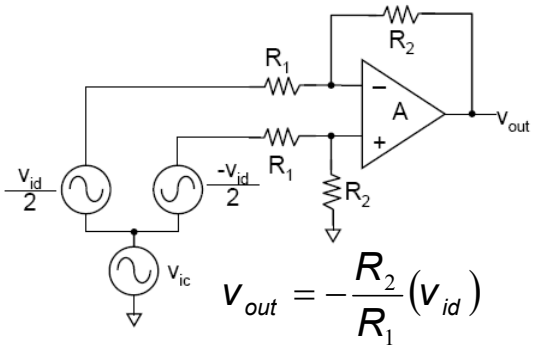
$$V_{out} = -V_T \ln\left(\frac{I_{in}}{I_S}\right)$$

Exponential Amplifier



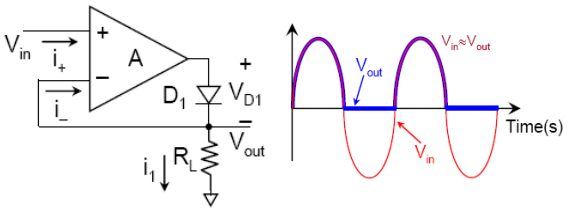
$$V_{out} = -R_1 I_S e^{V_{in}/V_T}$$

Instrumentation Amplifier

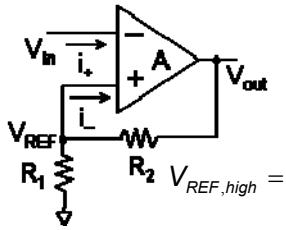


$$v_{out} = -\frac{R_2}{R_1}(v_{id})$$

Super Diode



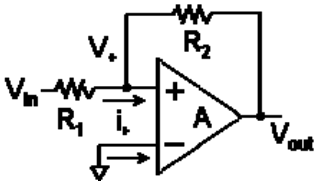
Inverting Comparator with Hysteresis



$$V_{REF,high} = \frac{R_1}{R_1 + R_2} \times V_{DD}$$

$$V_{REF,low} = \frac{R_1}{R_1 + R_2} \times (-V_{DD})$$

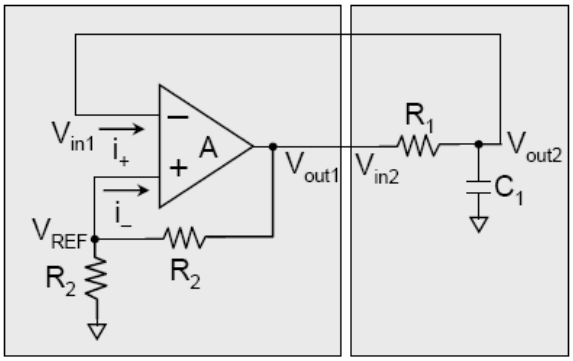
Comparator with Hysteresis



$$V_{REF,low} = -\frac{R_1}{R_2} V_{DD}$$

$$V_{REF,high} = \frac{R_1}{R_2} V_{DD}$$

Bistable Multivibrator



$$T = 2C_1R_1 \ln(3)$$

END OF PAPER