∆NATIONAL UNIVERSITY OF SINGAPORE

Department of Electrical and Computer Engineering

EE2021: Tutorial 2 (*pn* Junction)

<u>Homework 1</u>:

Homework 1 is Question 2 of Tutorial 2 and you will need to submit a hand-written, hardcopy in class <u>on Wednesday, 11 Feb 2015.</u>

- Unless otherwise stated, you may assume temperature, $T = 300$ K, $V_T = 0.025$V, and make use of the equations given in the lecture notes directly, without having to derive them. Assume that all the symbols are as defined in the lecture notes.

1. Calculate the parameters in the table below for the following 3 silicon *pn* junction diodes (junction area, $A = 1$ mm^2) under no applied external voltage condition, at $T = 300$K. N_A is the net acceptor doping on the p-type side, and N_D is the net donor doping on the n-type side. It is given that $n_i = 1.5 \times 10^{10}$ cm^{-3} for silicon at 300 K.

Diode	N_A / cm^{-3}	N_D / cm^{-3}	V_o / V	W_{dep} / µm	x_p / µm	x_n / µm
A	5×10^{15}	5×10^{15}				
B	5×10^{15}	5×10^{17}				
C	5×10^{17}	5×10^{17}				

Comment on how the above answers vary with the net doping concentrations of the *p* and *n* regions, N_A and N_D, respectively.

[Ans. For Diode A: $V_o = 0.636$ V, $W_{dep} = 0.574$ µm, $x_p = x_n = 0.287$ µm]

2. Consider a Si substrate with an initial doping of 3×10^{15} cm^{-3} of donors (Region 1). A pn junction is made in the Si substrate by doping a selected region (Region 2) with an additional 8×10^{15} cm^{-3} of acceptors, as shown in Fig. Q2.1. The temperature, T = 300 K, the intrinsic carrier concentration in Si, n_i = 1.5×10^{10} cm^{-3} and the thermal voltage, V_T = 0.025 V.

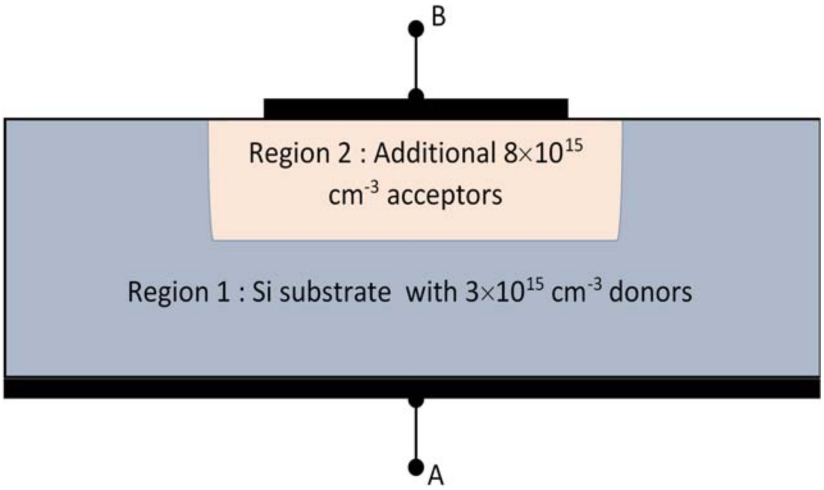

Fig. Q2.1

(a) In the Si substrate (Region 1), what are the majority carriers (i.e., electrons or holes?) and what are the minority carriers? What are the respective concentrations of the majority carriers and the minority carriers?

[4 marks]

(b) In Region 2, what are the majority carriers and the minority carriers ? What are their respective concentrations?

[6 marks]

(c) What is the built-in voltage V_0 of the pn junction?

[2 marks]

(d) Under the reverse bias condition, which of the two terminals (A and B) is at s higher voltage with respect to the other?

[2 marks]

(e) In Fig Q2.2 below, sketch the <u>respective minority carrier distributions</u> in the neutral p-region and n-region of the pn junction (i.e., where $x < -x_p$ and $x > x_n$) under a <u>reverse bias of 1 V</u> and indicate their concentrations at the boundaries of the neutral regions. The depletion region of the pn junction extends from $x = -x_p$ to $x = x_n$). You can assume that the neutral regions in the pn junction to be much longer than the respective minority carrier diffusion lengths.

[6 marks]

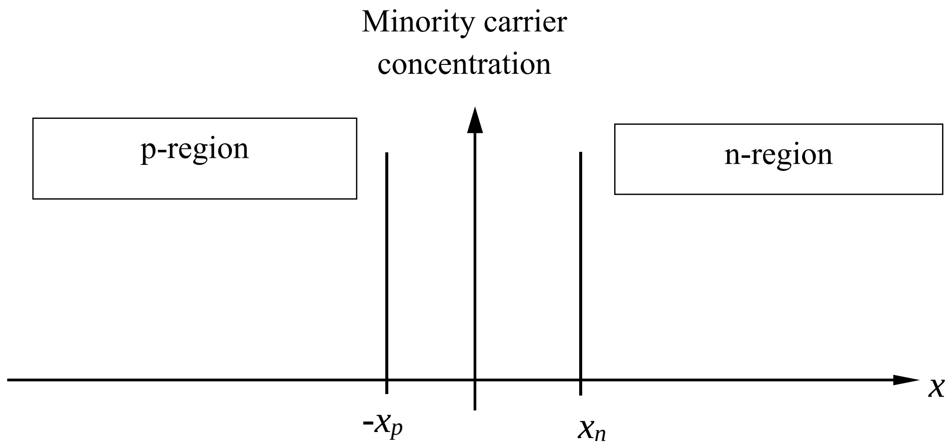

Fig. Q2.2

3. Figure Q3 shows a circuit consisting of a voltage source V_{DD}, two resistors R_1, R_2 and a Zener diode, which breaks down at a reverse voltage $V_Z = 6$ V. For reverse voltages less than V_Z, the reverse saturation current of the diode is negligible.

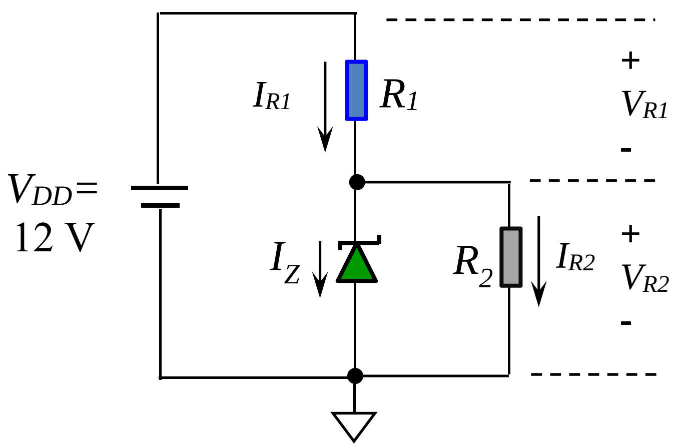

Fig. Q3

(a) Consider the case where $R_1 = 10$ kΩ and $R_2 = 2$ kΩ. *Assume* that the Zener diode is NOT operating in the breakdown region.

(i) Calculate the voltage V_{R2} across the Zener diode. Hence check whether the assumption that the Zener diode is NOT operating in the breakdown region is correct.
(ii) Calculate the voltages V_{R1} and the currents I_{R1}, I_{R2}, I_Z.

(b) Consider the case where R_1 = 2 kΩ and R_2 = 4 kΩ. Is the assumption that the Zener diode is NOT operating in the breakdown region valid in this case?

Determine the voltages V_{R1}, V_{R2} and the currents I_{R1}, I_{R2}, I_Z.

[Ans. (a) 2 V, 10 V, 1 mA, 1 mA, 0; (b) 6 V, 6 V, 3 mA, 1.5 mA, 1.5 mA]

4. The current (*I*) flowing through a semiconductor pn junction diode at various forward bias voltages (*V*) are measured and tabulated as follows:

V (V)	I (A)
0.00	0.00
0.10	~0.00
0.20	~0.00
0.30	~0.00
0.40	~0.00
0.50	4.70×10^{-5}
0.55	3.70×10^{-4}
0.60	2.52×10^{-3}
0.62	5.91×10^{-3}
0.64	1.38×10^{-2}
0.66	2.73×10^{-2}
0.68	6.40×10^{-2}
0.70	1.51×10^{-1}

(a) Plot the *I-V* characteristic of the diode from V = 0 to 0.7 V, and estimate the cut-in voltage of the diode.

(b) The *I-V* characteristic of the semiconductor diode is given as follows:

$$I = I_S\left(e^{V/V_T} - 1\right), \text{ where } V_T = 0.025\text{V}.$$

Estimate the value of the reverse saturation current (I_S) by devising a suitable plot between *I* and *V* in forward bias.

Take note that the values of *I* in the above table are measured, and are therefore likely to have experimental errors. Hence, one will not estimate I_S by applying a single set of *I* versus *V* values from the table to the above equation, as that will not be accurate. Also, different sets of *I* versus *V* values are likely to give different I_S.

[Hint: The range of voltage (V) of the plot to be devised is an important consideration, and you need to transform the above equation into the form of $y = mx + C$, i.e., a linear relation between y and x, where m and C are constants.]

(c) Consider the above diode where there is the series resistance, r_s, of the neutral p and n neutral regions. If, in a practical diode, r_s is 10 Ω, find the voltage drops across r_s using the currents at various voltages given in the table in part (a) when the voltage across the pn junction is 0.5, 0.6 and 0.7 V. Comment on your results. What are the actual voltages that would need to be applied to the real diode with r_s to have the same currents?

(d) Based on your calculations in part (c), discuss the effect on the I-V characteristic of the diode due to r_s.

[Ans: (a) 0.6 V, (b) $9.36\times10^{-14} \sim 10^{-13}$ A, (c) ~0.5 V, 0.6252 V and 2.21 V]

5. For the circuit shown in Fig. Q5, V_{DD} = 7 V and R = 3.3 kΩ, while the diode has parameters of I_s = 57.8 pA, and n = 1.56.

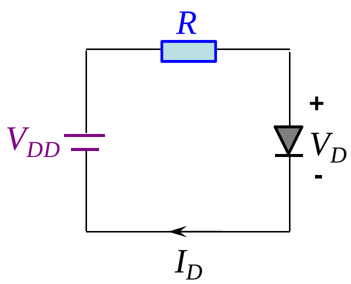

Fig. Q5

(a) Using the iteration method, find the values of I_D and V_D.

(b) In order to simplify the calculation, it is suggested to replace the diode in the circuit by a piecewise linear model which has parameters V_{DO} and r_D. Find appropriate values for V_{DO} and r_D if we wish the model to be accurate over the range of I_D from 1 mA to 3 mA.

[Hint: Use equation (2.41) of the pn-junction lecture notes, solve for 2 unknowns using 2 sets of (I,V) data.]

(c) Repeat the calculation for I_D and V_D in the circuit using the piecewise-linear model instead of the iteration method.

(d) Reflection:

(i) What is the error incurred in using the piecewise linear model?

(ii) How does the current range we use to determine V_{DO} and r_D influence the accuracy of the model?

(iii) The value of V_{DD} in the circuit is now changed to 1 V. If the model with the same parameter values is used to calculate I_D and V_D, would you expect the accuracy of the model to change? And why?

6. For the circuit shown in Fig. Q6, there are two current sources that supply currents of 101I and I, respectively, and two diodes D1 and D2. The I-V characteristics of D1 and D2 are given as follows:

$$I_{D1} \cong I_S e^{V_{D1}/V_T} \quad \text{and} \quad I_{D2} \cong 5 \times I_S e^{V_{D2}/V_T}\text{, respectively.}$$

(a) In the context of the circuit of Fig. Q6, what are the assumptions made to obtain the above 2 approximate diode equations?

(b) Note that the saturation current of D2 is 5 times that of D1. Suggest possible ways to achieve that.

(c) Obtain an expression for V_{OUT} in terms of I, $R1$ and V_T.

(d) If $R1=R0\times(1+0.02\times T)$, where T is the absolute temperature, specify the $R0$ and I relationship such that V_{OUT} is temperature independent, i.e. V_{OUT} remains constant while temperature changes.

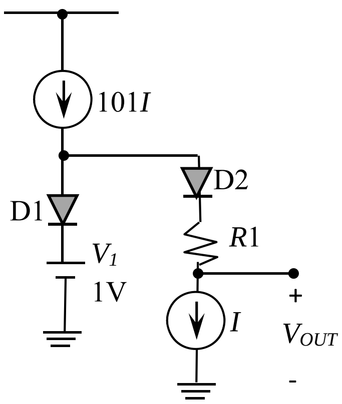

Fig. Q6