NATIONAL UNIVERSITY OF SINGAPORE
Department of Electrical and Computer Engineering

EE2021 : Tutorial 3 : Solutions

- Unless otherwise stated, you may assume temperature, $T = 300$ K, thermal voltage, $V_T = 0.025$ V, and silicon intrinsic carrier concentration, $n_i = 1.5 \times 10^{10}$ cm^{-3} and make use of the equations given in the lecture notes directly, without having to derive them.
- All the symbols are as defined in lecture notes.

Homework 2:
Homework 2 is Question 1 and Question 6 of Tutorial 3 and you will need to submit it in class on Wednesday 4 March 2015.

Q1. (a) An npn bipolar junction transistor has been designed with the following parameters:

Doping in the emitter, $N_{DE} = 10^{18}$ cm^{-3},
Doping in the base, $N_{AB} = 2\times10^{16}$ cm^{-3},
Diffusion coefficient of holes in the emitter, $D_p = 1$ cm^2/s,
Diffusion coefficient of electrons in the base, $D_n = 10$ cm^2/s,
Diffusion length of holes in the emitter, $L_p = 0.300$ μm,
Diffusion length of electrons in the base, $L_n = 20$ μm,
Width of the neutral region in the base, $w_B = 1$ μm.

Calculate the collector saturation current density, J_S, and the common emitter current gain, β, of the transistor. [4 marks]

(b) The transistor in part (a) is required to have a collector current $I_C = 2.5$ mA when it is operating in the forward active region at 300 K with $V_{BE} = 0.65$ V. The Early effect can be assumed to be negligible.

What is the additional design parameter that needs to be specified, and what should be the value of that parameter? [4 marks]

(c) It is desired to increase the β of the transistor in part(a) to 300 by adjusting one of the above design parameters. Assume that the base doping and the width of the neutral base region, as well as the electron and hole diffusion lengths, remain unchanged. Suggest a change in the design that would achieve the objective. [2 marks]

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1. (a) The collector current density,

$$J_S = q\frac{D_n}{w_B}\frac{n_i^2}{N_{AB}} = 1.602\times10^{-19}\times\frac{10}{1\times10^{-4}}\times\frac{\left(1.5\times10^{10}\right)^2}{2\times10^{16}} = 1.80\times10^{-10}\ \text{A cm}^{-2}.$$

[2 marks]

The common emitter current gain

$$\beta = \frac{D_n}{D_p}\frac{L_p}{w_B}\frac{N_{DE}}{N_{AB}} = \frac{10}{1}\times\frac{0.3\times10^{-4}}{1\times10^{-4}}\times\frac{1\times10^{18}}{2\times10^{16}} = 150.$$

[2 marks]

(b) The additional design parameter is the cross-sectional area of the transistor, A.

[1 mark]

When the transistor is operating in the forward active region at 300 K with V_{BE} = 0.65 V, the collector current

$$I_C = I_S \exp\left(\frac{V_{BE}}{V_T}\right) = AJ_S \exp\left(\frac{V_{BE}}{V_T}\right) = A\times1.80\times10^{-10}\times\exp\left(\frac{0.65}{0.025}\right) = A\times35.3.$$

$$A = \frac{I_C}{35.3} = \frac{2.5\times10^{-3}}{35.3} = 7.08\times10^{-5}\ \text{cm}^2.$$

[3 marks]

(c) The ratio of the dopings in the emitter and the base needs to be increased. Since the value of is to be doubled, and the base doping is to remain unchanged, the emitter doping would need to be increase by a factor of 2. i.e.,

$N_{DE} = 2\times10^{18}$ cm^{-3}. [2 marks]

Q2. The schematic cross section of a silicon **pnp** bipolar junction transistor (BJT) is shown in Fig. Q2. The doping concentrations of the emitter, base and collector are respectively, $N_{AE} = 2\times10^{19}$ cm^{-3}, $N_{DB} = 5\times10^{17}$ cm^{-3} and $N_{AC} = 5\times10^{15}$ cm^{-3}. You may assume that the emitter, base and collector are each uniformly doped.

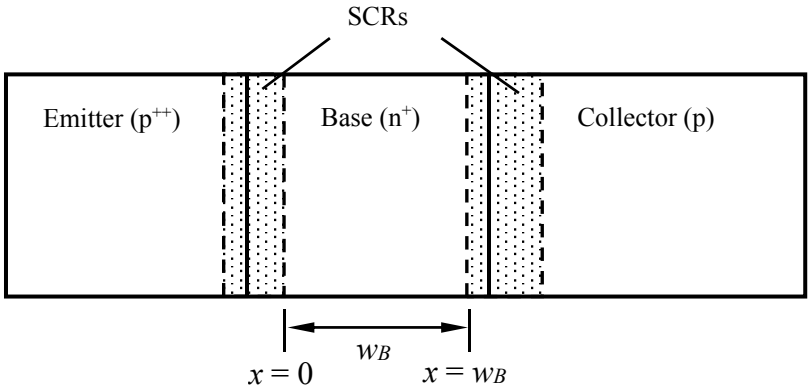

Fig. Q2 : Schematic cross-section of a **pnp** BJT.

The transistor is biased in the forward active mode with an emitter-base junction voltage, $V_{EB} = 0.67$ V, and a collector-base junction voltage, $V_{CB} = -2$ V. At these conditions, the width of the neutral part of the base, $w_B = 1$ μm. In the base, the diffusivity of the holes (minority carriers), $D_p = 9$ cm^2 s^{-1}, and the diffusion length of the holes, $L_p = 30$ μm. The cross-sectional area of the transistor, $A = 10^{-4}$ cm^2.

(a) Calculate the concentrations of the holes (minority carriers) at the edges of the space charge regions (SCRs) in the base, i.e., at $x = 0$ and $x = w_B$.

(b) Calculate the magnitude of the collector current. State and justify any approximation that you have used in the calculation.

(c) Discuss (without performing calculations)

(i) whether there is an increase, a decrease, or no change, in the collector current, compared to that in part (b), when V_{CB} is changed to - 5 V from -2 V;
(ii) whether there is an increase, decrease, or no change in the collector current, compared to that in part (b), when the doping in the collector is changed from 5×10^{15} cm^{-3} to 5×10^{17} cm^{-3}. $V_{CB} = -2$ V.

[Hint: observe the trend of the widths of the space-charge regions in Tutorial 2, Question 1.]

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2. (a) The equilibrium minority carrier (hole) concentration in the base

$$p_{n0} = \frac{n_i^2}{n_{n0}} = \frac{n_i^2}{N_{DB}} = \frac{\left(1.5\times10^{10}\right)^2}{5\times10^{17}} = 4.5\times10^2 \text{ cm}^{-3}.$$

$$\text{At } x = 0,\ p_n(0) = p_{n0}e^{V_{EB}/V_T} = 4.5\times10^2 \times e^{0.67/0.025} = 1.96\times10^{14} \text{ cm}^{-3}.$$
$$\text{At } x = w_B,\ p_n(w_B) = p_{n0}e^{V_{CB}/V_T} = 4.5\times10^2 \times e^{-2/0.025} = 0 \text{ cm}^{-3}.$$

(b)

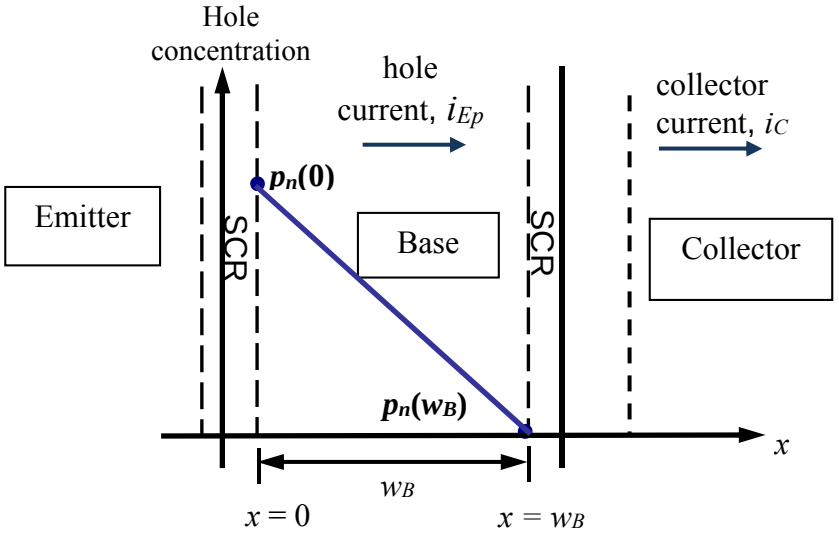

Fig. 2(b) : Hole concentration profile in the base (schematic, not to scale)

The minority carrier (hole) diffusion length in the base,

$L_p = 30\ \mu m >> w_B = 1\ \mu m$.

As the width of the neutral base (w_B) is much less than the minority carrier diffusion length (L_p), there is negligible recombination of the minority carriers as they diffuse through the base. The concentration profile of the minority carriers can therefore be assumed to be practically a straight line (as a result of constant rate of diffusion).

The collector current is due to the diffusion of the minority carriers (holes) through the base. The magnitude of the collector current,

$$|i_C| \approx |i_{Ep}| = \left| -qAD_p \frac{dp_n(x)}{dx} \right| = \left| -qAD_p \frac{p_n(0) - p_n(w_B)}{0 - w_B} \right|$$

$$= \left| -1.602\times10^{-19} \times 10^{-4} \times 9 \times \frac{1.96\times10^{14} - 0}{0 - 1\times10^{-4}} \right| = 2.83\times10^{-4}\ \text{A}.$$

(c) (i) V_{CB} is changed from -2 V to - 5 V.

The increase in the magnitude of the reverse bias at the collector-base junction will not change the minority carrier concentration at $x = w_B$, which is already zero. The reverse bias will cause the SCR at the base-collector junction to widen, which will then make the width of the neutral base region slightly shorter (see Fig. 2(c) below). This will lead to a slight increase in the gradient of the minority carrier concentration, $dp_n(x)/dx$, thus resulting in a slight increase of the collector current. This is called **base-width modulation effect**, also known as the **Early effect**.

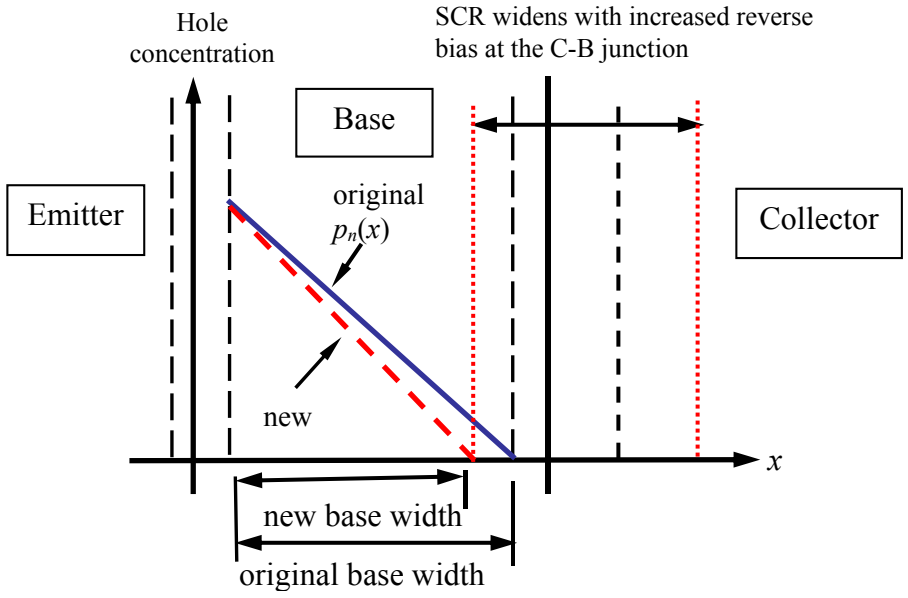

Fig. 2(c) : Hole concentration profile in the base (schematic, not to scale), when the reverse bias in the collector-base junction is increased.

(ii) When the doping in the collector is changed from 5×10^{15} cm^{-3} to 5×10^{17} cm^{-3}.

When $N_{DB} = 5\times10^{17}$ cm^{-3} and $N_{AC} = 5\times10^{15}$ cm^{-3}, the doping in the collector is 100 times less than that in the base. The SCR (also called depletion region) at the collector-base junction is predominantly on the collector side. (Refer to Q.1 of Tutorial 2). When the doping in the collector is increased to $N_{AC} = 5\times10^{17}$ cm^{-3}, there is a reduction in the overall width of the SCR, but the SCR width is now equally divided between the base and the collector. The SCR width in the base (x_n) is larger than that in part (b). Although the SCR widths x_n and x_p in Q1, Tutorial 2 are calculated for a p-n junction without an external bias, the ratio x_n / x_p is the same when a bias is applied to the p-n junction.

When a reverse bias is applied to the collector-base junction, the SCR will now extend equally into the base and the collector, instead of mostly into the collector as in part (b). There will thus be a greater reduction in the width of the neutral base region, and hence a greater base-width modulation effect. There will be a larger increase of the collector current for a given reverse bias of the collector-base junction. This is one reason why the collector is generally more lightly doped than the base.

Q3. Two BJT circuits are shown in Figure Q3. The transistor, Q_1, in both circuits has $\beta = 100$ and $V_A = 100$ V. You may assume $I_{R1} \approx I_{R2} >> I_B$ for both cases.

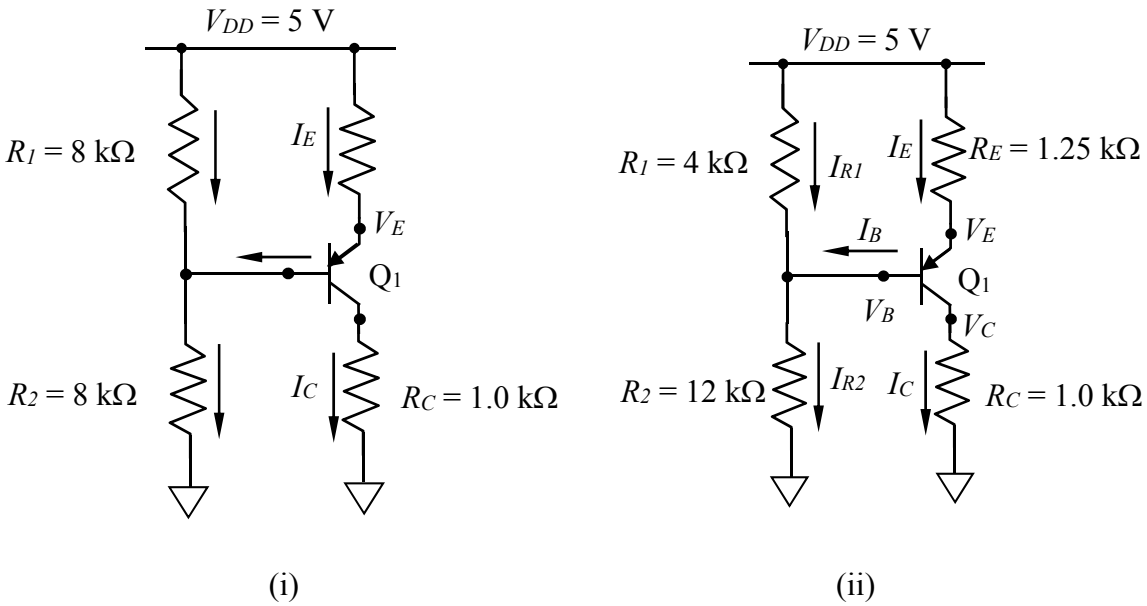

Fig. Q3

(a) When a BJT is operating in the forward active mode, the typical value assumed for the base-emitter junction voltage is 0.7 V. Is this assumption reasonable? Explain.

(b) Using the assumption of part (a), determine the collector current, I_C, for the circuit shown in Fig. Q3(i).

(c) Repeat the calculation of part (b) for the circuit shown in Fig. Q3(ii).

(d) If the actual value of the base-emitter junction voltage of the BJT is 0.8 V, what are the percentage errors incurred in the calculation of I_C in part (b) and part (c), respectively?

(e) Based on the results of part (d), discuss the implications of the assumed value of the base-emitter junction voltage of 0.7 V. Can this be resolved using the Thevenin equivalent for the base biasing circuit instead of the assumption of $I_{R1} \approx I_{R2} >> I_B$?

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3. (a) In forward active mode, the base-emitter junction is forward biased and for a forward biased junction, the voltage across the *pn* junction typically ranges from 0.6 – 0.8 V, hence the assumption of 0.7 V is reasonable.

(b) BJT is of the pnp type, $V_{EB} \cong 0.7$ V.

Assuming $I_{R1} \approx I_{R2} >> I_B$,

$$V_B \cong \frac{R_2}{R_1+R_2} V_{DD} = \frac{8k}{8k+8k} \times 5 = 2.5 \text{ V}$$

$$V_E = V_B + V_{EB} \cong 2.5 + 0.7 = 3.2 \text{ V}$$

$$I_E = \frac{V_{DD}-V_E}{R_E} = \frac{5-3.2}{1.25k} = 1.44 \text{ mA}$$

$$I_C = \frac{\beta}{(\beta+1)} I_E = 1.43\ mA \quad (\text{or } I_C \cong I_E = 1.44 \text{ mA})$$

Check:

$$I_B = \frac{I_E}{(\beta+1)} = 0.0143 \text{ mA} = 14.3 \text{ μA} << I_{R1} \cong I_{R2} = \frac{V_{DD}}{R_1+R_2} = 0.31 \text{ mA}.$$

(c) Assuming $I_{R1} \approx I_{R2} >> I_B$,

$$V_B \cong \frac{R_2}{R_1+R_2} V_{DD} = \frac{12k}{4k+12k} \times 5 = 3.75 \text{ V}$$

$$V_E = V_B + V_{EB} \cong 3.75 + 0.7 = 4.45 \text{ V}$$

$$I_E = \frac{V_{DD}-V_E}{R_E} = \frac{5-4.45}{1.25k} = 0.44 \text{ mA}$$

$$I_C = \frac{\beta}{(\beta+1)} I_E = 0.436 \text{ mA} \quad (\text{or } I_C \cong I_E = 0.44 \text{ mA})$$

Check:

$$I_B = \frac{I_C}{\beta} = 4.36\ \mu\text{A} << I_{R1} \cong I_{R2} = \frac{V_{DD}}{R_1+R_2} = 0.31\ \text{mA}$$

(d) **Circuit (i)**: With $V_{EB} = 0.8$ V

$$V_E = V_B + V_{EB} = 2.5 + 0.8 = 3.3\ \text{V}$$

$$I_E = \frac{V_{DD}-V_E}{R_E} = \frac{5-3.3}{1.25k} = 1.36\ \text{mA}$$

$$I_C = \frac{\beta}{(\beta+1)} I_E = 1.35\ \text{mA}$$

Percentage error in $I_C = \frac{1.43-1.35}{1.35} = 5.93\%$.

Circuit (ii): With $V_{EB} = 0.8$ V

$$V_E = V_B + V_{EB} = 3.75 + 0.8 = 4.55\ \text{V}$$

$$I_E = \frac{V_{DD}-V_E}{R_E} = \frac{5-4.55}{1.25k} = 0.36\ \text{mA}$$

$$I_C = \frac{\beta}{(\beta+1)} I_E = 0.356\ \text{mA}$$

Percentage error in $I_C = \frac{0.436-0.356}{0.356} = 22.47\%$

(e) Percentage error in I_C for circuit (i) is only 5.93% (< 10%), hence the assumed value of $V_{EB} \approx 0.7$ V is good enough.

Percentage error in I_C for circuit (ii) is 22.4 % (> 10%), which is too high, hence the assumed value of $V_{EB} \approx 0.7$ V is not good enough.

The above difference is caused by a **low** V_E with respect to V_{DD} (4.55 – 5 = - 0.55 V) for circuit (ii), which has a magnitude close to $V_{EB} \approx 0.7$ V. Hence, a 0.1 V error in V_{EB} can cause a large percentage change in V_E with respect to V_{DD}, which in turn translates to a large percentage change in I_E (or I_C).

Circuit (ii), in comparison to circuit (i), highlights that when V_E (with respect to V_{DD}) has a magnitude comparable to 0.7 V, it is not accurate to assume $|V_{BE}| = 0.7$ V in the calculation. The use of Thevenin equivalent cannot resolve the issue. In such cases, an accurate value for $|V_{BE}|$ is needed and can only be found by an exact solution, i.e., using an iterative method.

Q4. An n-channel MOSFET M_1 is connected as shown in Fig. 4a to perform I_D - V_{GS} measurements. The V_{GS} is changed by varying V_{DD} and the resulting I_D is measured through an current meter.

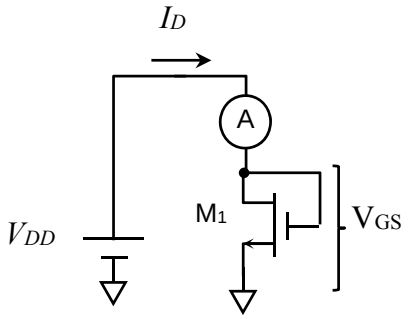


Fig. 4a

(a) Show that the transistor M_1 is operating in saturation region.

(b) The measured I_D - V_{GS} characteristic is shown in Fig. 4b. Also shown is the corresponding tabulated data. Due to experimental error, the measured points do not exactly follow the square law predicted by the drain current equation in the saturation region, i.e., $I_D = K_n (V_{GS}-V_{THN})^2$. Transform the drain current equation and devise a way such that you can easily extract the device parameters K_n and V_{THN}, which is the threshold voltage of the n-channel MOSFET. (Hint: Transform the drain current equation such that it follows a straight line equation format, such as $y = mx+C$.)

V_{GS} (V)	I_D (mA)
1.3	0.61
1.5	1.00
1.7	2.03
1.9	3.11
2.1	4.44
2.3	5.63
2.5	7.43
2.7	9.04
2.9	11.66
3.1	12.95
3.3	15.04
3.5	18.33
3.7	21.23
3.9	24.0

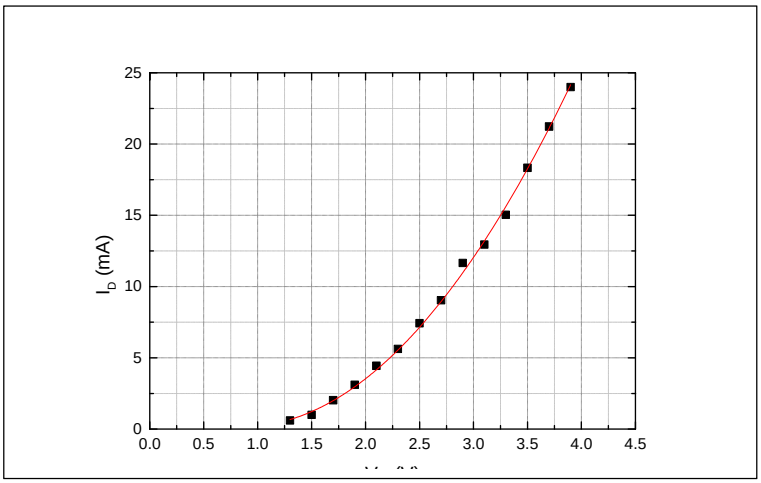


Fig. 4b

(c) Assuming that V_{THN} is unchanged, describe three ways of increasing K_n in the design of the MOSFET.

4. (a) In the circuit, $V_{DS} = V_{GS}$. For an n-channel MOSFET, $V_{THN} > 0$.

Therefore, $V_{DS} > V_{GS} - V_{THN}$.

Hence the MOSFET is operating in the saturation region.

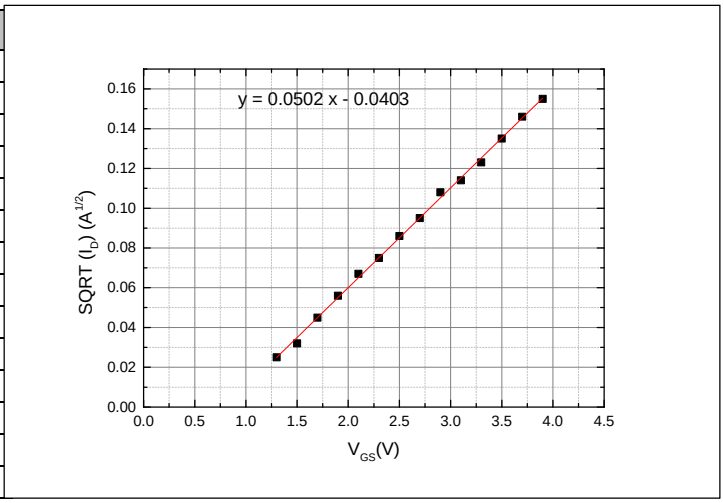
(b) $I_D = K_n(V_{GS} - V_{THN})^2 \implies \sqrt{I_D} = \sqrt{K_n}(V_{GS} - V_{THN}) = \sqrt{K_n}\,V_{GS} - \sqrt{K_n}\,V_{THN}$

This is an equation of the form $y = mx + C$ where

$$y = \sqrt{I_D}, \quad x = V_{GS}, \quad m = \sqrt{K_n}, \quad C = -\sqrt{K_n}\,V_{THN}.$$

Plot $\sqrt{I_D}$ versus V_{GS} and draw a best-fit straight line.

V_{GS}(V)	I_D (mA)	$\sqrt{I_D}$(A$^{-1/2}$)
1.3	0.61	0.025
1.5	1	0.032
1.7	2.03	0.045
1.9	3.11	0.056
2.1	4.44	0.067
2.3	5.63	0.075
2.5	7.43	0.086
2.7	9.04	0.095
2.9	11.66	0.108
3.1	12.95	0.114
3.3	15.04	0.123
3.5	18.33	0.135
3.7	21.23	0.146
3.9	24	0.155



From the plot, $\sqrt{K_n} = 0.0502 \implies K_n = 0.00252$ A V^{-2} = 2.52 mA V^{-2};

$\sqrt{K_n}\,V_{THN} = 0.0403 \implies V_{THN} = 0.803$ V.

(c) Any of the following ways can be used to increase K_n :

Method 1 : Increase C_{OX} by reducing the oxide thickness,

Method 2 : Increase C_{OX} by using a dielectric material with higher permittivity.

Method 3 : Increase the width W of the MOSFET,

Method 4 : Reduce the length L of the MOSFET.

Q5. Figure Q5 shows a MOSFET amplifier circuit. You may assume that the n-channel MOSFET, M_1, does not suffer from body effect (i.e., assume $V_S = V_B$) and it has the following device parameters : $K_n = 2$ mA/V^2, $V_{TH} = 0.5$ V.

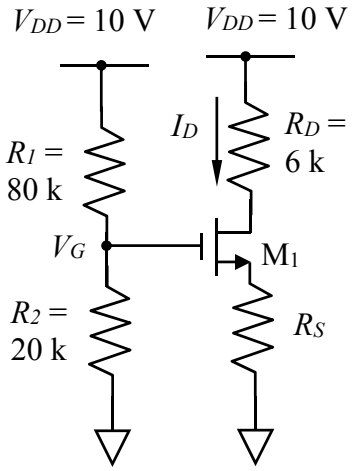


Fig. Q5

(a) By using the voltage divider method, find the voltage V_G. Is the use of the voltage divider method valid in this case? Why?

(b) *Assume* that the MOSFET is operating in the saturation region. Find the value of R_S which will give a drain current I_D =0.5 mA.

(c) Calculate the drain-source voltage, V_{DS}, and the gate source-voltage, V_{GS}, of the MOSFET amplifier. Hence check whether the assumption that the MOSFET is operating in the saturation region is valid.

(d) The channel length modulation factor of the MOSFET, $\lambda = 0.03$ V^{-1}. For the given d.c. operating condition, determine the values of the following small signal parameters of the MOSFET: transconductance, g_m, output resistance r_o.

(e) The circuit designer then decides to change the g_m to 3 mA V^{-1} by using the same MOSFET in the circuit in Fig. Q5. Explain how this can be done. What will be the new resulting value of r_o? [You need not perform the calculations of the actual values of the resistors in the circuit, but just explain how their values should be changed.]

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5. (a) $V_G = V_{DD} \times \dfrac{R_2}{R_1 + R_2} = 10 \times \dfrac{20\text{k}}{20\text{k} + 80\text{k}} = 2\text{ V}.$

The voltage divider method assumes that the same current flows through both R_1 and R_2. As the gate current in a MOSFET is zero, this condition is satisfied. Therefore, the use of the voltage divider method is valid.

(b) It is *assumed* that the MOSFET is operating in the saturation region.

$$I_D = K_n(V_{GS} - V_{TH})^2 = K_n(V_G - V_S - V_{TH})^2 = K_n(1.5 - V_S)^2 \qquad \text{eqn. (1)}$$

By substituting 0.5 mA in eqn. (1),

$$2\text{ m} \times (1.5 - 0.5R_S)^2 = 0.5\text{ m}$$
$$(1.5 - 0.5R_S)^2 = 0.25$$
$$0.5R_S - 1.5 = \pm 0.5$$

$$R_S = 2(1.5 \pm 0.5) = 4k \;\; or \;\; 2k$$

Hence for NMOS, V_S =2 V or 1 V.

However NMOS is off at V_S = 2V as

$$(V_{GS}) = 2 - 2 = 0V < V_{TH} = 0.5\text{ V}.$$

Hence R_S = 2 k.

(c) $V_{GS} = V_G - V_S = 2 - 1 = 1$ V.

$V_D = 10 - I_D R_D = 10 - 0.5$ mA $\times 6$ k $= 10 - 3 = 7$ V.

$V_{DS} = V_D - V_S = 7 - 1 = 6$ V.

$V_{GS} - V_{TH} = 1 - 0.5 = 0.5$ V.

Since $V_{DS} > V_{GS} - V_{TH}$, the assumption that the MOSFET is operating in the saturation region is valid.

(d) Transconductance,

$$g_m = 2\sqrt{K_n I_D} = 2\sqrt{2 \times 10^{-3} \times 0.5 \times 10^{-3}} = 2 \times 10^{-3}\text{ A V}^{-1} = 2\text{ mA V}^{-1}.$$

Output resistance,

$$r_0 = \frac{1}{\lambda I_D} = \frac{1}{0.03 \times 0.5 \times 10^{-3}} = 66.7\text{ k}\Omega.$$

(e) Yes, it can be done by increasing I_D from 0.5 mA to 1.125 mA, as $g_m = 2\sqrt{(K_n I_D)}$. To increase I_D to 1.125 mA, the value of R_S, R_D will need to be reduced and R_2 will need to be changed.

Q6. Figure Q6 shows an amplifier circuit. The n-MOSFET is operating in the saturation region and has the following device parameters : K_n = 1 mA V^{-2}, V_{TH} = 1 V. The source and body of the n-MOSFET are connected together, i.e., there is no body effect. The voltage supply V_{DD} = 5 V. The circuit designer decided that the drain current I_D is to be set at 1 mA and chose R_1 = 60 kΩ, and R_S = 1 kΩ. Complete the design of the circuit by following steps (a) to (d).

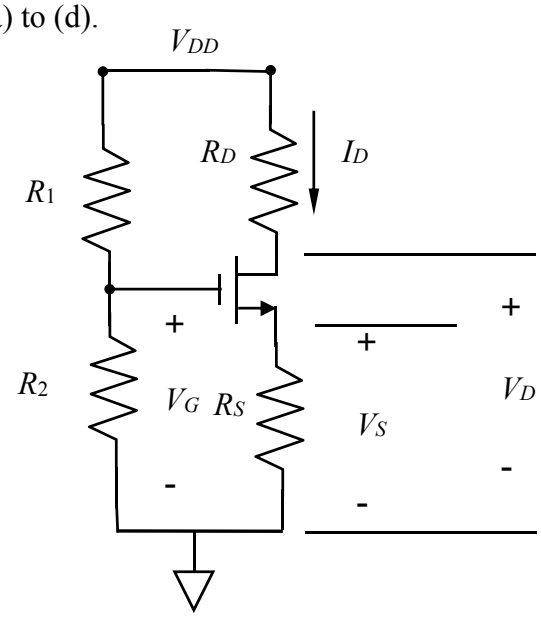

Fig. 6

(a) Determine the value of V_G. [3 marks]

(b) Determine the value of R_2. [2 marks]

(c) What is the minimum value of the drain voltage V_D such that the MOSFET is operating in the saturation region under the given conditions? [3 marks]

(d) What is the maximum value of R_D for the MOSFET to be operating in the saturation region in this circuit? [2 marks]

6.

(a) $I_D = K_n(V_{GS} - V_{TH})^2$

$1mA = 1\ mA/V^2\ (V_{GS} - V_{TH})^2$;

From the above, $V_{GS} = V_G - V_S = 2$ V; as $V_{GS} = 0$ is not a valid solution. [2 marks]

$V_S = R_S I_D = 1$ V; Therefore $V_G = 3$ V. [1 mark]

(b) $\frac{R_2}{R_2+R_1} V_{DD} = 3V$

$5\ R_2 = 3\ (R_1 + R_2) = 3(60\ \text{k}\Omega + R_2)$

$R_2 = 90\ \text{k}\Omega$. [2 marks]

(c) For the MOSFET to operate in the saturation :

$V_{DS} \geq (V_{GS} - V_{TH}) = (2 - 1)\ \text{V} = 1\ V$. [2 marks]

$V_{DS} = V_D - V_S \geq 1\ V$, therefore $V_D \geq 2\ V$.

The minimum value of V_D is 2 V. [1 mark]

(d) $V_D > 2V \Rightarrow V_{DD} - V_D = V_{RD} = I_D R_D < 3\ V$,

Since $I_D = 1$ mA, $R_D < 3\ \text{k}\Omega$.

The maximum value of R_D is 3 kΩ. [2 marks]
