NATIONAL UNIVERSITY OF SINGAPORE

EXAMINATION FOR

(Semester II: 2013/2014)

EE2021/EE2021E –DEVICES AND CIRCUITS

April/May 2014 - Time Allowed: 2.5 Hours

MATRIC. NO | |

SECTION A	Marks
Q.1	
Q.2	
Q.3	
Q.4	
Q.5	
Q.6	
Q.7	
Q.8	
SECTION A TOTAL	

SECTION B	Marks
Q.9	
Q.10	
Q.11	
SECTION B TOTAL	

TOTAL MARKS	

INSTRUCTIONS TO CANDIDATES:

1. This paper contains **SECTIONS A and B** and comprises **TWENTY EIGHT (28)** printed pages.
2. Section A contains **EIGHT (8)** short questions (Total marks of 60) and Section B contains **THREE (3)** longer questions (Total marks of 40).
3. Answer all questions. **Write your answers on this examination paper.**
4. The questions **DO NOT** carry equal marks.
5. This is a **CLOSED BOOK** examination.
6. Programmable calculators are allowed in this examination.
7. The following information can be used where applicable:

Electronic charge	q	=	1.602×10^{-19} C
Boltzmann constant	k	=	1.381×10^{-23} J K^{-1}
	=		8.618×10^{-5} eV K^{-1}
Thermal energy (T = 300 K)	kT	=	0.025 eV
Thermal voltage (T = 300 K)	V_T	=	0.025 V
Permittivity of free space	ε_0	=	8.854×10^{-14} F cm^{-1}

For silicon at 300 K:

Intrinsic carrier concentration	n_i	=	1.5×10^{10} cm^{-3}
Relative permittivity of silicon	ε_r (Si)	=	11.7
Relative permittivity of silicon dioxide	ε_r (SiO_2)	=	3.9

8. A set of formulas and tables is given in a **SEPARATE APPENDIX** for your reference.

Section A

Q.1 A piece of silicon is uniformly doped with donor and acceptor impurities with concentrations of 2×10^{19} cm^{-3} and 3×10^{19} cm^{-3}, respectively. It is at thermal equilibrium at 300 K. The electron and hole mobilities are, respectively, $\mu_n = 140$ cm^2 V^{-1} s^{-1} and $\mu_p = 70$ cm^2 V^{-1} s^{-1}.

(a) Calculate the ionized donor concentration and the ionized acceptor concentration. Identify the majority carrier and calculate the majority carrier concentration. Assume that all the dopants are ionized.

[4 marks]

(b) Calculate the resistivity of the piece of silicon.

[2 marks]

(a)
The ionized donor concentration 2×10^{19} cm^{-3}

The ionized acceptor concentration 3×10^{19} cm^{-3}

Majority carrier hole
Hole concentration 10^{19} cm^{-3}

(b) $\rho = 8.92$ mΩ cm

Q.2 (a) In Fig. Q2(a), V_{DD} = 10 V, R_1 = 6 kΩ and R_2 = 4 kΩ. Calculate the voltage V_2.

[1 mark]

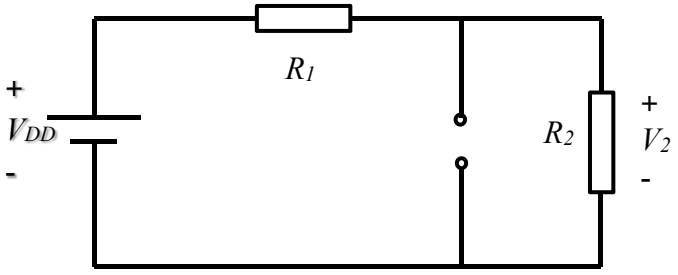


Fig. Q2(a)

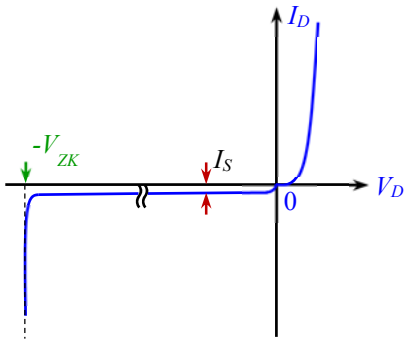


Fig. Q2(b)

(b) Fig. Q2(b) shows the $I_D - V_D$ characteristic of a silicon diode. The parameters of the diode are : $I_S = 10^{-14}$ A, n = 1, V_{ZK} = 3 V.

What is the most likely breakdown mechanism of the diode?

[1 mark]

(c)

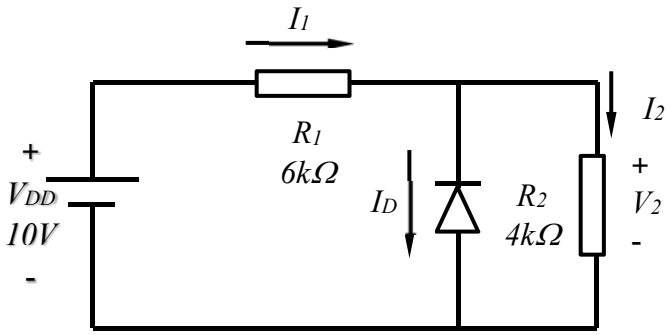


Fig. Q2(c)

The diode is connected in the circuit as shown in Fig. Q2(c). Is the diode forward biased or reverse biased?

[1 mark]

Calculate the voltage V_2, the currents I_D, I_1 and I_2.

[5 marks]

(a) $V_2 = 4\,\text{V}$.

(b) No numerical answer.

(c) No numerical answer.

(d)

$V_2 = 3$ V.

$I_2 = 0.75\,\text{mA}$.

$I_1 = 1.167\,\text{mA}$.

$I_D = 0.417$ mA.

Q.3 For each of the statements below about the Bipolar Junction Transistor (BJT), circle TRUE if the statement is correct, and FALSE if the statement is wrong.

[4 marks]

(Marks will be deducted for each wrong answer you give. No mark will be deducted if you do not answer. The minimum mark for this question is zero.)

(a) When used in an amplifier circuit, the BJT should be biased such that its operating point is in the saturation region.

~~TRUE~~/FALSE

(b) In a **pnp** BJT, the emitter should be more heavily doped than the base in order to achieve a high β.

TRUE/~~FALSE~~

(c) In a BJT, there is no body effect when the base and the collector are connected together.

~~TRUE~~/FALSE

(d) In the small signal model of the BJT, the output resistance r_0 is used to model the effect of base width modulation.

TRUE/~~FALSE~~

Q.4 In the circuit shown in Fig. Q4, Q_1 and Q_2 are two identical **npn** BJTs with β=100. Find the value of R_{REF} such that the DC collector current of the BJT Q_2 is equal to 1.5 mA.

[4 marks]

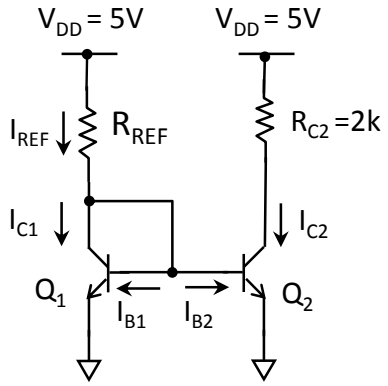


Fig. Q4

Ans : $R_{REF} = 2.81k\Omega$

Q.5 For the amplifier circuit shown in Fig. Q5, the NMOS transistor M_1 has the following parameters: K_n=500 μA/V^2 and V_{TH}=1 V. Use the information in the appendix where appropriate.

(a) Calculate the DC drain current and the parameters of the AC small signal model for the transistor M_1. Verify any assumption you have made in your calculation.

[8 marks]

(b) Calculate the input resistance, R_{in}.

[2 marks]

(c) Calculate the output resistance, R_{out}.

[2 marks]

(d) Estimate the voltage gain, A_v (=V_{out} / V_{in}).

[3 marks]

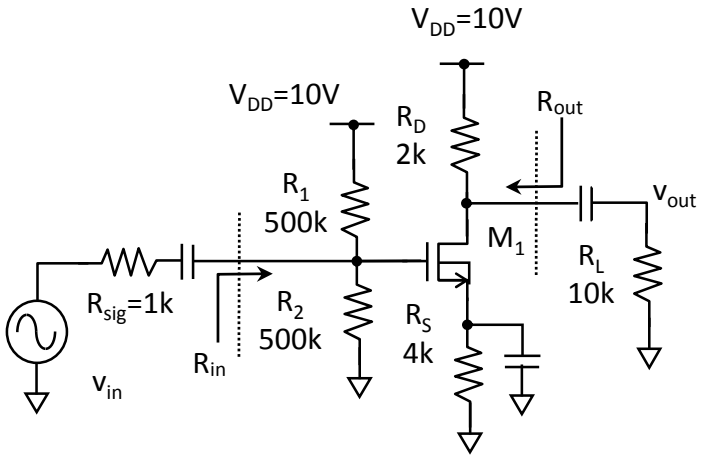


Fig. Q5

(a) I_D= 0.70 mA

$g_m = 1.18 mA/V$

$r_o = \infty$

(b) R_{in} = 250 kΩ

(c) R_{out} = 2 kΩ

(d) $A_V = -1.97$

Q.6 Draw the pull down network (PDN) and pull up network (PUN) of the following logic function:

$$Y = \overline{\{[(A.B) + C].D\} + (E.F)}\ .$$

[8 marks]

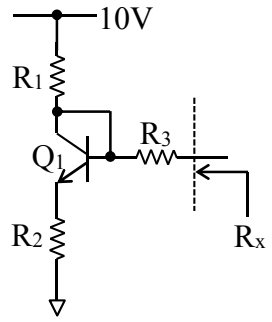
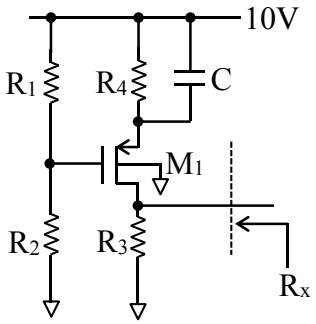
Determine also the best case propagation delay of the above PUN, $t_{pLH,best}$, in terms of that of an inverter, $t_{pLH,inv}$. All NMOS and PMOS transistors in the above logic networks and the inverter have sizing of $(W/L)_n = n$ and $(W/L)_p = p$, respectively.

[4 marks]

$$t_{pLH,best} = \frac{11}{10} t_{pLH,inv}$$

Q.7 Assume that the AC small signal parameters of the BJT are $g_{m,Q1}$, $r_{\pi,Q1}$ and $r_{o,Q1}$; and the AC small signal parameters of the MOSFET are $g_{m,M1}$, $g_{mb,M1}$ and $r_{o,M1}$. Write down the expression for the small signal AC equivalent resistance (R_x) of each of the following configurations:

[7 marks]

(a)  	No numerical answer
(b)  	No numerical answer

Q.8 The following statements refer to a silicon NMOS transistor that is operating in the saturation region with no channel length modulation. In each of the statements below, only the quantity mentioned in the statement is changed.

For each of the statements below in the context of the NMOS transistor above, circle TRUE if the statement is correct, and FALSE if the statement is wrong.

[4 marks]

(Marks will be deducted for each wrong answer you give. No mark will be deducted if you do not answer. The minimum mark for this question is zero.)

(a) The transconductance g_m of the NMOS transistor will increase if its (W/L) ratio is increased.

TRUE/~~FALSE~~

(b) The transconductance g_m of the NMOS transistor will increase if the oxide thickness under its gate is increased.

~~TRUE~~/FALSE

(c) The transconductance g_m of the NMOS transistor will increase if its gate to source voltage, V_{GS} is increased.

TRUE/~~FALSE~~

(d) The transconductance g_m of the NMOS transistor will increase if its drain to source voltage, V_{DS} is increased.

~~TRUE~~/FALSE

END OF SECTION A

Section B

Q.9 A npn bipolar junction transistor in a circuit is required to have a collector current I_C = 2.5 mA and base current I_B = 5 μA when the transistor is in the forward active region at 300K with V_{BE} = 0.65 V. The Early effect can be assumed to be negligible.

(a) What should be the values for the saturation current I_S and β of this transistor?

[2 marks]

(b) A transistor has been partially designed to meet the requirements in part (a). In this unfinished design, the values of the following transistor parameters have been chosen as stated:

Doping in the base, $N_{AB} = 10^{16}$ cm^{-3},
Diffusion coefficient of holes in the emitter, D_p = 1 cm^2/s,
Diffusion coefficient of electrons in the base, D_n = 10 cm^2/s,
Diffusion length of holes in the emitter, L_p = 0.300 μm
Diffusion length of electrons in the base, L_n = 20 μm
Width of the neutral region in the base, w_B = 1 μm

You are required to complete the design of this transistor.

(i) What are the 2 additional parameter values you would need to determine in order to complete the design?

[2 marks]

(ii) What are the required values of the 2 parameters to complete the design?

[6 marks]

(a) $I_S = 12.77 \times 10^{-15}$ A.

$\beta = 500$

(b) (i) donor concentration, N_{DE}, and area A.

(ii) $N_{DE} = 1.67 \times 10^{18}$ cm^{-3},

$A = 35.47 \times 10^{-6}$ cm^2

Q.10

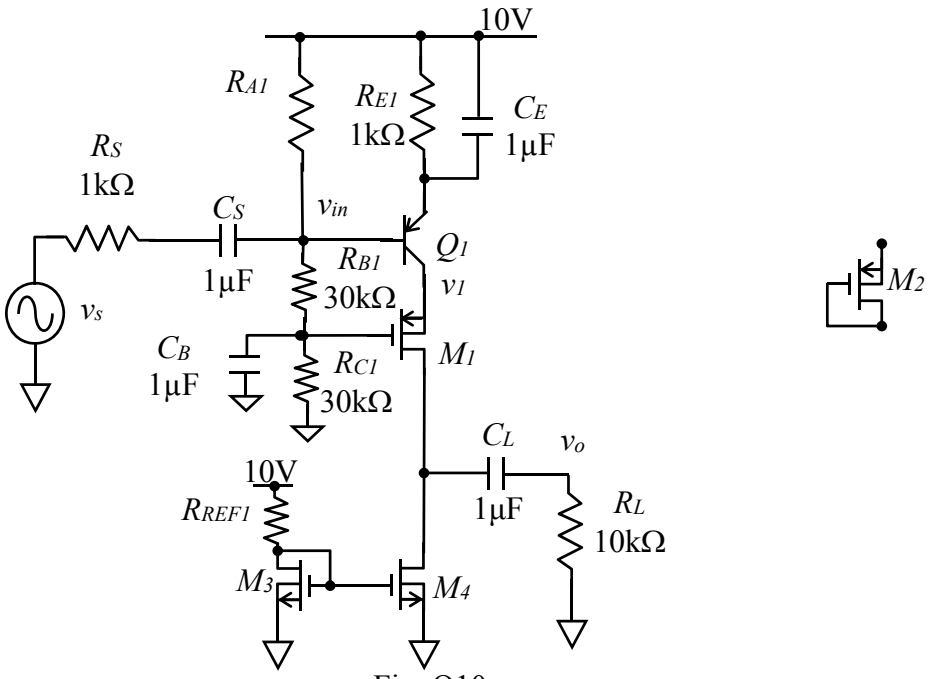


Fig. Q10

In the two-stage amplifier circuit shown in Fig. Q10, assume that the pnp BJT, the NMOS transistors and the PMOS transistors have the following device parameters:

- V_A = 100 V and β = 100 for the BJT, Q_1;
- K_n = 2m A/V^2, V_{THN} = 1 V, λ_n = 0.001V^{-1} and no body effect for the NMOS transistors, M_3 and M_4.
- K_p = 2m A/V^2, V_{THP} = -1 V, λ_p = 0.001V^{-1} and no body effect for the PMOS transistors, M_1 and M_2.

(a) Identify the configuration of each stage of the multi-stage amplifier.

[2 marks]

(b) Design R_{REF1} such that M_1, M_3 and M_4 each has a drain current of 1 mA assuming these transistors are operating in saturation region.

[3 marks]

(c) Estimate the small signal parameters of M_1, i.e. g_{m_M1}, and r_{o_M1} and the small signal parameters of Q_1, i.e. g_{m_Q1}, r_{π_Q1}, r_{o_Q1}, assuming the value of the drain current in part (b).

[3 marks]

(d) Design R_{A1} to ensure the operation condition such that M_1, M_3 and M_4 each has a drain current of 1 mA assuming these transistors are operating in saturation region.

[2 marks]

(e) Estimate the overall gain, i.e., v_o/v_s.

[6 marks]

Question Q.10 continues on Page 22

(f) Diode connected transistor M_2 shown in the right of Fig. Q10 can be used to replace R_{E1}. Comment whether the overall gain will be affected and if the gain is affected, which component values need to be changed to restore the gain in part (e).

[4 marks]

(a) Identify the configuration of each stage of the multi-stage amplifier.

[2 marks]

No numerical answer

(b) Design R_{REF1} such that M_1, M_3 and M_4 each has a drain current of 1 mA.

[3 marks]

$$R_{REF1} = 8.3k$$

(c) Estimate the small signal parameters of M_1, i.e. g_{m_M1}, and r_{o_M1} and the small signal parameter of Q_1, i.e. g_{m_Q1}, r_{π_Q1}, r_{o_Q1} assuming the value of the drain current in (b).

[3 marks]

$$g_{m,M1} = 2.8mA/V, r_{o,M1} = 1M$$
$$g_{m,Q1} = 40mA/V, r_{\pi,Q1} = 2.5k, r_{o,Q1} = 100k$$

(d) Design R_{A1} such that the circuit can function properly.

[2 marks]

$$R_{A1} = 12.3k$$

(e) Estimate the overall gain, i.e., v_o/v_s.

[6 marks]

$$\frac{v_o}{v_s} = 264$$

(f) Diode connected M_2 as shown in the right of Fig. Q10 can be used to replace R_{E1}. Comment whether the overall gain will be affected and if the gain is affected, which component values need to be changed.

[4 marks]

No numerical answer

Q.11 You are given a task to build an arbitrary signal generator. You may assume that a square wave voltage source is readily available.

(a) Show an opamp circuit that can produce a triangular wave from a square wave input with 50% duty cycle, i.e. $T_{POS}=T_{NEG}$, as shown in Fig. Q11(a).

[2 marks]

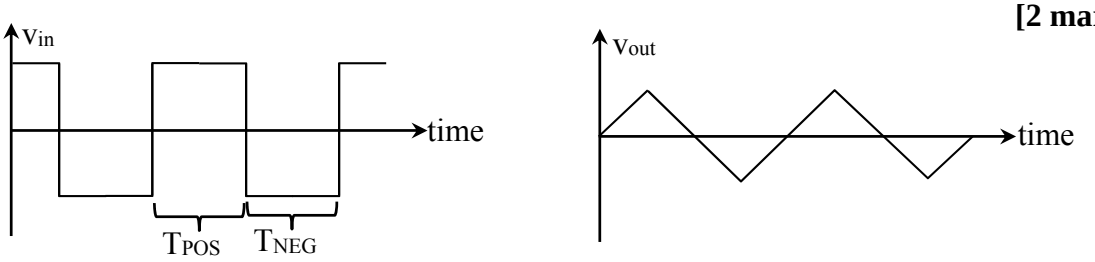


Fig. Q11(a)

(b) Consider the opamp circuit shown in Fig. Q11(b). The switch will short circuit the capacitor whenever the input voltage is negative. Sketch the output waveform (v_{out}) when the input is a square wave with 50% duty cycle.

[3 marks]

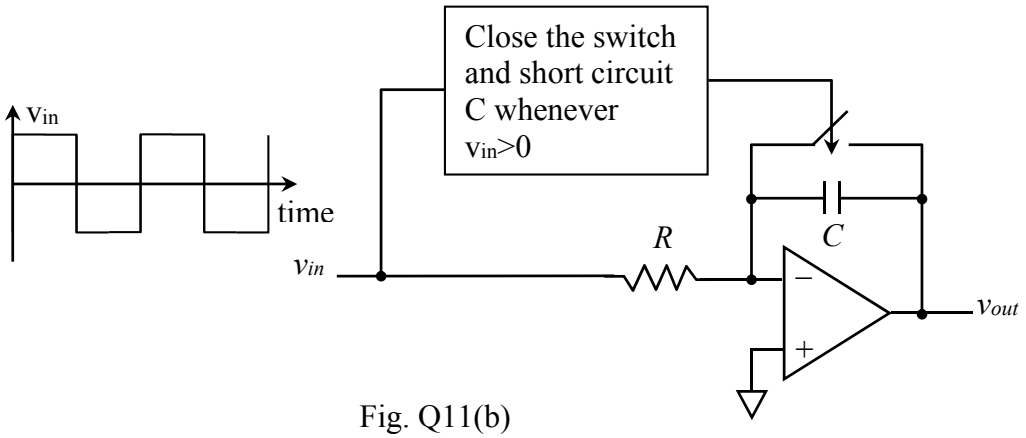


Fig. Q11(b)

(c) Show an opamp circuit that can produce a saw tooth wave from a square wave input with 50% duty cycle as shown in Fig. Q11(c).

[5 marks]

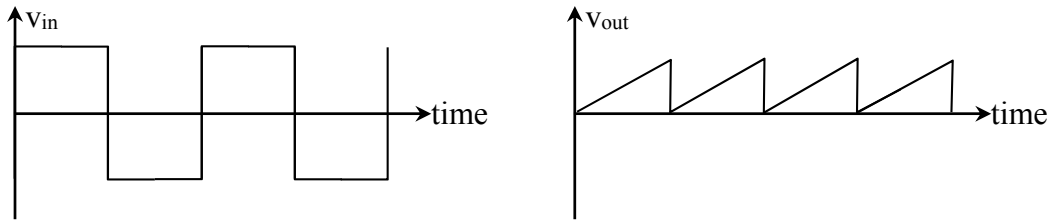


Fig. Q11(c)

No numerical answer to this question.

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