# SiGe BiCMOS Technology with 3.0 ps Gate Delay

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**Abstract**

This work reports on a 130 nm BiCMOS technology with high-speed SiGe:C HBTs featuring a transit frequency of 255 GHz and a maximum oscillation frequency of 315 GHz at an emitter area of 0.17 x 0.53 μm$^2$. A minimum gate delay of 3.0 ps was achieved for CML ring oscillators. Breakdown voltages of the HBTs are measured to be $BV_{CEO}$=1.8 V, $BV_{CBO}$=5.6 V, and $BV_{EBO}$=1.9 V.

## Introduction

Emerging high-frequency markets such as high-speed optical communications (>100 Gb/s) and automotive radar (77GHz) call for ever increasing transistor and circuit speed at a high level of integration. The realization of SiGe HBTs with $f_T/f_{max}$ values of 300 GHz and above [1, 2] has extended application frequencies of SiGe technologies into the millimeter-wave band. BiCMOS technologies with high-speed HBTs integrated with state-of-the-art CMOS and high-quality passive components will facilitate mixed-signal and system-on-chip applications for these frequency bands.

Ring oscillator gate delays have been widely used to benchmark the capability of technologies for high-speed circuit operation. There have been reports of record gate delays of 3.2-3.3 ps for SiGe bipolar [1-3] and III-V technologies [4] and 3.5-3.6 ps for SiGe BiCMOS technologies [5, 6].

Here, we present a 130 nm BiCMOS technology with SiGe:C HBTs featuring $f_T/f_{max}$ values of 255/315 GHz and CML ring oscillator gate delays of 3.0 ps. The improved gate delay compared to previously reported data for SiGe bipolar and BiCMOS technologies results from the improved HBT speed combined with a metal interconnect layout optimized for low parasitics. The used HBTs with an effective emitter size of 0.17 x 0.53 μm$^2$ show moderate breakdown voltages of $BV_{CEO}$=1.8 V, $BV_{CBO}$=5.6 V, and $BV_{EBO}$=1.9 V. The HBT module was integrated in a 130 nm BiCMOS technology suitable for millimeter-wave mixed-signal applications at a high level of integration.

## Process Overview

The flow of the BiCMOS process is shown schematically in Fig. 1. The process sequence for HBT fabrication consists of

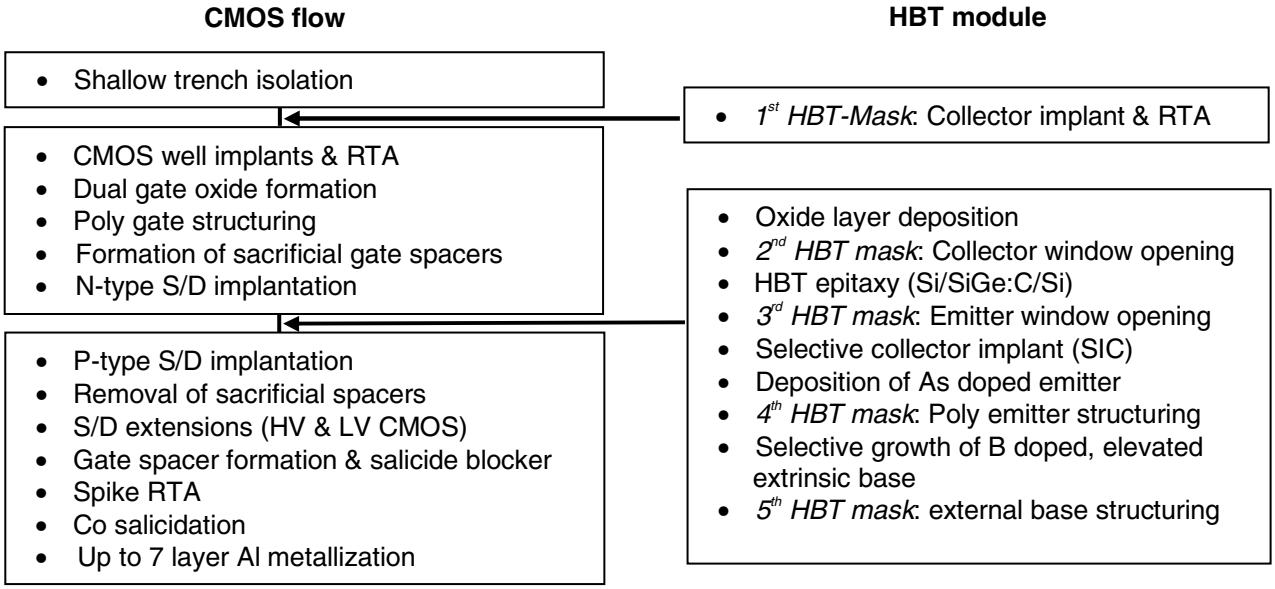


Fig. 1: Schematic BiCMOS flow

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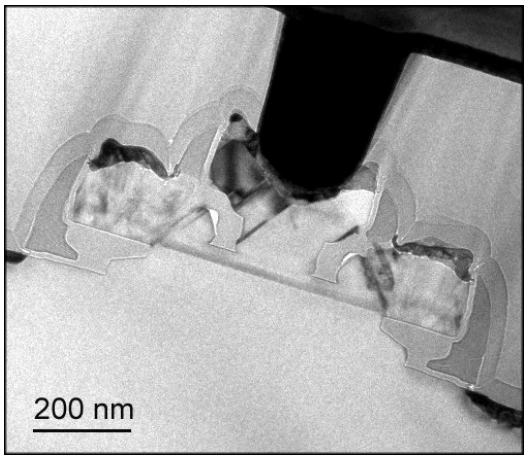


Fig. 2: TEM cross section of an HBT with self-aligned elevated extrinsic base and an effective emitter width of 0.17 µm.

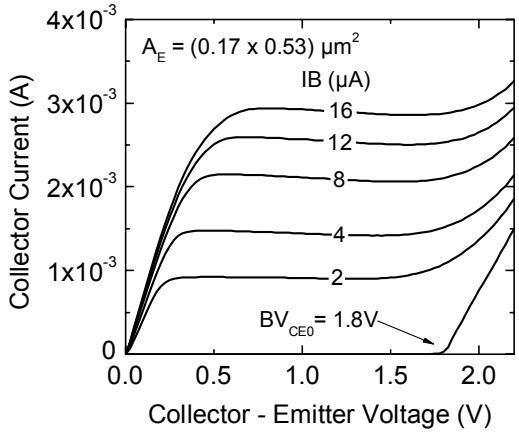


Fig. 3: HBT output characteristics at high injection.

five lithographic mask steps. It begins with the formation of the collector wells by high-dose ion implantation. The collector wells are laterally confined by shallow trench regions. The major part of the HBT fabrication is performed after structuring the CMOS gates. The basic processing steps for base and emitter formation are as described in [6]. The active collector region is defined by depositing and patterning an oxide layer. A selectively-grown Si buffer layer and the non-selectively-grown SiGe:C base layer and Si cap layer are formed in one epitaxial step. After epitaxy, a sacrificial layer is deposited, and emitter windows are structured. Additional inside spacers are formed before depositing and structuring the As-doped crystalline emitter. B-doped elevated extrinsic base regions are grown by selective epitaxy after emitter formation. A TEM image of the final HBT structure is shown in Fig. 2. The emitter areas are completely enclosed by elevated extrinsic base regions. Minimization of HBT device parasitics ($R_B$, $C_{BC}$, $R_C$) for highest RF performance is addressed here primarily by the self-aligned device design and reduced device dimensions due to the use of 130 nm design rules.

The CMOS process features dual gate oxides of 2.0 nm and 7.0 nm for 1.2 V logic and 3.3 V I/O devices, respectively. The 1.2V CMOS process was optimized for low-power applications. NMOS and PMOS transistors with 110 nm gate length have an $I_{off}$ of 50pA/µm and $I_{on}$ of 440 µA/µm and 200 µA/µm, respectively.

The BEOL consists of up to seven aluminum interconnect layers including five fine-structured layers with a pitch of 0.34 µm for metal 1 and 0.41 µm for metals 2 to 5. Two thick Al layers (2 and 3 µm thick) are provided for high-quality inductors and transmission lines. Various types of poly resistors and MIM capacitors with 1.5 fF/µm² are available. HBTs are contacted with non-square tungsten plugs (contact bars) to minimize contact resistances.

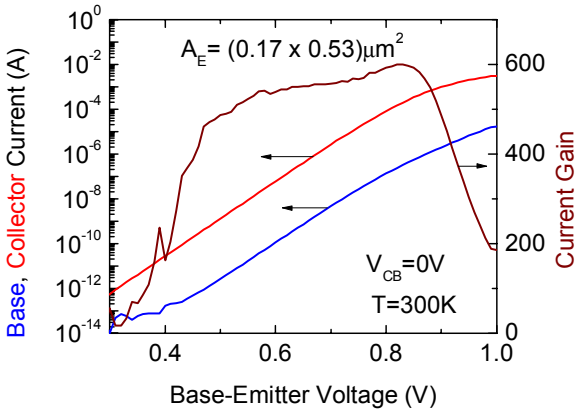


Fig. 4: Gummel characteristics of an HBT with an effective emitter area of 0.17 x 0.53 µm².

## HBT Device Results

### *A. DC characteristics*

Output and Gummel characteristics of HBTs with an emitter area of 0.17 x 0.53 µm² are shown in Figs. 3 and 4. The devices have a maximum current gain of 600. Ideal base and collector currents are obtained for single HBTs and for 4k transistor arrays. Fig. 5 shows the superposition of Gummel plots of the 4k HBT arrays of all 61 chips from an 8 inch wafer. The measurement shows ideal characteristics for 93% of the arrays demonstrating the manufacturability of the process. Measured breakdown characteristics of the HBTs are plotted in Fig. 6. We obtained $BV_{CEO}$=1.8 V, $BV_{CBO}$=5.6 V, and $BV_{EBO}$=1.9 V

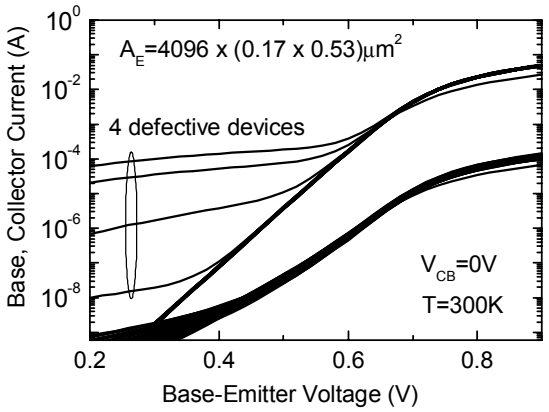


Fig. 5: Gummel characteristics of arrays of 4096 HBTs in parallel for all 61 dies of an 8 inch wafer.

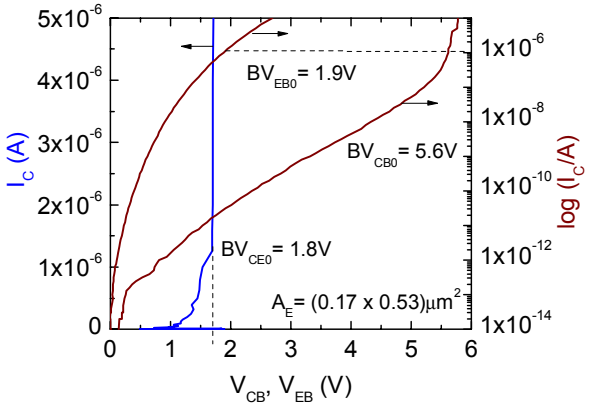


Fig. 6: Breakdown characteristics. $BV_{CEO}$ was extracted from $I_C$ at open-base on the linear scale and $BV_{CBO}$ and $BV_{EBO}$ are taken at $I_C$=1µA.

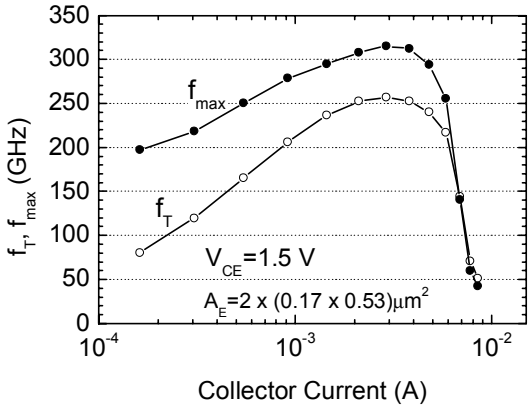


Fig. 7: HBT transit frequency $f_T$ and maximum oscillation frequency $f_{max}$ vs. collector current.

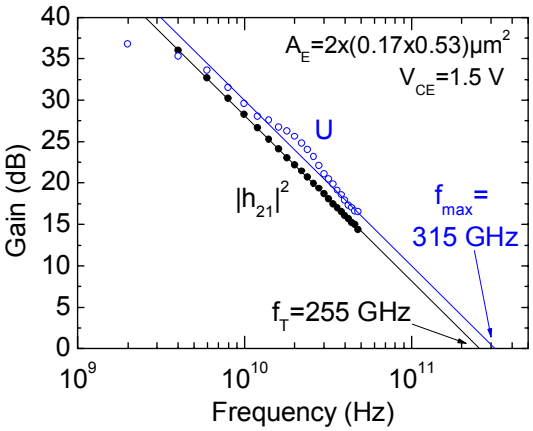


Fig. 8: Gain vs. frequency with -20 dB/dec lines fitted to the data points from 40 to 48 GHz.

*B. RF characteristics*

Figs. 7 and 8 show $f_T(I_C)$, $f_{max}(I_C)$ and gain curves for the standard transistor geometry with an emitter area of 0.17 x 0.53 µm$^2$. This device features a peak $f_T$ of 255 GHz and a peak $f_{max}$ of 315 GHz. Fig. 9 summarizes peak $f_T$ and $f_{max}$ values for a series of HBTs with different emitter lengths and a fixed emitter width of 0.17 µm. We measured $f_T$ values of about 250 GHz for emitter lengths down to 0.4 µm. For the shortest emitter lengths, $f_{max}$ increases significantly due to the lower specific base resistance resulting from the complete enclosure of the active emitter with salicided base poly. The data of the 2.08 µm and 1.04 µm long devices in Fig. 9 correspond to a standard CBEBC layout with scalable emitter length. The demonstrated outstanding RF performance down to smallest emitter sizes is beneficial for the realization of very high speed digital circuit blocks at moderate power consumption.

## Ring Oscillators

CML ring oscillators with HBTs of the standard emitter size of 0.17 x 0.53 µm$^2$ were investigated for two layouts mainly differing in the interconnect parasitics (Fig. 10). Both designs consist of 53 stages. RO1 has the same layout of the metal interconnects as the ring oscillators investigated in [6] in a 0.25 µm process. Despite of the significantly improved $f_T$ and $f_{max}$ in the present process, the minimum gate delay of RO1 of 3.5 ps beats the result of [6] by only 0.1 ps. This is attributed to larger parasitics of the metal interconnects in the 130 nm process. In particular, the reduced thicknesses of interlayer dielectrics caused a larger capacitive substrate coupling of the interconnect lines which were formed mainly in the metal 2 layer. This indicates the importance of the optimization of all parasitic components for transforming highest transistor speed into highest circuit speed. In the layout of RO2, interconnect parasitics were significantly reduced due to reduced lateral dimensions of the metal lines

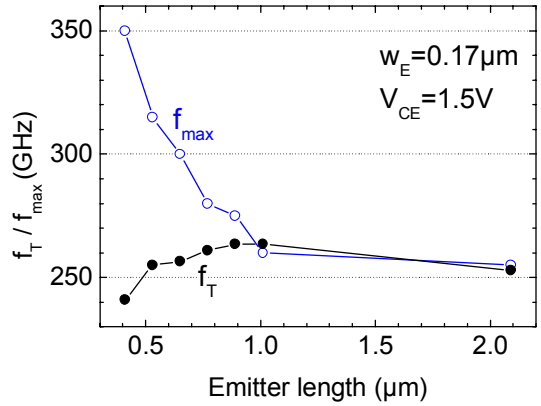


Fig. 9: $f_T$ and $f_{max}$ of HBT with 0.17µm emitter width as a function of emitter length.

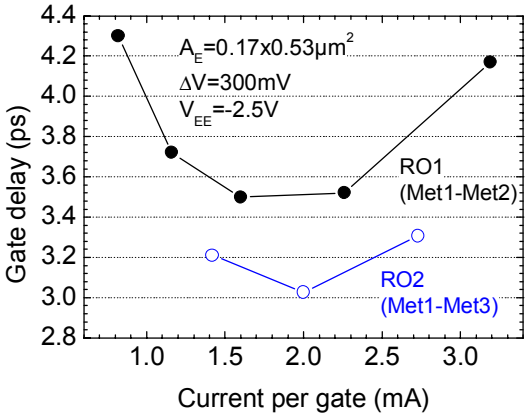


Fig. 10: CML gate delays vs. current for ring oscillators with 53 stages. Two designs with different interconnect parasitics are compared.

and the inclusion of metal 3 connections. A minimum gate delay of 3.0 ps was achieved. This speed exceeds results of most advanced scaled CMOS technologies with a record gate delay of 3.58 ps [7] and of previous SiGe bipolar and BiCMOS technologies.

## Conclusions

In summary, we have demonstrated ring oscillator delays of 3.0 ps per stage and $f_T/f_{max}$ values of 255/315 GHz in a 130 nm SiGe:C BiCMOS technology suitable for millimeter-wave digital and analog system-on-chip applications. We have shown that for highest circuit speed high $f_T/f_{max}$ values have to be combined with a minimization of interconnect parasitics which becomes increasingly difficult with technology scaling.

Table I: Summary of HBT parameter .

| | |
|---|---|
| Emitter area | 0.17 x 0.53 µm$^2$ |
| ß | 600 |
| $R_{SBi}$ | 4 kΩ/sq. |
| $BV_{CB0}$ | 5.6 V |
| $BV_{CE0}$ | 1.8 V |
| $BV_{EB0}$ | 1.9 V |
| $C_{EB}$ | 1.8 fF |
| $C_{BC}$ | 1.7 fF |
| $R_B$ | 150 Ω |
| $R_C$ | 55 Ω |
| $R_E$ | 50 Ω |
| $f_T$ | 255 GHz |
| $f_{max}$ | 315 GHz |
| CML gate delay | 3.0 ps |


## Acknowledgment

The authors thank the team of the IHP pilot line for excellent support.


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