NATIONAL UNIVERSITY OF SINGAPORE

EXAMINATION FOR

(Semester I: 2014/2015)

EE2021/EE2021E –DEVICES AND CIRCUITS

November/December 2014 - Time Allowed: 2.5 Hours

MATRIC. NO | |

SECTION A	Marks
Q.1	
Q.2	
Q.3	
Q.4	
Q.5	
Q.6	
SECTION A TOTAL	

SECTION B	Marks
Q.7	
Q.8	
Q.9	
SECTION B TOTAL	

TOTAL MARKS	

INSTRUCTIONS TO CANDIDATES:

1. This paper contains **SECTIONS A and B** and comprises **TWENTY SIX (26)** printed pages.
2. Section A contains **SIX (6)** questions (Total marks of 60) and Section B contains **THREE (3)** questions (Total marks of 40).
3. Answer all questions. **Write your answers on this examination paper.**
4. The questions **DO NOT** carry equal marks.
5. This is a **CLOSED BOOK** examination.
6. Programmable calculators are allowed in this examination.
7. The following information can be used where applicable:

Electronic charge	q	=	1.602×10^{-19} C
Boltzmann constant	k	=	1.381×10^{-23} J K^{-1}
		=	8.618×10^{-5} eV K^{-1}
Thermal energy (T = 300 K)	kT	=	0.025 eV
Thermal voltage (T = 300 K)	V_T	=	0.025 V
Permittivity of free space	ε_0	=	8.854×10^{-14} F cm^{-1}

For silicon at 300 K:

Intrinsic carrier concentration	n_i	=	1.5×10^{10} cm^{-3}
Relative permittivity of silicon	ε_r (Si)	=	11.7
Relative permittivity of silicon dioxide	ε_r (SiO_2)	=	3.9

8. A set of formulas and tables is given in a **SEPARATE APPENDIX** for your reference.

Section A

Q.1 There are two samples of silicon, A and B. Each of them is uniformly doped with both donor and acceptor impurities. Assume that the silicon samples are at thermal equilibrium at 300 K, that all the dopants are ionized, and that the intrinsic carrier concentration, $n_i = 1.5 \times 10^{10}$ cm^{-3}. Complete the table below by filling in the missing values of N_D, N_A and n_0.

Silicon Sample	Donor conc. N_D (cm^{-3})	Acceptor conc. N_A (cm^{-3})	Equilibrium electron conc. n_0 (cm^{-3})	Equilibrium hole conc. p_0 (cm^{-3})
Sample A	1×10^{17}	9.5×10^{16}	5×10^{15}	4.5×10^{4}
Sample B	8×10^{15}	8×10^{15}	1.5×10^{10}	1.5×10^{10}

Is Sample A n-type or p-type? Ans: ___n - type_____

Is Sample B n-type or p-type? Ans: Neither. It is intrinsic

Q.2

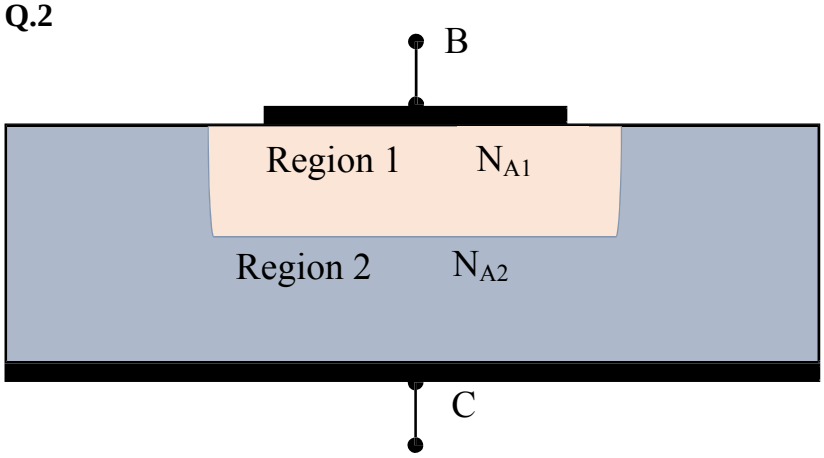


Fig. Q2

A semiconductor wafer has two regions as shown in Fig. Q2. Region 1 is uniformly doped with acceptors with a concentration of N_{A1} and Region 2 is uniformly doped with acceptors with an acceptor concentration of N_{A2}. It is given that $N_{A1} >> N_{A2}$. The wafer is at thermal equilibrium at room temperature and with all the dopants ionised. There is no external connection between B and C.

For each of the following statements which refer to the wafer above, circle TRUE if the statement is correct, and FALSE if the statement is wrong.

(Marks will be deducted for each wrong answer you give. No mark will be deducted if you do not answer.)

[8 marks]

i. There is a continuous net motion of holes from Region 2 to Region 1 because of the difference between the doping concentrations in the two regions.

~~TRUE~~/FALSE

ii. The hole concentrations of Region 1 and Region 2 are equal and have a value somewhere between N_{A2} and N_{A1}.

~~TRUE~~/FALSE

iii. Holes move by diffusion from Region 1 to Region 2 and holes also move by drift from Region 2 to Region1 but there is no net motion of holes.

TRUE/~~FALSE~~

iv. A potential barrier exists across the junction between Region 1 and Region 2.

TRUE/~~FALSE~~

Q.3 Fig. Q3 below shows a single stage amplifier with current mirror biasing.

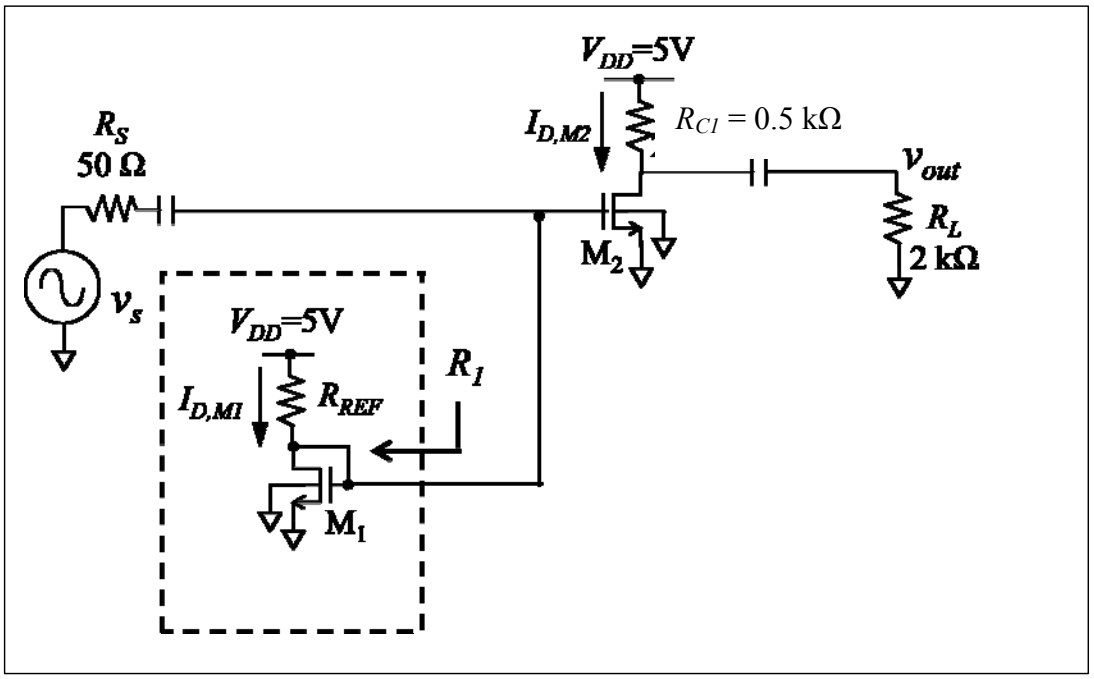


Fig. Q3

For the two n-channel MOSFETs, $V_{THN1} = V_{THN2} = 1$ V, $\lambda_{M1} = \lambda_{M2} = 0$, $K_{n,M1} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_{M1} = 2$ mA V^{-2}, $K_{n,M2} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_{M2} = 4$ mA V^{-2}, where $\left(\frac{W}{L}\right)_{M2} = 2\left(\frac{W}{L}\right)_{M1}$.

(a) Design R_{REF} such that $I_{D,M1} = 2$ mA.

[4 marks]

(b) What is the value of $I_{D,M2}$?

[2 mark]

(c) Calculate the small signal parameters of the two MOSFETs, i.e., $g_{m,M1}$, $r_{o,M1}$, $g_{m,M2}$, $r_{o,M2}$.

[4 marks]

(d) Calculate the value of the a.c. equivalent resistance, R_1, of the circuit enclosed in the dashed box in Fig. Q4.

[3 marks]

(e) Identify the configuration of the single stage amplifier.

[1 mark]

(f) Determine the parameters, G_m, R_{in} and R_{out} of the two-port network of the amplifier.

[3 marks]

(a) Design R_{REF} such that $I_{D,M1} = 2$ mA.

$R_{REF} = 1.5\ \text{k}\Omega$.

(b) What is the value of $I_{D,M2}$?

$I_{D,M2} = 4$ mA.

(c) Calculate the small signal parameters of the two MOSFETs, i.e., $g_{m,M1}$, $r_{o,M1}$, $g_{m,M2}$, $r_{o,M2.}$

$g_{m,M1} = 4\ \text{mA V}^{-1}$.

$r_{o,M1} = \infty$

$g_{m,M2} = 8\ \text{mA V}^{-1}$.

$r_{o,M2} = \infty$

(d) Calculate the value of the a.c. equivalent resistance, R_1, of the circuit enclosed in the dashed box in Fig. Q.3.

$R_1 = 214.3\ \Omega$.

(e) Identify the configuration of the single stage amplifier.

Common source amplifier.

(f) Determine the parameters, G_m, R_{in} and R_{out} of the two-port network of the amplifier.

$G_m = g_{m,M2} = 8\ \text{mA V}^{-1}$.

$R_{in} = R_1 \,//\, \infty = 214.3\ \Omega$.

$R_{out} = R_C \,//\, \infty = 0.5\ \text{k}\ \Omega$.

Q.4 (a) Design the pull down network of the following logic function :

$$Y = \overline{(A+B)\cdot C\cdot(D+E)}.$$

[4 marks]

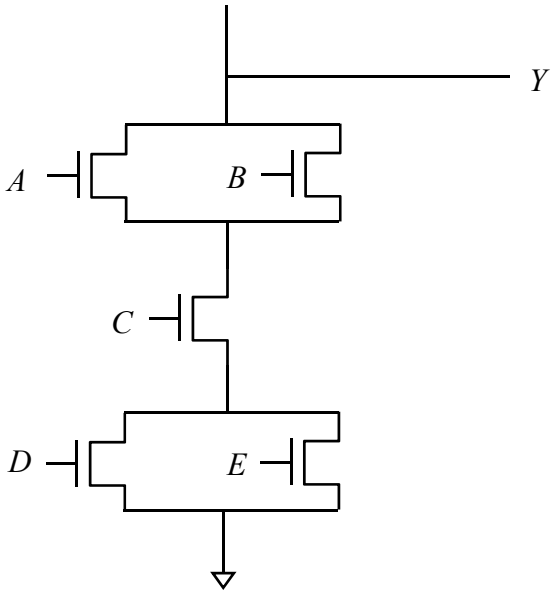
(b) Assume that all the transistors have a sizing of $(W/L)_{min}$. Compare the worst case t_{pHL} of the logic circuit with the t_{pHL} of an inverter with the same transistor sizing.

[4 marks]

(c) Suggest possible sizing of transistors of logic circuit such that its tpHL equals to an tpHL of an inverter with sizing of $(W/L)_{min}$.

[2 marks]

(a)



(b)

$$\frac{t_{pHL,\log ic}}{t_{pHL,inverter}} = \frac{\left(\frac{W}{L}\right)_{\min}}{\frac{1}{3}\left(\frac{W}{L}\right)_{\min}} = 3$$

(c) Make the sizing of each of the transistors in the logic circuit equal to $3(W/L)_{min}$.

Q.5 Assume that the AC small signal parameters of the BJT are $g_{m,Qi}$, $r_{\pi,Qi}$ and $r_{o,Qi}$; and the AC small signal parameters of the MOSFET are $g_{m,Mj}$, $g_{mb,Mj}$ and $r_{o,Mj}$. Write down the expression for the small signal AC equivalent resistances (R_{x1}, R_{x2}, R_{x3}) in the circuit in Fig. Q5.

[9 marks]

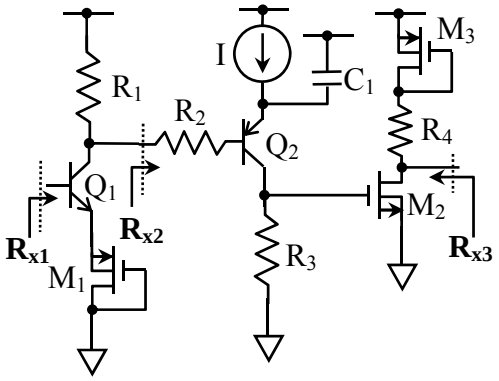


Fig. Q5

$$R_{x1} = r_{\pi,Q1}\left(1 + g_{m,Q1}\frac{1}{g_{m,M1}}\right)$$

$$R_{x2} = R_2 + r_{\pi,Q2}$$

$$R_{x3} = r_{o,M2} // \left(R_4 + \frac{1}{g_{m,M3}}\right)$$

Q.6 Show an opamp circuit that can generate the following transfer characteristic in Fig. Q6:

[8 marks]

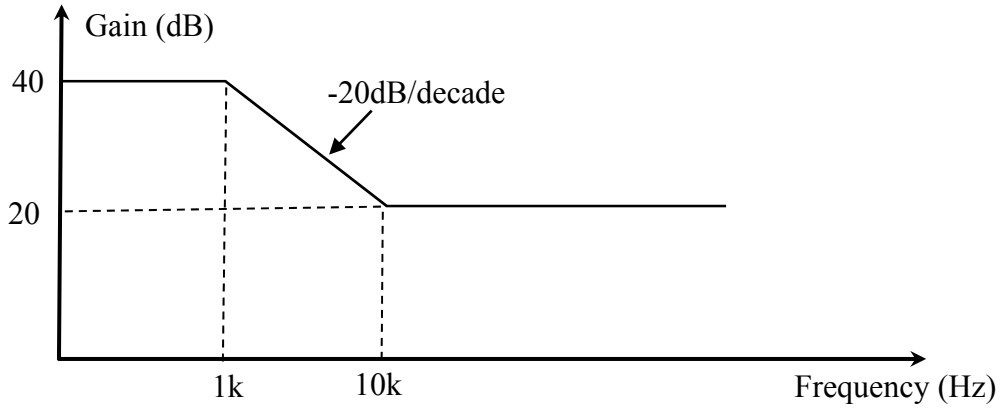
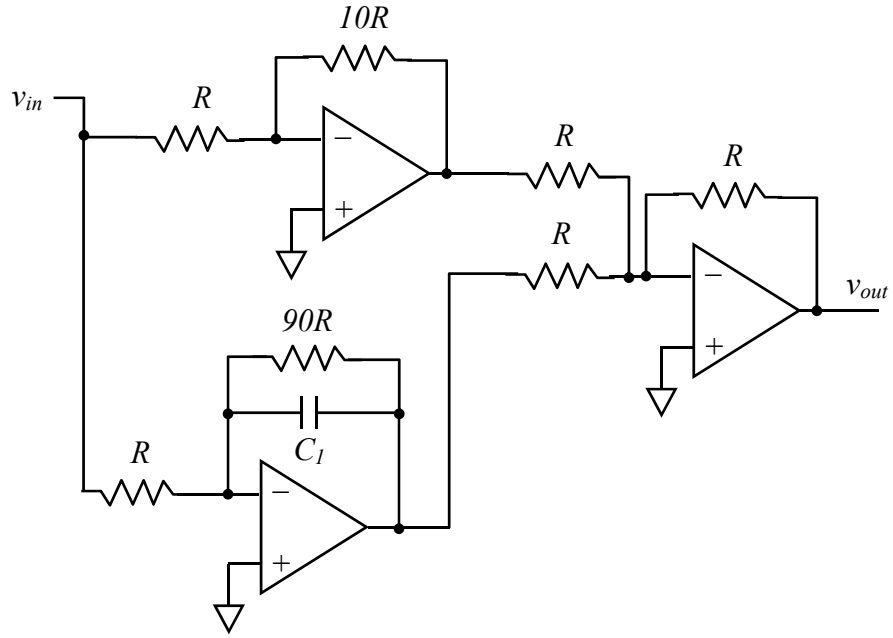


Fig. Q6

[Note : Gain(dB) =20×$\log_{10}$(V_{out}/V_{in}). Hence, 40dB is equivalent to V_{out}/V_{in}=100, 20dB is equivalent to V_{out}/V_{in}=10]



$$C_1 = \frac{2\pi 1k}{90R}$$

Section B

Q.7 The minority carrier concentration distributions in the neutral region of the emitter, base and collector of a bipolar junction transistor (BJT) are shown in Fig. Q7. The emitter, base and collector are each uniformly doped. The thermal equilibrium electron concentration in the emitter and collector are n_{E0} = 11.25 cm^{-3} and n_{C0} = 2.25×10^{5} cm^{-3}, respectively. The neutral base width, w_B = 1 μm, and the thermal equilibrium hole concentration in the base, p_{B0}, has a magnitude between n_{E0} and n_{C0}. In Fig. Q7,

- $p_B\,(x = 0)$ is the hole concentration in the neutral base region, at the edge of the emitter-base space charge region (SCR).
- $n_E\,(x' = 0)$ is the electron concentration in the neutral emitter region, at the edge of the emitter-base SCR.
- $p_B\,(x = w_B) \approx 0$ is the hole concentration in the neutral base region, at the edge of the base-collector SCR.
- $n_C\,(x'' = 0) \approx 0$ is the electron concentration in the neutral collector region, at the edge of the base-collector SCR.

It is known that one of the junctions of the BJT is forward biased with a voltage of magnitude 0.7 V across it, while the other junction is reverse biased with a voltage of magnitude 2 V across it. You are also given that the base-collector junction capacitance, C_j, under the above given biased condition is 0.5 times that at zero bias.

(a) Is the BJT operating in the forward active mode? Explain your answer.

[2 marks]

(b) What are the doping type and doping concentration of the collector?

[3 marks]

(c) Determine the built-in voltage, V_o, of the base-collector junction?

[3 marks]

(d) What is the value of $p_B\,(x = 0)$?

[3 marks]

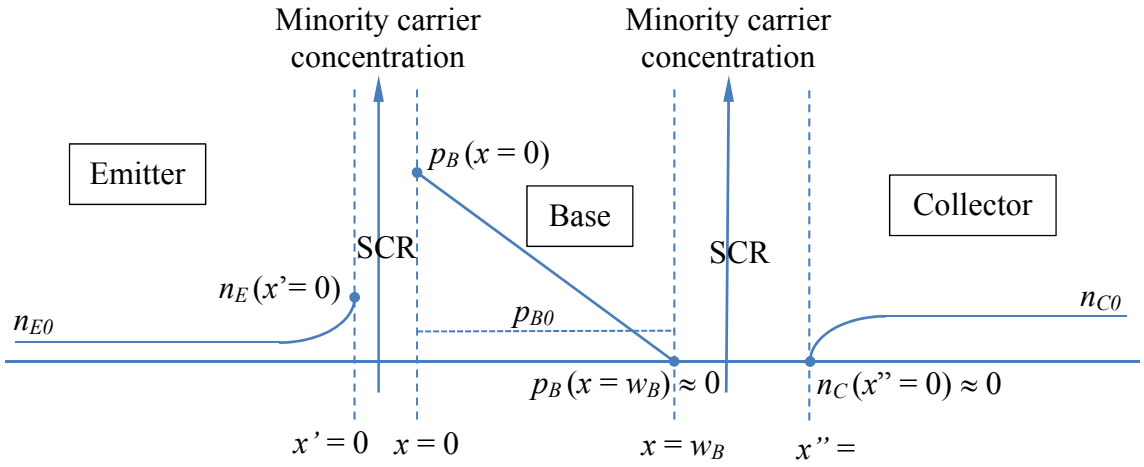


Fig. Q7

(a) Yes.

(b) p-type $N_{AC} = 10^{15}$ cm^{-3}

(c) $V_o = 0.67$ V

(d) $p_B(x = 0) = 3.33 \times 10^{15}$ cm^{-3}

Q.8 The Zener diode circuit within the dashed box shown in Fig. Q8 is used to provide the DC biasing to the transistor circuit. The breakdown voltage of the Zener diode, D_1, is 5 V. The transistor, Q_1, has $\beta = 100$ and $V_A = 100$ V. You may assume $I_{R1} \approx I_{R2} >> I_B$.

(a) Determine the current supplied by the Zener diode circuit I_L.

[4 marks]

(b) What is the maximum allowable R_S such that the Zener diode will function properly?

[3 marks]

(c) What is the impact of choosing R_S much smaller than the value in part (b).

[2 marks]

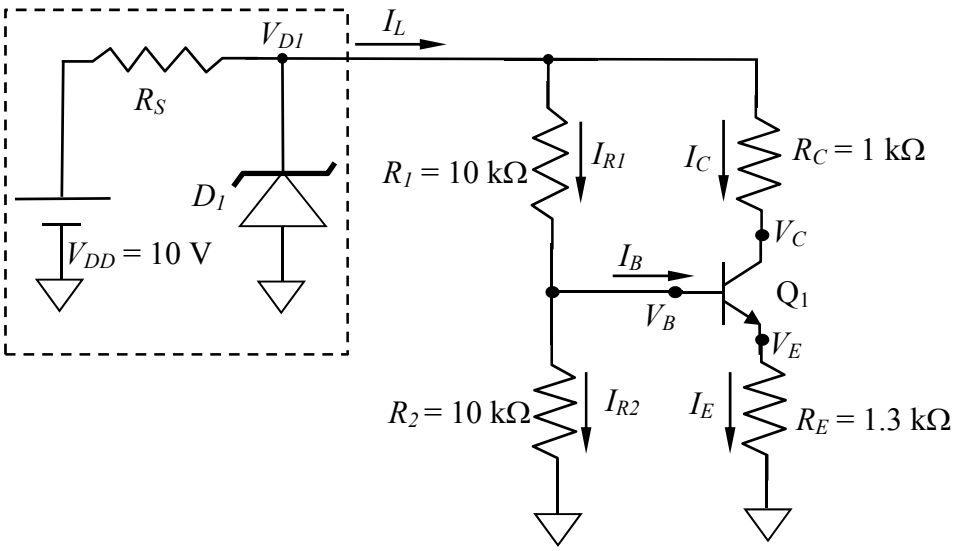


Fig. Q8

(a) $I_L = 1.63$ mA.

(b) Maximum R_S allowable = 3.07 kΩ.

(c) The current through the Zener diode will be much large than the value corresponding to R_S = 3.07 kΩ.

Q.9

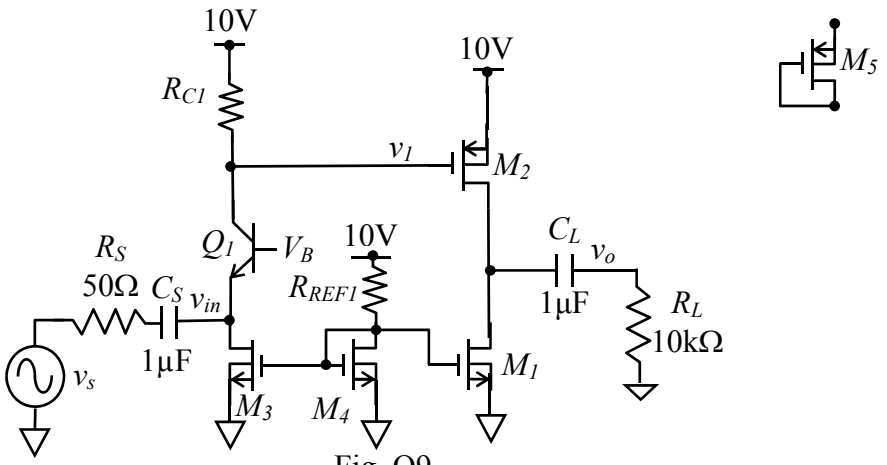


Fig. Q9

In the two-stage amplifier circuit shown in Fig. Q9, assume that the pnp BJT, the NMOS transistors and the PMOS transistors have the following device parameters:

- V_A = 100 V and β = 100 for the BJT, Q_1;
- K_n = 2m A/V^2, V_{THN} = 1 V, λ_n = 0.001V^{-1} and no body effect for the NMOS transistors, M_3 and M_4.
- K_p = 2m A/V^2, V_{THP} = -1 V, λ_p = 0.001V^{-1} and no body effect for the PMOS transistors, M_1 and M_2.

Further assume that R_{REF1} is chosen such that M_1, M_3 and M_4 each has a drain current of 1mA. (You are not required to find R_{REF1}.)

(a) Identify the configuration of each stage of the multi-stage amplifier.

[2 marks]

(b) Estimate the small signal parameters of M_2, i.e. $g_{m,M2}$, and $r_{o,M2}$ and the small signal parameters of Q_1, i.e., $g_{m,Q1}$, $r_{\pi,Q1}$, $r_{o,Q1}$.

[3 marks]

(c) Design R_{C1} to ensure that M_2 has the same current as M_1 assuming these transistors are operating in the saturation region.

[2 marks]

(d) Estimate the overall gain, i.e., v_o/v_s.

[6 marks]

(e) What is the minimum V_B value allowed such that M_3 is operating in saturation region?

[4 marks]

(f) If R_{C1} is replaced with M_5, would it create any biasing issue? Would the overall gain be larger or smaller?

[3 marks]

(a) CB-CS

(b)

$$g_{m,M2} = 2.8\text{mA/V}, r_{o,M1} = 1\text{M}\Omega$$
$$g_{m,Q1} = 40\text{mA/V}, r_{\pi,Q1} = 2.5\text{k}\Omega, r_{o,Q1} = 100\text{k}\Omega$$

(c) R_{C1} = 1,71 kΩ

(d) v_o / v_s = 638.4

(e) $V_{B,min}$ = 1.407 V

(f) Biasing would not be an issue. Overall gain would be smaller.

END OF PAPER