Q. 1 (a) Figure 1.1 shows a two-stage amplifier circuit. Obtain an expression for the overall voltage gain v_o/v_s. (5 marks)

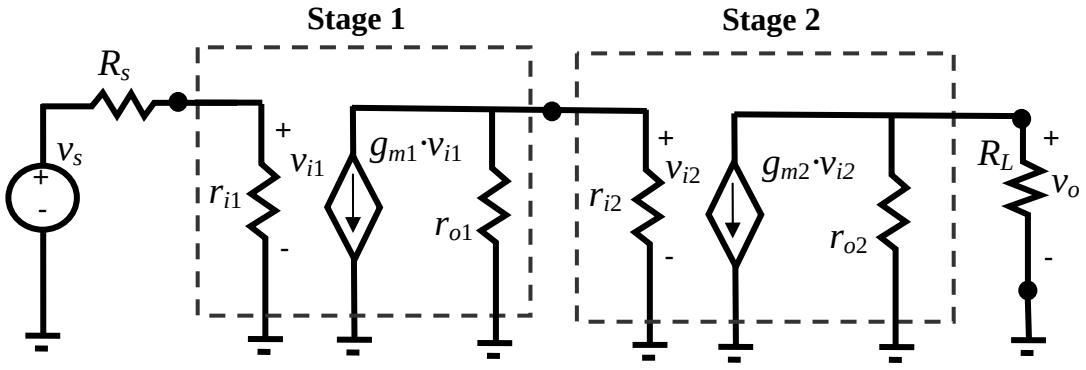


Figure 1.1.

(b) Figure 1.2 shows a circuit which comprises a forward-biased diode at room temperature with an ideality factor $n = 1$, and three resistors R_1, R_2, and R_3, where $R_1 = R_2 = R_3 = 1$ kΩ. There is also one voltage source V_a. In the absence of small signal, $V_a = V_A = 2$ V.

(i) Find the Thevenin's Equivalent of the circuit in the dashed box in the absence of small signal. (3 marks)

(ii) Assume that the voltage V_D across the diode is 0.7 V. Find the value of the DC diode current I_D. (2 marks)
Hint: Use the Thevenin's Equivalent circuit obtained in (i).

(iii) What is the DC voltage at node B? (2 marks)

(iv) What is the DC current flowing through R_1? (2 marks)

(v) What is the DC current flowing through R_2? (2 marks)

Now, we consider the presence of a small signal v_a. $V_a = V_A + v_a = 2\text{V} + v_a$.

(vi) What is the small-signal equivalent resistance r_d for the diode? (2 marks)

(vii) Draw the small-signal equivalent circuit for Figure 1.2. (4 marks)

(viii) Express v_d in terms of v_a, R_1, R_2, R_3, and r_d. (3 marks)

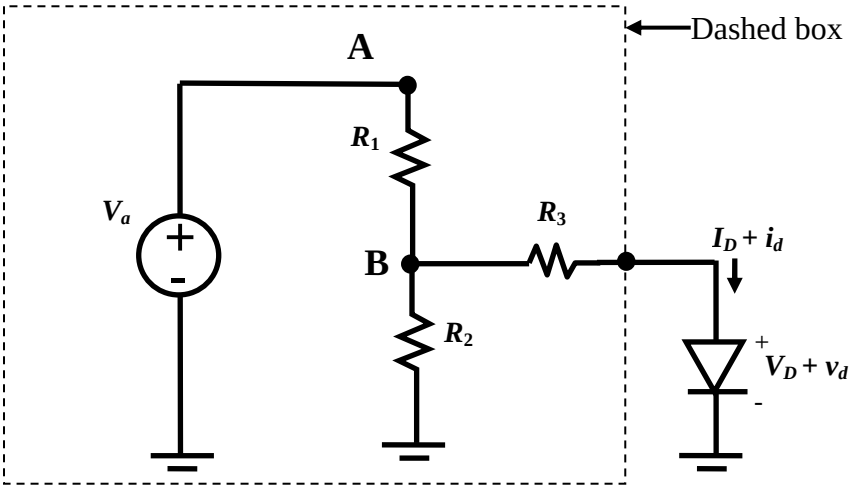


Figure 1.2.

Q. 2 (a) (i) State the logic function Y implemented by the circuit in Figure 2.1, that is, express Y in terms of A, B, C, D, and E. (4 marks)

(ii) Draw the Pull-Down Network for the logic circuit in Figure 2.1. (5 marks)

(iii) State the logic function Y implemented by the circuit in Figure 2.2, that is, express Y in terms of A, B, C, D, and E. (4 marks)

(iv) Draw the Pull-Up Network for the logic circuit in Figure 2.1. (5 marks)

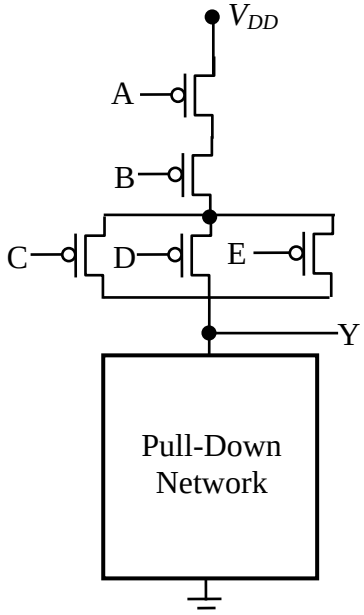


Figure 2.1

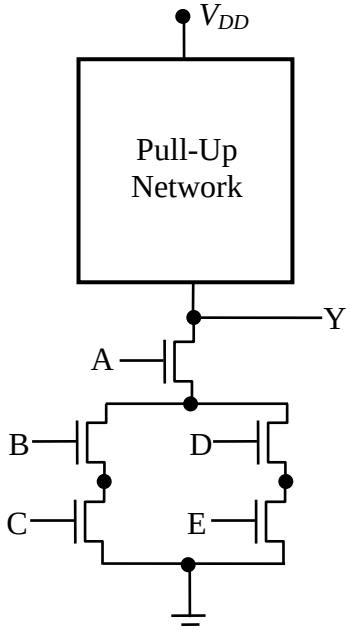


Figure 2.2

(b) A three-input logic gate implementing $\overline{X} = A \cdot (B + C)$ (Figure 2.3) is constructed using minimum-sized transistors for all transistors, i.e. $(W/L)_{min}$, for all six n-channel and p-channel transistors.

We shall compare the dynamic performance of the logic gate of Figure 2.3 with that of a symmetric inverter where $(W/L)_N = (W/L)_{min}$, and $(W/L)_P = (\mu_n/\mu_p)(W/L)_N = 2.5(W/L)_{min}$. The symmetric inverter has a high-to-low propagation delay $t_{PHL(inv)}$ equal to its and low-to-high propagation delay $t_{PLH(inv)}$.

(i) How much longer will the logic gate's high-to-low propagation delay $t_{PHL(X)}$ be compared to that of the symmetric inverter? Give the best case and worst case values if appropriate. (4 marks)

(ii) What is the best possible low-to-high propagation delay $t_{PLH(X)}$ for this logic gate, expressed in terms of the low-to-high propagation delay $t_{PLH(inv)}$ of the symmetric inverter? (3 marks)

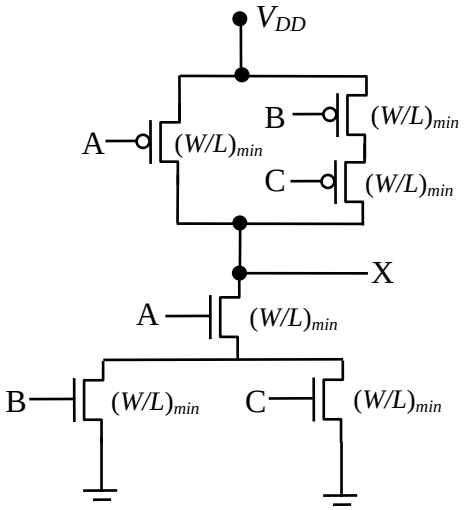


Figure 2.3

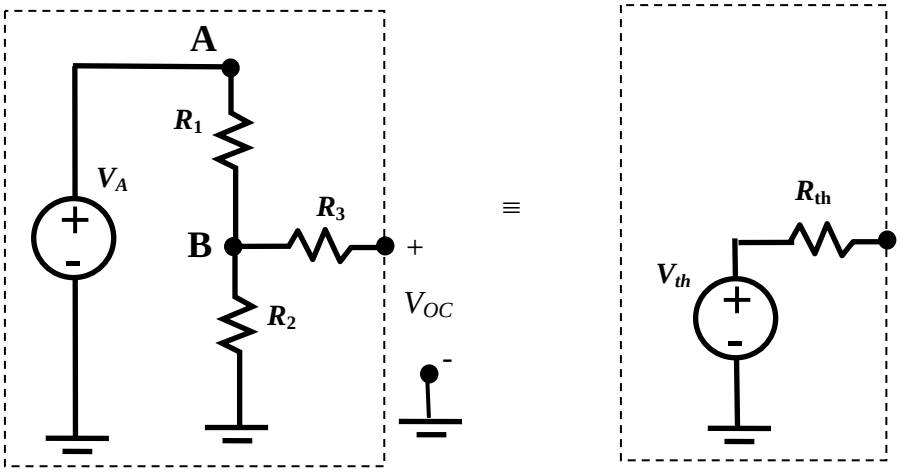
Q. 1(a)

$$v_{i1} = [r_{i1}/(r_{i1} + R_s)]v_s$$
$$v_{i2} = -g_{m1} \cdot v_{i1} \, (r_{o1} // \, r_{i2})$$
$$v_o = -g_{m2} \cdot v_{i2} \cdot (r_{o2} // \, R_L)$$
$$= -g_{m2} \cdot (r_{o2} // \, R_L) \cdot [-g_{m1} \cdot (r_{o1} // \, r_{i2})] \cdot [r_{i1}/(r_{i1} + R_s)]v_s$$

$$(v_o/v_s) = g_{m1}g_{m2} \cdot [r_{o2} \, R_L /(r_{o2} + R_L)] \cdot [r_{o1} \, r_{i2} /(r_{o1} + r_{i2})] \cdot [r_{i1}/(r_{i1} + R_s)]$$

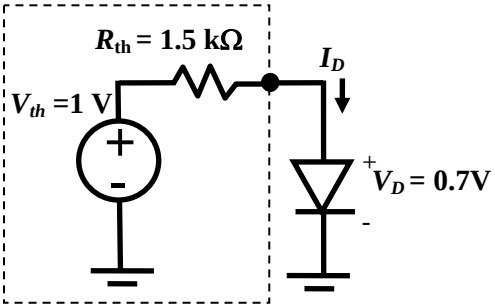
(5 marks)

Q. 1(b) (i) Thevenin's equivalent circuit is obtained as follows.



The Thevenin's voltage or open-circuit voltage is
$V_{th} = V_{OC} = [R_2/(R_1 + R_2)] \cdot V_A = 1$ V.
$R_{th} = R_3 + (R_1//R_2) = 1.5$ kΩ. (3 marks)

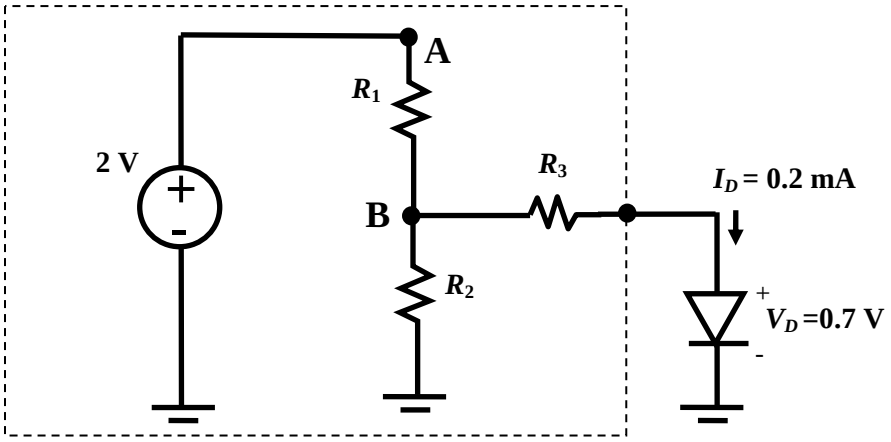
(ii)



Voltage across R_{th} = (1 – 0.7)V
= 0.3 V

I_D = 0.3V/1.5kΩ = 0.2 mA
(2 marks)

(iii) The DC biasing condition for the circuit is shown here:



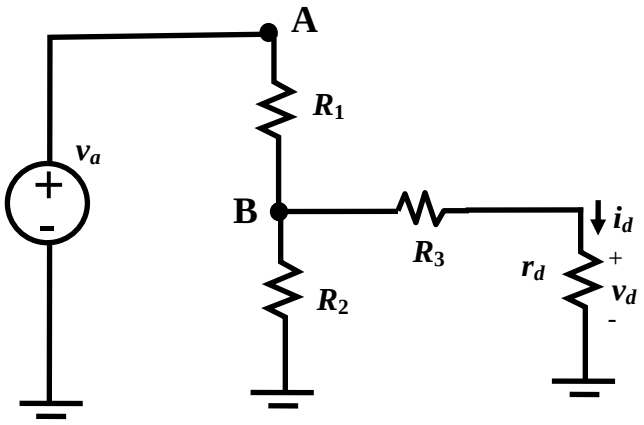
DC Voltage at node B with respect to the ground $V_B = I_D R_3 + V_D$
$= (0.2\text{mA})(1\ \text{k}\Omega) + 0.7\text{V}$
$= 0.9\ \text{V}$
(2 marks)

(iv) The current flowing through $R_1 = (V_A - V_B)/R_1 = (2 - 0.9)\text{V}/1\ \text{k}\Omega$
$= 1.1\ \text{mA}$ (2 marks)

(v) The current flowing through $R_2 = V_B/R_2 = 0.9\text{V}/1\ \text{k}\Omega$
$= 0.9\ \text{mA}$ (2 marks)

(vi) The small signal resistance for the diode $r_d = V_T/I_D$
$= 0.025\text{mV}/0.2\text{mA}$
$= 12.5\ \Omega$ (2 marks)

(vii) The small signal equivalent circuit is shown here:



(4 marks)

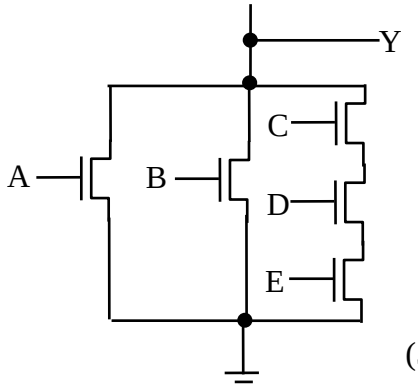
(viii)

$$v_d = \frac{R_2//(R_3 + r_d)}{R_1 + [R_2//(R_3 + r_d)]} \cdot \frac{r_d}{R_3 + r_d} v_a$$ (3 marks)

Q. 2. (a) (i) Examining the Pull-Up Network,

$$Y = \overline{A} \cdot \overline{B} \cdot [\overline{C} + \overline{D} + \overline{E}\,] \qquad \text{(4 marks)}$$

(ii) The Pull-Down Network for the logic circuit in Fig. 2.1 should be:



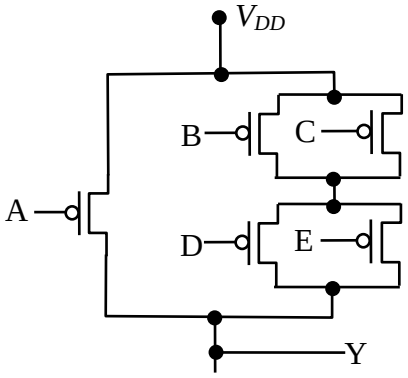
(5 marks)

(iii) Examining the Pull-Down Network,

$$\overline{Y} = A \cdot (B \cdot C + D \cdot E)$$

$$Y = \overline{A \cdot (B \cdot C + D \cdot E)} \qquad \text{(4 marks)}$$

(iv) The Pull-Up Network for the logic circuit in Fig. 2.2 should be:



(5 marks)

(b)(i) Consider the high-to-low dynamic operation of the logic gate.

- In the best case, all N-MOSFETs are turned on. Transistors B and C (which are in parallel) will be turned on. The effective W/L of the parallel combination of B and C will be $2(W/L)_{min}$. This is in series with transistor A.

  During the high-to-low dynamic operation,
  $(W/L)_{eq} = \{[(W/L)_{min}]^{-1} + [2(W/L)_{min}]^{-1}\}^{-1} = (2/3)\ (W/L)_{min}$

  Therefore, we deduce that in the best case,
  $$t_{PHL\ (X)} = (3/2)\ t_{PHL(inv)}$$ (2 marks)

- In the worst case, Transistor A is turned on, and either Transistor B or Transistor C are turned on. During the high-to-low dynamic operation,
  $(W/L)_{eq} = \{[(W/L)_{min}]^{-1} + [(W/L)_{min}]^{-1}\}^{-1} = (1/2)\ (W/L)_{min}$

  Therefore, we deduce that in the worst case,
  $$t_{PHL\ (X)} = 2\ t_{PHL(inv)}$$ (2 marks)

(b)(ii) Consider the best case low-to-high dynamic operation of the logic gate.
All P-MOSFETs with a size of $(W/L)_{min}$ are turned on.

Transistors B and C in series gives $0.5(W/L)_{min}$.

$(W/L)_{eq} = [(W/L)_{min}] + [0.5(W/L)_{min}] = 1.5\ (W/L)_{min}$

We know that $t_{PLH} \propto 1/(W/L)_{eq}$. Thus, we have
$t_{PLH(X)} = t_{PLH(inv)}[2.5(W/L)_{min}]/[1.5(W/L)_{min}] = 1.67\ t_{PLH(inv)}$. (3 marks)