NATIONAL UNIVERSITY *of* SINGAPORE

Department of Electrical and Computer Engineering

EE2021 – Devices and Circuits

Homework 4

Homework 4:

You have to submit the homework assignment (Q.1) in hardcopy in class on Wednesday 8 April 2015.

Unless otherwise stated, you may use the tables of the amplifier configurations and equivalent resistances in your lecture notes in your solutions to the questions.

Q.1

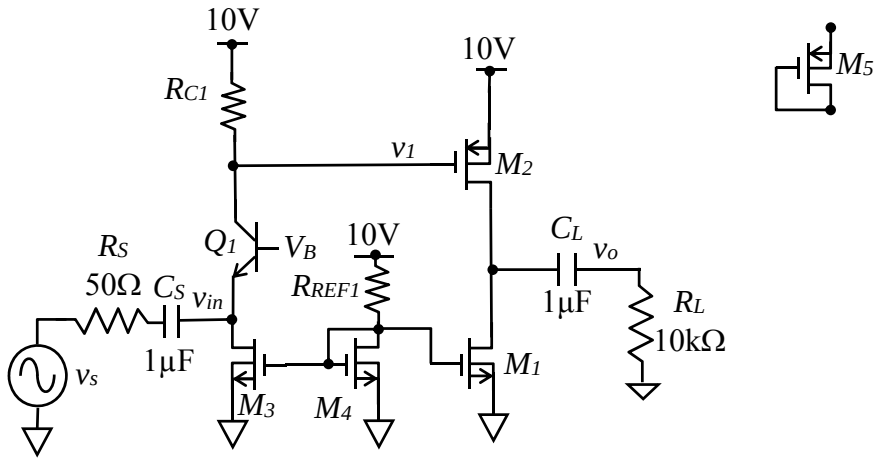

Fig. Q1

In the two-stage amplifier circuit shown in Fig. Q1, assume that the npn BJT, the NMOS transistors and the PMOS transistors have the following device parameters:

- V_A = 100 V and β = 100 for the BJT, Q_1;
- K_n = 2m A/V^2, V_{THN} = 1 V, λ_n = 0.001V^{-1} and no body effect for the NMOS transistors, M_1, M_3 and M_4.
- K_p = 2m A/V^2, V_{THP} = -1 V, λ_p = 0.001V^{-1} and no body effect for the PMOS transistors, M_5 and M_2.

Further assume that R_{REF1} is chosen such that M_1, M_3 and M_4 each has a drain current of 1 mA. (You are not required to find R_{REF1}.)

(i) Identify the configuration of each stage of the multi-stage amplifier.

[2 marks]

(ii) Estimate the small signal parameters of M_2, i.e. $g_{m,M2}$, and $r_{o,M2}$ and the small signal parameters of Q_1, i.e., $g_{m,Q1}$, $r_{\pi,Q1}$, $r_{o,Q1}$.

[3 marks]

(iii) Design R_{C1} to ensure that M_2 has the same current as M_1 assuming these transistors are operating in the saturation region.

[2 marks]

(iv) Estimate the overall gain, i.e., v_o/v_s.

[6 marks]

(v) What is the minimum V_B value allowed such that M_3 is operating in the saturation region?

[4 marks]

(vi) If R_{C1} is replaced with M_5, would it create any biasing issue? Would the overall gain be larger or smaller?

[3 marks]