EE2021 : Devices and Circuits

Groups and Module Lecturers :

- **Group 1 : Room E3-06-08**

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  – **Tel : 6516 1628;**

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- **Group 2 : Room E3-06-07**

  Dr Tan Leng Seow

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  – **Office : E4-05-05.**

- **Group 3 : Room E3-06-09**

  Dr Chor Eng Fong

  – **Email : elecef;**

  – **Tel : 6516 2294;**

  – **Office : E4-06-15.**

- **Group 4 : Room E5-03-19**

  Dr Daniel Chan

  – **Email : elecshd;**

  – **Tel : 6516 2117;**

  – **Office : E4-05-23.**

Class Schedules

1. Lectures

- 4 hours per week of lectures and tutorials.

- Schedule:
  - Mondays 9.00 – 11.00 am
  - Wednesdays 12.00 noon – 2.00 pm

- Note : Many Wednesdays will be used for lectures; not all tutorials are on Wednesdays.

- There will be two lectures to be held on Saturdays to make up for those that will be missed on public holidays. Please refer to module schedule on IVLE for details,

2. Tutorials

- Total of 5 Tutorials (9 hours). See Schedule posted in IVLE Workbin for the dates of the tutorials.

3. No Laboratory Experiments

Assessments

- **Homework : 15%**
  - 4 sets of homework in total, each comprising 1 - 2 questions.
  - Each homework assignment with be posted about 2 weeks before due date for submission.
  - Homework must be submitted immediately after class on the due date.
  - The homework will be graded and returned during the following week.
  - Homework submission must be in hard copy and hand-written. Plagiarism will not be tolerated.
- **Mid-term Quiz : 20%**
  - Tentatively scheduled around mid-October (after the mid-semester break).
- **Final Exam : 65%**
  - Scheduled on 2 December 2014, 1.00 pm.
  - Duration of exam paper is 2.5 hours
  - Closed book, but an extensive list of formulas will be provided.

Module Learning Outcomes

After completing this module, students should be able to:

1. Apply the bond model of semiconductors to explain physical processes in semiconductors such as the origin of electrons and holes, doping, carrier motion.

2. Describe the I-V characteristics of p-n junctions, bipolar transistors and MOSFETs respectively, and to explain the physical mechanisms underlying their operation.

3. Explain the equivalent circuit models of p-n junctions, bipolar transistors and MOSFETs respectively, and to apply these models for circuit analysis.

4. Construct CMOS logic circuits from given logic functions and to derive the appropriate logic function from a given CMOS logic circuit.

5. Analyze and design multi-stage amplifier circuits to meet the desired specifications of gain, and input and output resistances.

6. Analyze an operational amplifier circuit and to synthesize a circuit which implements a given function.