EE2021 / EE2021 E : Device and Circuits

Semester 1, AY2012/2013

Q.1 A piece of silicon is uniformly doped with two dopants, X and Y, together. It is known that X is a donor with concentration of 3.1×10^{16} cm^{-3}, and that the mobilities of the electrons and holes in the silicon sample, μ_n and μ_p , are 900 cm^2 V^{-1} s^{-1} and 300 cm^2 V^{-1} s^{-1}, respectively.

It is found that the conductivity of the silicon sample is 5.77 (Ω cm)$^{-1}$.

a) If Y is a donor, what would be the concentration of Y? _______________ **[2 marks]**

b) If Y is an acceptor, what would be the concentration of Y? _____________ **[3 marks]**

$$N_{D,Y} = 9.02 \times 10^{15}\ cm^{-3}$$
$$N_{A,Y} = 1.51 \times 10^{17}\ cm^{-3}$$

Q.2 Consider a pn junction diode under forward bias condition. Which of the following statements are correct? (Circle either True or False) **[5 marks]**

(i) There is a net current flowing from the p-side to the n-side. (True/False)

(ii) The depletion layer width has increased with respect to that under open circuit condition. (True/False)

(iii) The barrier voltage across the depletion layer has decreased with respect to that under open circuit condition. (True/False)

(iv) The junction capacitance, C_j, is greater than that under open circuit condition. (True/False)

(v) The electric field in the depletion region points from the p-side to the n-side. (True/False)

Q.3 Consider an npn bipolar junction transistor (BJT) biased in the forward active mode. Which of the following statements are correct? (Circle either True or False) **[5 marks]**

(i) The collector current depends strongly on the base-emitter junction voltage, v_{BE}. (True/False)

(ii) The collector current depends strongly on base-collector junction voltage, v_{BC}. (True/False)

(iii) The emitter current depends strongly on the base-collector junction voltage, v_{BC}. (True/False)

(iv) Electrons are injected from the collector into the base. (True/False)

(v) Electrons are injected from the emitter into the base. (True/False)

Q.4 Consider the circuit shown in Fig. Q4. Draw the small signal equivalent circuit for AC analysis by replacing transistors with hybrid-pi model. **[5 marks]**

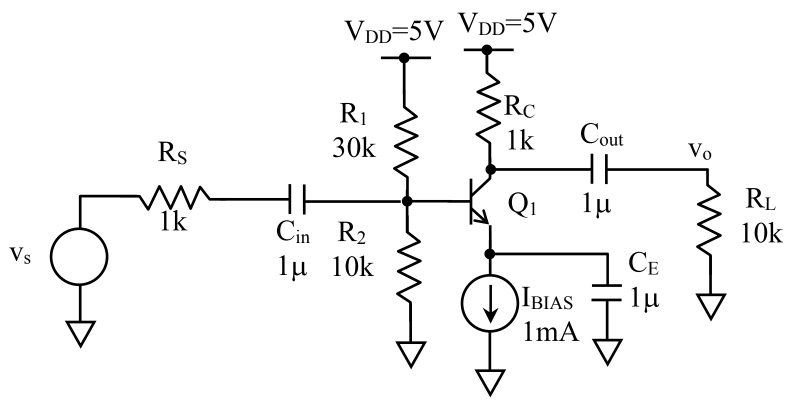


Fig. Q4.

No numerical answer

Q.5 Consider a metal-oxide-semiconductor field effect transistor (MOSFET) operating in the linear region. Which of the following statements are correct? (Circle either True or False)

[5 marks]

(i) The magnitude of the gate-to-source voltage, $|V_{GS}|>|V_{TH}|$, where V_{TH} is the threshold voltage. (True/False)

(ii) The magnitude of the drain-to-source voltage, $|V_{DS}|>|V_{GS}|-|V_{TH}|$. (True/False)

(iii) There is current flow between the source and gate. (True/False)

(iv) There is current flow between the source and drain. (True/False)

(v) The channel is pinched off at the drain end. (True/False)

Q.6 Consider the PMOS circuit shown in Fig. Q6. Determine which of the following resistors combination will result in transistor operate in saturation region. You may assume the following PMOS device parameters: **[5 marks]**

- K_p=2mA/V^2, V_{THP}=-1V, λ_p=0.001 and no body effect

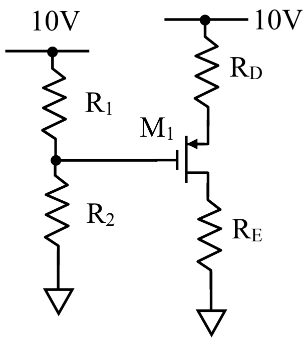


Fig. Q6

(i) R_1=2k, R_2=8k, R_D=0, R_E=0. (Yes/No)

(ii) R_1=60k, R_2=40k, R_D=2k, R_E=2k. (Yes/No)

(iii) R_1=40k, R_2=60k, R_D=5k, R_E=13.8k. (Yes/No)

Q.7 Consider the pull-up network shown in Fig. Q7. Write down the corresponding logic function.

Y=______________________________ **[5 marks]**

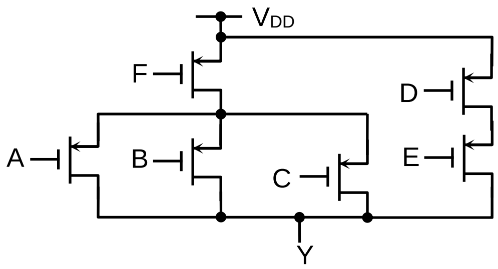


Fig. Q7

No numerical answer

Q.8 Assume the PMOS transistors used in (Q.7) has size of p and PMOS of inverter with size of p has the following propagation delay, $t_{plh,inv}$, estimate the $t_{plh,logic,best}$ of the above pull-down network in terms of $t_{plh,inv}$. **[5 marks]**

$$t_{plh,logic,best} = \frac{4}{5} t_{plh,inv}$$

Q.9 Consider the circuit shown in Fig. Q9.

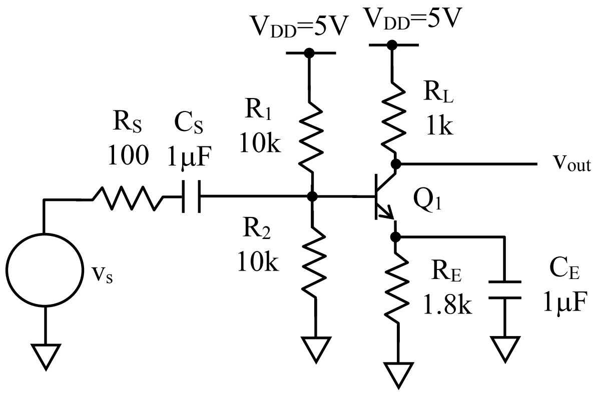


Fig. Q9.

Assume $I_S=10^{-15}$, $\beta=100$ and $V_A=100V$, **[5 marks]**

a) Calculate $I_{C,Q1}$.

$$I_{C,Q1} \approx 1mA$$

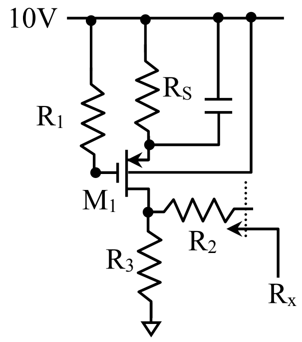
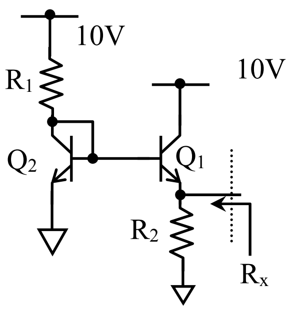
b) What would be $I_{C,Q1}$ if $R_1=1M\Omega$ and $R_2=1M\Omega$?

$$I_{C,Q1} = 264\mu A$$

c) Calculate the overall gain, v_{out}/v_s for $I_{C,Q1}$ in (a).

$$\frac{v_{out}}{v_s} = -37.74$$

Q.10 Assume the AC small signal parameters for BJT are $g_{m,Qi}$, $r_{\pi,Qi}$, $r_{o,Qi}$, and the AC small signal parameters for MOSFET are $g_{m,Mj}$, $g_{mb,Mj}$, $r_{i,Mj}$, $r_{o,Mj}$, where i and j are the corresponding device indices. Write down the expression for the small signal AC equivalent resistance (R_x) of the following configurations: **[10 marks]**

	No numerical answer
	No numerical answer

Q.11 The junction capacitance, C_j, of a pn junction diode at a given bias voltage, V, is given by the following expression -

$$C_j = A\sqrt{\frac{q\varepsilon_S}{2}\left[\frac{N_A N_D}{N_A + N_D}\right]\frac{1}{(V_0 - V)}},$$

where A is the cross-sectional area of the junction, q is the electronic charge = 1.602×10^{-19} C, N_A is the acceptor concentration of the p-side, N_D is the donor concentration of the n-side, and V_0 is the built-in voltage of the junction. In the above expression, ε_s is the permittivity of semiconductor = $11.7\varepsilon_0$ for silicon, where ε_0 is the permittivity of free space = 8.854×10^{-14} F/cm.

For a silicon p^+n junction diode (i.e., $N_A >> N_D$) at T = 300 K, C_j is measured to be 1.3×10^{-12} F at a reverse bias, V = - 0.05 V. The junction area, $A = 10^{-5}$ cm^2 and the built-in voltage, V_0 = 0. 95 V.

(a) Show that for a p^+n junction diode,

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(3 marks)

$$C_j = A\sqrt{\frac{q\varepsilon_s N_D}{2}\frac{1}{(V_0 - V)}}$$

(b) Using the result in part (a), find the doping concentration of the lightly-doped side of the p^+n junction diode. (4 marks)

$N_D = 2.04\times10^{17}$ cm^{-3}

(c) Find the doping concentration of the heavily-doped side of the p^+n junction diode. (3 marks)

$N_A = 3.5\times10^{19}$ cm^{-3}

Q.12

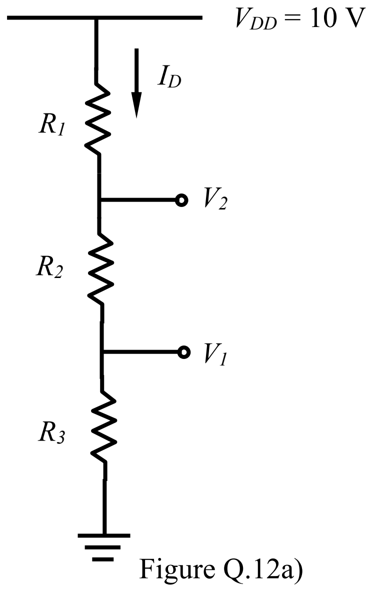

Figure Q.12a)

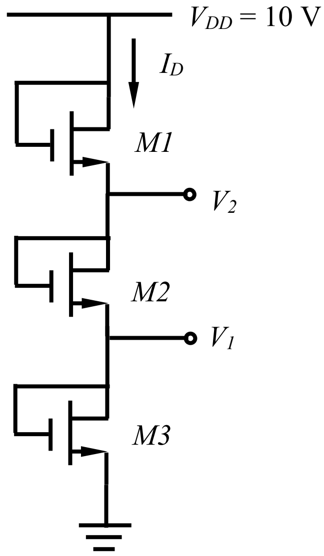

Figure Q.12(b)

(a) In the resistor network shown in Fig. Q.12(a), determine the values of R_1, R_2, and R_3 such that I_D = 0.5 mA, V_1 = 2.5 V, V_2 = 6.5 V.

(2 marks)

$$R_3 = 5k \quad R_1 = 7k \quad R_2 = 8k$$

(b) The function of the resistor network in Fig. Q.12(a) can also be implemented using MOSFETs, as shown in Fig. Q.12(b).

All the n-channel MOSFETs have $\mu_n C_{ox}$ = 60 × 10^{-6} A/V^2, V_{TH} = 1 V, λ = 0 and no body effect, but they have different ratios of (W/L), where W is the width, and L the length, of the MOSFET respectively.

Show that all the transistors are operating in the saturation region.

(2 marks)

No numerical answer.

Design the W/L ratio of each of the MOSFETs to achieve the following : I_D = 0.5 mA, V_1 = 2.5 V, V_2 = 6.5 V.

$$\left(\frac{W}{L}\right)_{M3} = 7.4$$

$$\left(\frac{W}{L}\right)_{M2} = 1.85$$

(6 marks)

$$\left(\frac{W}{L}\right)_{M1} = 2.67$$

Q.13

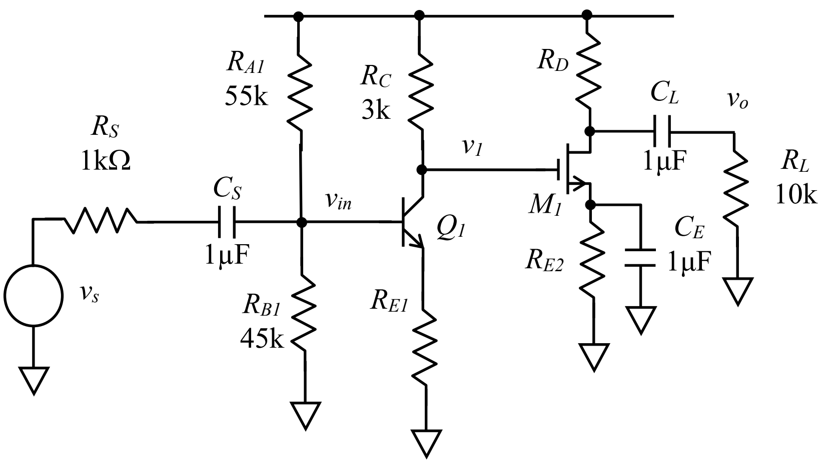

Figure Q.13

Assume that the npn BJT and the NMOS have the following device parameters:

- V_A = 100 V and β = 100 for the BJT, Q_1;
- K_n = 2m A/V^2, V_{THN} = 1 V, λ_n = 0.001 and no body effect for the MOSFET, M_1.

(a) Identify the configuration of each stage of the multi-stage amplifier.

(2 marks)

No numerical answer

(b) Design R_{E1} and R_{E2} to obtain $I_{C,Q1} = I_{D,M1}$ = 1 mA.

$$R_{E1} = \frac{3.8}{1mA} = 3.8k$$

$$R_{E2} = \frac{5.29}{1mA} = 5.29k$$

(4 marks)

(c) Calculate the small signal parameters for Q_1 and M_1.

$$g_{m,Q1} = 40mA/V \quad r_{\pi,Q1} = 2.5k \quad r_{o,Q1} = 100k$$

$$g_{m,M1} = 2.8mA/V \quad r_{o,M1} = 1M$$

(2 marks)

(d) Write down the overall gain expression in terms of transistors' small signal parameters and circuit components, i.e., v_o/v_s. (4 marks)

No numerical answer

Q.14 (a) The output voltage of a temperature sensor as a function of time is given as $v_{TEMP}(t)$. Write down the expression for the time average of $v_{TEMP}(t)$ over a time period T. (3 marks)

No numerical answer

(b) Consider the opamp circuit shown in Fig. Q.14. The output voltage, $v_{OUT}(t)$, will be reset to zero by closing the switch (S) periodically at the end of every period T.

Write down the relation between T, R and C such that $v_{OUT}(t)$ can be used to estimate the time average of $v_{TEMP}(t)$, where R is the resistor and C is the capacitor. (5 marks)

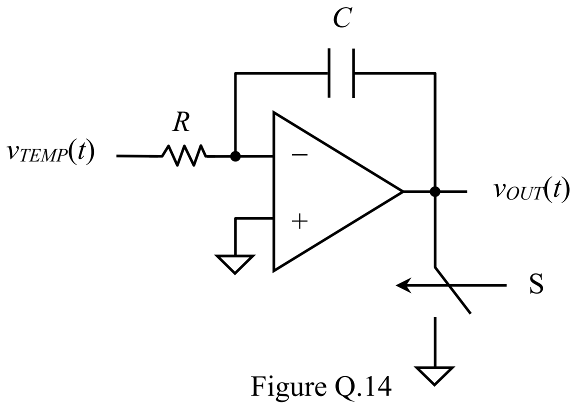

Figure Q.14

No numerical answer

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