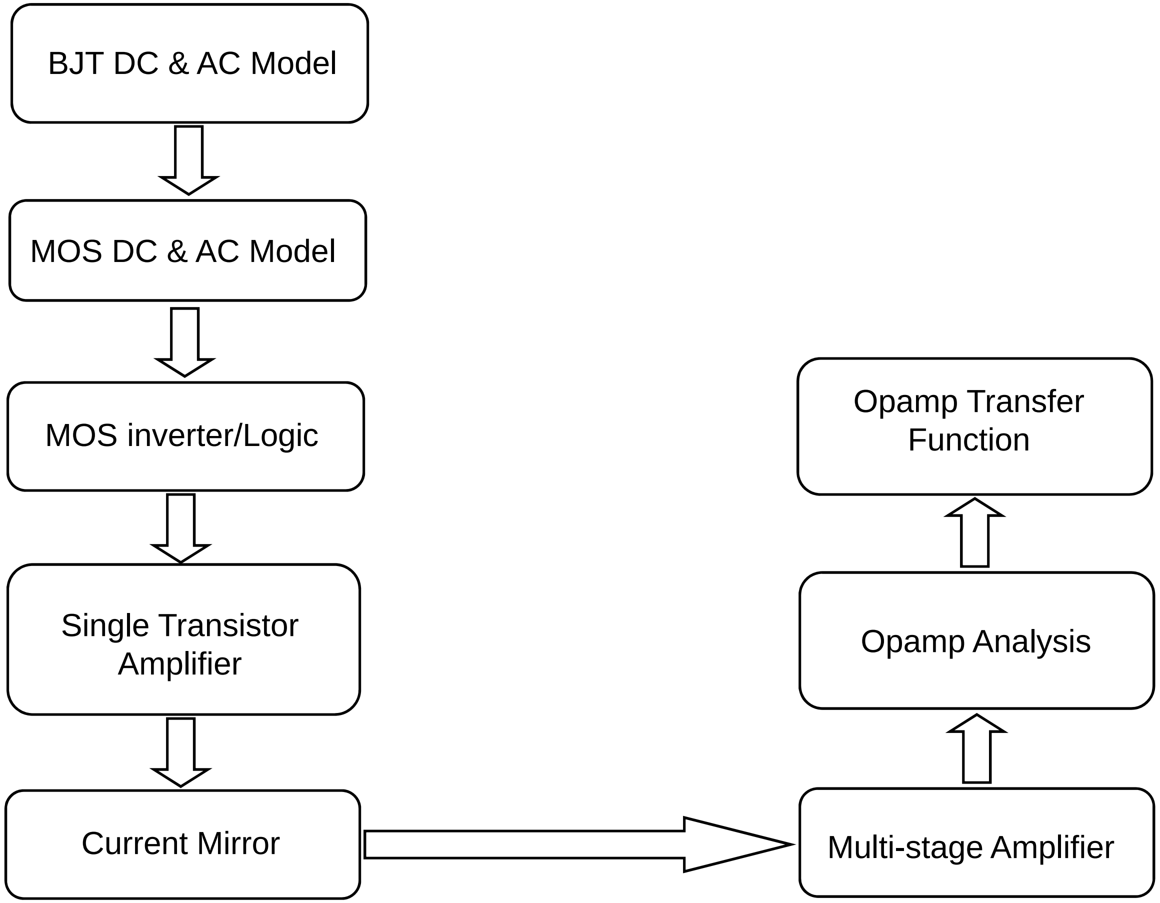
EE2021
Devices and Circuits

Revision

Summary on Materials Covered



Rev-2

Logic Synthesis

$$Y = \overline{(A+B+C)\cdot(D+E)\cdot(F+G)}$$

$=$

Hint: Demorgan Theorem

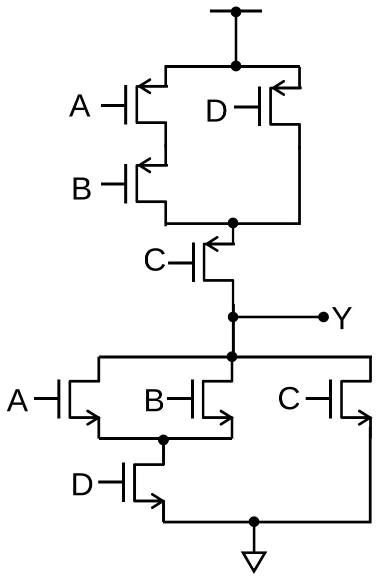
$=$

Pull Down Network

Pull Up Network (Duality)

Rev-3

Logic Function

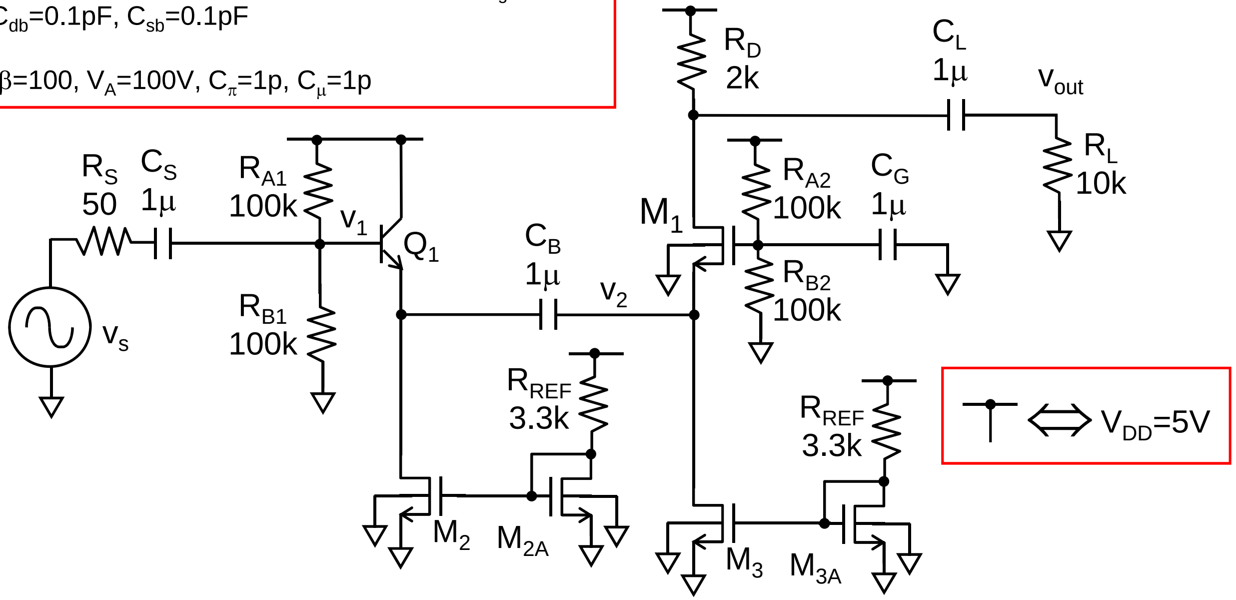


$Y =$

Rev-4

DC Analysis : Identifying

NMOS :
K_n=2mA/V^2, V_{THN0}=1V, λ_n=0.01V^{-1}, γ_n=0.5, $2\phi_f$=0.6, C_{gd}=1pF, C_{gs}=1pF, C_{db}=0.1pF, C_{sb}=0.1pF
BJT :
I_S=10^{-15}A, β=100, V_A=100V, C_π=1p, C_μ=1p



- Identify AC source, load and non-ideal current source

DC Analysis : DC Biasing

NMOS :
K_n=2mA/V^2, V_{THN0}=1V, λ_n=0.01V^{-1}, γ_n=0.5, $2\phi_f$=0.6, C_{gd}=1pF, C_{gs}=1pF, C_{db}=0.1pF, C_{sb}=0.1pF
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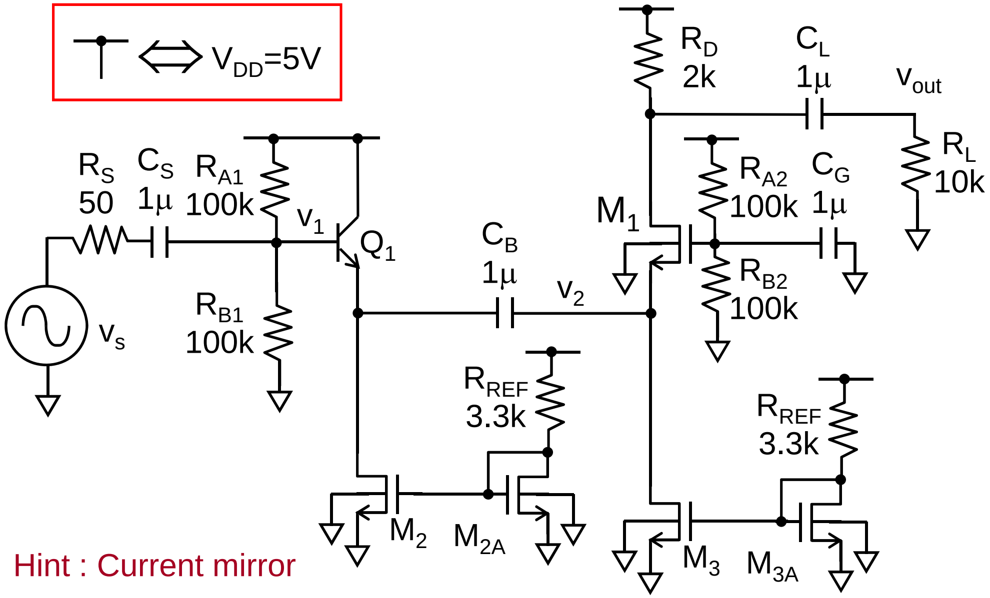


Hint : Current mirror

- Find the DC biasing current for Q_1 and M_1

Determine DC Biasing

$I_{D,M2A} =$

$I_{D,M2A} =$

$\Rightarrow I_{C,Q1} \approx$

$\Rightarrow I_{D,M1} =$

Rev-6

AC Analysis : Simplify the Circuit and Find Out AC Small Signal Parameter

Replace current mirror with non-ideal current source

Simplify the circuit for AC analysis

Determine AC small signal parameter

$g_{m,M1} =$

$g_{mb,M1} =$

$r_{o,M1} = r_{o,M3} = r_{o,M2} =$

$g_{m,Q1} =$

$r_{\pi,Q1} =$

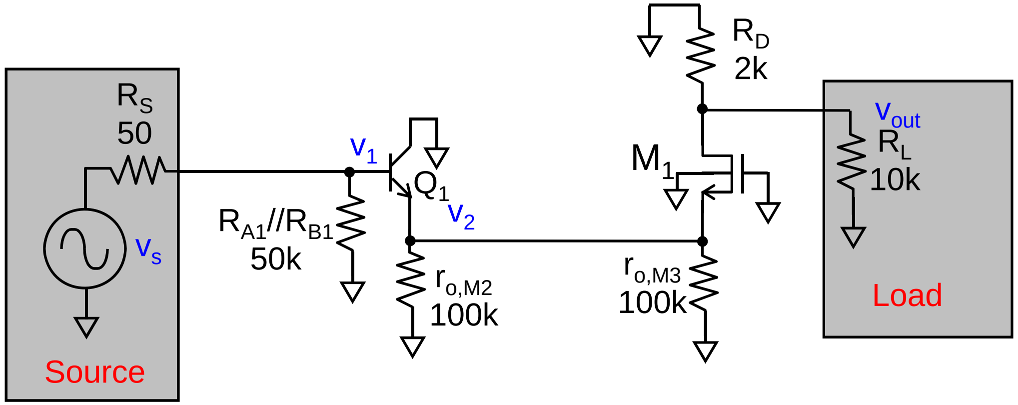
$r_{o,Q1} =$

Hint :

1) DC voltage source→AC ground
2) DC current source→Open circuit
3) DC block/bypass capacitor→AC short circuit

- Simplify the circuit for AC analysis by replacing current mirror with non-ideal current source
- Find out the AC small signal parameters (g_m, r_π, r_o) for transistors Q_1, M_1, M_2, M_3

AC Analysis : Identify Amplifier



1^{st} stage amplifier configuration :

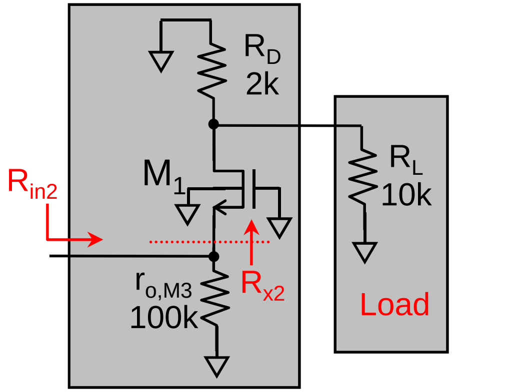
2^{nd} stage amplifier configuration :

1^{st} stage amplifier G_{m1} :

2^{nd} stage amplifier G_{m2} :

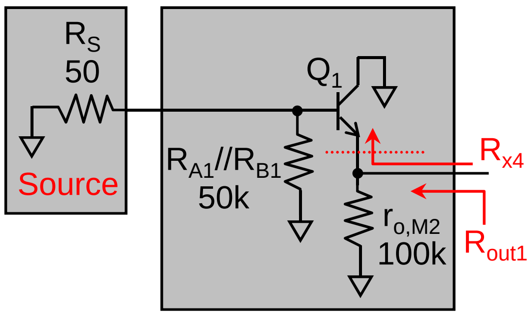
- Identify the 1^{st} and 2^{nd} stage amplifiers by drawing rectangular box surrounding them
- Write down the corresponding two ports-network parameters

AC Analysis : Identify Two-ports Network Parameters (R_{in2}, R_{out1})



$R_{x2} =$

$R_{in2} =$

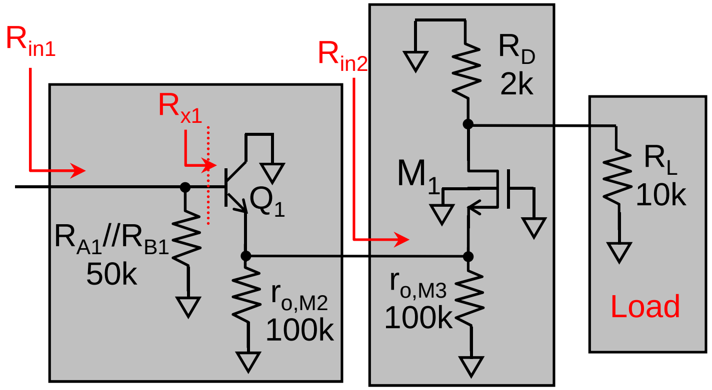


$R_{x4} =$

$R_{out1} =$

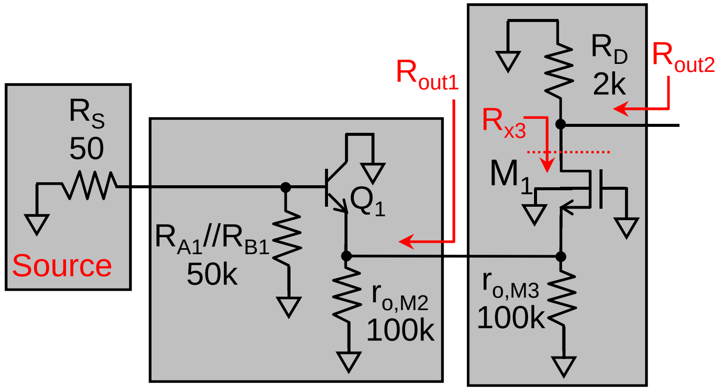
- Estimate R_{in2} and R_{out1} (Throw away half the circuit)

AC Analysis : Identify Two-ports Network Parameters (R_{in1}, R_{out2})



$R_{x1} =$

$R_{in1} =$

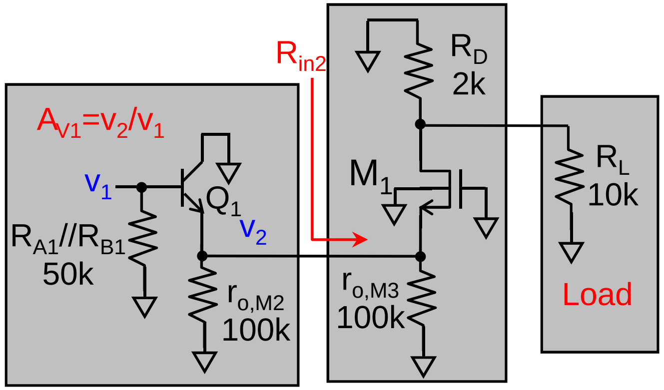


$R_{x3} =$

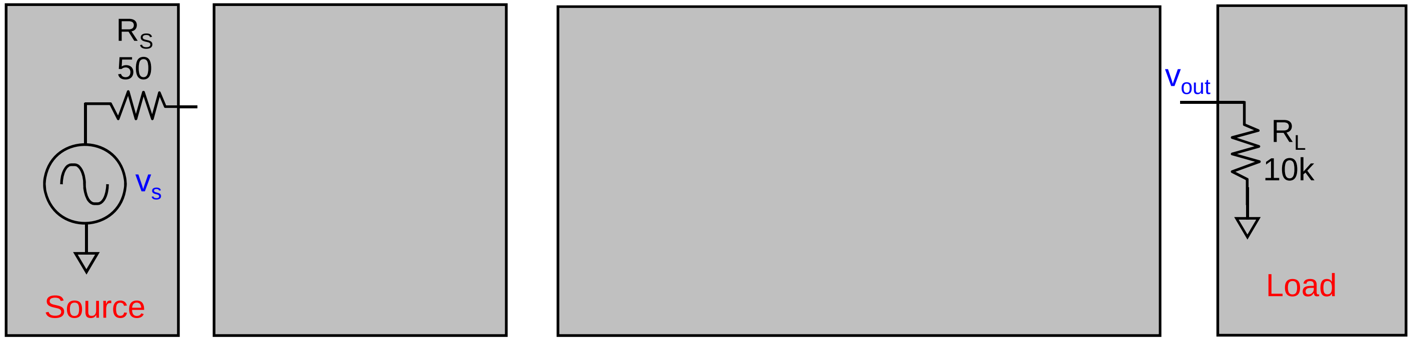
$\Rightarrow R_{out2} \approx$

- Estimate R_{in1} and R_{out2}

AC Analysis : Identify $A_{V1}=v_2/v_1$

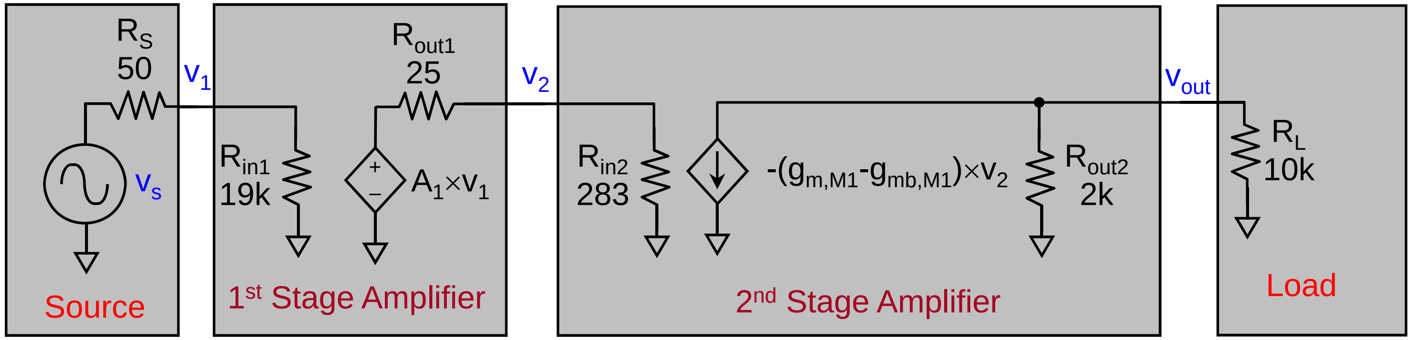


$$A_{V1}=\frac{v_2}{v_1}$$



- Estimate $A_{V1}=v_2/v_1$
- Draw out two-ports network equivalent

AC Analysis : Overall Gain $A_V = v_{out}/v_s$



$$v_1 =$$

$$v_2 =$$

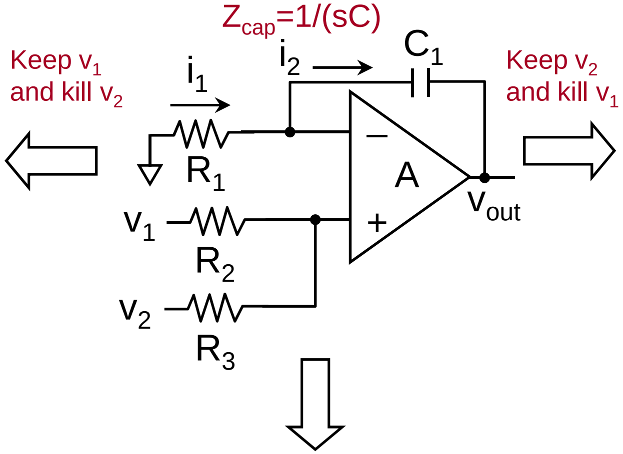
$$v_{out} =$$

$$A_V = \frac{v_{out}}{v_s} =$$

- Estimate overall gain $A_V = v_{out}/v_s$

Opamp Circuit Analysis

Keep v_1 and kill v_2



Keep v_2 and kill v_1

$v_+ =$

$\Rightarrow v_{out} =$

$= v_1 \times$

Superposition :

$v_{out} =$

$v_+ =$

$\Rightarrow v_{out} =$

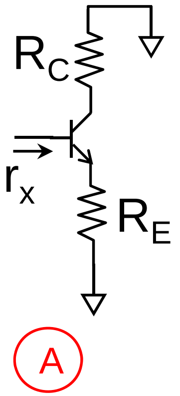
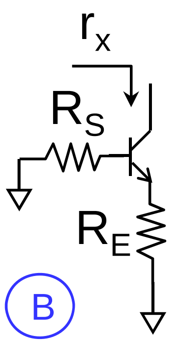
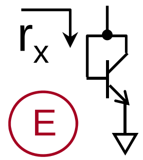
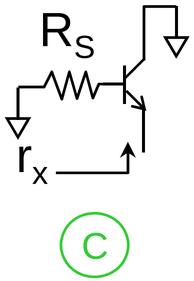
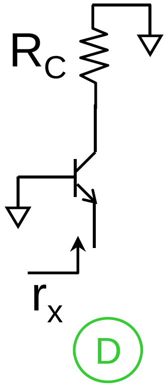
$= v_2 \times$

- Virtual short ($v_+ \approx v_-$)
- Infinite input resistance ($i_+ = i_- = 0$)
- Superposition

Rev-13

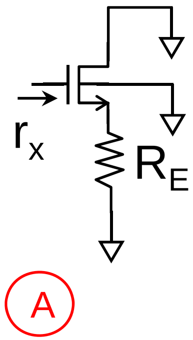
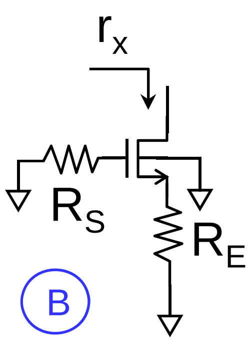
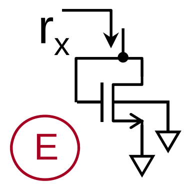
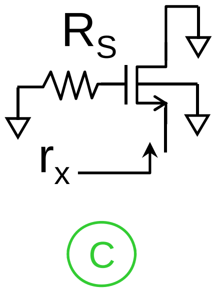
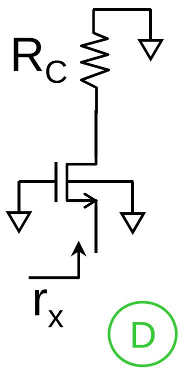
BJT Equivalent Resistance Summary (Table 1)

Blue: look into collector terminal   Red: look into base terminal   Green: look into emitter terminal

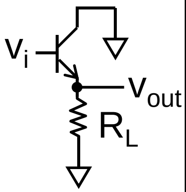
Conf	r_x	Conf	r_x	Conf	r_x
	$r_\pi + (1+\beta)R_E$ $\approx r_\pi(1+g_m R_E)$		$r_o\left\{1+g_m\left[(r_\pi+R_S)//R_E\right]\left(\frac{r_\pi}{r_\pi+R_S}\right)\right\}$ *If* $R_S=0$ *and* $r_\pi << R_E$ $\Rightarrow r_{x,\max} = r_o(\beta+1)$		$\frac{1}{g_m}$
	$\frac{R_S+r_\pi}{1+\beta}//r_o$ $\approx \frac{R_S}{1+\beta}+\frac{1}{g_m}$		$\frac{1}{g_m}\times\frac{r_o+R_C}{r_o+R_C/\beta}$		

MOS Equivalent Resistance Summary (Table 2)

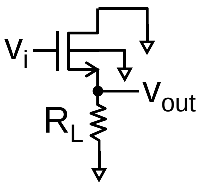
Blue: look into drain terminal   Red: look into gate terminal   Green: look into source terminal

Conf	r_x	Conf	r_x	Conf	r_x
	∞		$r_o\left[1+\left(g_m-g_{mb}\right)R_E\right]$		$\frac{1}{g_m}$
	$\frac{1}{g_m-g_{mb}}$		$\frac{1}{g_m-g_{mb}}\times\frac{r_o+R_C}{r_o}$		

BJT Summary (Table 3)

BJT	G_m	A_V
CE A	g_m	Derive Based on 2-ports Network
CB B	$-g_m$	Derive Based on 2-ports Network
CC C 	Not Applicable	$\dfrac{g_m R_L}{1+g_m R_L}$
CE with Emitter Degeneration D	$\dfrac{g_m}{1+g_m R_E}$	Derive Based on 2-ports Network

MOS Summary (Table 4)

MOS	G_m	A_V
CS A	g_m	Derive Based on 2-ports Network
CG B	$-(g_m - g_{mb})$ $Drop\ \ g_{mb}\ \ if\ \ no\ \ body\ \ effect$	Derive Based on 2-ports Network
CD  C	Not Applicable	$\frac{g_m R_L}{1+(g_m - g_{mb})R_L} \approx \frac{g_m}{g_m - g_{mb}}$ $Drop\ \ g_{mb}\ \ if\ \ no\ \ body\ \ effect$
CS with R_E D	$\frac{g_m}{1+(g_m - g_{mb})R_E}$ $Drop\ \ g_{mb}\ \ if\ \ no\ \ body\ \ effect$	Derive Based on 2-ports Network