NATIONAL UNIVERSITY OF SINGAPORE

Department of Electrical and Computer Engineering

EE2021: Tutorial 3 (*Bipolar Junction Transistors and MOSFETs*)

- Unless otherwise stated, you may assume temperature, $T = 300$ K, thermal voltage, $V_T = 0.025$ V, and silicon intrinsic carrier concentration, $n_i = 1.5 \times 10^{10}$ cm^{-3} and make use of the equations given in the lecture notes directly, without having to derive them.
- All the symbols are as defined in lecture notes.

Homework 2:
Homework 2 is Question 1 and Question 6 of Tutorial 3 and you will need to submit it in class on Wednesday 4 March 2015.

Q1. (a) An npn bipolar junction transistor has been designed with the following parameters:

Doping in the emitter, $N_{DE} = 10^{18}$ cm^{-3},
Doping in the base, $N_{AB} = 2\times10^{16}$ cm^{-3},
Diffusion coefficient of holes in the emitter, $D_p = 1$ cm^2/s,
Diffusion coefficient of electrons in the base, $D_n = 10$ cm^2/s,
Diffusion length of holes in the emitter, $L_p = 0.300$ μm,
Diffusion length of electrons in the base, $L_n = 20$ μm,
Width of the neutral region in the base, $w_B = 1$ μm.

Calculate the collector saturation current density, J_S, and the common emitter current gain, β, of the transistor.

[4 marks]

(b) The transistor in part (a) is required to have a collector current $I_C = 2.5$ mA when it is operating in the forward active region at 300 K with $V_{BE} = 0.65$ V. The Early effect can be assumed to be negligible..

What is the additional design parameter that needs to be specified, and what should be the value of that parameter?

[4 marks]

(c) It is desired to increase the β of the transistor in part(a) to 300 by adjusting one of the above design parameters. Assume that the base doping and the width of the neutral base region, as well as the electron and hole diffusion lengths, remain unchanged. Suggest a change in the design that would achieve the objective.

[2 marks]

Q2. The schematic cross section of a silicon **pnp** bipolar junction transistor (BJT) is shown in Fig. Q2. The doping concentrations of the emitter, base and collector are respectively, $N_{AE} = 2\times10^{19}$ cm^{-3}, $N_{DB} = 5\times10^{17}$ cm^{-3} and $N_{AC} = 5\times10^{15}$ cm^{-3}. You may assume that the emitter, base and collector are each uniformly doped.

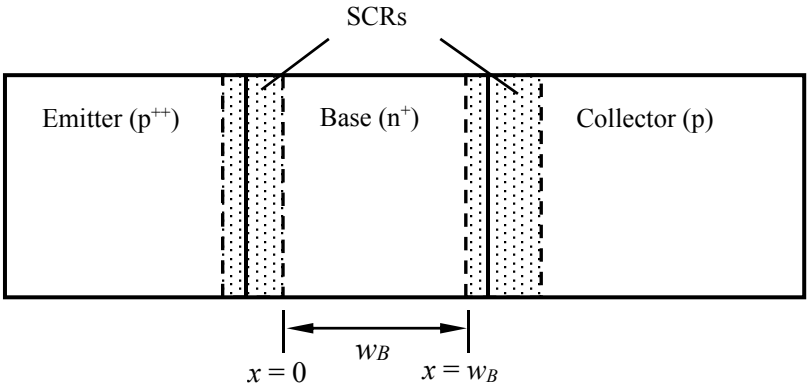


Fig. Q2 : Schematic cross-section of a **pnp** BJT (not to scale).

The transistor is biased in the forward active mode with an emitter-base junction voltage, $V_{EB} = 0.67$ V, and a collector-base junction voltage, $V_{CB} = -2$ V. At these conditions, the width of the neutral part of the base, $w_B = 1$ μm.

In the base, the diffusivity of the holes (minority carriers), $D_p = 9$ cm^2 s^{-1}, and the diffusion length of the holes, $L_p = 30$ μm. The cross-sectional area of the transistor, $A = 10^{-4}$ cm^2.

(a) Calculate the concentrations of the holes (minority carriers) at the edges of the space charge regions (SCRs) in the base, i.e., at $x = 0$ and $x = w_B$.

[Ans. 1.96×10^{14} cm^{-3}, 0 cm^{-3}]

(b) Calculate the magnitude of the collector current. State and justify any approximation that you have used in the calculation.

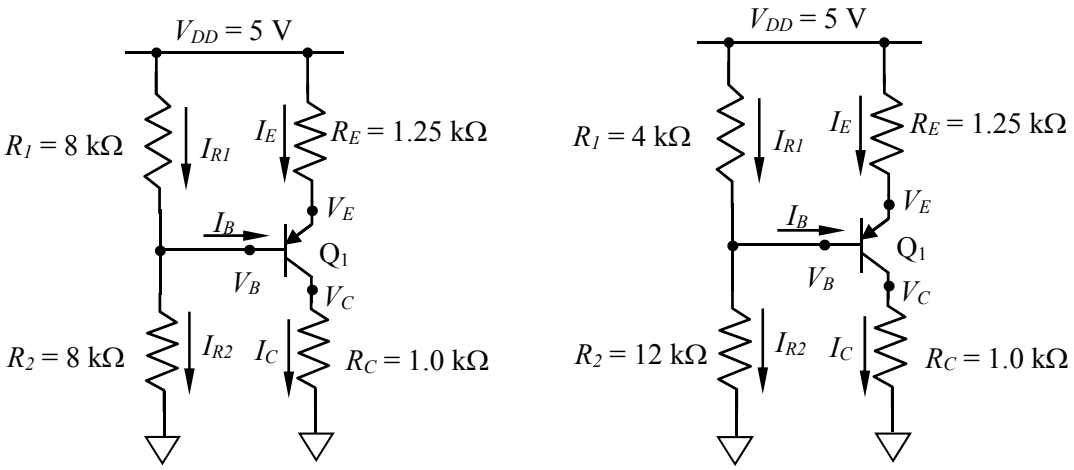
[Ans. 2.83×10^{-4} A]

(c) Discuss (without performing calculations)

(i) whether there is an increase, a decrease, or no change, in the collector current, compared to that in part (b), when V_{CB} is changed to - 5 V from -2 V;
(ii) whether there is an increase, decrease, or no change in the collector current, compared to that in part (b), when the doping in the collector is changed from 5×10^{15} cm^{-3} to 5×10^{17} cm^{-3}. $V_{CB} = -2$ V.

[Hint: observe the trend of the widths of the space-charge regions in Tutorial 2, Question 1.]

Q3. Two BJT circuits are shown in Figure Q3. The transistor, Q_1, in both circuits has β = 100 and V_A = 100 V. You may assume $I_{R1} \approx I_{R2} >> I_B$ for both cases.



(i) (ii)

Fig. Q3

(a) When a BJT is operating in the forward active mode, the typical value assumed for the base-emitter junction voltage is 0.7 V. Is this assumption reasonable? Explain.

(b) Using the assumption of part (a), determine the collector current, I_C, for the circuit shown in Fig. Q3(i).

[Ans. 1.43 mA]

(c) Repeat the calculation of part (b) for the circuit shown in Fig. Q3(ii).

[0.436 mA]

(d) If the actual value of the base-emitter junction voltage of the BJT is 0.8 V, what are the percentage errors incurred in the calculation of I_C in part (b) and part (c), respectively?

[-5.93%, -22.47%]

(e) Based on the results of part (d), discuss the implications of the assumed value of the base-emitter junction voltage of 0.7 V. Can this be resolved using the Thevenin equivalent for the base biasing circuit instead of the assumption of $I_{R1} \approx I_{R2} >> I_B$?

Q4. An n-channel MOSFET M_1 is connected as shown in Fig. 4a to perform I_D - V_{GS} measurements. The V_{GS} is changed by varying V_{DD} and the resulting I_D is measured through an current meter.

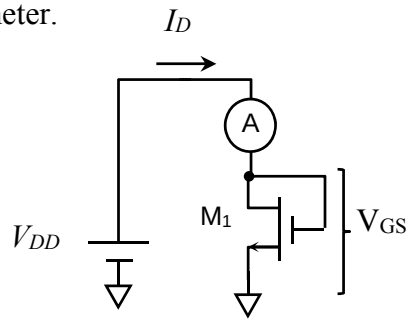


Fig. 4a

(a) Show that the transistor M_1 is operating in saturation region.

(b) The measured I_D - V_{GS} characteristic is shown in Fig. 4b. Also shown is the corresponding tabulated data. Due to experimental error, the measured points do not exactly follow the square law predicted by the drain current equation in the saturation region, i.e., $I_D = K_n (V_{GS}-V_{THN})^2$. Transform the drain current equation and devise a way such that you can easily extract the device parameters K_n and V_{THN}, which is the threshold voltage of the n-channel MOSFET. (Hint: Transform the drain current equation such that it follows a straight line equation format, such as $y = mx+C$.)

V_{GS} (V)	I_D (mA)
1.3	0.61
1.5	1.00
1.7	2.03
1.9	3.11
2.1	4.44
2.3	5.63
2.5	7.43
2.7	9.04
2.9	11.66
3.1	12.95
3.3	15.04
3.5	18.33
3.7	21.23
3.9	24.0

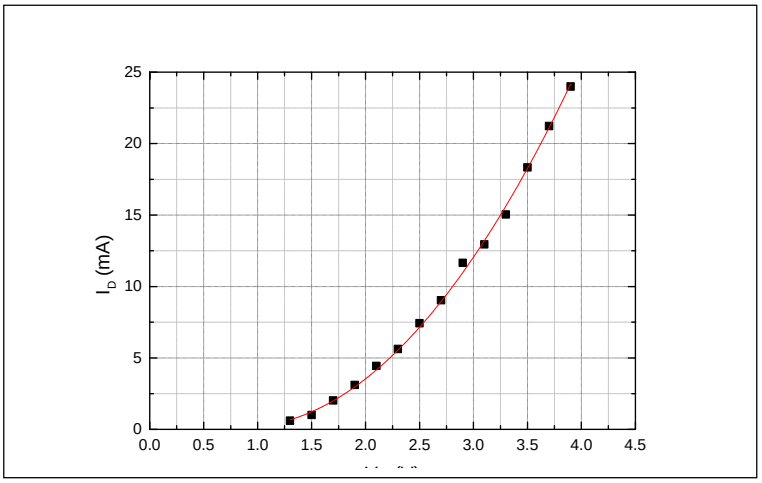


Fig. 4b

[Ans. 0.00252 A V^{-2}, 0.803 V]

(c) Assuming that V_{THN} is unchanged, describe three ways of increasing K_n in the design of the MOSFET.

Q5. Figure Q5 shows a MOSFET amplifier circuit. You may assume that the n-channel MOSFET, M_1, does not suffer from body effect (i.e., assume $V_S = V_B$) and it has the following device parameters : $K_n = 2$ mA/V^2, $V_{TH} = 0.5$ V.

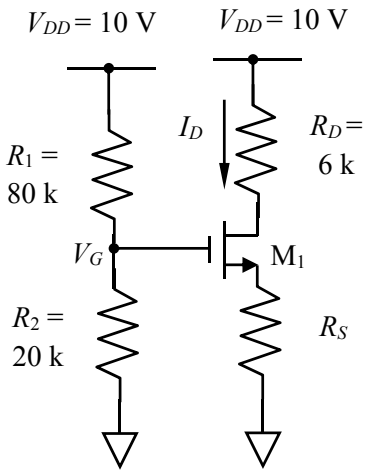


Fig. Q5

(a) By using the voltage divider method, find the voltage V_G. Is the use of the voltage divider method valid in this case? Why?

[2 V]

(b) *Assume* that the MOSFET is operating in the saturation region. Find the value of R_S which will give a drain current I_D =0.5 mA.

[2 kΩ]

(c) Calculate the drain-source voltage, V_{DS}, and the gate source-voltage, V_{GS}, of the MOSFET amplifier. Hence check whether the assumption that the MOSFET is operating in the saturation region is valid.

[6 V, 1V]

(d) The channel length modulation factor of the MOSFET, $\lambda = 0.03$ V^{-1}. For the given d.c. operating condition, determine the values of the following small signal parameters of the MOSFET: transconductance, g_m, output resistance r_0.

[2 mA V^{-1}, 66.7 k Ω]

(e) The circuit designer then decides to change the g_m to 3 mA V^{-1} by using the same MOSFET in the circuit in Fig. Q5. Explain how this can be done. What will be the new resulting value of r_o? [You need not perform the calculations of the actual values of the resistors in the circuit, but just explain how their values should be changed.]

Q6. Figure Q6 shows an amplifier circuit. The n-MOSFET is operating in the saturation region and has the following device parameters : K_n = 1 mA V^{-2}, V_{TH} = 1V. The source and body of the n-MOSFET are connected together, i.e., there is no body effect. The voltage supply V_{DD} = 5 V. The circuit designer decided that the drain current I_D is to be set at 1 mA and chose R_1 = 60 kΩ, and R_S = 1 kΩ. Complete the design of the circuit by following steps (a) to (d).

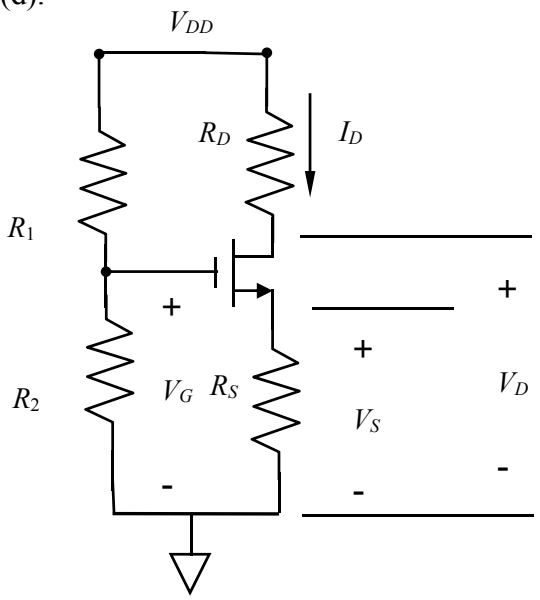


Fig. Q6

(a) Determine the value of V_G. [3 marks]

(b) Determine the value of R_2. [2 marks]

(c) What is the minimum value of the drain voltage V_D such that the MOSFET is operating in the saturation region under the given conditions? [3 marks]

(d) What is the maximum value of R_D for the MOSFET to be operating in the saturation region in this circuit? [2 marks]