WP 25.6 A 1000-MIPS/W Microprocessor using Speed-Adaptive Threshold-Voltage CMOS with Forward Bias

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Substrate bias is continuously controlled from –1.5V (backward bias) to 0.5V (forward bias) to compensate for fabrication fluctuation, supply voltage variation, and operating temperature variation. A speed-adaptive threshold-voltage (SA-Vt) CMOS with forward bias is used in a 4.3M transistor microprocessor. The SA-Vt CMOS with forward bias occupies 320x400μm^2 and consumes 4mA. The processor provides 400 VAX MIPS at 1.5 to 1.8 V with 320 to 380mW dissipation. It achieves >1000-MIPS/W performance.

MOS device size for low-power CMOS LSIs is being scaled down and supply voltages are decreasing. Fabrication-process deviation, supply-voltage variation, and operating-temperature variation prevent performance of such LSIs from being increased [1]. Substrate-bias (Vbb) control to reduce the performance degradation is studied, but does not improve performance of CMOS LSIs because they generate backward-substrate biases in MOS transistors [2,3,4]. Therefore the SA-Vt CMOS uses forward-backward-substrate bias.

The SA-Vt CMOS is composed of a delay line controlled through the Vbb, a delay comparator, a decoder, and a Vbb generator. It generates the Vbb to keep the delay line delay constant. The circuit makes the Vbb backward and forward (Figure 25.6.1). Substrate bias between 3.1 and 1.1V is applied to the n-wells of pMOS transistors and a substrate bias between 0.5 and -1.5V is applied to the p-wells of nMOS transistors. Thus the maximum forward bias is 0.5V and the maximum backward bias is -1.5V for nMOS transistors. Vbb is used in an LSI active mode. In the standby mode, the LSI receives the maximum backward bias of -1.5V [5]. The amplifiers shown in Figure 25.6.1 supply the substrate-biases Vbp and Vbn.

The dependence of threshold voltage (Vth) on Vbb in nMOS transistors is shown in Figure 25.6.2. Curve (ii) represents a typical nMOS transistor whose Vth is 0.15V at 0V Vbb. If the Vth variation is ±0.1V, curves (i), (ii), and (iii) represent the distribution of Vth. To compensate this Vth distribution by using only backward bias, the Vth is reduceded in advance. In this case, the Vth distribution becomes curves (ii), (iii), and (iv). Therefore Vbb of 1.7V is required to eliminate the Vth distribution (shown by (x)). However, if forward bias is supplied, it is unnecessary to prepare the device with lower Vth. The 0.7V backward bias (y) and the 0.4V forward bias (z) are applied. 1.1V Vbb is enough to reduce the Vth deviation.

Figure 25.6.3 shows the short-channel effect, which depends on Vbb of nMOS transistors. In a 0.2μm gate-length device, a ±10% size deviation results in 0.04V Vth variation as shown in (iii). When only backward bias is used, a 1.7V backward bias makes the Vth variation as broad as 0.08V as shown in (i). The Vth variation is forced to become wider by the backward bias [6]. On the contrary, the 0.4V forward bias makes the Vth variation as small as 0.02V as shown in (iv). The forward bias is therefore useful for reducing short-channel effect.

The fabrication-process deviation causes not only chip-to-chip characteristic deviations but also within-chip characteristic deviations. Within-chip characteristic deviations are another matter of concern since the SA-Vt CMOS supplies the same Vbb to the whole LSI chip [6]. Here, the saturation currents (Ids) of MOS transistors distribute as $\mu 0+\sigma 0$, where $\mu 0$ is the mean and $\sigma 0$ is the standard deviation. From the central limit theorem in mathematical statistics [7], it is clear that the performance of the circuits constructed with n-pieces of MOS transistors varies according to:

$$\mu 1 + \sigma 1 = n*\mu 0 + \sqrt{(n)}*\sigma 0. \quad \text{(Eq. 25.6.1)}$$

Consequently:

$$\sigma 1/\mu 1 = (1/\sqrt{(n)})(\sigma 0/\mu 0). \quad \text{(Eq. 25.6.2)}$$

Figure 25.6.4a shows the measured distribution of the saturation currents of 1290 nMOS transistors within a single chip. Figure 25.6.4b shows the measured frequency distribution of 256 ring oscillators within the same chip. The ring oscillator is made of 49 inverters. From these data, n=49, $\sigma 0/\mu 0$=2.4%, and $\sigma 1/\mu 1$=0.55%. These measured deviations agree closely with that from Eq. 25.6.2. If the number of MOS transistors used in a circuit is larger, the circuit performance variation becomes smaller than the within-chip characteristic variation. To raise LSI performance, it is therefore more realistic to manage chip-to-chip characteristic deviations rather than control within-chip characteristic deviations.

The SA-Vt CMOS with forward bias is used experimentally in a 4.3M-transistor microprocessor. The microprocessor and the SA-Vt CMOS with forward bias use a 0.2μm CMOS technology with a 4.5nm gate insulator, 0.15V Vth, 5 layers of inter-connective metal, and triple-well structure. The microprocessor chip properties are listed in Figure 25.6.5. Figure 25.6.6 shows a microprocessor chip micrograph. The SA-Vt CMOS occupies 320x400μm^2, only 0.2% of the chip. It consumes a current of 2mA with a 1.6V source and 1mA with 3.0V and –1.5V sources. These currents are negligible compared with the chip active power dissipated.

The effect of the SA-Vt CMOS with forward bias on the Dhrystone-1.1 benchmark in the microprocessor is shown in Figure 25.6.7. Figure 25.6.7a shows the supply-voltage variation control of the microprocessor. The SAVt CMOS keeps the processor maximum frequency at 220MHz for supply between 1.5 and 1.8V. When the supply varies from 1.5 to 1.7V at a 1.6V power source (±0.1V source fluctuation), it compensates the frequency change of 18%. The current consumption during the supply-voltage control is shown in Figure 25.6.7b. Forward bias compensates the LSI performance. It is possible to use the 0.5V forward bias because no latch-up effect is observed up to a 4V supply [8]. But leakage current of a parasitic bipolar-transistor in a substrate caused by the forward bias may still be a problem. The current increases with forward bias in Figure 25.6.7b. This is mainly because operating frequency is high. The leakage current of the parasitic bipolar-transistor in the substrate by the forward bias is almost unobservable. Therefore, the microprocessor achieves 100MIPS/W performance at the worst conditions. In the standby mode, the SA-Vt CMOS is suspended and it supplies a -1.5V backward bias. Microprocessor standby current is therefore reduced to 30μA.

Acknowledgements:
The authors are indebted to H. Mizuno, O. Nishii, T. Shimura, and K. Sasaki for discussions, and thank S. Ikeda for sample preparation.

References:

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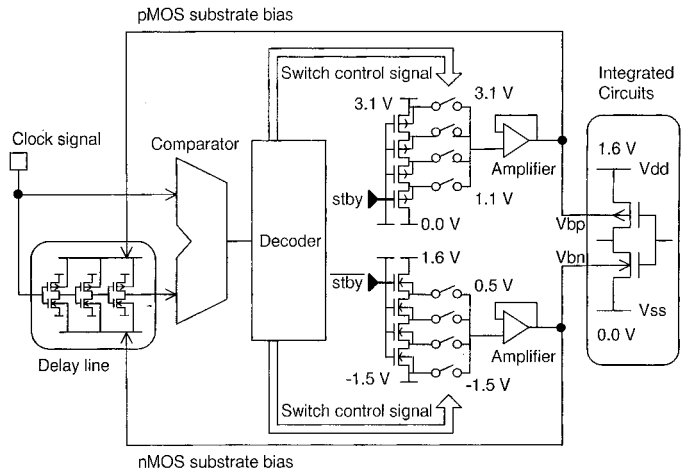

Figure 25.6.1: SA-Vt CMOS scheme with forward bias.

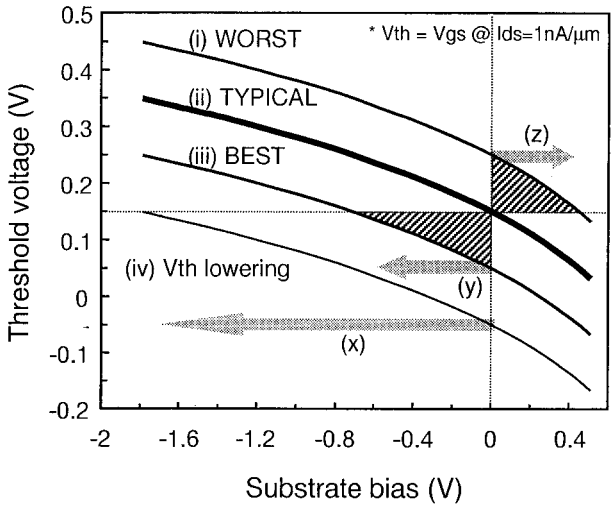

Figure 25.6.2: Threshold-voltage dependence on substrate bias.

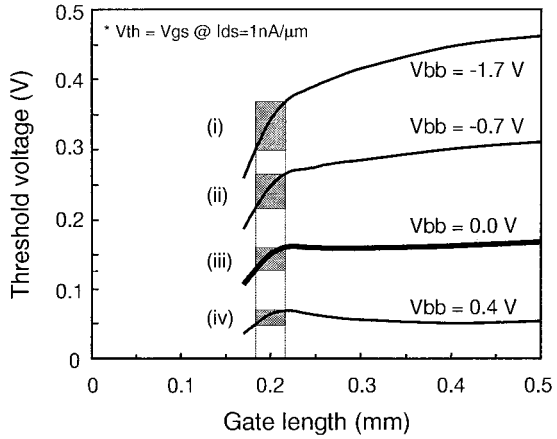

Figure 25.6.3: Short-channel effect.

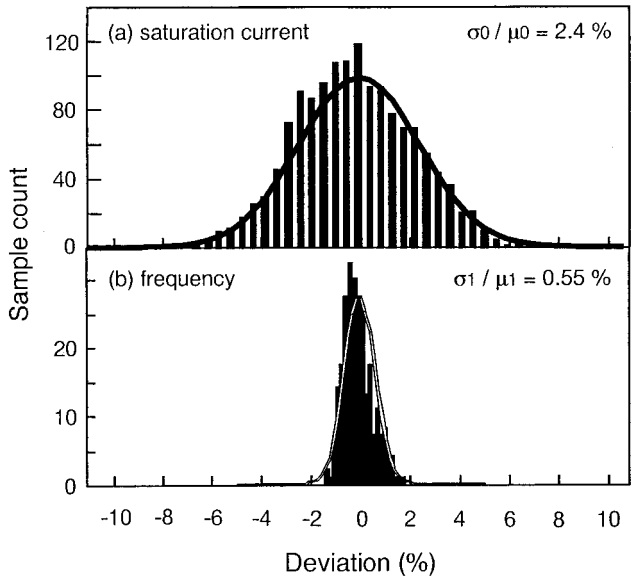

Figure 25.6.4: Measured distributions:
(a) saturation current of nMOS transistors,
(b) frequency of ring oscillators.

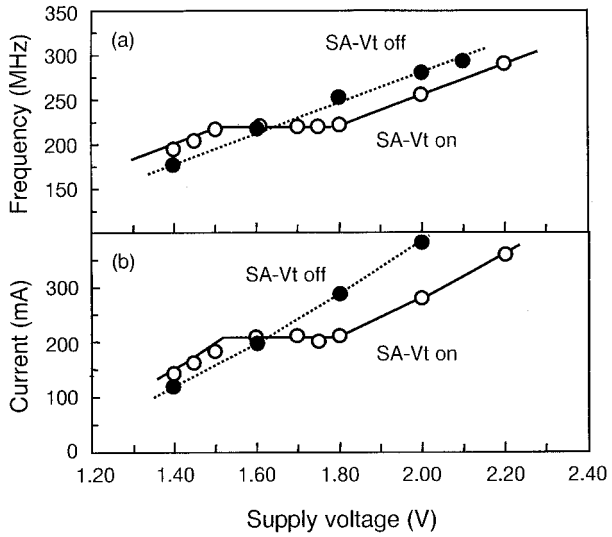

Figure 25.6.7: Measured frequency and current as a function of supply voltage on Dhrystone 1.1.

Supply voltage	**1.5 - 1.8V**
Clock frequency	**220MHz**
Power consumption	**320 - 380mW**
Standby current	**30μA**
Performance	**400 VAX MIPS**
Architecture	**2-way superscalar**
Cache	**8kB I-cache, 16kB D-cache**
Transistor	**4.3M transistors**
Area	**7 x 7.8mm²**

Figure 25.6.5: Chip features.

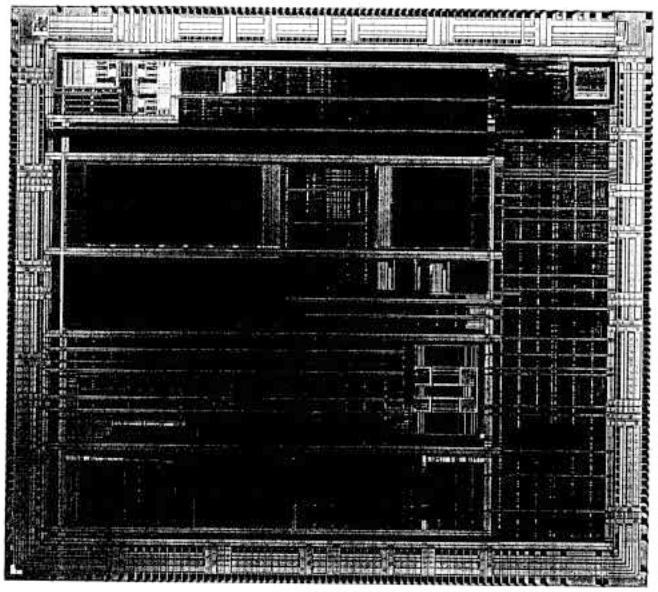

Figure 25.6.6: Chip micrograph.