NATIONAL UNIVERSITY OF SINGAPORE

EXAMINATION FOR

(Semester I: 2011/2012)

EE2021 –DEVICES AND CIRCUITS

November/December 2011 - Time Allowed: 2.5 Hours

INSTRUCTIONS TO CANDIDATES:

1. This paper contains **FOUR (4)** questions and comprises **SIXTEEN (16)** printed pages.
2. Answer all questions. **Start each question on a new page.**
3. All questions carry equal marks.
4. This is a **CLOSED BOOK** examination.
5. Programmable calculators are allowed in this examination.
6. The following information can be used where applicable:

Elementary charge	e	=	1.602×10^{-19} C
Boltzmann constant	k	=	1.381×10^{-23} J K^{-1}
		=	8.618×10^{-5} eV K^{-1}
Thermal energy (T = 300 K)	kT	=	0.0259 eV
Thermal voltage (T = 300 K)	V_t	=	0.0259 V
Permittivity of free space	ε_0	=	8.854×10^{-14} F cm^{-1}

For silicon at 300 K:

Intrinsic carrier concentration	n_i	=	1.5×10^{10} cm^{-3}
Relative permittivity of silicon	ε_r (Si)	=	11.7
Relative permittivity of silicon dioxide	ε_r (SiO_2)	=	3.9

7. Formulas and other information are given in the APPENDIX for your reference.

Q.1 (a) A piece of silicon is uniformly doped with 8×10^{15} cm^{-3} acceptors and 2×10^{15} cm^{-3} donors. The silicon is at thermal equilibrium at a temperature $T = 300$ K. Calculate the conductivity of the silicon sample.

You may make use of the carrier mobility versus dopant concentration data given in Figure Q.1.1.

[4 marks]

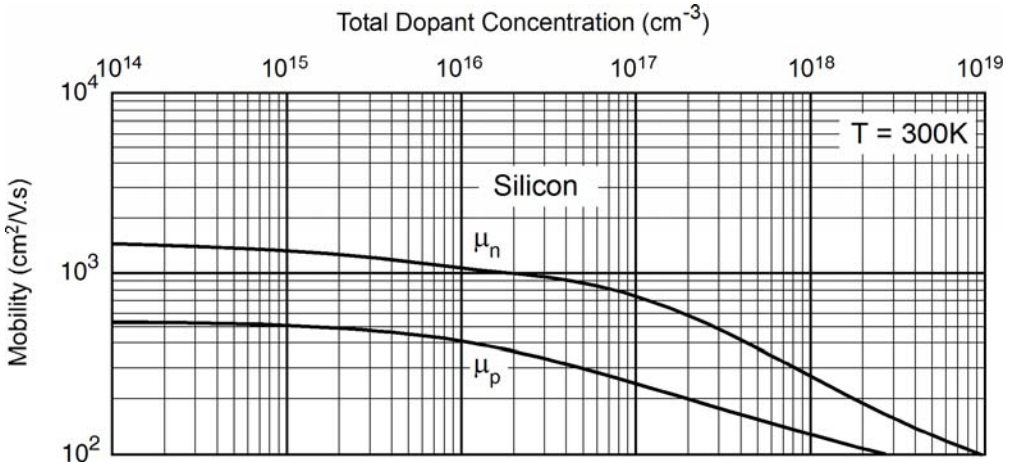


Figure Q.1.1: Electron (μ_n) and hole (μ_p) mobilities in silicon at 300 K, as a function of total dopant concentration.

(b) The silicon sample is uniformly illuminated with light, such that the steady state concentrations of the excess electrons and holes generated are each equal to 10^{14} cm^{-3}. The temperature $T = 300$ K. What is the conductivity of the sample?

[4 marks]

(c) The lifetimes of the excess electrons and holes are, respectively, $\tau_n = 10^{-4}$ s, $\tau_p = 10^{-3}$ s. At time $t = 0$ s, the illumination is switched off. Calculate the excess electron and hole concentrations at time $t = 10^{-3}$ s. Hence calculate the conductivity of the silicon sample at $t = 10^{-3}$ s.

[4 marks]

Question Q.1 continues on Page 3

(d) Figure Q.1.2 shows a sketch (not to scale) of the charge density profile, $\rho(x)$, in the space charge region (SCR) of a silicon p-n junction diode, at thermal equilibrium. The doping, N_A, on the p-type side is much greater than the doping, N_D, on the n-type side.

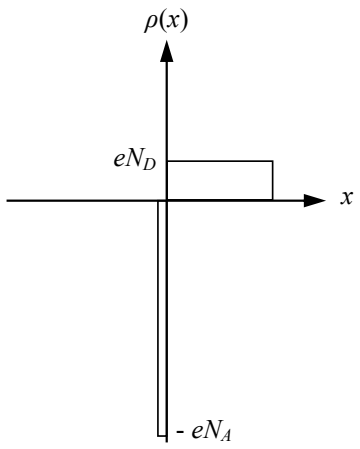


Figure Q.1.2 : Charge density profile of a p-n junction (not to scale).

Sketch the electric field profile $E(x)$ in the SCR of the p-n junction. Your sketch need not be to scale, but should be consistent with the charge density profile.

[4 marks]

(e) Show that the magnitude of the maximum electric field, E_{max}, in the p-n junction at equilibrium can be expressed approximately as

$$E_{\max} = \left[\frac{2eV_{bi}}{\varepsilon_0 \varepsilon_r} \times N_D \right]^{1/2}.$$

[4 marks]

(f) When the p-n junction is reverse-biased, it will break down when the magnitude of the maximum electric field in the p-n junction exceeds the critical electric field, $E_{critical}$. For silicon, $E_{critical} = 3 \times 10^5$ V cm^{-1}. The reverse bias voltage at which breakdown occurs is called the breakdown voltage.

Determine the doping, N_D, on the n-type side of the p-n junction such that the breakdown voltage is 500 V. State clearly any approximation you made in your calculations.

[5 marks]

Q.2 Figure Q.2.1 is a schematic diagram of the active region of a **p-n-p** bipolar junction transistor.

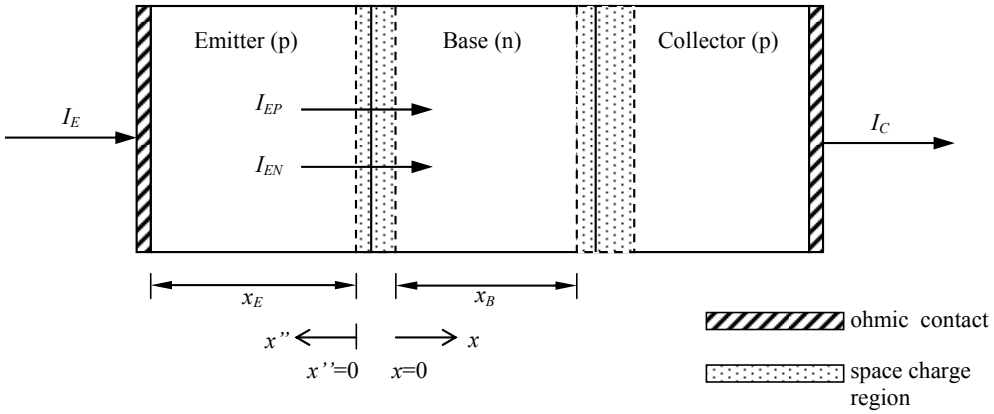


Figure Q.2.1 : Schematic diagram of the active region of a p-n-p bipolar junction transistor.

The bipolar transistor has the following specifications :
Emitter doping, $N_{AE} = 10^{19}$ cm^{-3},
Base doping, $N_{DB} = 10^{17}$ cm^{-3},
Minority carrier diffusivity in the emitter, $D_{nE} = 2.5$ cm^2 s^{-1},
Minority carrier diffusivity in the base, $D_{pB} = 10$ cm^2 s^{-1},
Minority carrier diffusion length in the emitter, $L_{nE} = 5 \times 10^{-6}$ cm,
Minority carrier diffusion length in the base, $L_{pB} = 2 \times 10^{-3}$ cm,
Cross-sectional area, $A = 0.01$ cm^2.

The bipolar transistor is biased in the forward active mode, with an emitter-base voltage, $V_{EB} = 0.6$ V, and a collector-base voltage, $V_{CB} = -5$ V. Under these conditions, the widths of the neutral regions in the emitter and the base, x_E and x_B respectively, are each equal to 5×10^{-5} cm.

(a) Determine the concentrations of the excess electrons at $x'' = 0$, and excess holes at $x = 0$, respectively.

[4 marks]

(b) Sketch, and explain briefly, the shapes of the excess minority carrier profiles, $\delta n_E(x'')$ and $\delta p_B(x)$ in the emitter and the base, respectively.

[6 marks]

(c) Calculate I_{En} and I_{Ep}, where I_{En} is the component of the emitter current due to the injection of electrons from the base into the emitter, and I_{Ep} is the component of the emitter current due to the injection of holes from the emitter into the base.

[4 marks]

(d) Assume that recombination of excess carriers in the base is negligible, calculate the emitter current, I_E, and the collector current I_C.

[2 marks]

Question Q.2 continues on Page 5

(e) A silicon n-channel MOSFET has the following dimensions : length, L = 2 μm, width, W = 10 μm, thickness of the silicon dioxide under the gate, t_{ox} = 10 nm. The mobility of the electrons in the channel is 500 $cm^2\ V^{-1}\ s^{-1}$. The threshold voltage, V_{TH} = 0.5 V.

The source of the MOSFET is grounded and a voltage of 3 V is applied to the gate. The $I_D - V_{DS}$ characteristic of the MOSFET is shown in Figure Q.2.2.

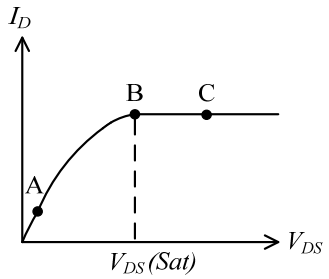


Figure Q.2.2. : The $I_D - V_{DS}$ characteristic of the n-channel MOSFET at a given gate bias of 3 V.

Calculate the gate oxide capacitance per unit area, C_{ox}, of the MOSFET.

Determine the drain current I_D that corresponds to point "B" in the above characteristic.

[5 marks]

(f) For operation corresponding to point "B" in Figure Q.2.2, sketch the cross-sectional view of the MOSFET showing the MOS structure including the channel inversion layer and the depletion layer. The shape of the channel inversion layer must be qualitatively correct in your sketch.

[4 marks]

Q.3

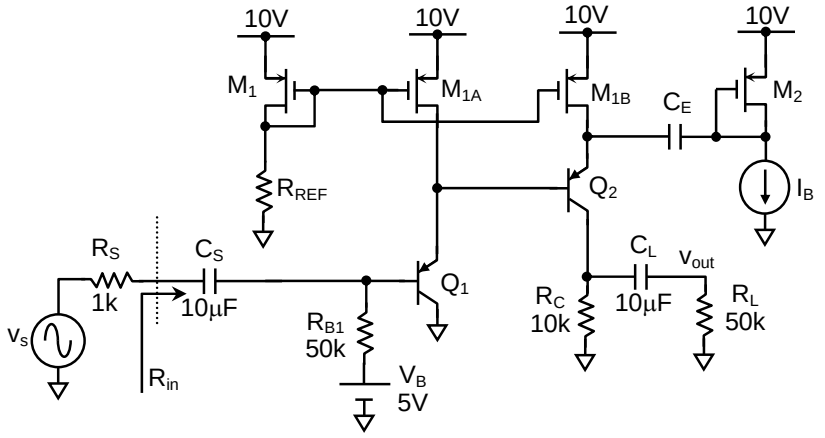


Figure Q.3 : Multistage amplifier circuit.

A multistage amplifier is shown in Figure Q.3. You may assume that the body and the source terminal of each of the PMOS are connected together, i.e., no body effect for PMOS. You may also assume the following device parameters and that all pnp BJT and PMOS devices are identical:

- β=100, V_A=100, C_π=4.9pF, C_μ=1.7pF.
- K_p=2mA/V^2, V_{THP}= –1V, λ_p=0.001V^{-1}.

(a) Design R_{REF} such that $I_{D,M1}$ is 500μA. Work out the small signal AC parameters of Q_1.

[5 marks]

(b) Identify the two stage amplifier configuration. **[2 marks]**

(c) Obtain the expression for the small signal gain (v_{out}/v_s) of the amplifier. You can use the variable $g_{m,M2}$ in your expression as I_B is not given.

[8 marks]

(d) Estimate the value of I_B in order to have a gain (v_{out}/v_s) of -20. **[6 marks[**

(e) Design C_E such that f_L is 100Hz. **[4 marks]**

Q.4 (a) Draw the pull-up and pull-down network for the following logic function:

$$Y = \overline{(A + B \cdot C) \cdot D \cdot (E + F)}$$ **[8 marks]**

(i) Define the respective logic values of A, B, C, D, E and F such that it will lead to the worst case t_{pHL}.

[2 marks]

(ii) Assume that all NMOS transistors in the designed pull-down network have a sizing of 2n, and that the NMOS transistor in the symmetric inverter has a sizing of n. Find the relationship between $t_{pHL,logic}$ and $t_{pHL,inv}$.

[3 marks]

(b) (i) The LED circuit shown in Figure Q4 is a small part of a Christmas light decoration. The LED will light up if a current of 1 mA flows through it. Assuming that the LED has an I–V characteristic similar to that of normal diodes, estimate the resistance (R_1) needed to obtain the 1 mA current. You can assume that when the MOSFET turns on, $V_{DS,M1}$ is negligible.

[2 marks]

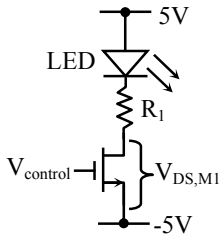


Figure Q.4 : LED circuit.

(ii) Suggest an opamp-based circuit that can generate the proper $V_{control}$ such that the LED in part (i) will blink a few times per minute.

[5 marks]

(iii) For the proposed opamp circuit in (ii), select the component values such that the LED will blink 3 times per minute.

[5 marks]

END OF QUESTIONS

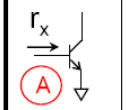
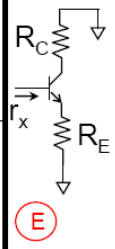
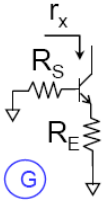
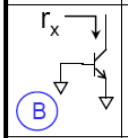
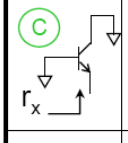
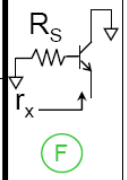
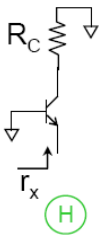
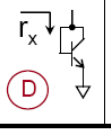
APPENDIX

1. Law of mass action	$p_0 n_0 = n_i^2$
2. Space-charge density	$\rho = e\left(p + N_D^+ - n - N_A^-\right)$
3. Conductivity	$\sigma = e\left(n\mu_n + p\mu_p\right)$
4. Current densities	$J_n = en\mu_n E + eD_n \frac{dn}{dx}$ $J_p = ep\mu_p E - eD_p \frac{dp}{dx}$
5. Einstein Relation	$\frac{D_n}{\mu_n} = \frac{D_p}{\mu_p} = \frac{kT}{e}$
6. Decay of excess minority carrier concentration as a function of time, under low-level injection conditions, where τ is the minority carrier lifetime.	$\delta n(t) = \delta n(0)\exp\left(\frac{-t}{\tau}\right)$ $\delta p(t) = \delta p(0)\exp\left(\frac{-t}{\tau}\right)$
7. Poisson's equation (Gauss's Law)	$\frac{dE}{dx} = -\frac{d^2\phi}{dx^2} = \frac{\rho(x)}{\varepsilon_r \varepsilon_0}$
8. Built-in potential of an abrupt p-n junction diode.	$V_{bi} = \frac{kT}{e}\ln\left(\frac{n_{n0}}{n_{p0}}\right) = \frac{kT}{e}\ln\left(\frac{p_{p0}}{p_{n0}}\right) = \frac{kT}{e}\ln\left(\frac{N_A N_D}{{n_i}^2}\right)$
9. Space-charge region width of an unbiased abrupt pn junction diode.	$W = \left[\frac{2\varepsilon_r \varepsilon_0 V_{bi}}{e}\left(\frac{N_A + N_D}{N_A N_D}\right)\right]^{\frac{1}{2}}$
10. Magnitude of the maximum electric field in an abrupt pn junction diode.	$E_{\max} = \frac{eN_A N_D}{\varepsilon_r \varepsilon_0 (N_A + N_D)} W$

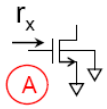
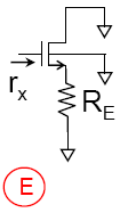
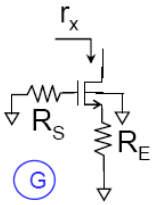
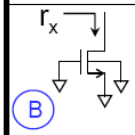
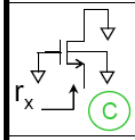
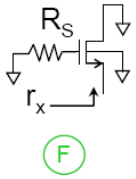
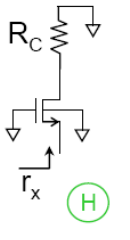
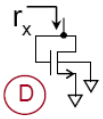
11. Excess carrier concentration with respect to position for a long-base abrupt pn junction diode under low-level injection conditions	$\delta n_p(x') = \delta n_p(0) \cdot \exp\left(-\frac{x'}{L_n}\right)$ $\delta p_n(x'') = \delta p_n(0) \cdot \exp\left(-\frac{x''}{L_p}\right)$
12. Excess carrier concentration at the edges of the space-charge region of an abrupt pn junction diode under low-level injection conditions.	$\delta n_p(0) = n_{p0}\left[\exp\left(\frac{e\,V}{k\,T}\right)-1\right]$ $\delta p_n(0) = p_{n0}\left[\exp\left(\frac{e\,V}{k\,T}\right)-1\right]$
13. Minority carrier diffusion lengths.	$L_n = \sqrt{D_n \tau_n}$ $L_p = \sqrt{D_p \tau_p}$
14. Ideal diode current density-voltage equation for an abrupt, pn junction diode.	$J = J_s\left[\exp\left(\frac{eV_a}{k\,T}\right)-1\right]$, where V_a is the applied voltage, and $J_s = J_{s,p} + J_{s,n}$
14a. For "long" n-type neutral region	$J_{s,p} = e\frac{D_p}{L_p}p_{n0}$
14b. For "short" n-type neutral region	$J_{s,p} = e\frac{D_p}{W_n}p_{n0}$
14c. For "long" p-type neutral region	$J_{s,n} = e\frac{D_n}{L_n}n_{p0}$
14d. For "short" p-type neutral region	$J_{s,n} = e\frac{D_n}{W_p}n_{p0}$
15. Junction capacitance of an abrupt pn junction diode.	$C_j = \frac{\varepsilon_0 \varepsilon_{r(Si)} A}{W}$
16. Incremental resistance of a pn junction diode	$r_d = \frac{V_t}{I_Q}$
17a. Emitter injection efficiency of an **npn** bipolar junction transistor (short base and long emitter)	$\gamma = \frac{I_{En}}{I_E} = \frac{1}{1+\frac{D_E}{D_B}\frac{x_B}{L_E}\frac{N_B}{N_E}}$

17b. Emitter injection efficiency of an **npn** bipolar junction transistor (short base and short emitter)	$\gamma = \frac{I_{En}}{I_E} = \frac{1}{1+\frac{D_E}{D_B}\frac{x_B}{x_E}\frac{N_B}{N_E}}$
18a. Base transport factor of an **npn** bipolar transistor (general definition)	$\alpha_T = \frac{I_{Cn}}{I_{En}}$
18b. Base transport factor of an **npn** bipolar transistor (short base)	$\alpha_T = 1 - \frac{1}{2}\left(\frac{x_B}{L_n}\right)^2$
Note : For **pnp** bipolar transistors, interchange the roles of the electrons and holes.	
19. Common base current gain of a bipolar junction transistor	$\alpha = \frac{I_C}{I_E}$
20. Common emitter current gain of a bipolar junction transistor.	$\beta = \frac{I_C}{I_B} = \frac{\alpha}{1-\alpha}$
21. Gate oxide capacitance of a MOSFET (per unit area of the capacitor)	$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}} = \frac{\varepsilon_o \times \varepsilon_{r(SiO_2)}}{t_{ox}}$
22. Drain current in the linear region of an n-channel MOSFET	$I_D = \mu_n \frac{W}{L} C_{ox}\left[(V_G - V_T)V_D - \frac{1}{2}{V_D}^2\right]$
23. Drain current in the saturation region of an n-channel MOSFET	$I_D = \frac{1}{2}\mu_n \frac{W}{L} C_{ox}\left(V_G - V_T\right)^2$
24. Transconductance of a MOSFET	$g_m \equiv \frac{dI_D}{dV_G}$

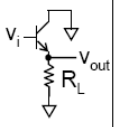
BJT DP Summary (Table 1)

Conf	DP r_x	Conf	DP r_x	Conf	DP r_x
	$\frac{\beta}{g_m}$		$r_\pi + (1+\beta)R_E$ $\approx r_\pi(1+g_m R_E)$		$r_o\left\{1+g_m\left[(r_\pi+R_S)\,//\,R_E\right]\left(\frac{r_\pi}{r_\pi+R_S}\right)\right\}$ *If* $R_S=0$ *and* $r_\pi \ll R_E$ $\Rightarrow r_{x,\max}=r_o(\beta+1)$
	$\frac{V_A}{I_C}$				
	$\frac{1}{g_m}$		$\frac{R_S+r_\pi}{1+\beta}\,//\,r_o$ $\approx \frac{R_S}{1+\beta}+\frac{1}{g_m}$		$\frac{1}{g_m}\times\frac{r_o+R_C}{r_o+R_C/\beta}$
	$\frac{1}{g_m}$				

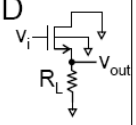
MOS DP Summary (Table 2)

Conf	DP r_x	Conf	DP r_x	Conf	DP r_x
	∞		∞		$r_o\left[1+(g_m-g_{mb})R_E\right]$
	$\frac{1}{\lambda I_D}$				
	$\frac{1}{g_m-g_{mb}}$		$\frac{1}{g_m-g_{mb}}$		$\frac{1}{g_m-g_{mb}}\times\frac{r_o+R_C}{r_o}$
	$\frac{1}{g_m}$				

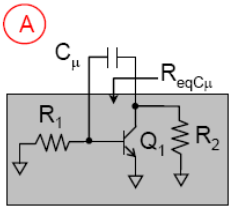
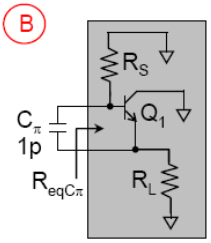
BJT Summary (Table 3)

BJT	G_m	A_V
CE (A)	g_m	Derive Based on 2-ports Network
CB (B)	$-g_m$	Derive Based on 2-ports Network
CC (C) 	Not Applicable	$\frac{g_m R_L}{1+g_m R_L}$
CE with Emitter Degeneration (D)	$\frac{g_m}{1+g_m R_E}$	Derive Based on 2-ports Network

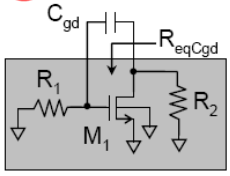
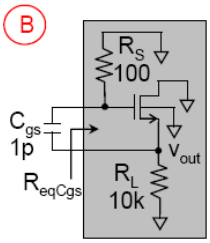
MOS Summary (Table 4)

MOS	G_m	A_V
CS (A)	g_m	Derive Based on 2-ports Network
CG (B)	$-(g_m - g_{mb})$ *Drop g_{mb} if no body effect*	Derive Based on 2-ports Network
CD (C) 	Not Applicable	$\frac{g_m R_L}{1+(g_m - g_{mb})R_L} \approx \frac{g_m}{g_m - g_{mb}}$ *Drop g_{mb} if no body effect*
CS with R_E (D)	$\frac{g_m}{1+(g_m - g_{mb})R_E}$ *Drop g_{mb} if no body effect*	Derive Based on 2-ports Network

BJT Frequency Summary Table (Table 5)

A 	$R_{eqC\mu}$ $R_{eqi} = R_1 // r_{\pi,Q1} \quad R_{eqo} = R_2 // r_{o,Q1}$ $R_{eqC_\mu} = R_{eqi} + (1 + g_{m,Q1}R_{eqi})R_{eqo}$ $= (R_1 // r_{\pi,Q1}) + [1 + g_m(R_1 // r_{\pi,Q1})](R_2 // r_{o,Q1})$ *Miller Theorem Validity :* $g_{m,Q1}R_{eqi} >> 1$	$\tau_{eqC\mu}$ $\tau_{eqC\mu} = C_\mu R_{eqC\mu}$
B 	$R_{eqC\pi}$ $R_{eqC\pi} = r_{\pi,Q1} // \left(\dfrac{R_S + (R_L // r_{o,Q1})}{1 + g_{m,Q1}(R_L // r_{o,Q1})} \right)$	$\tau_{eqC\pi}$ $\tau_{eqC\pi} = C_\pi R_{eqC\pi}$

MOS Frequency Summary Table (Table 6)

A 	R_{eqCgd} $R_{eqi} = R_1 \quad R_{eqo} = R_2 // r_{o,M1}$ $R_{eqCgd} = R_{eqi} + (1 + g_{m,M1}R_{eqi})R_{eqo}$ $= R_1 + (1 + g_m R_1)(R_2 // r_{o,M1})$ *Miller Theorem Validity :* $g_{m,M1}R_{eqi} >> 1$	τ_{eqCgd} $\tau_{eqCgd} = C_{gd}R_{eqCgd}$
B 	R_{eqCgs} $R_{eqCgs} = \dfrac{R_S[1 - g_{mb,M1}(R_L // r_{o,M1})] + (R_L // r_{o,M1})}{1 + (g_{m,M1} - g_{mb,M1})(R_L // r_{o,M1})}$	τ_{eqCgs} $\tau_{eqCgs} = C_{gs}R_{eqCgs}$

1) Logic Gates:

For K transistor in series:

$$\left(\frac{W}{L}\right)_{eq} = \left[\left(\frac{W}{L}\right)_1^{-1} + \left(\frac{W}{L}\right)_2^{-1} + \cdots + \left(\frac{W}{L}\right)_K^{-1}\right]^{-1}$$

For K transistor in parallel:

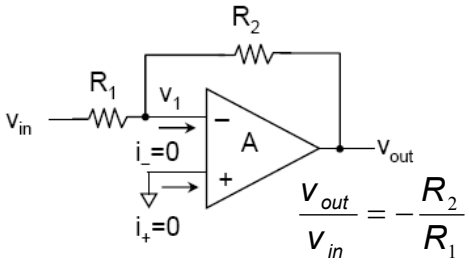
$$\left(\frac{W}{L}\right)_{eq} = \left(\frac{W}{L}\right)_1 + \left(\frac{W}{L}\right)_2 + \cdots + \left(\frac{W}{L}\right)_K$$

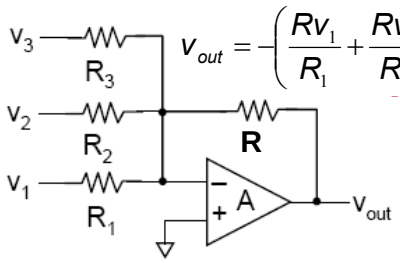
2) SCTC and OCTC:

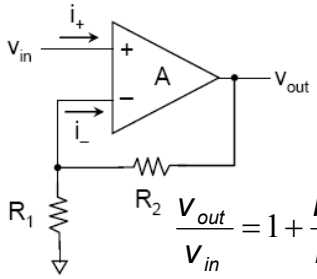
$$2\pi f_L = b_1 = \sum \frac{1}{\tau_i}$$

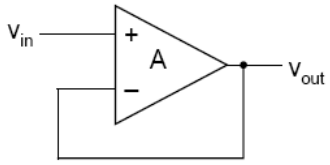
$$2\pi f_U = \frac{1}{a_1} = \frac{1}{\sum \tau_i}$$

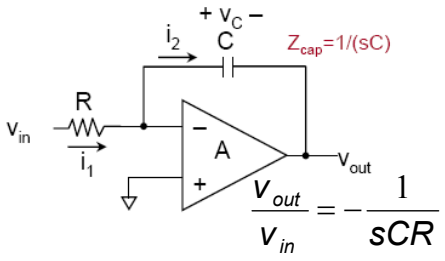
3) Opamp Circuits:

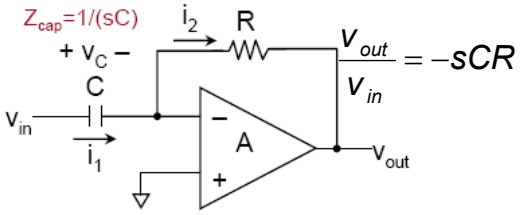
<table>
<tr>
<td>Inverting Amplifier
 

$\frac{v_{out}}{v_{in}} = -\frac{R_2}{R_1}$</td>
<td>Summing Amplifier
 

$v_{out} = -\left(\frac{Rv_1}{R_1} + \frac{Rv_2}{R_2} + \frac{Rv_3}{R_3}\right)$</td>
</tr>
<tr>
<td>Non-inverting Amplifier
 

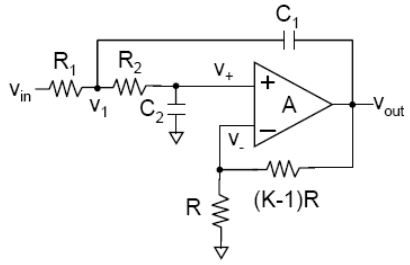
$\frac{v_{out}}{v_{in}} = 1 + \frac{R_2}{R_1}$</td>
<td>Buffer
 

$\frac{v_{out}}{v_{in}} = 1$</td>
</tr>
<tr>
<td>Integrator
 

$\frac{v_{out}}{v_{in}} = -\frac{1}{sCR}$</td>
<td>Differentiator
 

$\frac{v_{out}}{v_{in}} = -sCR$</td>
</tr>
</table>

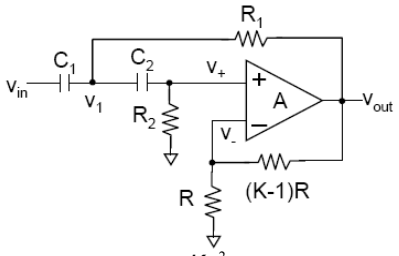
SK Lowpass Filter



$$\frac{v_{out}}{v_{in}} = \frac{\frac{K}{C_1C_2R_1R_2}}{s^2 + s\left(\frac{1}{C_1R_1} + \frac{1}{C_2R_2} + \frac{1}{C_1R_2} - \frac{K}{C_2R_2}\right) + \frac{1}{C_1C_2R_1R_2}}$$

$$= \frac{H_o\omega_o^2}{s^2 + \frac{\omega_o}{Q}s + \omega_o^2}$$

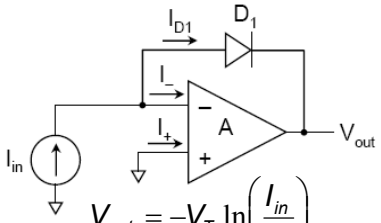
SK Highpass Filter



$$\frac{v_{out}}{v_{in}} = \frac{Ks^2}{s^2 + s\left(\frac{1}{C_2R_2} + \frac{1}{C_1R_2} + \frac{1}{C_1R_1} - \frac{K}{C_1R_1}\right) + \frac{1}{C_1C_2R_1R_2}}$$

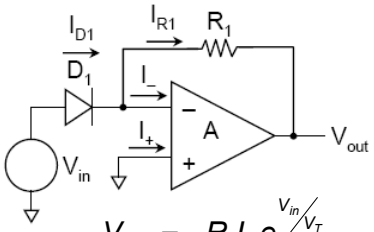
$$= \frac{H_o s^2}{s^2 + \frac{\omega_o}{Q}s + \omega_o^2}$$

Logarithm Amplifier



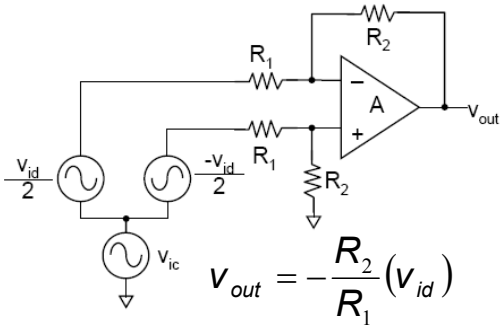
$$V_{out} = -V_T \ln\left(\frac{I_{in}}{I_S}\right)$$

Exponential Amplifier



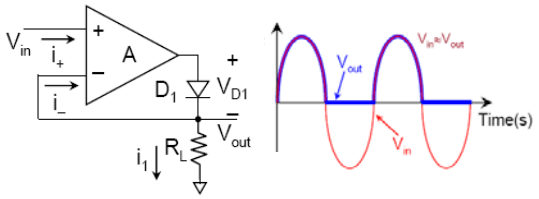
$$V_{out} = -R_1 I_S e^{V_{in}/V_T}$$

Instrumentation Amplifier

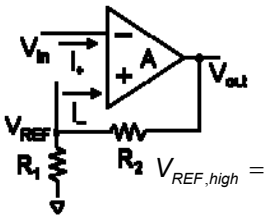


$$v_{out} = -\frac{R_2}{R_1}(v_{id})$$

Super Diode



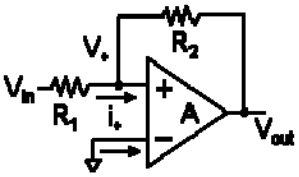
Inverting Comparator with Hysteresis



$$V_{REF,high} = \frac{R_1}{R_1 + R_2} \times V_{DD}$$

$$V_{REF,low} = \frac{R_1}{R_1 + R_2} \times (-V_{DD})$$

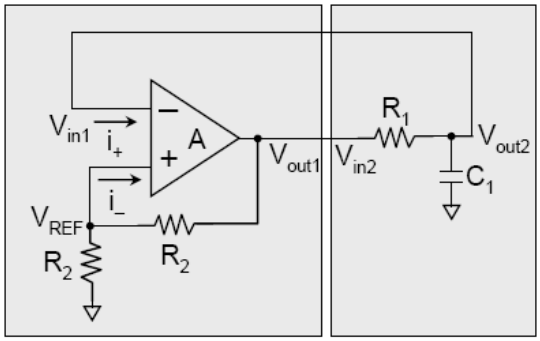
Comparator with Hysteresis



$$V_{REF,low} = -\frac{R_1}{R_2} V_{DD}$$

$$V_{REF,high} = \frac{R_1}{R_2} V_{DD}$$

Bistable Multivibrator



$$T = 2C_1R_1 \ln(3)$$

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