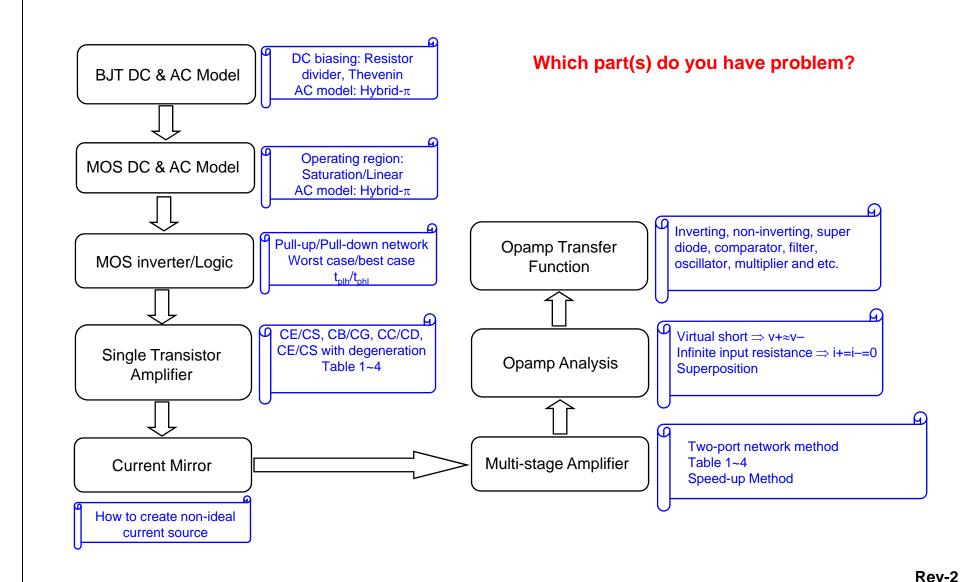
EE2021 Devices and Circuits

Revision

Summary on Materials Covered



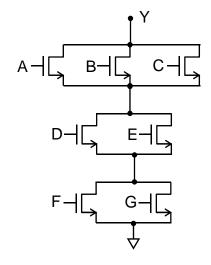
NUS EE2021 CH Heng

Logic Synthesis

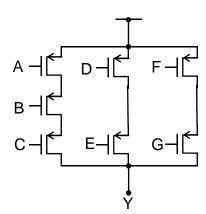
$$Y = \overline{(A+B+C)\cdot(D+E)\cdot(F+G)}$$

$$= \overline{(A+B+C)} + \overline{(D+E)} + \overline{(F+G)}$$
 Hint: Demorgan Theorem
$$= \overline{(A\cdot\overline{B}\cdot\overline{C})} + \overline{(D\cdot\overline{E})} + \overline{(F\cdot\overline{G})}$$

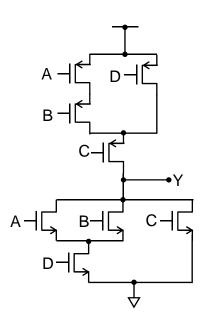
Pull Down Network



Pull Up Network (Duality)



Logic Function



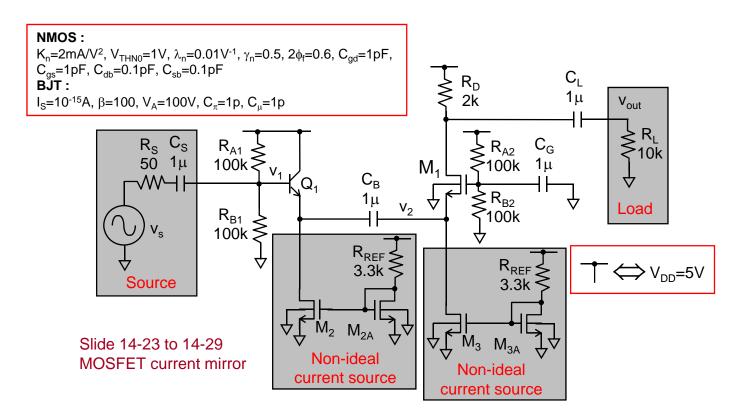
$$Y = \overline{(A+B) \cdot D + C}$$

$$= \overline{(A+B) \cdot D} \cdot \overline{C}$$

$$= \overline{(A+B) + D} \cdot \overline{C}$$

$$= \overline{(A+B) + D} \cdot \overline{C}$$

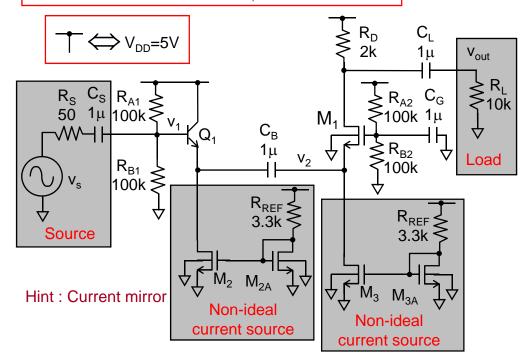
DC Analysis: Identifying



• Identify AC source, load and non-ideal current source

DC Analysis: DC Biasing

NMOS: $K_n=2mA/V^2$, $V_{THN0}=1V$, $\lambda_n=0.01V^{-1}$, $\gamma_n=0.5$, $2\phi_f=0.6$, $C_{nd}=1pF$, $C_{as} = 1pF, C_{db} = 0.1pF, C_{sb} = 0.1pF$ $I_S=10^{-15}A$, $\beta=100$, $V_A=100V$, $C_{\pi}=1p$, $C_{\mu}=1p$



Find the DC biasing current for Q₁ and M₁

Determine DC Biasing

Determine DC Biasing
$$I_{D,M2A} = K_n (V_{GS,M2A} - V_{THN0})^2 \cdot \dots \cdot (1)$$

$$I_{D,M2A} = \frac{V_{DD} - V_{GS,M2A}}{R_{REF}} \cdot \dots \cdot (2)$$

$$\Rightarrow 6.6V_{GS,M2A}^2 - 13.2V_{GS,M2A} + 6.6 = 5 - V_{GS,M2A}$$

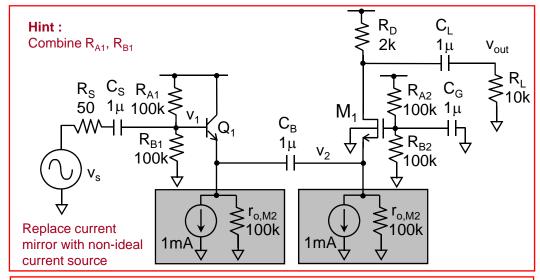
$$\Rightarrow 6.6V_{GS,M2A}^2 - 12.2V_{GS,M2A} + 1.6 = 0$$

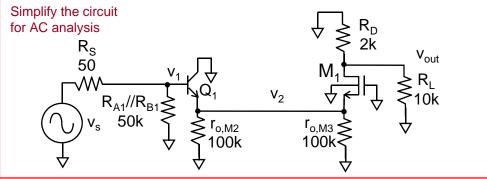
$$\Rightarrow V_{GS,M2A} = \frac{-(-12.2) \pm \sqrt{(12.2)^2 - 4(6.6)(1.6)}}{2(6.6)}$$

$$= 1.71 \quad or \quad 0.142(< V_{THN0} \Rightarrow invalid)$$

$$\Rightarrow I_{C,Q1} \approx I_{D,M2A} = I_{D,M2} = 1mA$$
Similarly
$$\Rightarrow I_{D,M1} = I_{D,M3} = I_{D,M3A} = 1mA$$

AC Analysis: Simplify the Circuit and Find Out AC Small Signal Parameter





Determine AC small signal parameter

$$g_{m,M1} = \sqrt{4K_nI_{D,M1}} = 2.83mA/V$$

$$g_{mb,M1} = -\frac{g_{m,M1}}{4} = -0.71 mA/V$$

$$r_{o,M1} = r_{o,M3} = r_{o,M2} = \frac{1}{\lambda_n I_{D,M1}} = 100k$$

$$g_{m,Q1} = \frac{I_C}{V_T} = 40 \, mA / V$$

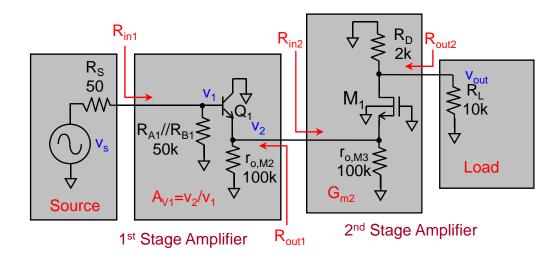
$$r_{\pi,Q1} = \frac{\beta}{g_{m,Q1}} = 2.5k$$

$$r_{o,Q1} = \frac{V_A}{I_{C,Q1}} = 100 k$$

Hint:

- 1) DC voltage source→AC ground
- 2) DC current source→Open circuit
- 3) DC block/bypass capacitor→AC short circuit
- Simplify the circuit for AC analysis by replacing current mirror with non-ideal current source
- Find out the AC small signal parameters (g_m, r_π, r_0) for transistors Q_1, M_1, M_2, M_3

AC Analysis: Identify Amplifier



1st stage amplifier configuration: Common Collector (CC)

2nd **stage amplifier configuration** : Common Gate (CG)

1st stage amplifier G_{m1} :
Not applicable
Table 3 Configuration C

2nd stage amplifier G_{m2} :
-($g_{m,M1}$ - $g_{mb,M1}$)=-3.54mA/V
Table 4 Configuration B

- Identify the 1st and 2nd stage amplifiers by drawing rectangular box surrounding them
- Write down the corresponding two ports-network parameters

AC Analysis: Identify Two-ports Network Parameters (R_{in2}, R_{out1})

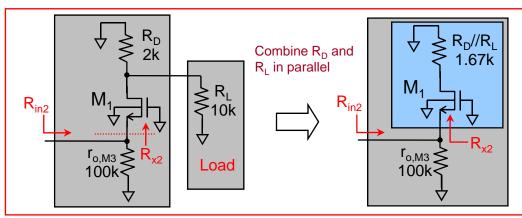
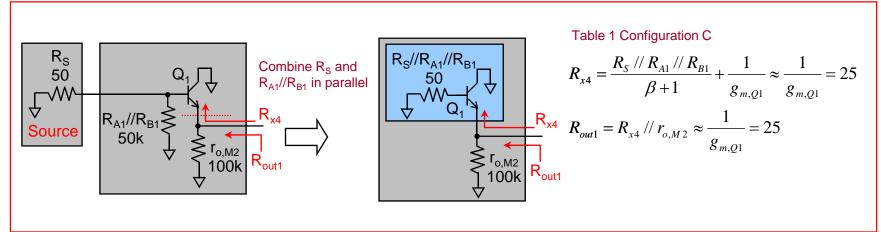


Table 2 Configuration D

$$R_{x2} = \frac{1}{g_{m,M1} - g_{mb,M1}} \frac{r_{o,M1} + (R_D // R_L)}{r_{o,M1}}$$

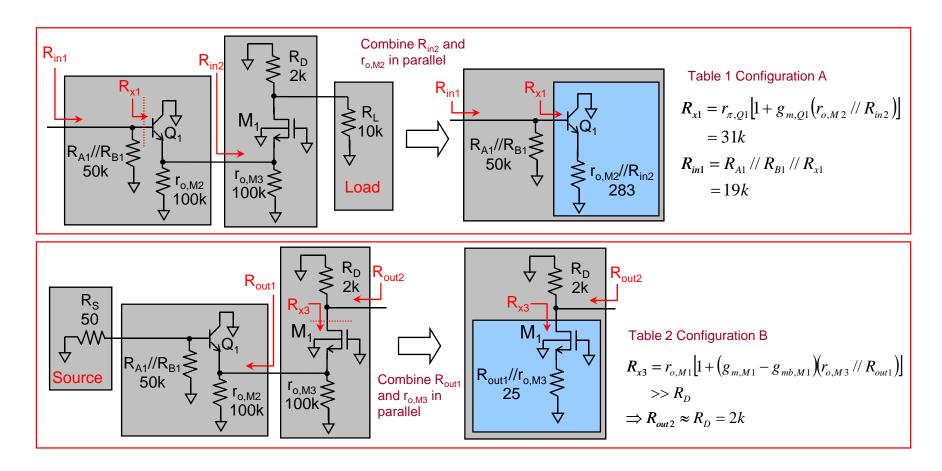
$$\approx \frac{1}{g_{m,M1} - g_{mb,M1}} = 283$$

$$R_{in2} = R_{x2} // r_{o,M3} \approx R_{x2} = \frac{1}{g_{m,M1} - g_{mb,M1}} = 283$$



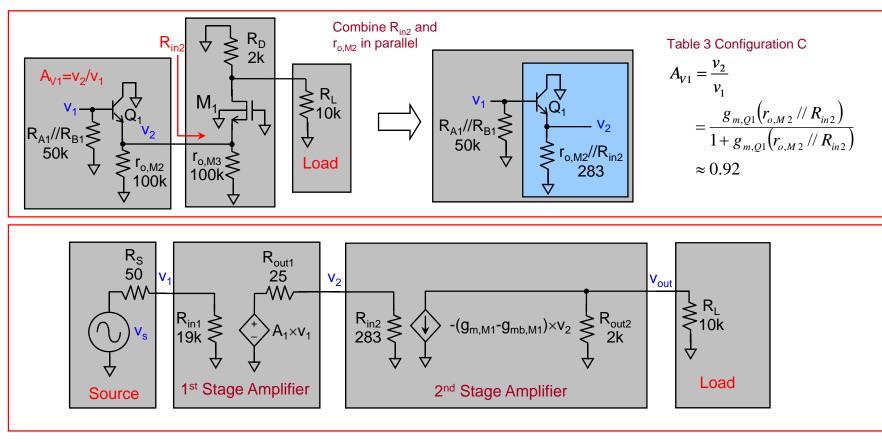
Estimate R_{in2} and R_{out1} (Throw away half the circuit)

AC Analysis: Identify Two-ports Network Parameters (R_{in1}, R_{out2})



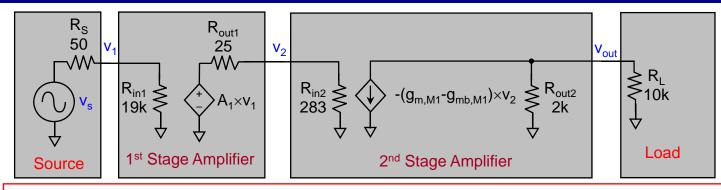
Estimate R_{in1} and R_{out2}

AC Analysis: Identify $A_{V1} = V_2/V_1$



- Estimate A_{V1}=v₂/v₁
- Draw out two-ports network equivalent

AC Analysis: Overall Gain A_V=v_{out}/v_s



$$V_{1} = \frac{R_{in1}}{R_{in1} + R_{S}} \times V_{s} \approx V_{s}$$

$$V_{2} = \frac{g_{m,Q1}(r_{o,M2} // R_{in2})}{1 + g_{m,Q1}(r_{o,M2} // R_{in2})} \times V_{1} \approx 0.92 \times V_{1} \approx 0.92 \times V_{s}$$

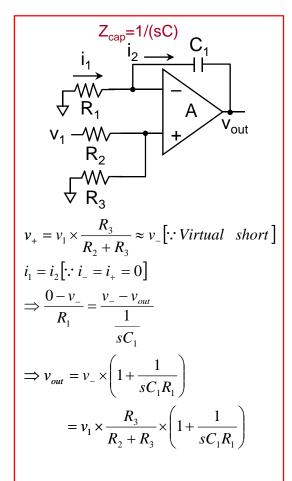
$$V_{out} = (g_{m,M1} - g_{mb,M1})(V_{2}) \times (R_{out2} // R_{L}) \approx 5.91 \times V_{2} \approx 5.43 \times V_{s}$$

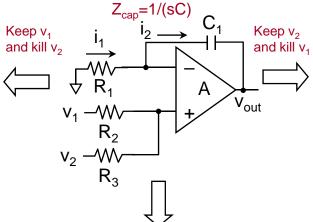
$$A_{V} = \frac{V_{out}}{V_{s}} = \frac{R_{in1}}{R_{in1} + R_{S}} \times \underbrace{A_{V1}}_{CC} \times \underbrace{G_{m2}(R_{out2} // R_{L})}_{CG}$$

$$= \underbrace{R_{in1}}_{Resistor \ Divider} \times \underbrace{\frac{g_{m,Q1}(r_{o,M2} // R_{in2})}{1 + g_{m,Q1}(r_{o,M2} // R_{in2})}}_{CC} \times \underbrace{\left(g_{m,M1} - g_{mb,M1}\right)(R_{out2} // R_{L}\right)}_{CG} = 5.43$$

Estimate overall gain A_V=v_{out}/v_s

Opamp Circuit Analysis

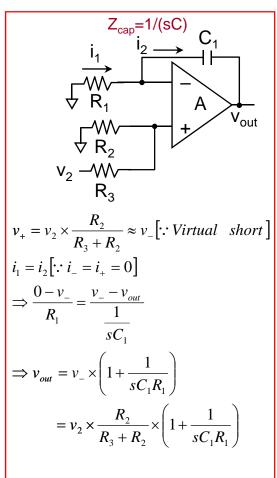




Superposition:

$$v_{out} = \left(\frac{v_1 \times R_3 + v_2 \times R_2}{R_2 + R_3}\right) \left(1 + \frac{1}{sC_1R_1}\right) \qquad \Rightarrow \frac{0 - v_-}{R_1} = \frac{v_- - v_{out}}{\frac{1}{sC_1}}$$

- Virtual short (v₊≈v₋)
- Infinite input resistance (i₊=i₋ =0)
- Superposition



BJT Equivalent Resistance Summary (Table 1)

Blue: look into collector terminal Red: look into base terminal Green: look into emitter terminal

Conf	r _x	Conf	r _x	Conf	r _x
R_{C} r_{x} R_{E}	$r_{\pi} + (1 + \beta)R_{E}$ $\approx r_{\pi} (1 + g_{m}R_{E})$	r _x R _s R _E	$r_{o} \left\{ 1 + g_{m} \left[(r_{\pi} + R_{S}) / / R_{E} \right] \left(\frac{r_{\pi}}{r_{\pi} + R_{S}} \right) \right\}$ $If R_{S} = 0 and r_{\pi} << R_{E}$ $\Rightarrow r_{x, \text{max}} = r_{o} (\beta + 1)$	r _x E	$\frac{1}{g_m}$
R _S W	$\frac{R_{S} + r_{\pi}}{1 + \beta} / / r_{o}$ $\approx \frac{R_{S}}{1 + \beta} + \frac{1}{g_{m}}$	R _C r _x	$\frac{1}{g_m} \times \frac{r_o + R_C}{r_o + \frac{R_C}{\beta}}$		

MOS Equivalent Resistance Summary (Table 2)

Blue: look into drain terminal

Red: look into gate terminal

Green: look into source terminal

Conf	r _x	Conf	r _x	Conf	r _x
r _x R _E	~	r _x R _S R _E	$r_o \left[1 + \left(g_m - g_{mb} \right) R_E \right]$	r _x	$\frac{1}{g_m}$
R _s V r _x C	$\frac{1}{g_m - g_{mb}}$	R _C	$\frac{1}{g_m - g_{mb}} \times \frac{r_o + R_C}{r_o}$		

BJT Summary (Table 3)

BJT	G_m	A_V
CE A	g_{m}	Derive Based on 2-ports Network
СВ	$-g_m$	Derive Based on 2-ports Network
CC $V_i \rightarrow V_{out}$	Not Applicable	$\frac{g_m R_L}{1 + g_m R_L}$
CE with Emitter Degeneration	$\frac{g_m}{1+g_m R_E}$	Derive Based on 2-ports Network

MOS Summary (Table 4)

MOS	G_{m}	A_V
CS	O.	Derive Based on 2-ports Network
A	g_{m}	
CG	$-(g_m-g_{mb})$	Derive Based on 2-ports Network
В	Drop g_{mb} if no body effect	
CD VJ	Not Applicable	$\frac{g_m R_L}{1 + (g_m - g_{mb}) R_L} \approx \frac{g_m}{g_m - g_{mb}}$
C VIII Vout		$(1+(g_m-g_{mb})R_L g_m-g_{mb})$ $(Drop g_{mb} if no body effect)$
\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\		Drop g_{mb} if no body effect
CS with R _E	g_m	Derive Based on 2-ports Network
	$\frac{g_m}{1+(g_m-g_{mb})R_E}$	
(6	Drop g_{mb} if no body effect	