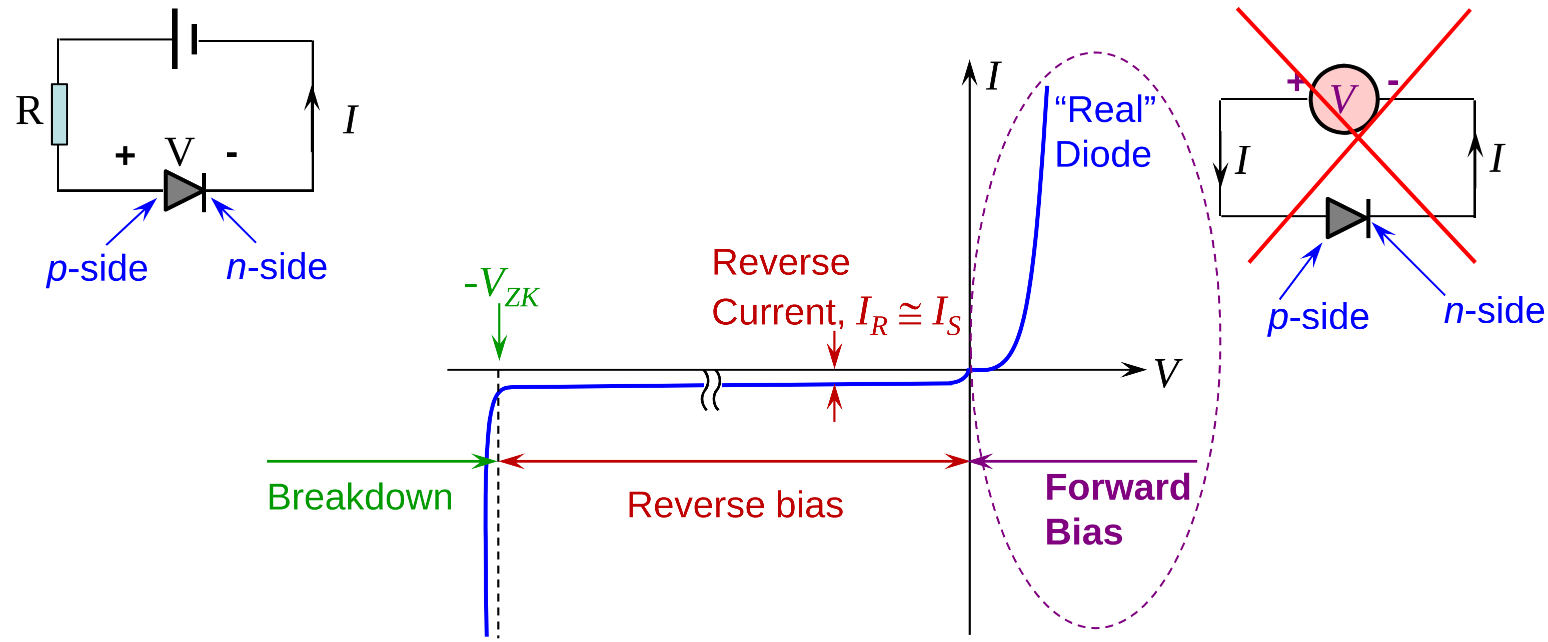
***pn* Junction**

1. Introduction
2. Open-Circuit Conditions
3. Reverse-Bias Conditions
4. Breakdown Region
5. Forward-Bias Conditions
6. Terminal Current-Voltage Characteristics
7. Depletion Capacitance and Diffusion Capacitance
8. Modeling the Diode
9. The *pn* Junction Circuit(s): Rectifier

Reference

- A.D. Sedra & K.C. Smith, "Microelectronic Circuits – Theory and Application", 5th Edition (International Version), Oxford University Press, Section 2.7.5.

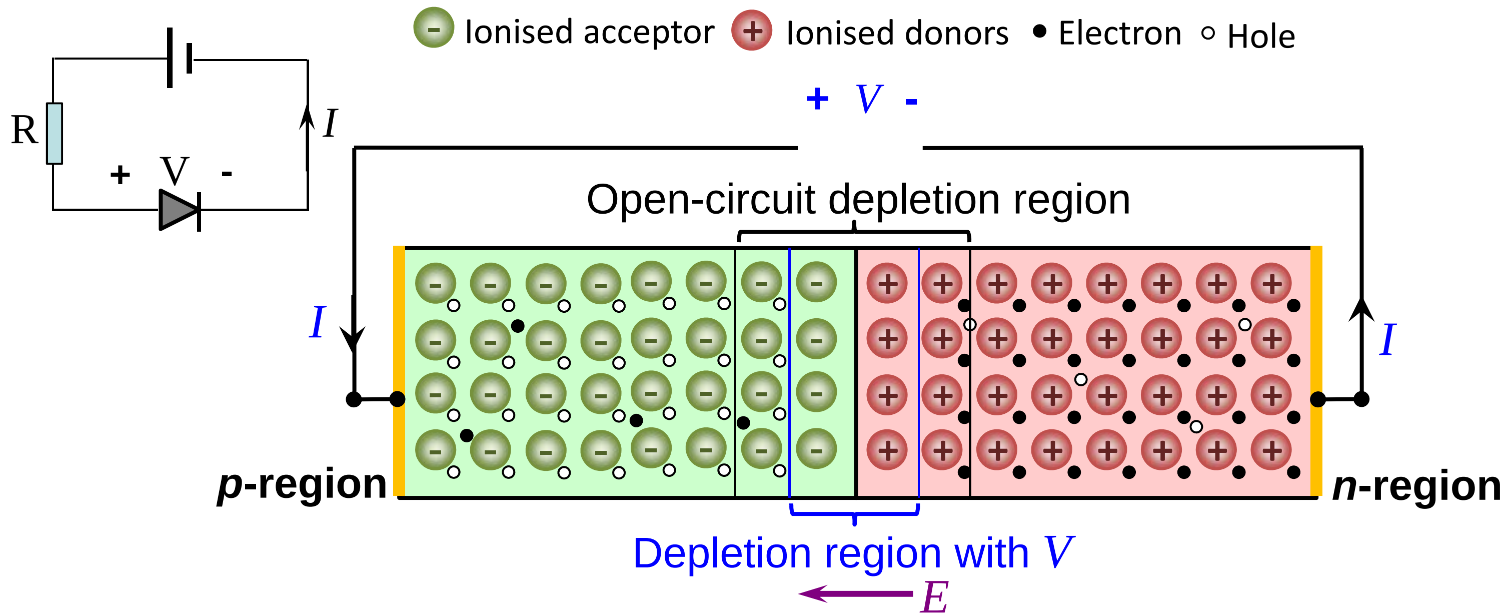
pn Junction – Forward-Bias Conditions



- Under forward-bias, an external voltage V is applied across the *pn* junction such that the *p*-region is at a positive voltage with respect to the *n*-region.

- A current flows from the positive terminal of V, through the *pn* junction (from *p*-region to *n*-region), to the negative terminal of V.

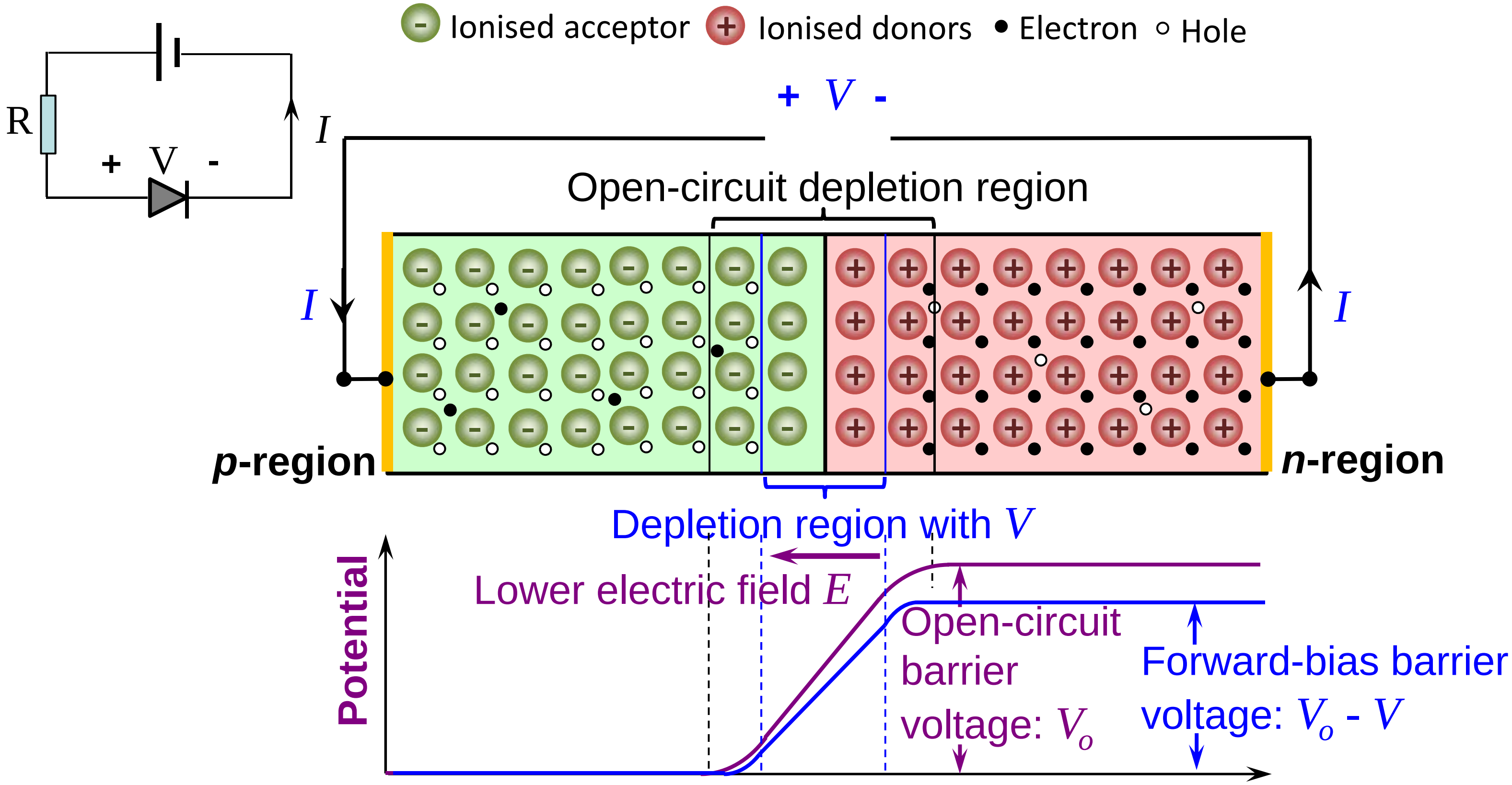
pn Junction – Foward-Bias Conditions



- Holes are supplied by the positive voltage terminal of V to the *p*-side.
- Holes (majority carriers) flow towards depletion region and will neutralize some of the uncovered negative bound charge (ionized acceptors), causing less charge in the depletion region.

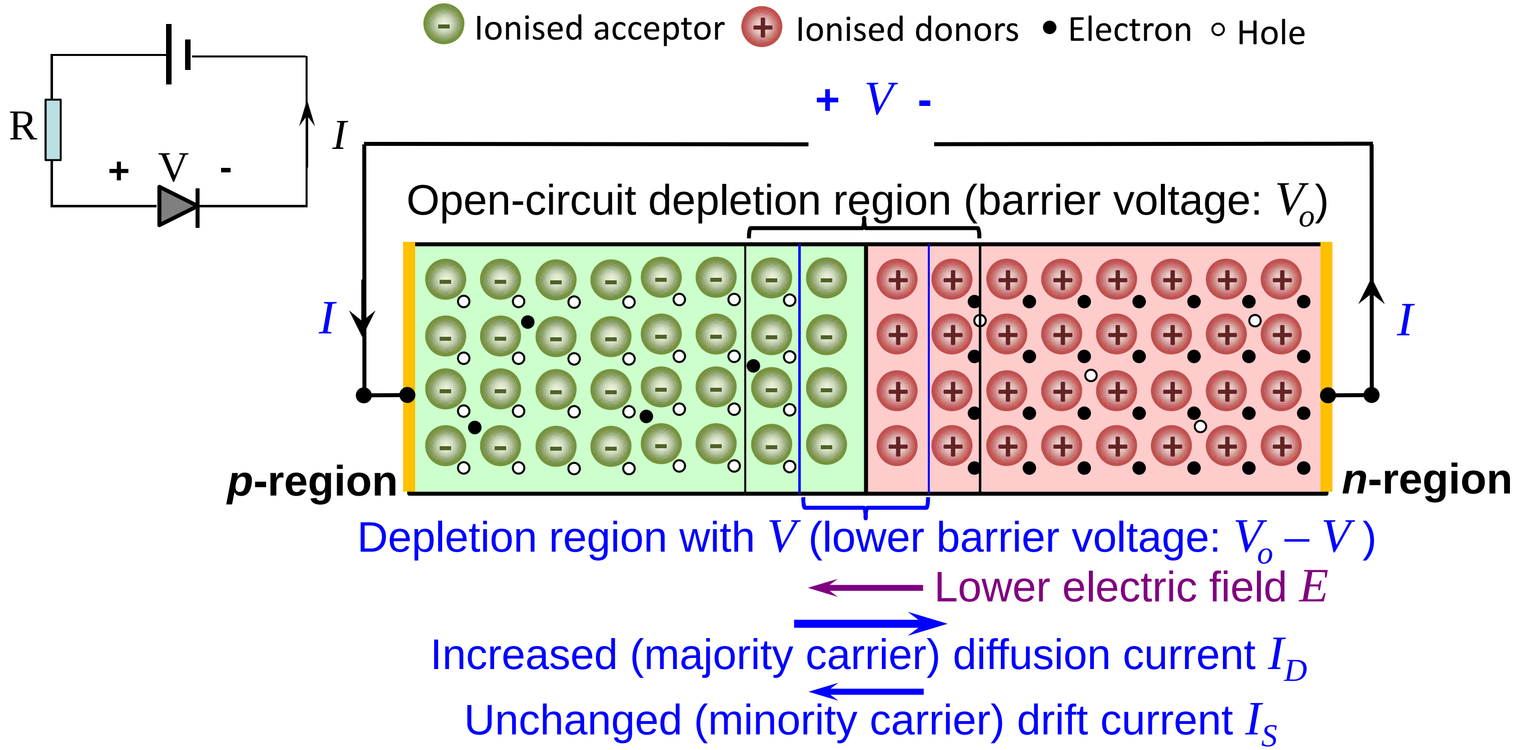
- Electrons are supplied by the negative voltage terminal of V to the *n*-side.
- Electrons (majority carriers) flow towards the depletion region and will neutralize some of the uncovered positive bound charge (ionized donors), causing less charge in the depletion region.

pn Junction – Forward-Bias Conditions



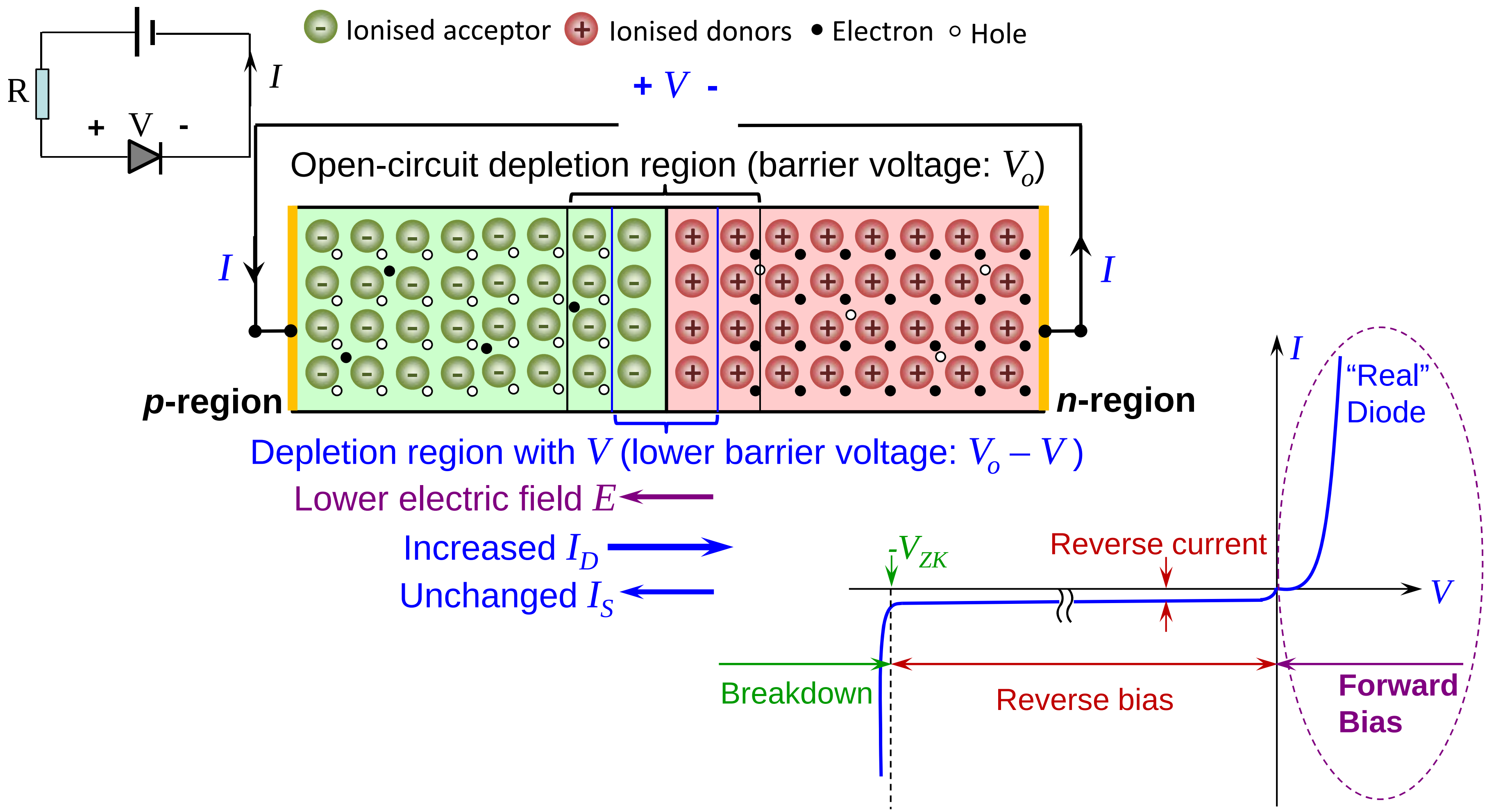
- Reduced bound charge leads to narrower depletion region (with respect to that under open-circuit conditions in slide pn-1.18)
  - Lower electric field and lower (barrier) voltage across the narrower depletion region
  - Barrier voltage of narrower depletion region is given by $V_o - V$

pn Junction – Forward-Bias Conditions



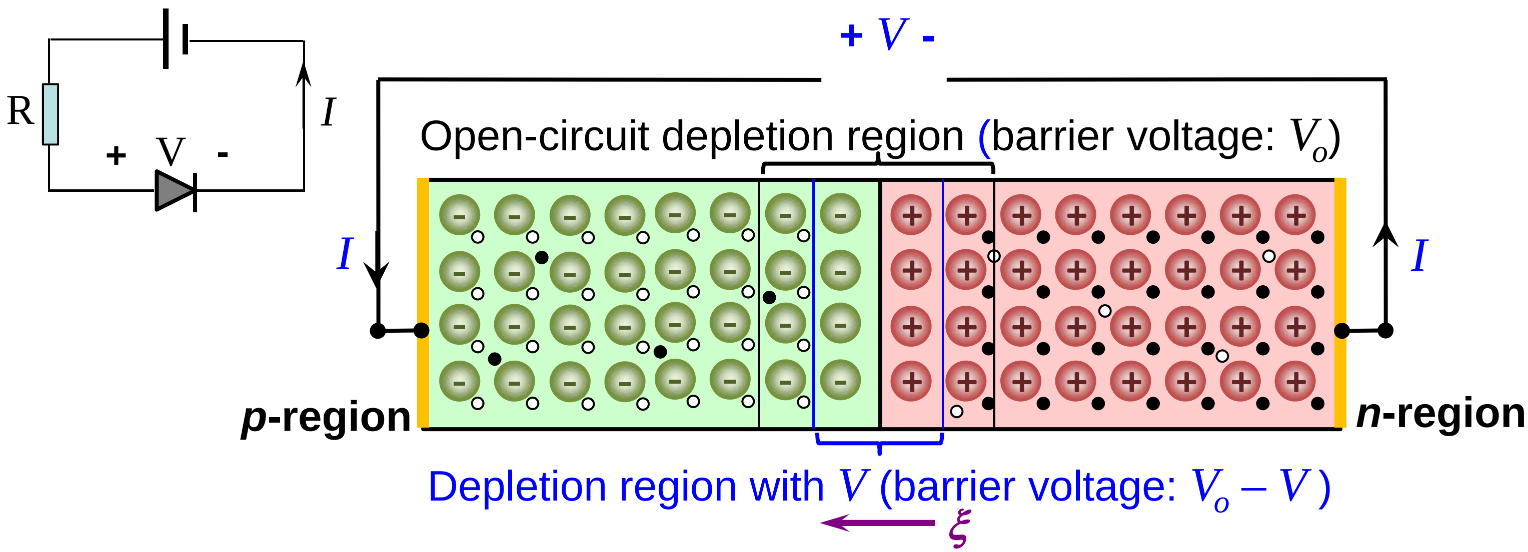
- Lower barrier voltage ($V_o - V$) allows more (majority) holes to cross the barrier from the *p*-region to the *n*-region, and more (majority) electrons from the *n*-region to the *p*-region. Hence, the diffusion current I_D increases.
- I_D increases rapidly with increasing forward bias as it is due to majority carriers, which are in large supply (Slide pn-1.8).
- The minority carrier drift current I_S is independent on depletion region barrier, hence it is not changed (Slide pn-1.15).

pn Junction – Forward-Bias Conditions



- In summary, under forward-bias, a (net) current flows through the *pn* junction (from *p*-region to *n*-region): $I = I_D - I_S \cong I_D$, and it increases rapidly with increasing forward bias (since I_D is due to majority carriers)

pn Junction – Forward-Bias Conditions



- Width of the depletion region under (low) forward-bias is given by equation (2.3) by replacing V_o, the barrier voltage across the depletion region under open-circuit conditions, by $(V_o - V)$ –

$$W_{dep} = x_p + x_n = \sqrt{\frac{2\varepsilon_s}{q}\left[\frac{1}{N_A} + \frac{1}{N_D}\right](V_o - V)} \qquad (2.5)^*$$

- Equation (2.2) that relates x_p and x_p is still valid – $\frac{x_p}{x_n} = \frac{N_D}{N_A}$ (2.2)

*Take note that the validity of Eq.(2.5) is not good at high *V* .

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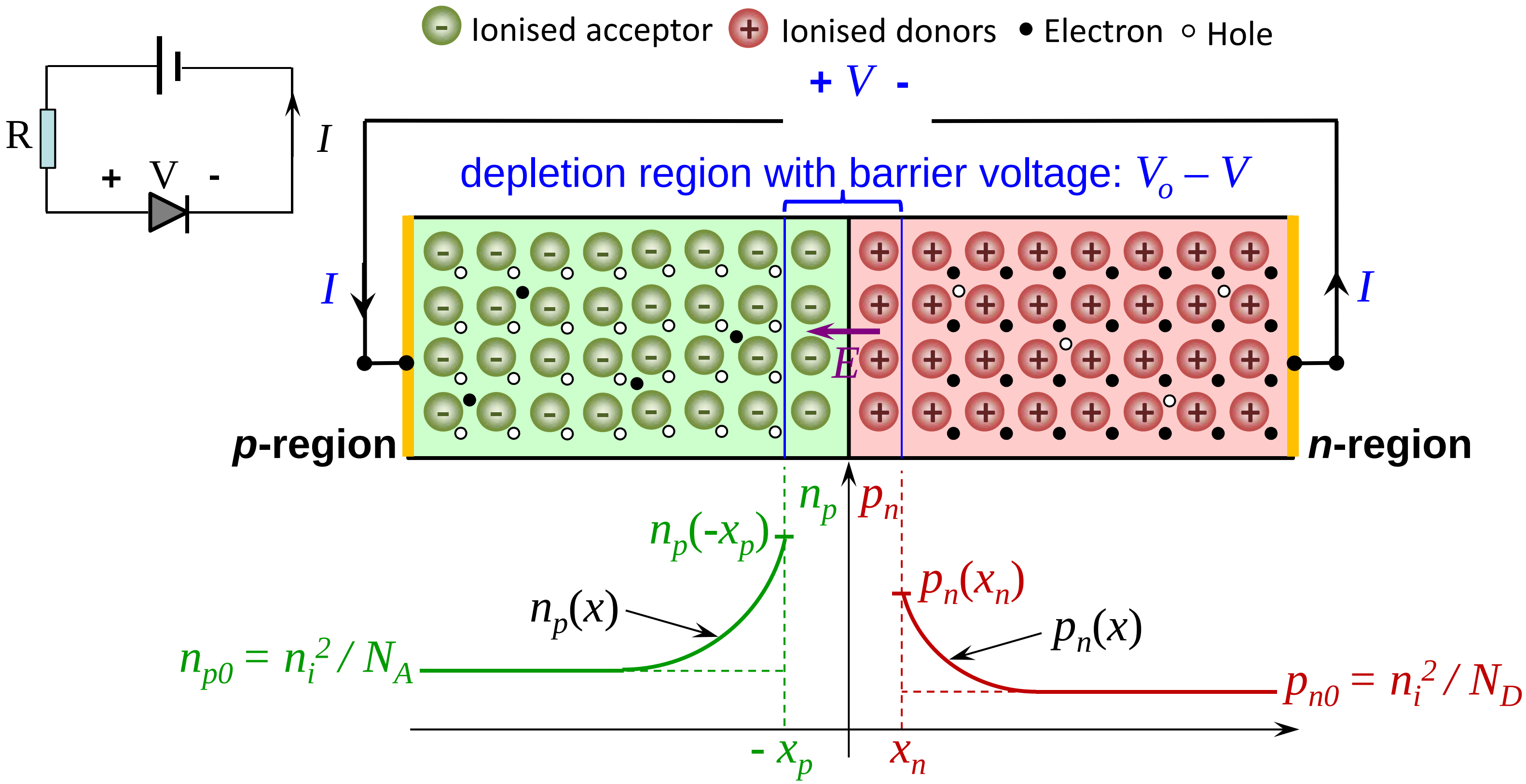
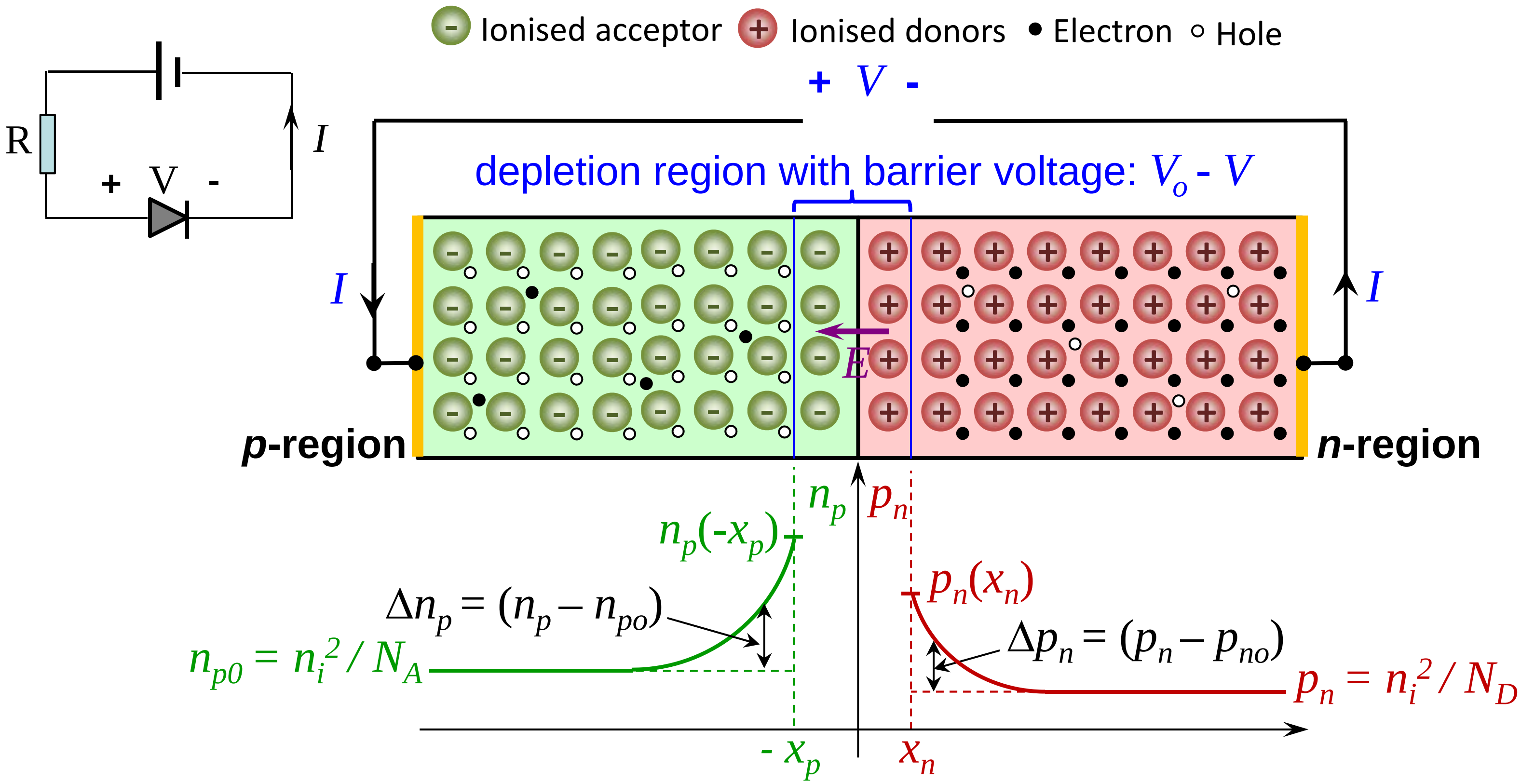
pn Junction – Terminal Current-Voltage Characteristics



- Under forward-bias, owing to the decreased barrier voltage ($V_o - V$), holes are injected from the *p*-region across the junction into the *n*-region, and electrons are injected from the *n*-region across the junction into the *p*-region

- Injected holes in the *n*-region will cause the minority carrier concentration there, p_n, to exceed the thermal equilibrium value, p_{n0} (= n_i^2 / N_D) (Slide 1.44).

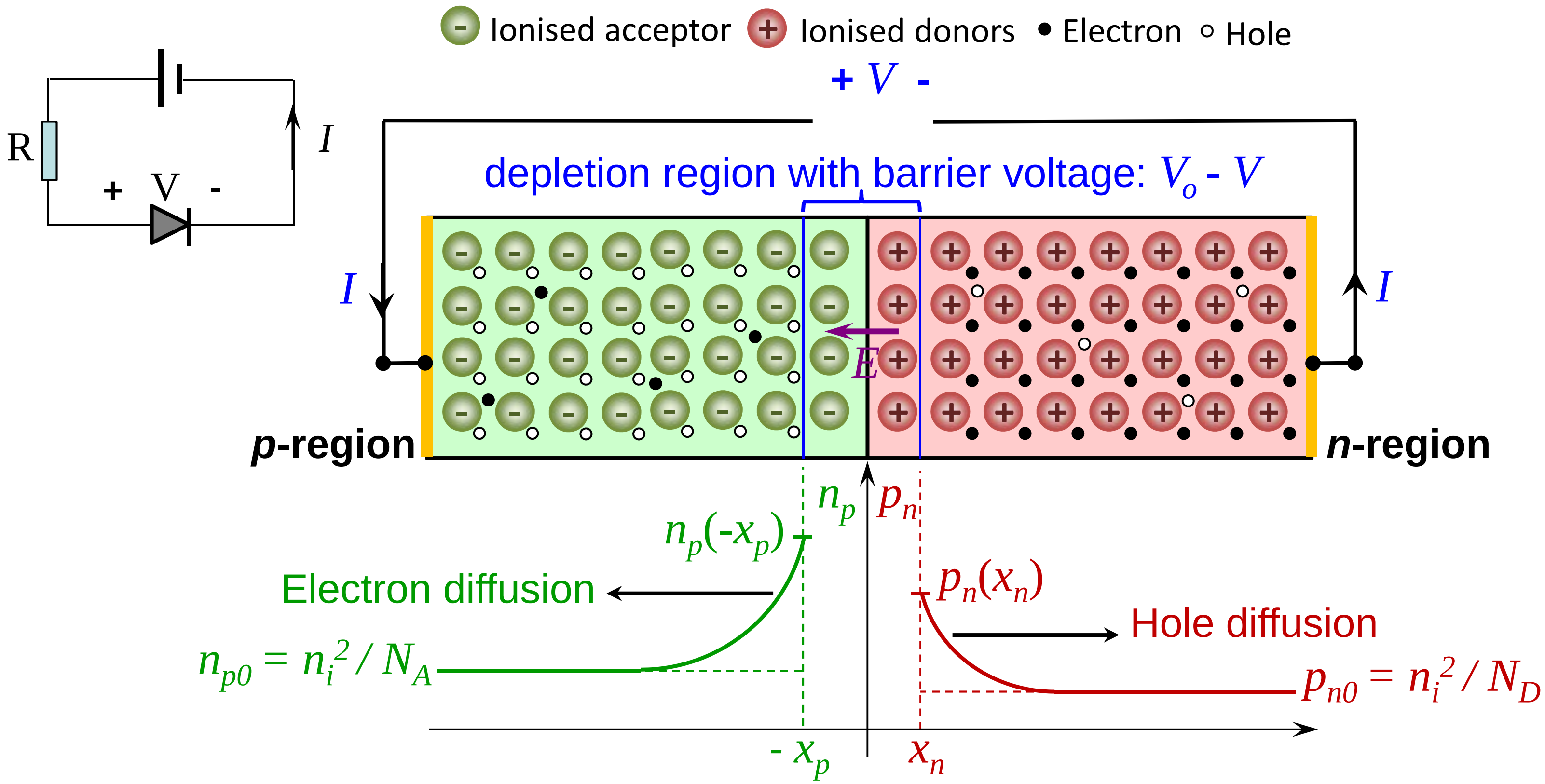
pn Junction – Terminal Current-Voltage Characteristics



- Similarly, injected electrons in the *p*-region will cause the minority carrier concentration there, n_p, to exceed the thermal equilibrium value, $n_{p0}(= n_i^2 / N_A)$.

- The excess hole (minority carrier) concentration in the *n*-region $\Delta p_n = (p_n - p_{n0})$ is highest near the edge of the depletion region and will decrease away from the junction. The same can be said of the excess electron (minority carrier) concentration in the *p*-region $\Delta n_p = (n_p - n_{p0})$.

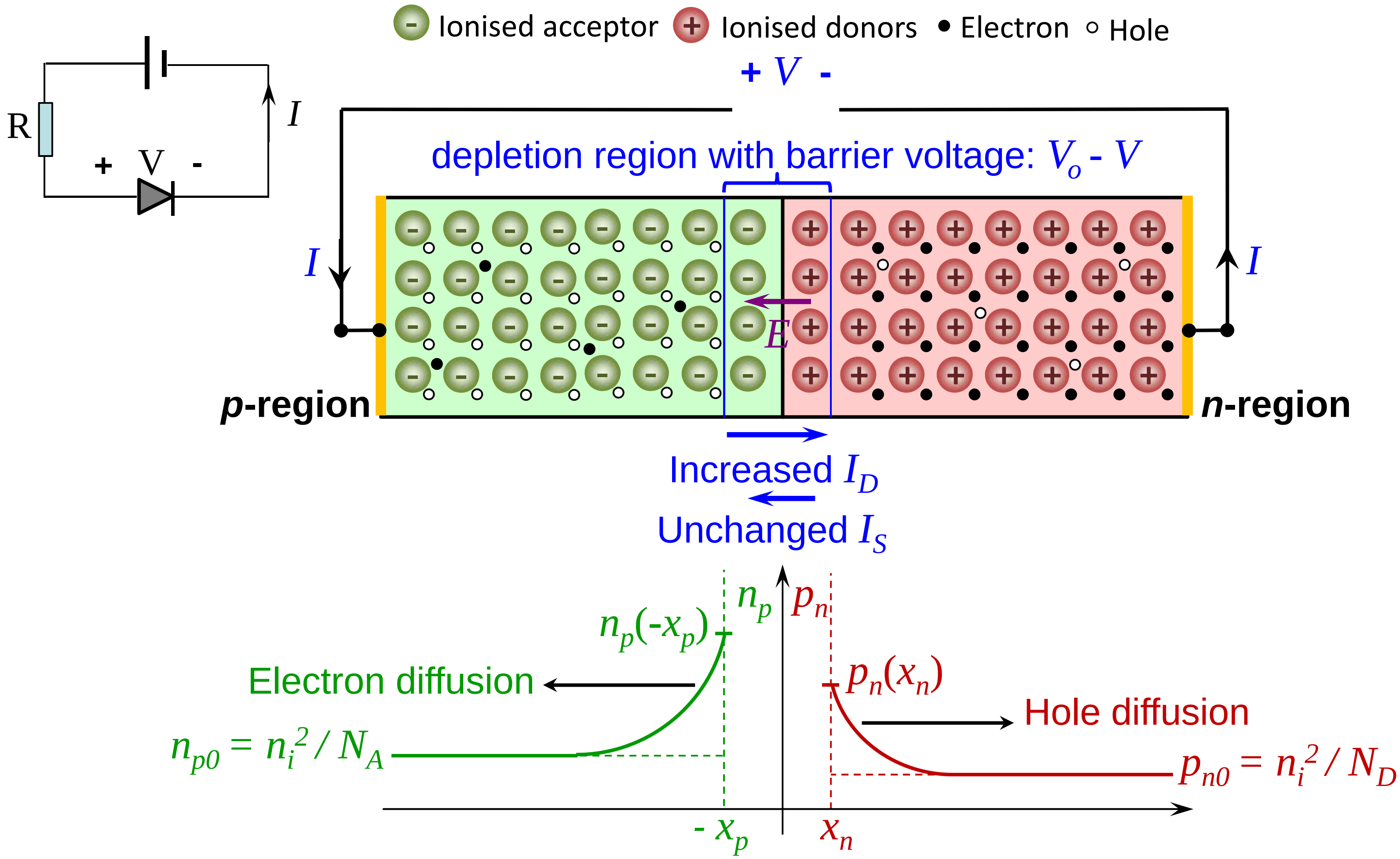
pn Junction – Terminal Current-Voltage Characteristics



- Injected/excess holes will diffuse away from the junction into the *n*-region and disappear by recombination. An equal number of electrons will be supplied by bias V to replenish the electron supply in the *n*-region.

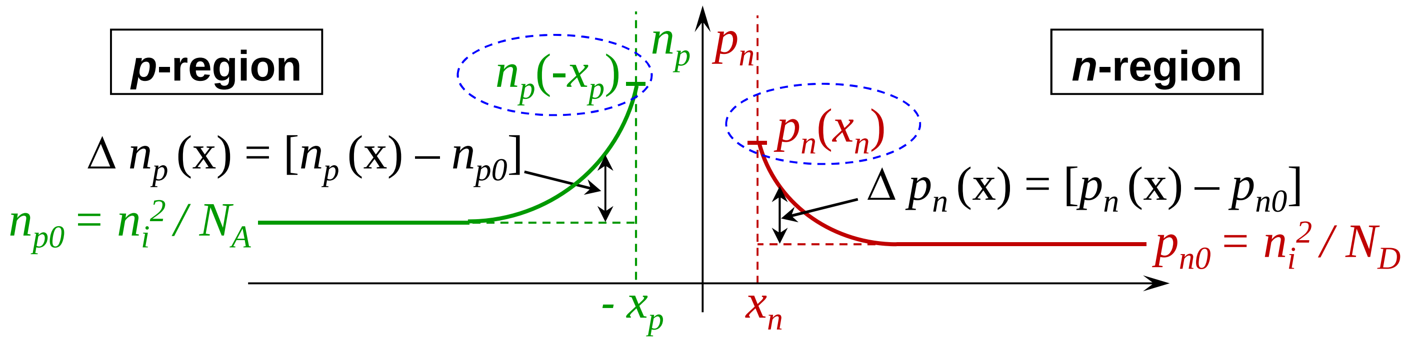
- Similar statements can be made about the injected /excess electrons in the *p*-region and an equal number of holes will be supplied by bias V to replenish the holes supply in the *p*-region.

pn Junction – Terminal Current-Voltage Characteristics



- The diffusion of excess minority carriers (holes in neutral *n*-region and electrons in neutral *p*-region) gives rise to the increase of diffusion current I_D above I_S.

pn Junction – Forward-Bias Conditions



Minority carrier concentration distribution

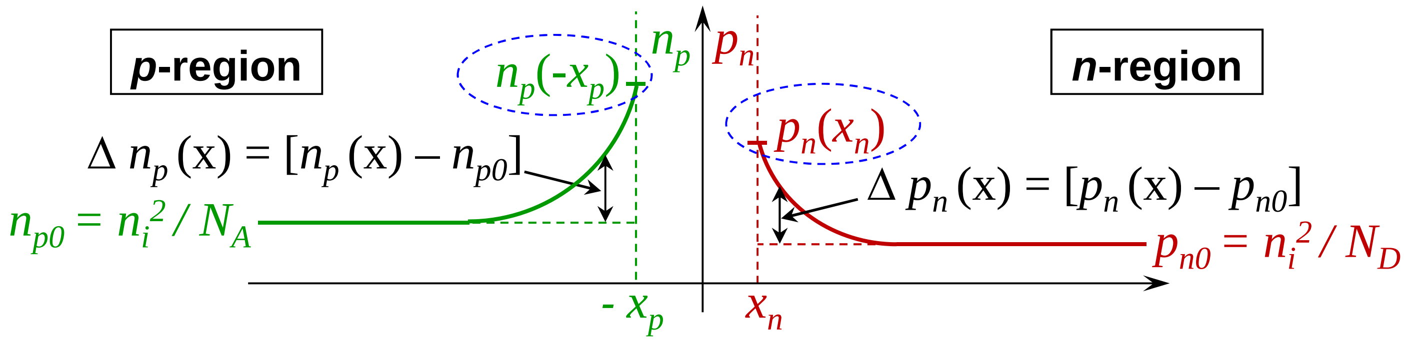
- The concentration of minority carriers at the depletion edge is found using the Law of Junction:

concentration of minority carriers at the depletion edge = (the equilibrium minority carrier concentration at the edge) x exponential of (V/V_T).

- Hence the concentration of minority carriers (holes) $p_n(x_n)$ at the edge of the depletion region located at $x = x_n$ is given by the Law of Junction:
  - *n*-region: $p_n(x_n) = p_{n0}\, e^{V/V_T}$ (2.6)
- Similarly, the concentration of minority carriers (electrons) $n_p(-x_p)$ at the edge of the depletion region located at $x = -x_p$ is given by the Law of Junction:
  - *p*-region: $n_p(-x_p) = n_{p0}\, e^{V/V_T}$ (2.7)

pn Junction – Forward-Bias Conditions

Minority carrier distribution



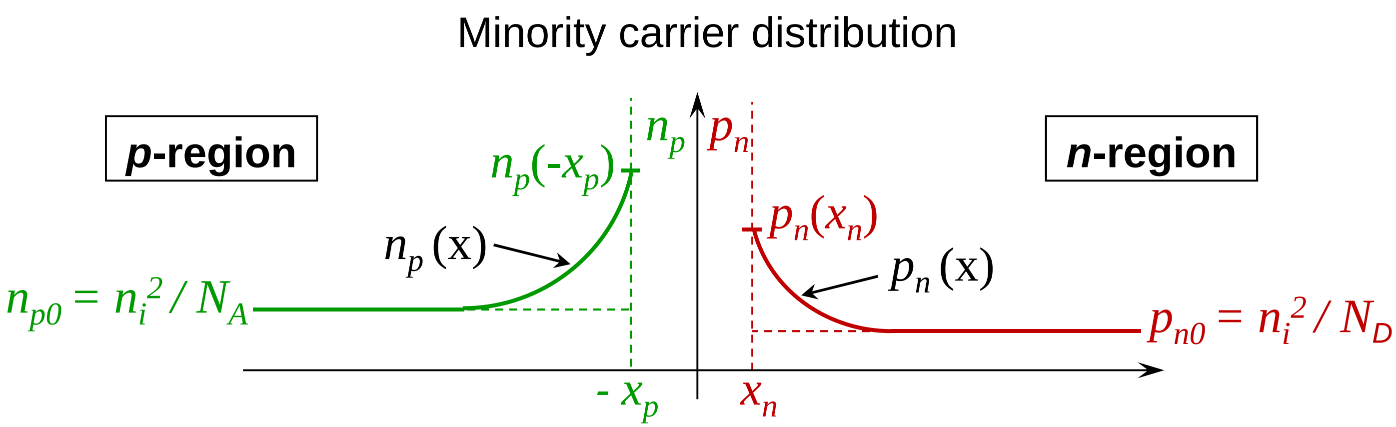
Minority carrier concentration distribution

- The excess concentration of minority carriers is given by

Excess minority carrier concentration = (Actual concentration of minority carriers) – (equilibrium concentration of minority carriers).

- The distribution of excess minority carrier concentration is exponentially decaying from the edge of the depletion region:
  - *n*-region: $\Delta p_n(x) = p_n(x) - p_{n0} = [p_n(x_n) - p_{n0}]e^{-(x-x_n)/L_p}$ (2.8)
  - *p*-region: $\Delta n_p(x) = n_p(x) - n_{p0} = [n_p(-x_p) - n_{p0}]e^{(x+x_p)/L_n}$ (2.9)

pn Junction – Terminal Current-Voltage Characteristics

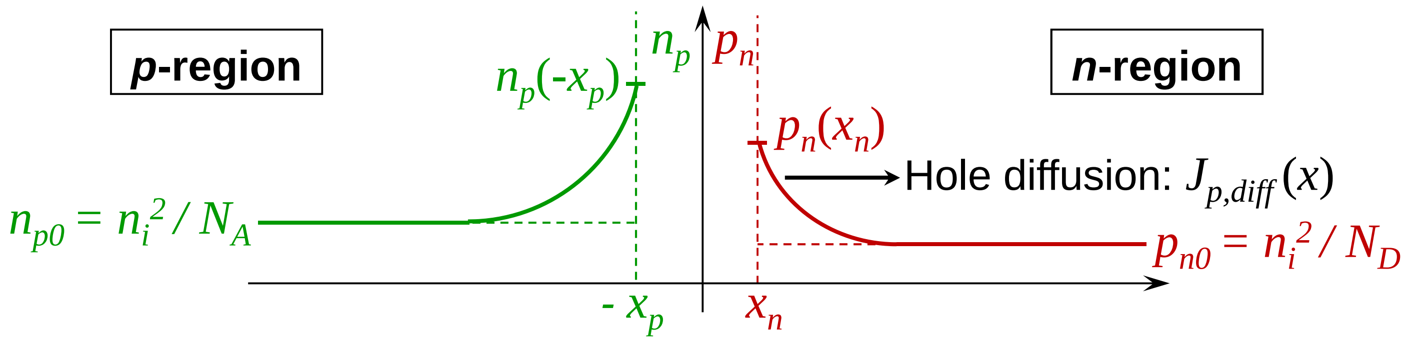


Minority carrier concentration distribution

- The distribution of minority carrier concentration is also exponentially decaying from the edge of the depletion region:
  - *n*-region: $p_n(x) = p_{n0} + [p_n(x_n) - p_{n0}]e^{-(x-x_n)/L_p}$ (2.10)
  - *p*-region: $n_p(x) = n_{p0} + [n_p(-x_p) - n_{p0}]e^{(x+x_p)/L_n}$ (2.11)
- L_p is the diffusion length of holes (minority carrier) in the *n*-region, and L_n is the diffusion length of electrons (minority carrier) in the *p*-region. The diffusion length is an average distance over which minority carriers recombine.
- Smaller L_p means injected holes will recombine faster with majority electrons in the *n*-region, resulting in steeper decay of minority hole concentration $p_n(x)$.

pn Junction – Terminal Current-Voltage Characteristics

Minority carrier distribution



Minority carrier diffusion current

- Hole diffusion current density in the neutral *n*-region (i.e., beyond the depletion region) is given by (Slide 1.54)

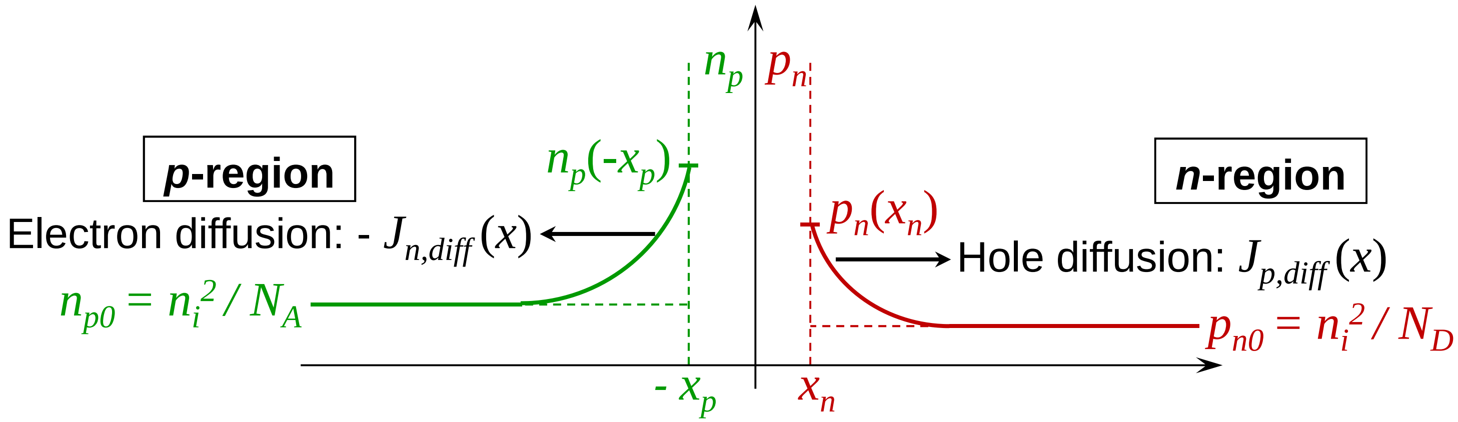
$$J_{p,diff}(x) = -qD_p \frac{dp_n(x)}{dx} \qquad (2.12)$$

- Substituting $p_n(x)$ by equations (2.10) and applying equation (2.6) gives

$$J_{p,diff}(x) = q\frac{D_p}{L_p} p_{n0}(e^{V/V_T} - 1)\, e^{-(x-x_n)/L_p} \qquad (2.13)$$

- $J_{p,diff}(x)$ is seen to be largest at the edge of the depletion region ($x = x_n$) and decays exponentially with increasing x (owing to recombination).

pn Junction – Terminal Current-Voltage Characteristics



Minority carrier diffusion current and total current

- Similar expression for electron diffusion current can be obtained to get

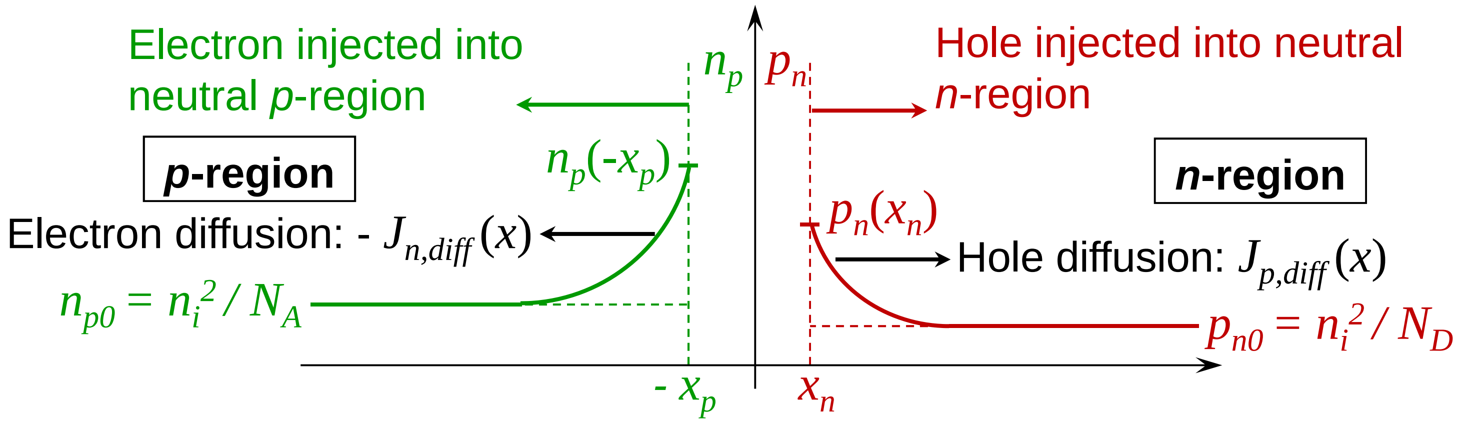
$$J_{n,diff}(x) = q\frac{D_n}{L_n} n_{p0}(e^{V/V_T} - 1)\, e^{(x+x_p)/L_n} \quad (2.14)$$

- The total current density J throughout the pn junction is the same throughout and is given by the sum of injected minority carrier diffusion current at the depletion edges from equations 2.13 and 2.14:

$$J = J_{p,diff}(x = x_n) + J_{n,diff}(x = -x_p)$$

$$= \frac{qD_p p_{n0}}{L_p}(e^{V/V_T} - 1) + \frac{qD_n n_{p0}}{L_n}(e^{V/V_T} - 1) \quad (2.15)$$

pn Junction – Terminal Current-Voltage Characteristics



<u>Current-voltage relationship</u>

- The total current flowing through the forward-bias *pn* junction, I, is J from equation 2.15 multiplied by the junction cross-sectional area *A* –

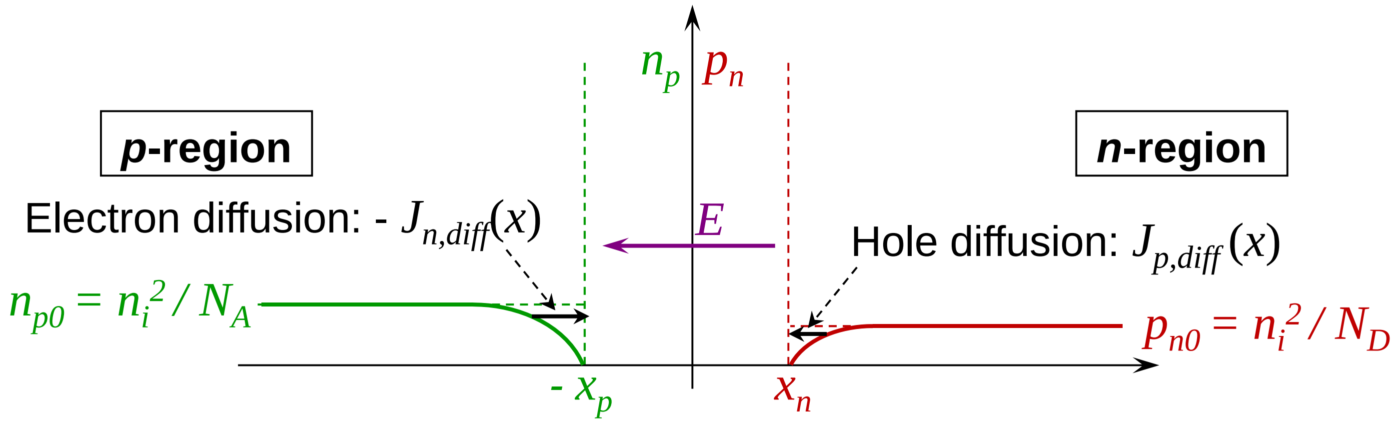
$$I = AJ = A\left(\frac{qD_p p_{n0}}{L_p} + \frac{qD_n n_{p0}}{L_n}\right)(e^{V/V_T} - 1) \qquad (2.16)$$

- Substituting for $p_{n0} = n_i^2 / N_D$ and for $n_{p0} = n_i^2 / N_A$ (Slide 1.44)

$$I = Aq\,n_i^2\left(\frac{D_p}{L_p N_D} + \frac{D_n}{L_n N_A}\right)(e^{V/V_T} - 1) \qquad (2.17)$$

- Equation (2.16)/(2.17) is also valid for reverse bias, where V becomes negative.

pn Junction – Terminal Current-Voltage Characteristics



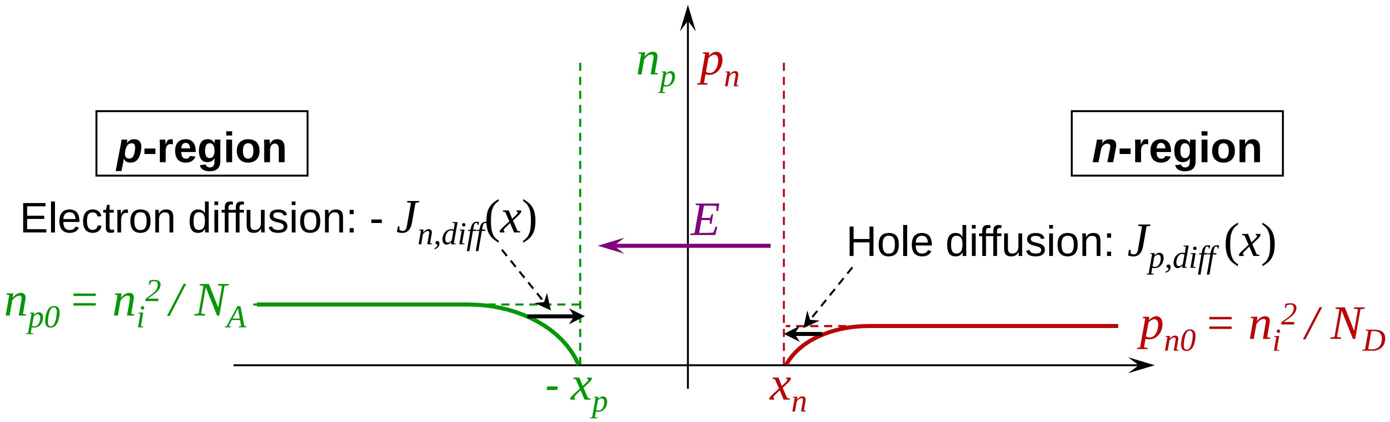
Minority carrier concentration distribution (reverse bias)

- In fact, equations (2.6) to (2.11) are also valid for reverse bias with V being negative –
  - *n*-region: $p_n(x_n) = p_{n0}\, e^{V/V_T}$ (2.6)

    $$p_n(x) = p_{n0} + [p_n(x_n) - p_{n0}]e^{-(x-x_n)/L_p} \quad (2.10)$$
  - *p*-region: $n_p(-x_p) = n_{p0}\, e^{V/V_T}$ (2.7)

    $$n_p(x) = n_{p0} + [n_p(-x_p) - n_{p0}]e^{(x+x_p)/L_n} \quad (2.11)$$
- Above figure shows the extraction of minority carriers under reverse bias conditions – minority carrier concentrations at edges of depletion region lower than equilibrium (open circuit) values.

pn Junction – Terminal Current-Voltage Characteristics



Current-voltage relationship (reverse bias)

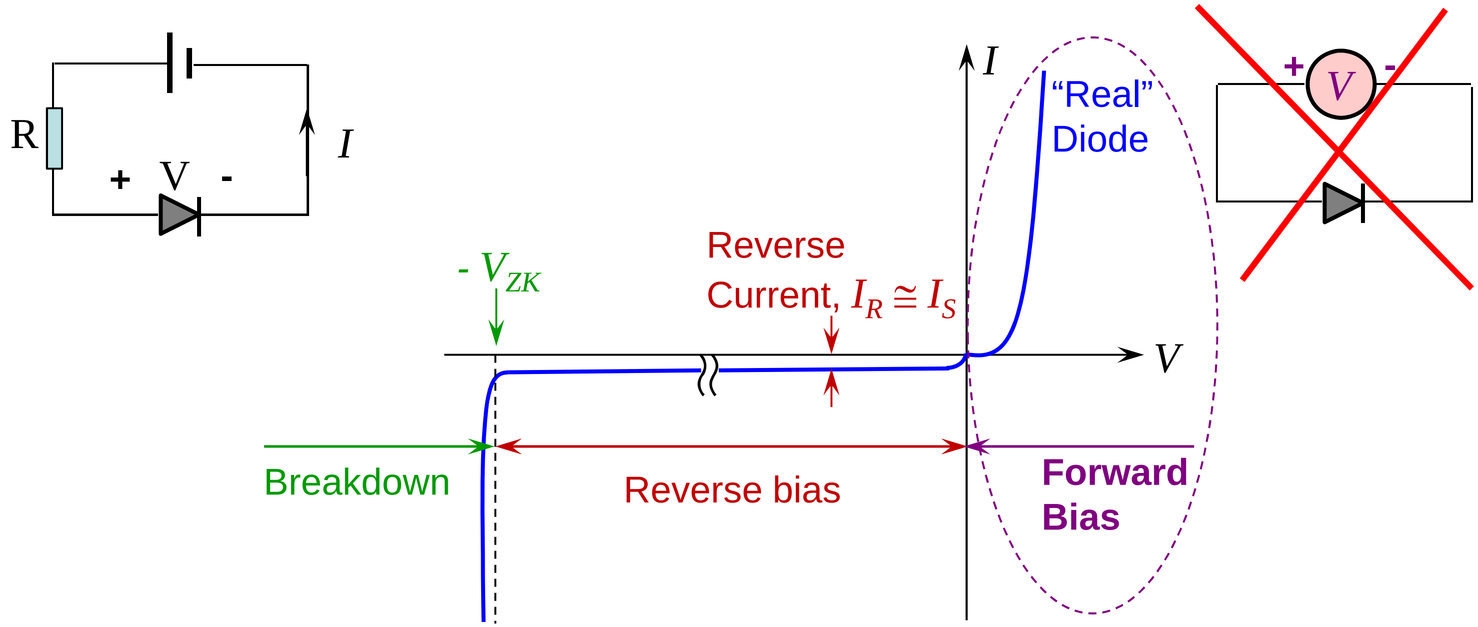
$$I = Aq\,n_i^2\left(\frac{D_p}{L_p N_D} + \frac{D_n}{L_n N_A}\right)\left(e^{V/V_T} - 1\right) \qquad (2.17)$$

- With high enough negative (reverse) bias V, the exponential term in equation (2.17) becomes much smaller than 1 and

$$I = -Aq\,n_i^2\left(\frac{D_p}{L_p N_D} + \frac{D_n}{L_n N_A}\right) = -I_S \qquad (2.18)$$

which gives a current flow in reverse bias that is independent on V for V < -0.1V , which is consistent with slide pn-1.31 and is the reverse current I_S.

pn Junction – Terminal Current-Voltage Characteristics



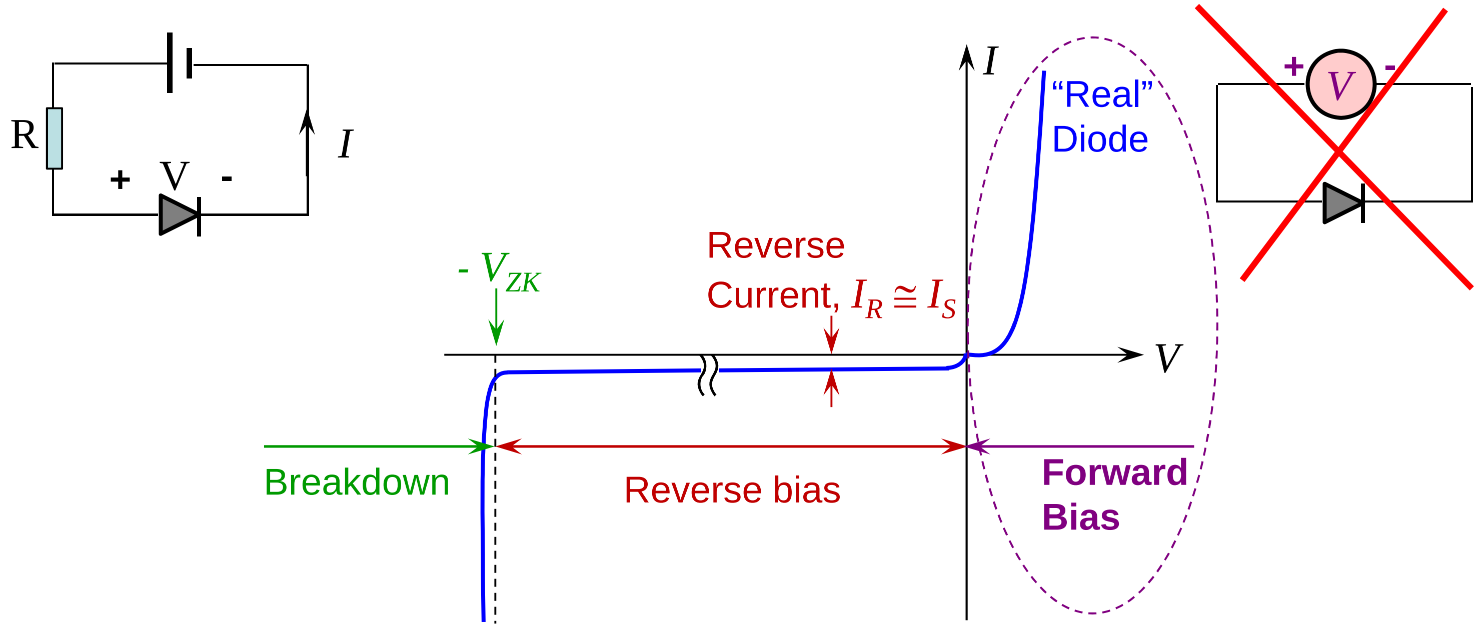
Current-voltage relationship

- $$I = Aqn_i^2\left(\frac{D_p}{L_pN_D}+\frac{D_n}{L_nN_A}\right)(e^{V/V_T}-1) = I_S(e^{V/V_T}-1) \qquad (2.19)$$

where $$I_S = Aqn_i^2\left(\frac{D_p}{L_pN_D}+\frac{D_n}{L_nN_A}\right) \qquad (2.20)$$

- I_S is called the (reverse) saturation current as it is independent on V. I_S is a function of n_i^2, hence a strong function of temperature.

pn Junction – Terminal Current-Voltage Characteristics



Current-voltage relationship (real diode)

- For real diode (*pn* junction), an exponential factor *n* is added to equation (2.19)

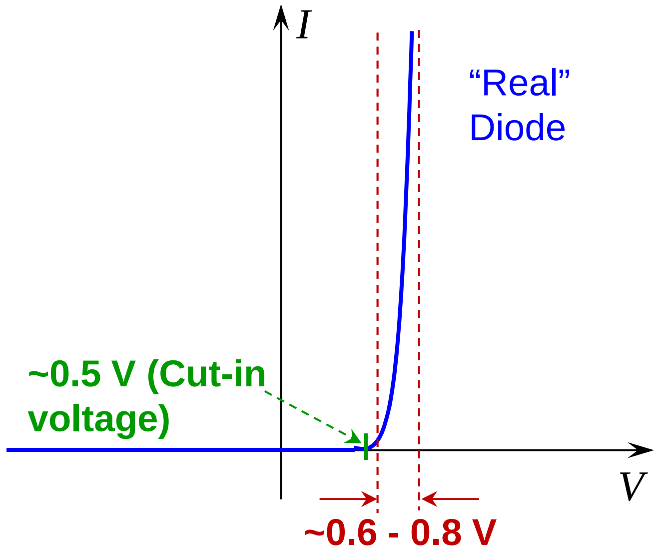
$$I = Aqn_i^2\left(\frac{D_p}{L_pN_D} + \frac{D_n}{L_nN_A}\right)\left(e^{\frac{V}{nV_T}} - 1\right) = I_S\left(e^{\frac{V}{nV_T}} - 1\right) \qquad (2.21)$$

- *n* has a value between 1 and 2, depending on the material and physical structure of the *pn* junction.

pn Junction – Terminal Current-Voltage Characteristics

Current-voltage (IV) relationship (summary)

$$I = I_S(e^{\frac{V}{nV_T}} - 1) \qquad (2.21)$$



- For substantial forward bias ($V > 0$), $e^{\frac{V}{nV_T}} >> 1$ in equation (2.21) and

$$I \cong I_S e^{\frac{V}{nV_T}} \qquad (2.22a)$$

or

$$V \cong nV_T \ln(I / I_S) \qquad (2.22b)$$

- Owing to the exponential IV relationship –
  - I is negligibly small for $V <$ ~0.5 V (this value is known as the cut-in voltage)
  - For a fully conducting *pn* junction (meaning with substantial current flowing through), the voltage drop across it lies in a narrow range, ~0.6 to 0.8 V.

- In reverse bias ($V < 0$, with $|V| >$ a few times V_T), $I \cong -I_S$.

- Equation (2.21) does not predict the breakdown characteristic.

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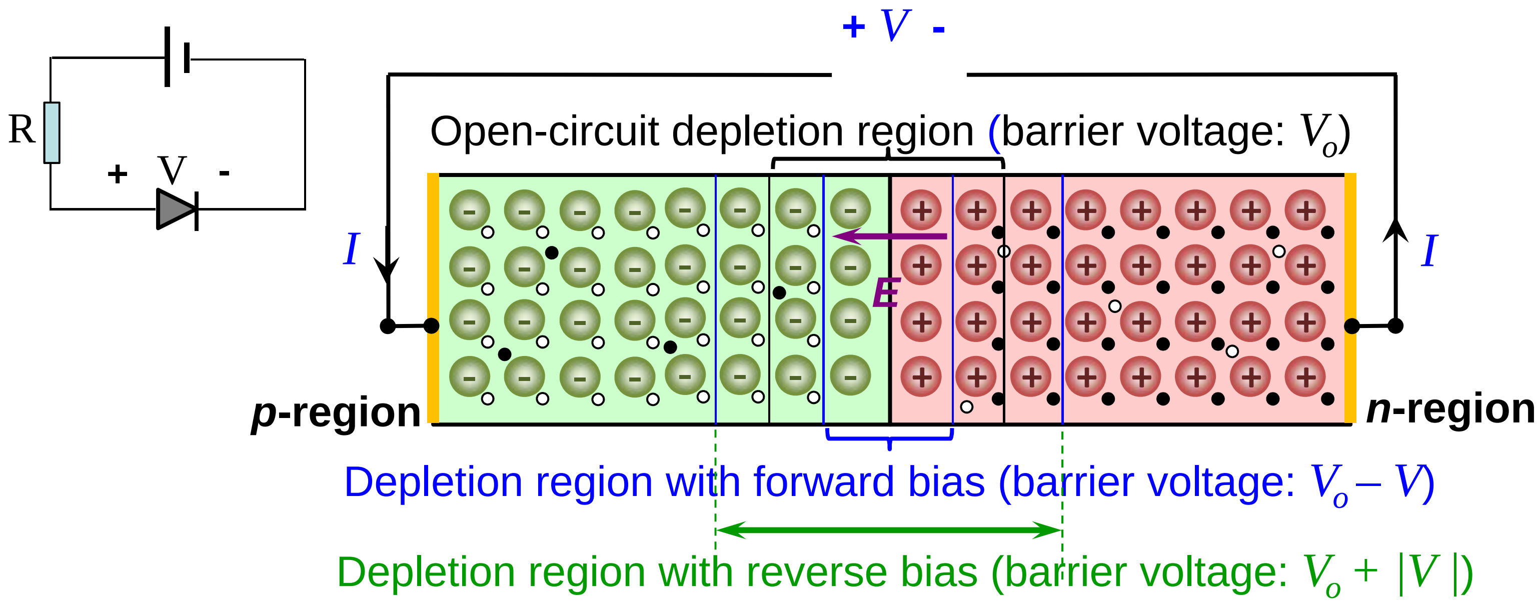
pn Junction – Depletion Capacitance and Diffusion Capacitance



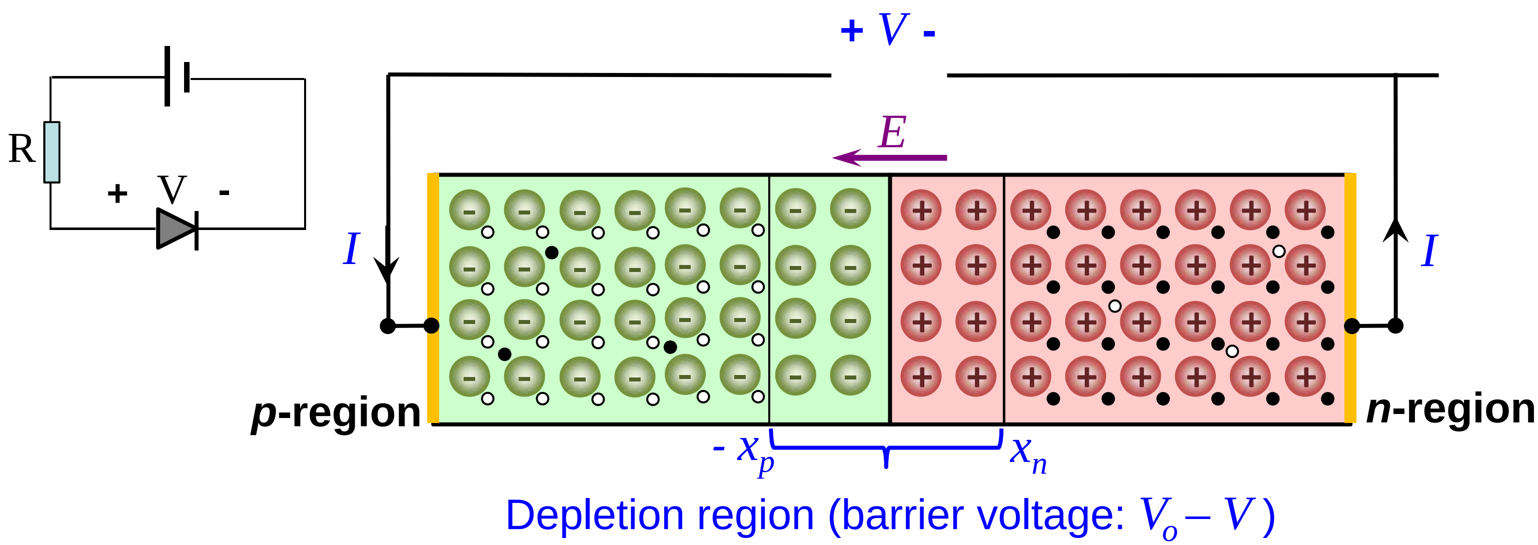
- We have seen that the width of the depletion region varies with the bias V -

$$W_{dep} = x_p + x_n = \sqrt{\frac{2\varepsilon_s}{q}\left[\frac{1}{N_A} + \frac{1}{N_D}\right](V_o - V)} \qquad (2.23)$$

where V is positive for forward bias and negative for reverse bias.

- Clearly, charge stored in the two sides of the depletion region also changes with V. This is analogous to a parallel plate capacitor.

pn Junction – Depletion Capacitance and Diffusion Capacitance



- Charge stored in either side of the depletion region are equal in magnitude and is given by

$$q_J = qx_p AN_A = qx_n AN_D \quad (2.24)$$

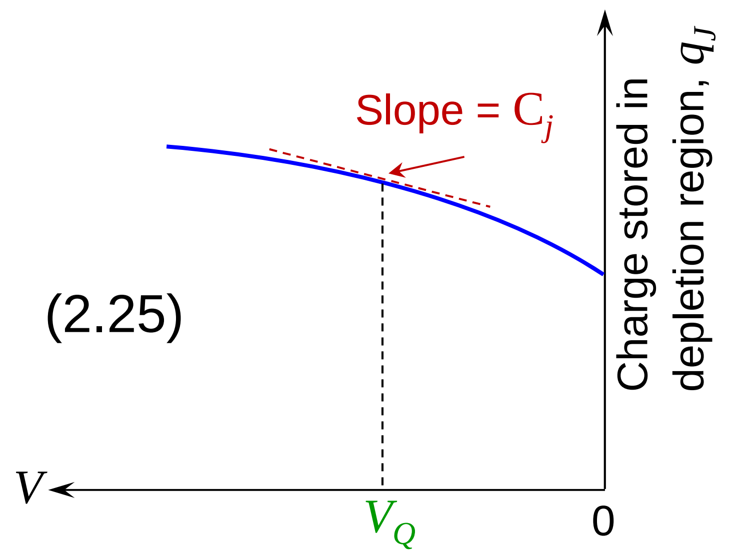
- Applying equation (2.23) to equation (2.24) gives

$$q_J = qAN_A x_p = qAN_D x_n = qA\frac{N_A N_D}{N_A + N_D}W_{dep}$$

$$= A\sqrt{2q\varepsilon_s\left[\frac{N_A N_D}{N_A + N_D}\right](V_o - V)} \quad (2.25)$$

pn Junction – Depletion Capacitance and Diffusion Capacitance

$$q_J = A\sqrt{2q\varepsilon_s\left[\frac{N_A N_D}{N_A + N_D}\right](V_o - V)} \quad (2.25)$$



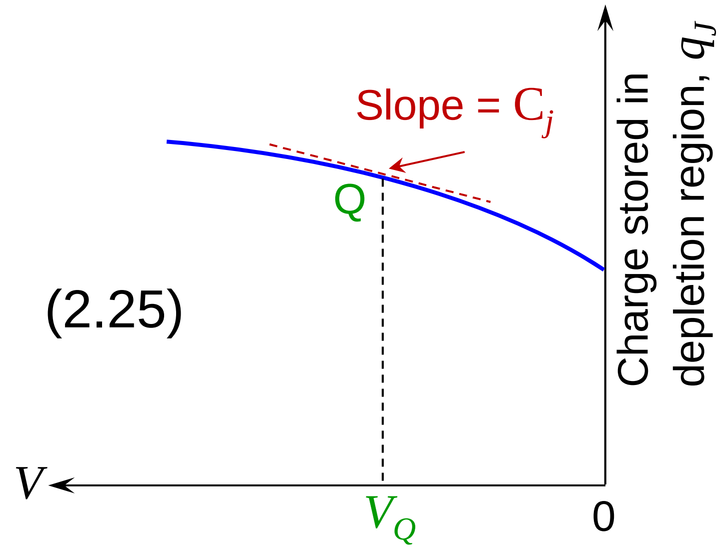
- Equation (2.25) yields an expression for the $q_J - V$ relationship, which is non-linear. This non-linear dependence is shown in the figure for a range of reverse bias. Hence, it does not represent a linear capacitor.

- In mathematics, if the derivative of a function is finite at a given value of the independent variable, such non-linear functions can be treated as linear over a small range around this value using Taylor series.

- In the case of electronic circuits that are used in this module, typically a DC bias voltage V_Q is applied to a pn-junction to meet some specifications and a small signal from the sources mentioned in the introduction produces small changes in this voltage.

pn Junction – Depletion Capacitance and Diffusion Capacitance

$$q_J = A\sqrt{2q\varepsilon_s\left[\frac{N_A N_D}{N_A + N_D}\right]\left(V_o - V\right)} \quad (2.25)$$



- Hence, a linear-capacitance approximation can be used, if the *pn*-junction is biased with a DC bias voltage V_Q and the voltage change due to the signal around the bias point is small, to analyze circuit response to the changes. At the bias point or Q point denoted by Q, the small-signal junction capacitance (or depletion capacitance), C_j , is given by the slope (magnitude) of the $q_J – V$ relationship at Q -

$$C_j = \left|\left.\frac{dq_J}{dV}\right|_{V=V_Q}\right| = \left. A\sqrt{\frac{q\varepsilon_s}{2}\left[\frac{N_A N_D}{N_A + N_D}\right]\frac{1}{\left(V_o - V\right)}}\right|_{V=V_Q} = A\sqrt{\frac{q\varepsilon_s}{2}\left[\frac{N_A N_D}{N_A + N_D}\right]\frac{1}{\left(V_o - V_Q\right)}} \quad (2.26)$$

pn Junction – Depletion Capacitance and Diffusion Capacitance

- Using equation (2.23), equation (2.26) can be simplified to

$$C_j = \frac{\varepsilon_s A}{W_{dep}} \tag{2.27}$$

- Equation (2.27) has a form similar to that for a parallel plate capacitor. However, note that W_{dep} is a function of V, as given by equation (2.23), which is unlike the fixed separation of a parallel plate capacitor.

- The expression for C_j at a given bias voltage V can be re-written as

$$C_j = \frac{AC_{j0}}{\sqrt{1 - \frac{V}{V_o}}} \tag{2.28}$$

- C_{j0} is the value of C_j per unit area at $V = 0$:

$$C_{j0} = \sqrt{\frac{q\varepsilon_s}{2}\left[\frac{N_A N_D}{N_A + N_D}\right]\frac{1}{V_o}} \tag{2.29}$$

- This makes it easier to find C_j in a circuit where the area and voltage of a pn-junction are determined by the designer and designed circuit.

pn Junction – Depletion Capacitance and Diffusion Capacitance

- A more general expression for C_j is

$$C_j = \frac{AC_{j0}}{\left[1 - \frac{V}{V_o}\right]^m} \qquad (2.30)$$

- where m is called the grading coefficient and has value ranges from 1/2 to 1/3, depending on the manner in which the doping concentration changes from the *p* to the *n* side of the junction.

- The expression for C_{j0} is also changed to

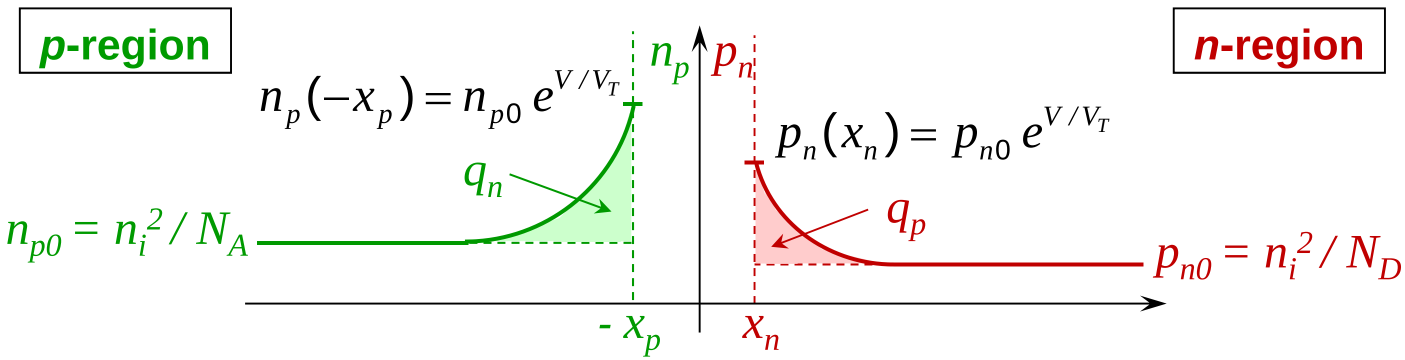
$$C_{j0} = \left[\frac{q\varepsilon_s}{2}\left[\frac{N_A N_D}{N_A + N_D}\right]\frac{1}{V_o}\right]^m \qquad (2.31)$$

- Accuracy of equation (2.26)/(2.28)/(2.30) is good under reverse bias with $V < 0$. The accuracy is rather poor under forward bias with $V > 0$. In fact, C_j becomes infinitely large when V approaches V_o, which is physically incorrect. As an alternative, the following approximation is used in circuit design –

$$C_j \cong 2AC_{j0} \text{ (for } V \text{ approaches } V_o\text{)}$$

pn Junction – Depletion Capacitance and Diffusion Capacitance

- In addition to junction (depletion) capacitance, C_j, another capacitive effect exists.



- The excess-minority carrier charge in the neutral *p*-region and neutral *n*-region varies with terminal voltage V.

- The change with respect to V of the excess-minority carrier charge stored in the neutral *p*-region (q_n) and the neutral *p*-region (q_p) means another capacitance effect exists and this gives rise to the diffusion capacitance, C_d.

- C_d increases with increasing forward bias V and is dominant in forward bias, while C_j is dominant in reverse bias.

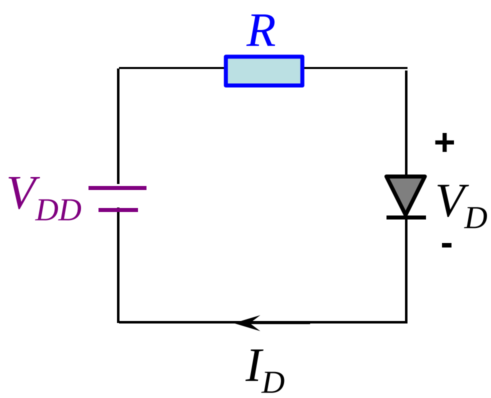
***pn* Junction**

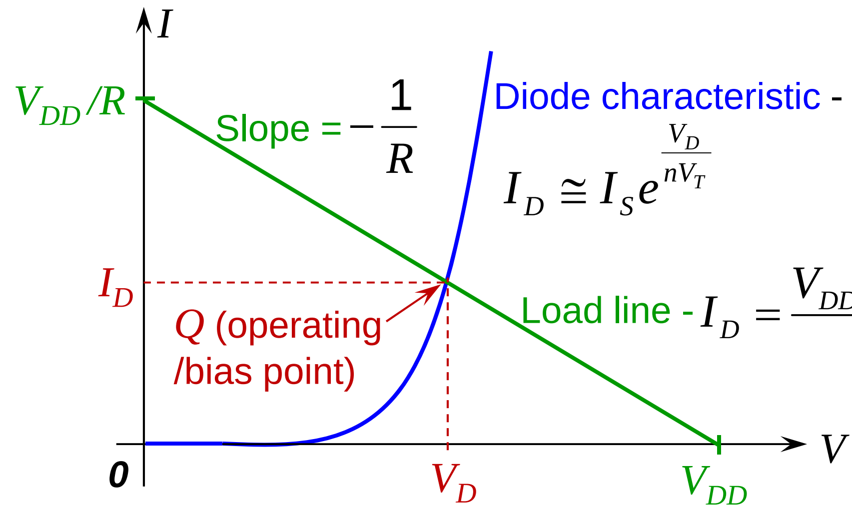
1. Introduction
2. Open-Circuit Conditions
3. Reverse-Bias Conditions
4. Breakdown Region
5. Forward-Bias Conditions
6. Terminal Current-Voltage Characteristics
7. Depletion Capacitance and Diffusion Capacitance
8. Modeling the Diode
9. The *pn* Junction Circuit(s): Rectifier

Reference

- A.D. Sedra & K.C. Smith, “Microelectronic Circuits – Theory and Application”, 5th Edition (International Version), Oxford University Press, Sections 2.1.1 & 2.3.

pn Junction – Modeling the Diode





- Consider the analysis of the above simple circuit shown, which uses a forward biased diode. Assuming V_{DD} > 0.5 V, the IV characteristic of the diode is

$$I_D = I_S(e^{\frac{V_D}{nV_T}} - 1) \cong I_S e^{\frac{V_D}{nV_T}} \qquad (2.38)$$

- I_D and V_D are also governed by the Kirchhoff voltage law –

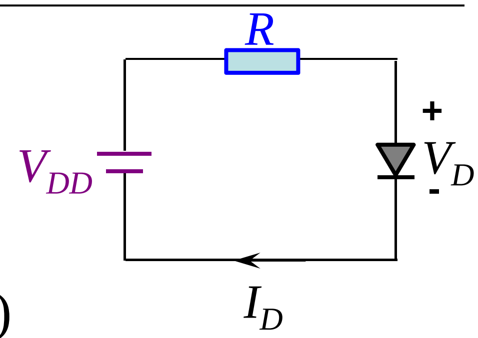
$$I_D = \frac{V_{DD} - V_D}{R} \qquad (2.39)$$

- Equation (2.39) is known as the load line of the circuit. I_D and V_D can be determined by the intersection of equations (2.38) and (2.39) graphically. They can also be solved using a simple iterative procedure.

pn Junction – Modeling the Diode

Exercise

Determine the current I_D and voltage V_D of the circuit shown below by means of iteration for V_{DD} = 5 V and R = 1 kΩ. It is given that the diode has a current of 1 mA at a voltage of 0.6 V and that its voltage drop changes by 0.1 V for every decade change in current.



- I_D and V_D are governed by equations (2.38) and (2.39).
- We should find nV_T in order to use (2.38) for iteration.

$$I_D = I_S(e^{\frac{V_D}{nV_T}} - 1) \cong I_S e^{\frac{V_D}{nV_T}} \Rightarrow V_D = nV_T \ln(I_D / I_S)$$

$$0.6V = nV_T \ln(1\text{mA} / I_S)$$

$$\Rightarrow V_D - 0.6V = nV_T \ln(I_D / I_S) - nV_T \ln(1\text{mA} / I_S) = nV_T \ln(I_D / 1mA)$$

- Given that V_D changes by 0.1 V for every decade change in I_D, i.e., for (V_D – 0.6V)= 0.1 V, I_D/ 1mA = 10, leading to

$$0.1 = nV_T \ln(10) \Rightarrow nV_T = 0.043\text{V}$$

pn Junction – Modeling the Diode

- To begin the iteration, initially, we assume V_{D0} = 0.7 V in the middle of the range on slide pn-2.23 and using equation (2.39), we make an estimate for I_D –

$$I_{D0} = \frac{V_{DD} - V_{D0}}{R} = \frac{5 - 0.7}{1000} = 4.3\,\text{mA}$$

- Using the estimated I_{D0} = 4.3 mA, we obtain a better estimate for V_D(=V_{D1})

$$V_D - 0.6V = nV_T \ln(I_D / 1mA) \Rightarrow V_{D1} - 0.6V = 0.043 \ln(4.3\text{mA} / 1mA)$$
$$\Rightarrow V_{D1} = 0.6627V$$

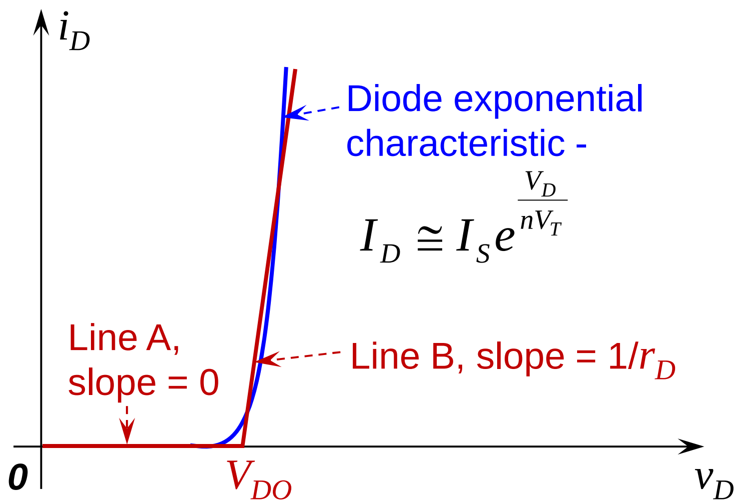
$$I_{D1} = \frac{V_{DD} - V_{D1}}{R} = \frac{5 - 0.6627}{1000} = 4.3373\text{mA}$$

- Thus, after the 1st iteration I_{D1} = 4.3373 mA and V_{D1} = 0.6627 V. The 2nd iteration proceeds in a similar manner:

$$V_{D2} - 0.6 = 0.043 \ln\left(\frac{4.3373}{1}\right) \Rightarrow V_{D2} = 0.6631\text{V}$$

2nd iteration yields I_{D2} = 4.3369 mA and V_{D2} = 0.6631 V, which are close to values obtained after the 1st iteration, hence further iterations are not necessary.

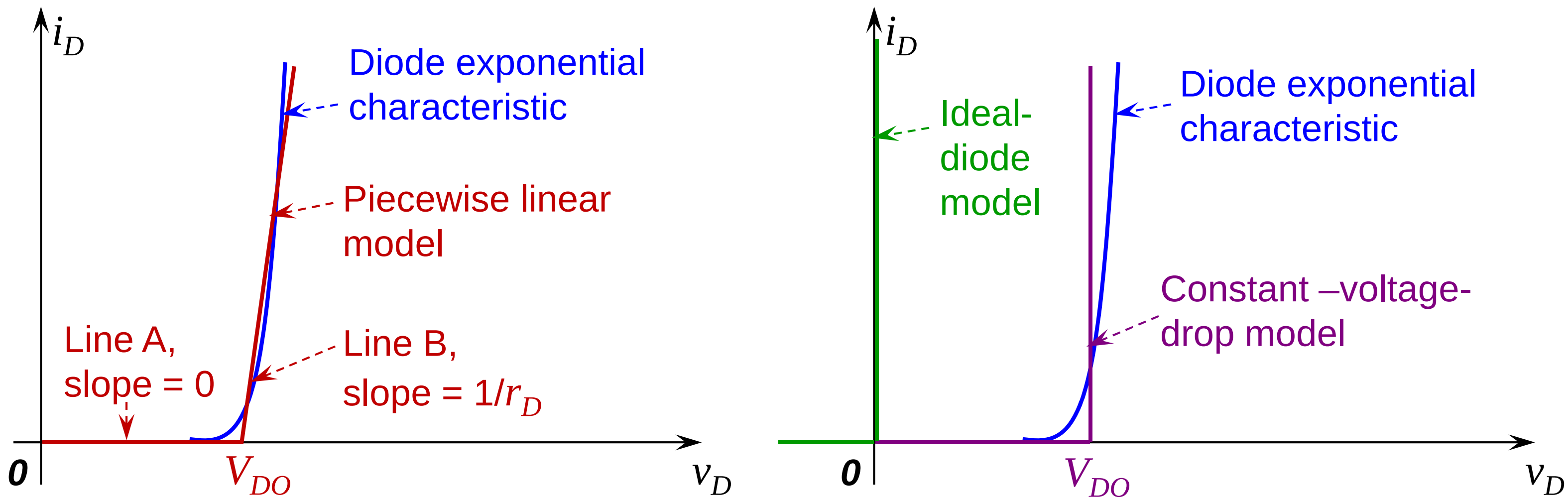
pn Junction – Modeling the Diode



Why the need to model diode?

- For more complex circuits, the analysis by means of the graphical method may not be possible and the iterative method may be too tedious owing to the exponential IV characteristic of diode.
- To speed up circuit analysis, simpler model for the diode is used. This is at the expense of precise results.
- The forward bias diode exponential characteristic can be approximated by two straight lines, line A with zero slope and line B with a slope $1/r_D$. This approximation is known as the piecewise-linear model.

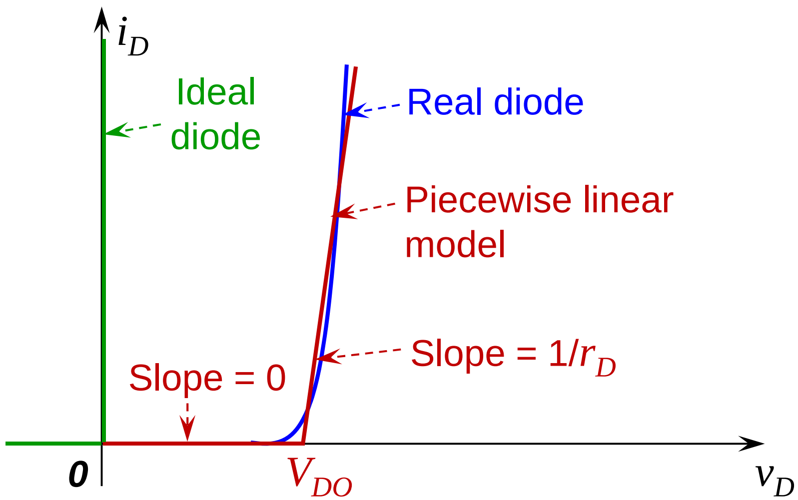
pn Junction – Modeling the Diode

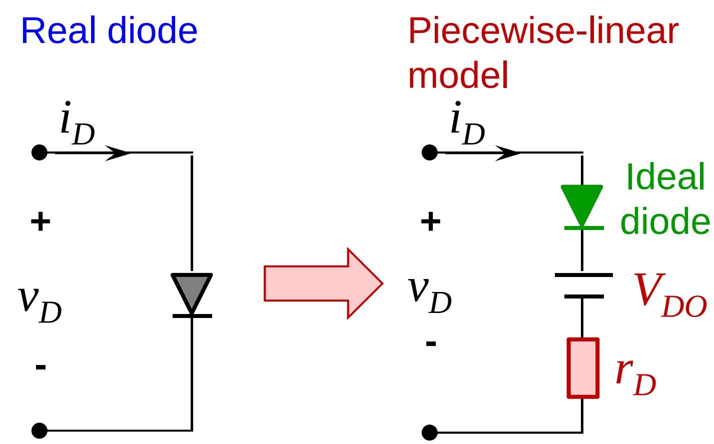


<u>The large signal model</u>

- The piecewise-linear model -
  - $i_D = 0, \qquad v_D \le V_{DO} \qquad (2.40)$
  - $i_D = (v_D - V_{DO})/r_D, \qquad v_D \ge V_{DO} \qquad (2.41)$
  - Choice of lines A and B is not unique.
  - Closer approximation obtained by restricting the operation range.
- The ideal-diode model: $V_{DO} = 0$ and $r_D = 0$.
- The constant-voltage-drop model: $r_D = 0$ and V_{DO} is usually taken as 0.7 V.

pn Junction – Modeling the Diode



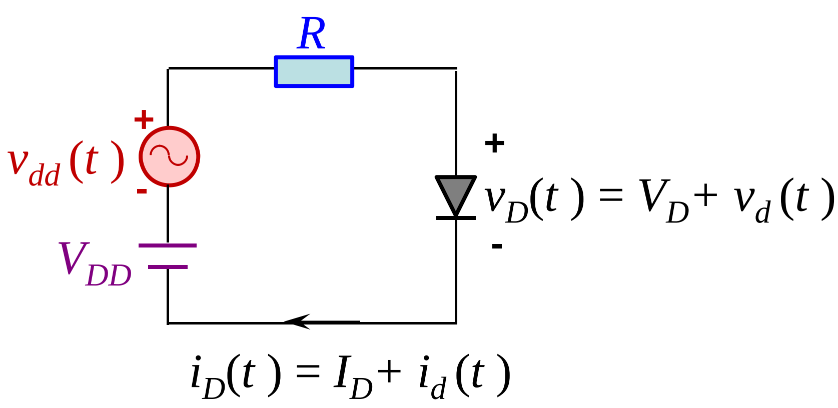


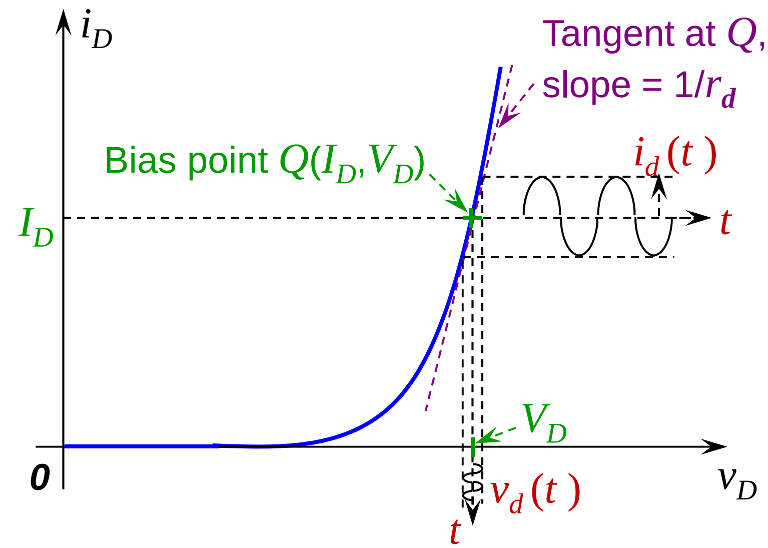
<u>The large signal model</u>

- In the equivalent circuit of the piecewise-linear model of diode, an ideal diode is included to restrict i_D flow in forward bias direction only.

- Symbols for diode current and voltage have been replaced by i_D and v_D. They represent the 'total' current and voltage of a diode and will be elaborated in subsequent slides.

pn Junction – Modeling the Diode

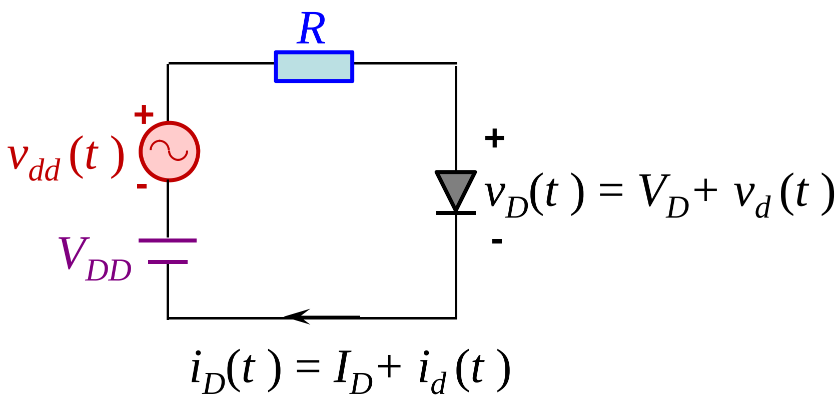


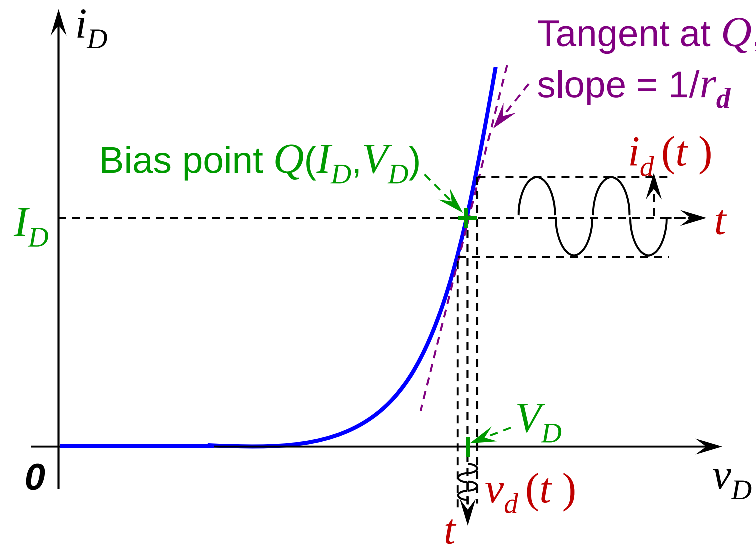


<u>The small-signal model</u>

- For applications where the diode is biased to operate at a point on the forward IV characteristic, $Q(I_D,V_D)$, and a small ac signal, $v_{dd}(t)$, is superimposed on the dc quantities, the small-signal model of diode is needed.
  - The dc bias point $Q(I_D,V_D)$ can first be determined using the piecewise-linear model.
  - To analyze the small-signal operation around $Q(I_D,V_D)$, the diode is modeled by a resistance equal to the inverse of the slope of the tangent to the exponential IV characteristic at the bias point, r_d .

pn Junction – Modeling the Diode





<u>The small-signal model</u>

- Without the small ac signal $v_{dd}(t)$, the diode voltage is V_D and its current I_D is

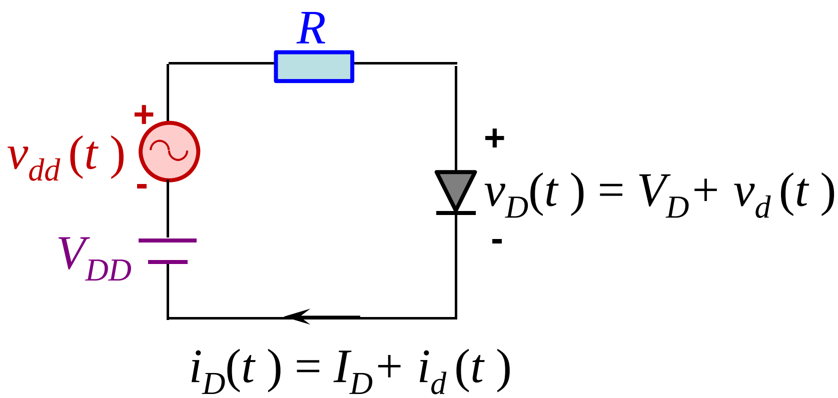
$$I_D = I_S e^{\frac{V_D}{nV_T}} \tag{2.42}$$

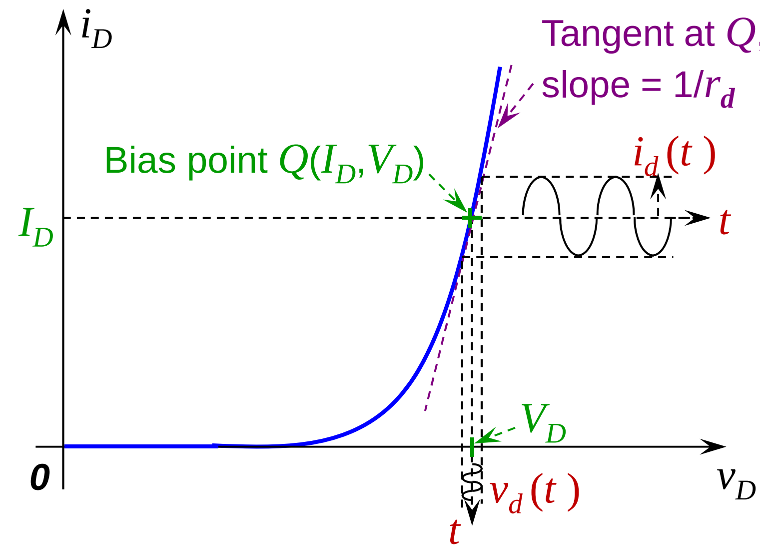
- With $v_{dd}(t)$ applied, the total instantaneous diode voltage and current, $v_D(t)$ and $i_D(t)$, are given below and plotted as shown above.

$$v_D(t) = V_D + v_d(t) \tag{2.43}$$

$$i_D(t) = I_S e^{\frac{v_D(t)}{nV_T}} = I_S e^{\frac{V_D + v_d(t)}{nV_T}} = I_S e^{\frac{V_D}{nV_T}} e^{\frac{v_d(t)}{nV_T}} = I_D e^{\frac{v_d(t)}{nV_T}} \tag{2.44}$$

pn Junction – Modeling the Diode





<u>The small-signal model</u>

- $v_d(t)$ is the diode small signal voltage and for $v_d(t) << nV_T$,

$$i_D(t) = I_D e^{\frac{v_d(t)}{nV_T}} \cong I_D[1 + \frac{v_d(t)}{nV_T}] \qquad (2.45)$$

- Since the total instantaneous diode current $i_D(t)$ is also given by

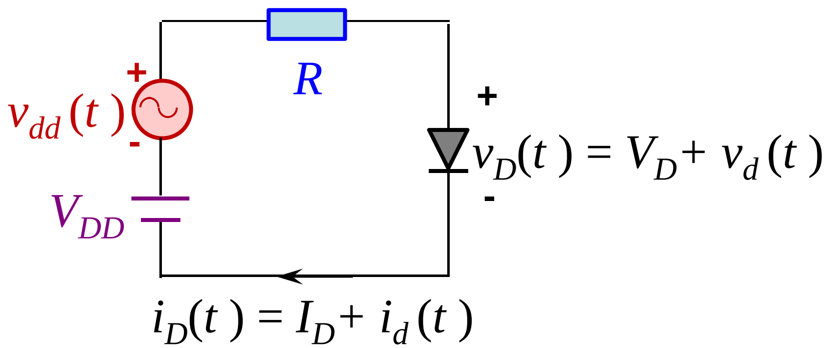
$$i_D(t) \cong I_D + i_d(t) \qquad (2.46)$$

where $i_d(t)$ is the diode small signal current. Hence,

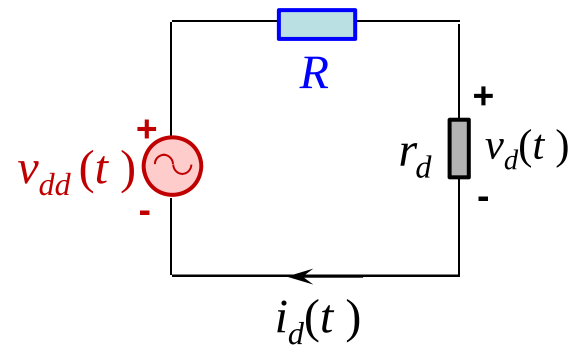
$$i_d(t) \cong \frac{I_D}{nV_T} v_d(t) = \frac{1}{r_d} v_d(t) \qquad (2.47)$$

pn Junction – Modeling the Diode

Actual circuit



Small signal equivalent circuit



<u>The small-signal model</u>

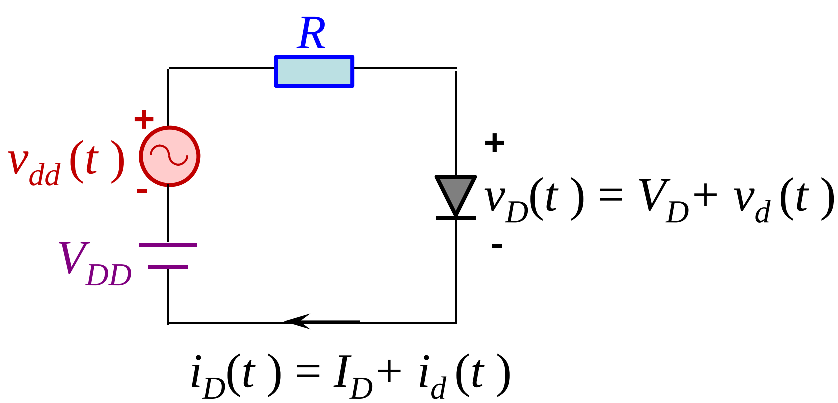
$$i_d(t) \cong \frac{I_D}{nV_T} v_d(t) = \frac{1}{r_d} v_d(t) \qquad (2.47)$$

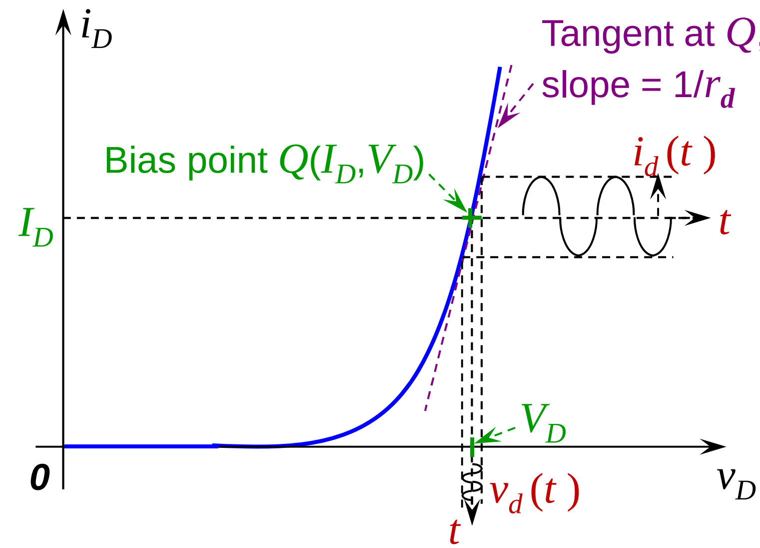
- Diode small signal current $i_d(t)$ is directly related to the small signal voltage $v_d(t)$ via r_d, which has the dimension of resistance and is called the diode small signal resistance

$$r_d = \frac{nV_T}{I_D} \qquad (2.48)$$

- For small signal analysis (around a dc bias point), there is no need for detailed calculation with time. The diode can actually be replaced by a resistance, r_d and the dc (large signal) source, V_{DD}, is replaced by a short circuit (known as ac short). The bias point and model data are needed to find r_d.

pn Junction – Modeling the Diode





The small-signal model

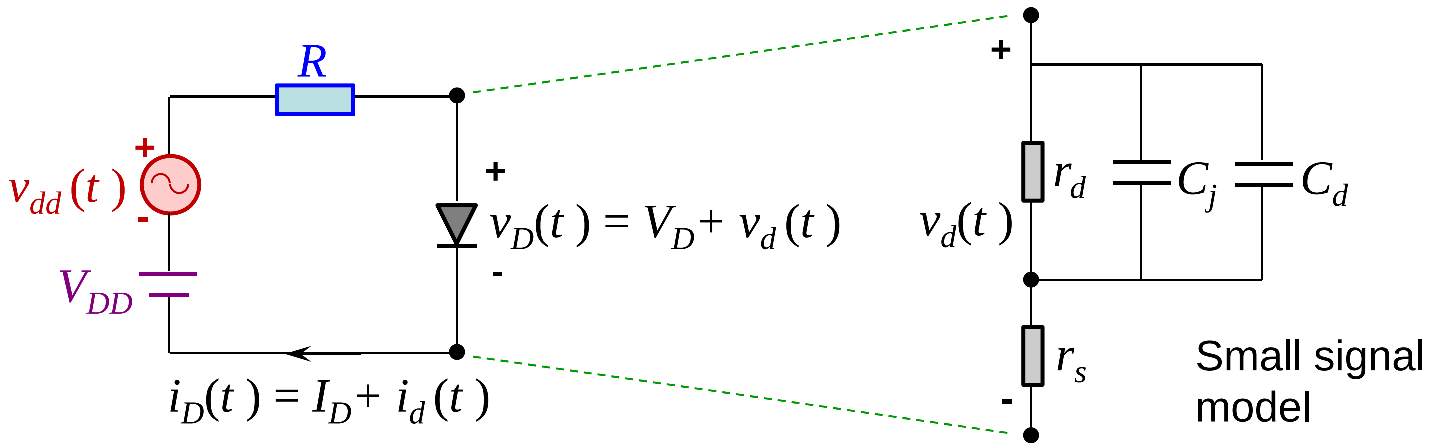
- It has been seen that the small signal analysis can be performed separately from the dc bias analysis.

- Note that r_d is given by the inverse of the slope of the diode exponential IV characteristic at $Q(I_D,V_D)$ -

$$\left.\frac{dI}{dV}\right|_{V=V_D} = \frac{I_D}{nV_T} = \frac{1}{r_d} \qquad (2.49)$$

- r_d is also known as the diode incremental resistance.

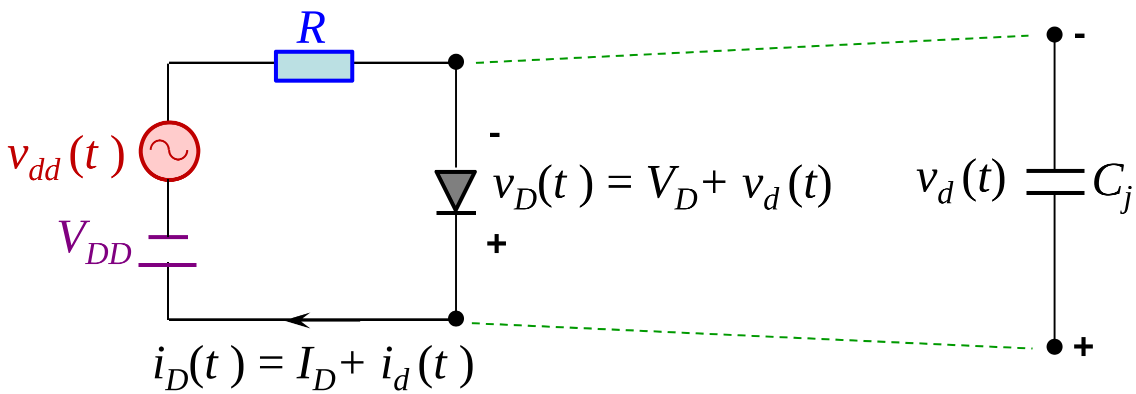
pn Junction – Modeling the Diode



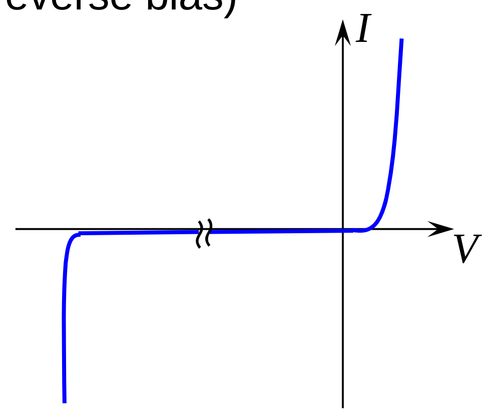
The small-signal model (inclusive of capacitance and series resistance effects)

- We can now construct a more comprehensive small-signal equivalent circuit of a biased *pn* junction. The circuit consists of:
  - The junction incremental (small signal) resistance, r_d
  - The depletion (junction) capacitance C_j, which is in parallel with r_d
  - The diffusion capacitance C_d, which is in parallel with r_d and C_j. Under forward bias, $C_d >> C_j$ and under reverse bias, $C_j >> C_d$.
  - The series resistance r_s from the neutral *p*-region and *n*-region

pn Junction – Modeling the Diode



Small signal model (reverse bias)



<u>The small-signal model (reverse bias)</u>

- The incremental resistance, $r_d \to \infty$, an open-circuit as reverse current is a constant
- The depletion (junction) capacitance C_j remains
- The diffusion capacitance C_d is much smaller than C_j
- The series resistance $r_s \to 0$, a short circuit, as the reverse current is very small and hence its effect is minimal

***pn* Junction**

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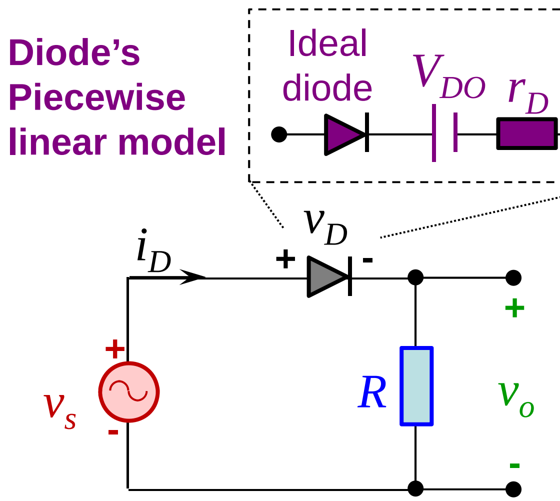
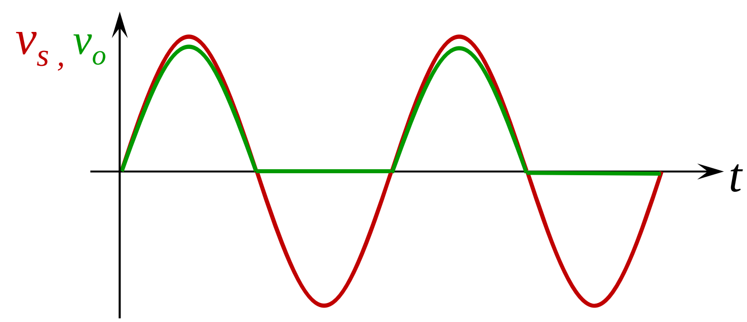
Reference

- A.D. Sedra & K.C. Smith, “Microelectronic Circuits – Theory and Application”, 5th Edition (International Version), Oxford University Press, Sections 2.1.2 & 2.5.

pn Junction – The *pn* Junction Circuit(s): Rectifier





Rectifying application of diode

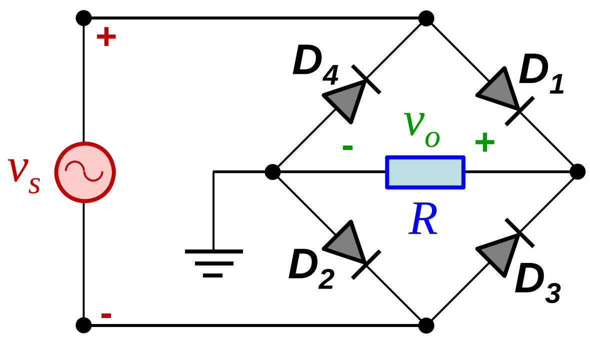
- During the positive half-cycles of v_s, current flows through the diode in the forward direction, hence $v_o \cong v_s - V_{DO}$ (>> $i_D r_D$)where AC source amplitude is v_s.

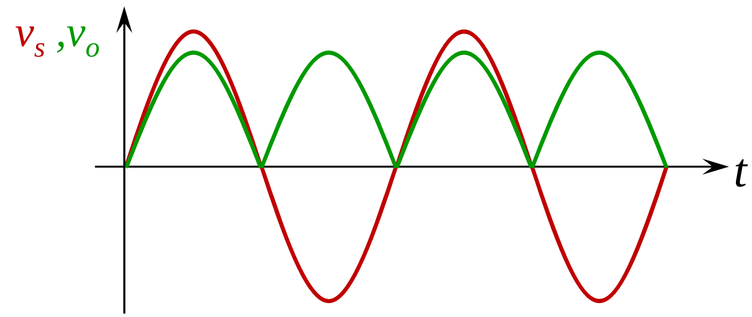
- During the negative half-cycles of v_s, the diode will not conduct, thus $v_o = 0$.

- Although v_s alternates in polarity and has a zero average value, v_o is unipolar /unidirectional and has a finite average value or a dc component.

- Above circuit is known as a half-wave rectifier as it utilizes alternate half-cycles of input sinusoidal AC source v_s.

pn Junction – The *pn* Junction Circuit(s): Rectifier





<u>Full-wave bridge rectifier</u>

- Full-wave rectifier utilizes both positive and negative half-cycles of input signal.
- Four diodes connected in Wheatstone bridge configuration is used.
- During the positive half-cycles of v_s, current conducts through diode D_1, load resistor R and diode D_2. In the meantime, D_3 and D_4 are reverse biased.
- During the negative half-cycles of v_s, current conducts through diode D_3, load resistor R and diode D_4, while diode D_1 and D_2 are reverse biased.
- Note that - $v_o \cong v_s - 2 \times V_{DO}$.