MOSFET

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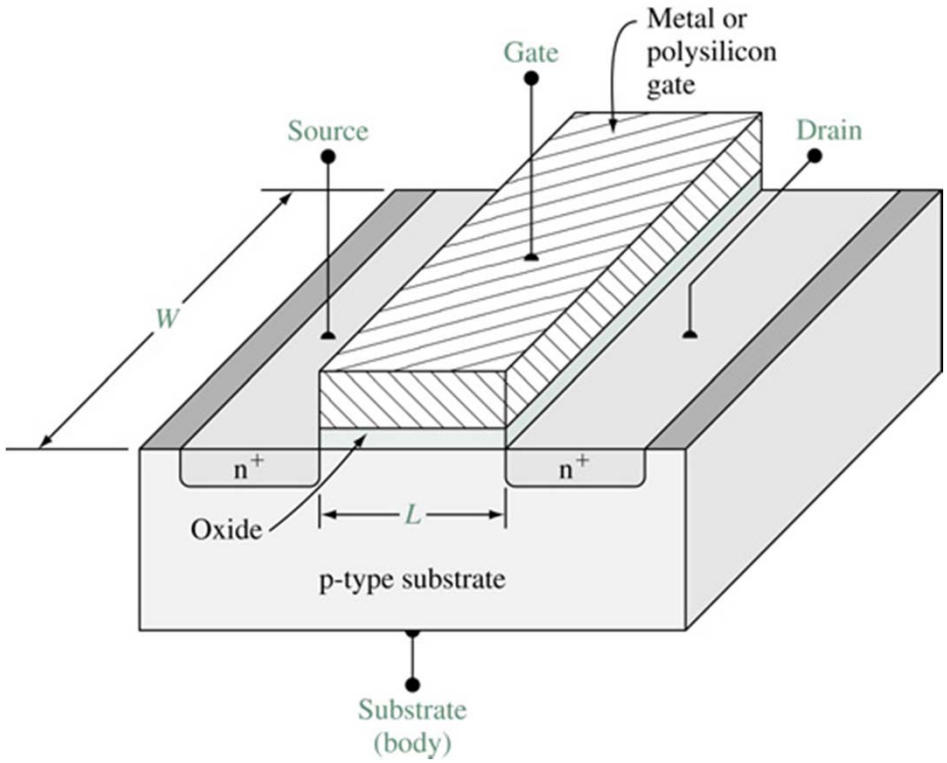
Reading

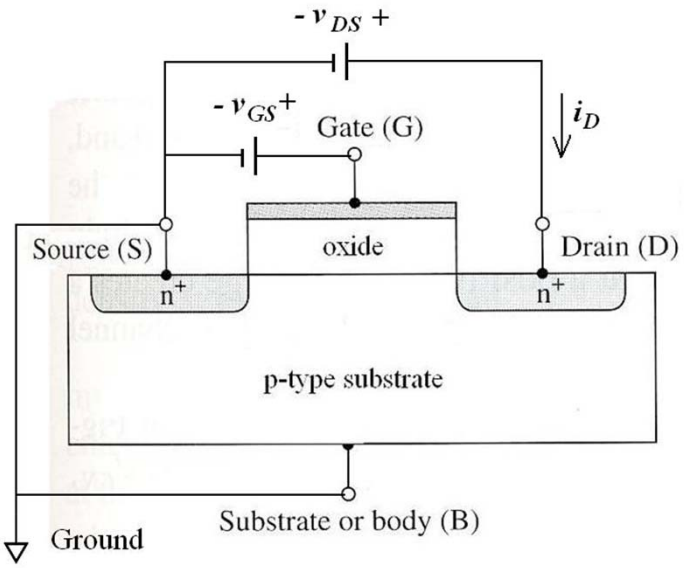
- Sedra and Smith, Microelectronic Circuits, Theory and Applications, Fifth Edition (International Version), Oxford (2004), pp. 325 – 349.

1. Concept of the MOSFET

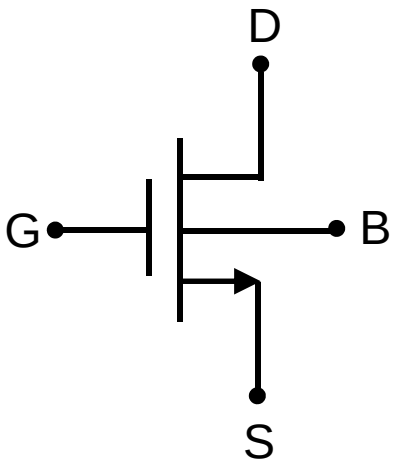


Basic structure of an n-channel MOSFET.

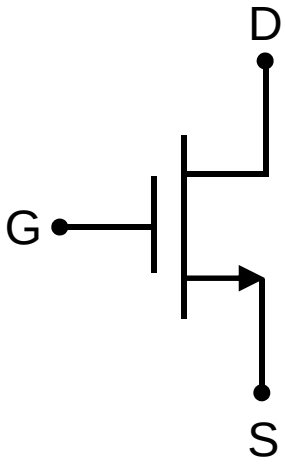
- We consider an n-channel MOSFET first as an example.
- In an n-channel MOSFET, the substrate is p-type, while heavily doped n-type regions form the “source” and “drain” regions.
- The electrode on top of the thin oxide (dielectric) layer is called the “gate”.
- The source terminal is the source of the carriers that will flow through the channel to the drain terminal.
- In this n-channel device, electrons flow from the source to the drain.
- Conventional current therefore enters from the drain terminal and flows out of the source terminal.
- Note that usually there is also a contact to the “substrate” or “body” of the MOSFET, and it is usually grounded.



Schematic cross-sectional view of an n-channel MOSFET.



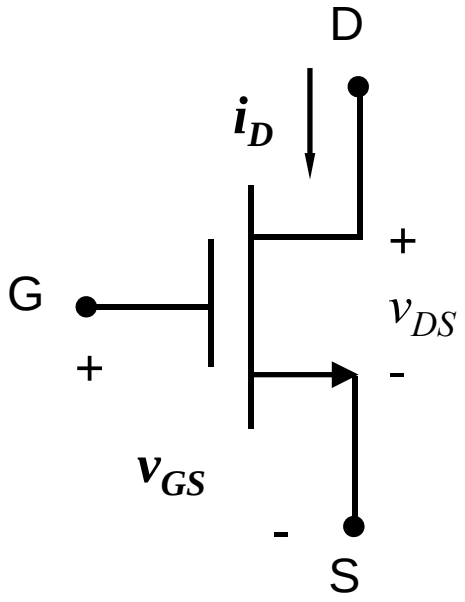
Circuit symbol of an n-channel MOSFET

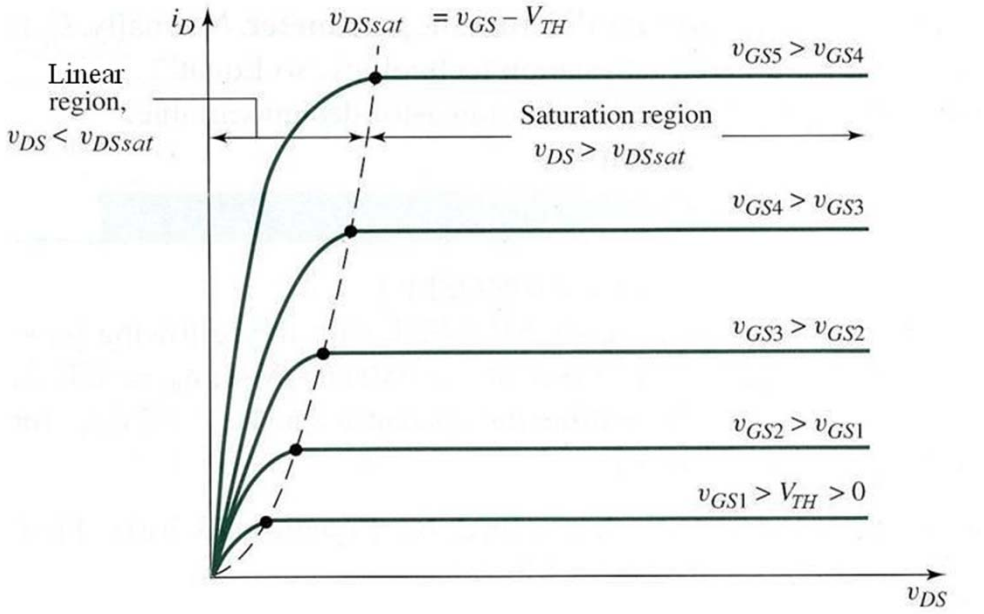


Simplified symbol of the n-channel MOSFET when the substrate is connected to ground.

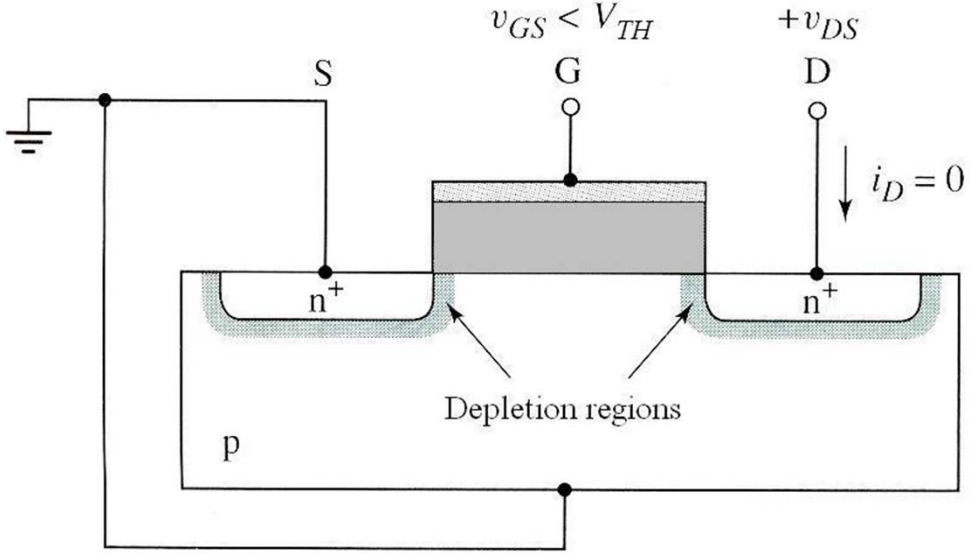
- In the above MOSFET, two p-n junctions exist in series between the drain and the source. One junction is between the n^+ drain region and the p-type substrate, the other is between the n^+ source region and the p-type substrate.

- The relationship between the drain i_D, the drain-source voltage v_{DS} and the gate-source voltage v_{GS} of an n-channel MOSFET is shown in the plot below.
- The regions on the MOSFET characteristics corresponding to the linear and saturation modes of operation are as indicated in the plot below.



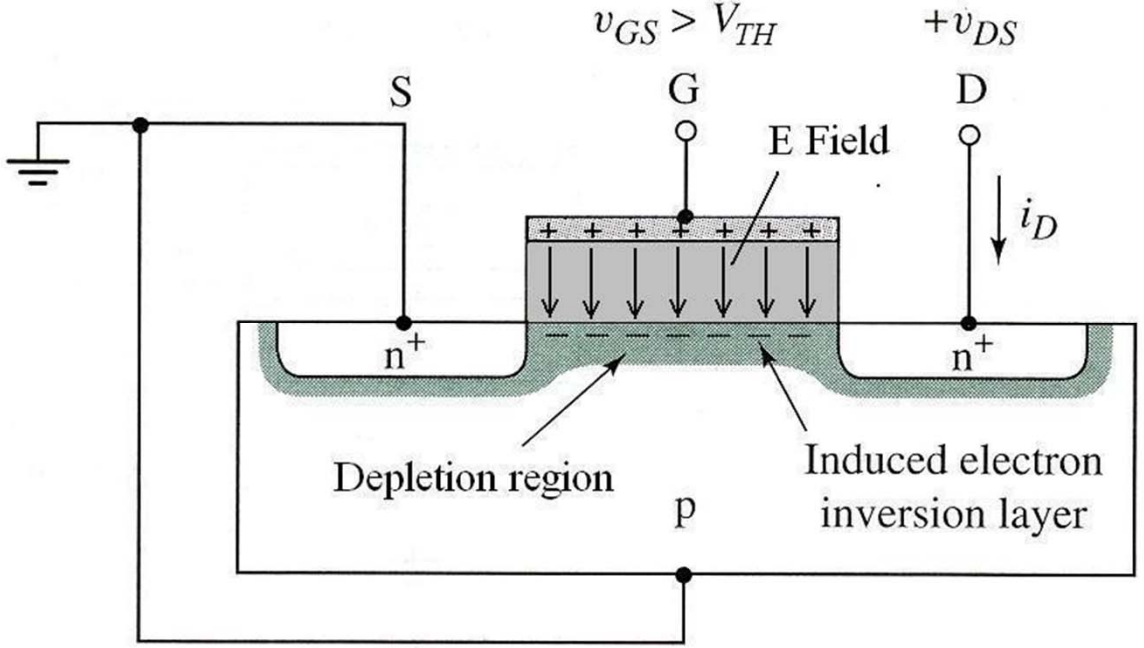


Note : Do not confuse the saturation region of operation of the MOSFET with that of the BJT. See Appendix



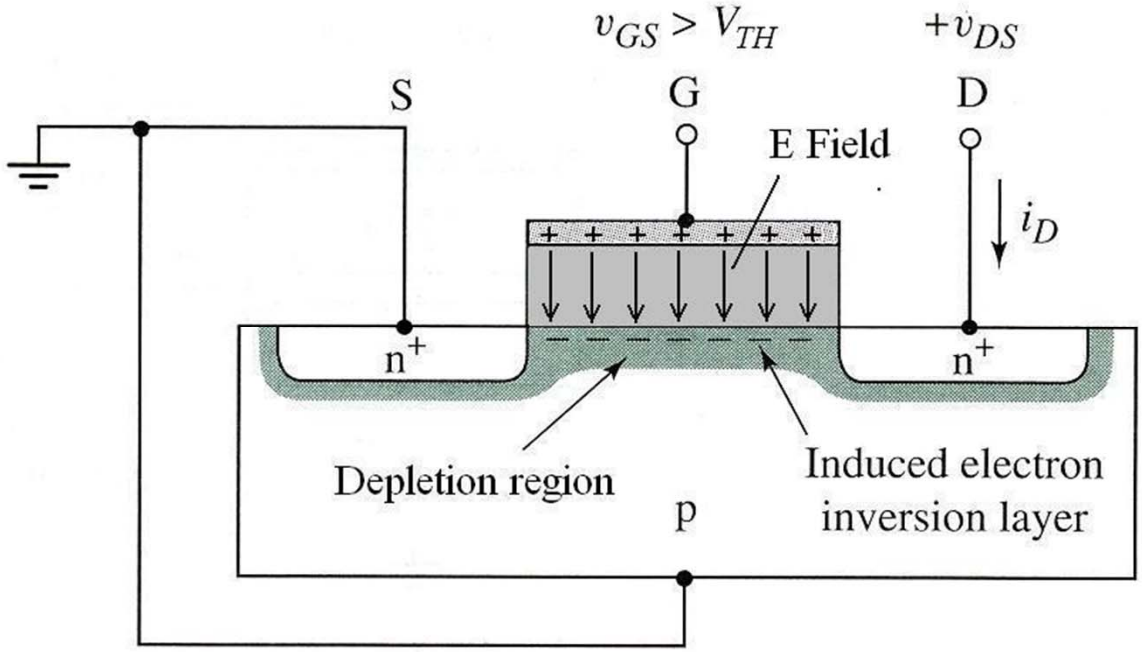
Note : The source is connected to the substrate or "body" of the device, and both are grounded, i.e., set at the reference potential. Unless otherwise stated, this configuration will be assumed in all the subsequent slides.

- Assume that a *positive* voltage v_{DS} is applied to the drain terminal. Assume also that a *positive* voltage v_{GS}, where v_{GS} is less than a certain voltage V_{TH}, is applied to the gate terminal.
- The positive voltage at the gate initially causes holes to be repelled from the region of the substrate under the gate (known as the channel region), thus producing a depletion region there which consists of ionised acceptors.
- This depletion region prevents electrons from flowing from the source to the drain. The drain current $i_D = 0$, even though a voltage is applied between the drain and the source.

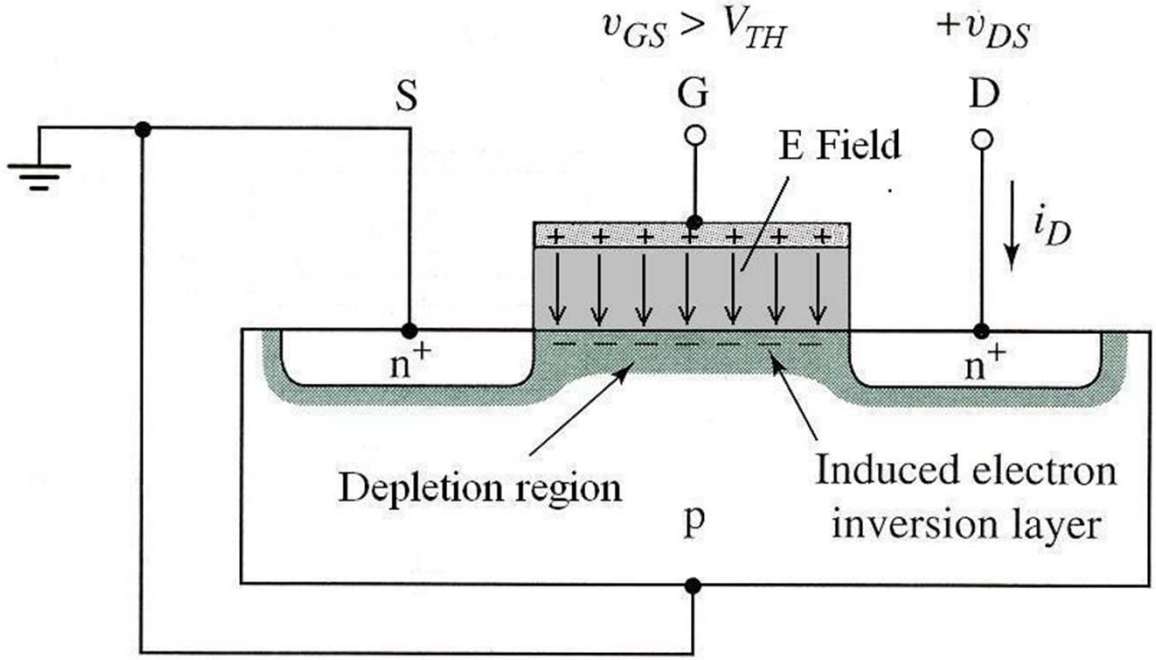


- As the gate voltage v_{GS} increases, it attracts electrons which flow from the drain and source regions into the channel region under the gate. With increasing v_{GS}, more and more electrons flow into the channel region.
- When v_{GS} has increased to a value such that the concentration of the electrons in the channel is equal to the concentration of holes in the p-type substrate, an “inversion” layer is said to be formed in the channel region. This is because the originally p-type region under the gate has in effect become n-type, i.e., “inverted”.
- The gate voltage v_{GS} at which inversion occurs is called the threshold voltage, V_{TH}^*.

*Note : The threshold voltage can be controlled in the design of the MOSFET through adjusting the oxide thickness, substratel doping, and the type of metal used for the gate, among other things.

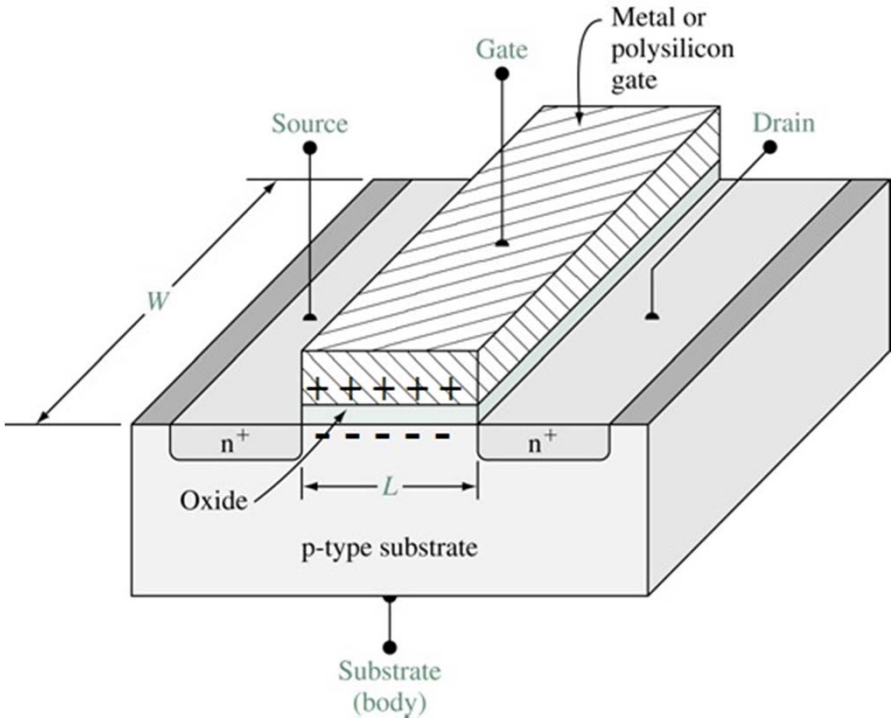


- The n-type source and drain regions are now connected through the n-type inversion layer, and a current can flow between the drain and the source if a bias (v_{DS}) is applied between the drain and the source.
- The device is called an n-channel MOSFET, or NMOS transistor. Note that an n-channel MOSFET is formed on a p-type substrate.
- The gate and the channel region of the MOSFET form a parallel plate capacitor structure, with the oxide layer acting as a dielectric. A vertical electric field exists between the positive charges on the gate and the electrons and ionised acceptors in the channel.



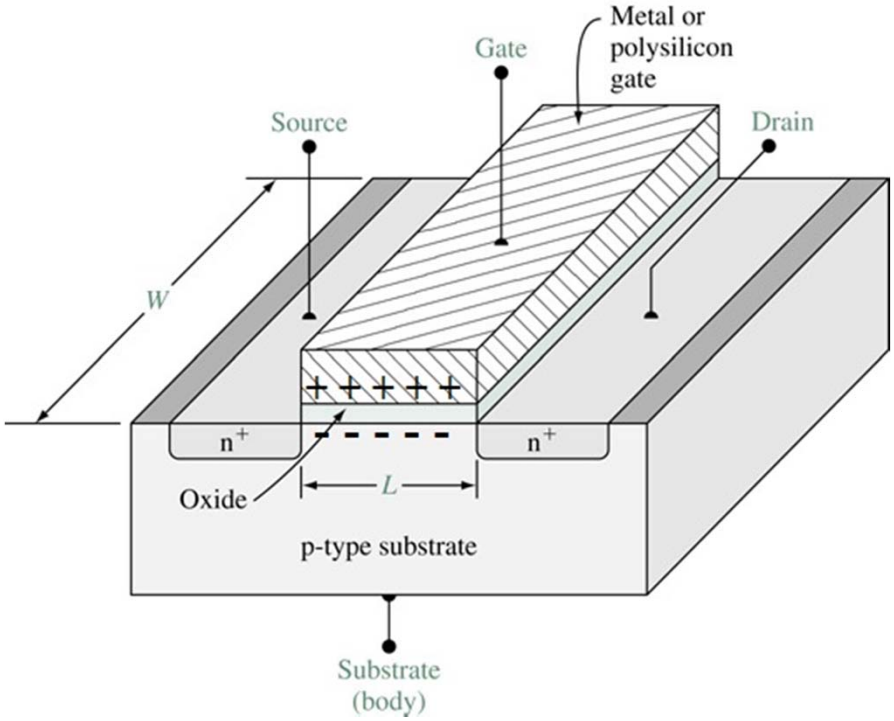
- When v_{GS} is increased to values greater than the threshold voltage V_{TH}, the vertical electric field between the gate and the channel increases. The additional positive charges on the gate induce more electrons in the channel. The channel conductivity increases and so does the drain current i_D, for a given v_{DS}.
- The current that flows between the drain and the source is thus controlled by this electric field, hence the name *Field Effect Transistor*.

2. i_D-v_{DS} Relationship of the MOSFET



We use an n-channel MOSFET as the example in the derivation. The assumptions are :

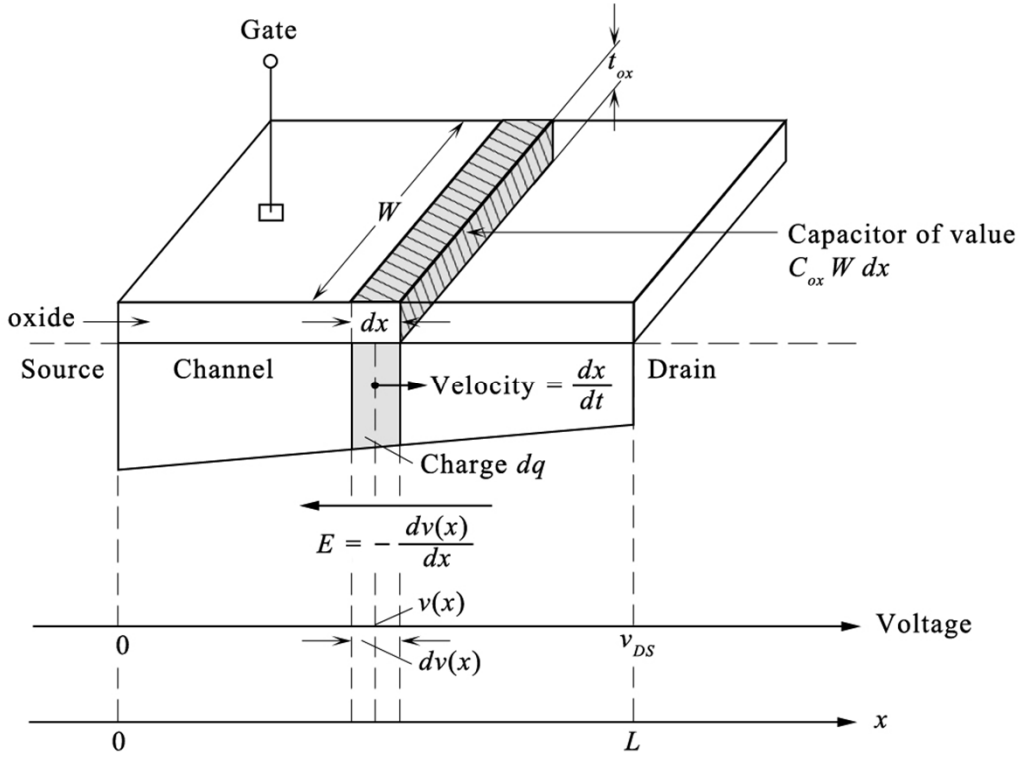
1. The current in the channel is due to drift and not diffusion.
2. There is no current flowing through the oxide
3. The carrier mobility in the channel is constant.



- The gate, oxide and channel of the MOSFET form a parallel plate capacitor.
- The capacitance per unit area, C_{ox}, is given by

$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}} \tag{4.1}$$

where t_{ox} is the thickness of the oxide, ε_{ox} is the permittivity of the oxide, and $\varepsilon_{ox} = \varepsilon_{r,ox} \times \varepsilon_0 = 3.9 \times 8.854 \times 10^{-14} = 3.45 \times 10^{-13}$ F cm^{-1}, for silicon dioxide.



- Consider a small strip of the channel of length dx, at a distance x from the source.
- Recall that, for an inversion layer to form, the gate voltage v_{GS} must be at least equal to the threshold voltage V_{TH}.
- Using the relation that, for a parallel plate capacitor,
  charge (on one plate) = capacitance x effective voltage across the plates,
  the charge in the strip of the channel dx,

$$dq = -C_{ox}\,(Wdx)\left[v_{GS} - v(x) - V_{TH}\right] \qquad (4.2)$$

  where $v(x)$ is the voltage at the point x in the channel, and Wdx is the area of the strip of the capacitor of width dx under consideration.

$$\frac{dq}{dx} = -C_{ox} W \left[v_{GS} - V_{TH} - v(x) \right] \qquad (4.3)$$

- The voltage V_{DS} applied between the drain and the source produces an electric field in the channel, in the $-x$ direction (directed from drain to source) :

$$E = -\frac{dv(x)}{dx} \qquad (4.4)$$

- The electric field $E(x)$ causes the electron charge in the channel to drift through the channel towards the drain, with a drift velocity

$$v_{drift} = \frac{dx}{dt} = -\mu_n E = -\mu_n \times \left(-\frac{dv}{dx} \right) = \mu_n \frac{dv}{dx} \qquad (4.5)$$

where μ_n is the mobility of the electrons in the channel.

- The current that flows in the channel (in the $+x$ direction), is, by definition

$$i = \frac{dq}{dt} = \frac{dq}{dx} \times \frac{dx}{dt} \qquad (4.6)$$

Note : The leading negative sign in eqns (4.2) and (4.3) indicates that the charge "dq" in the channel is negative because they are made up of electrons, for the n-channel MOSFET.

- By substituting for $\frac{dq}{dx}$ using eqn (4.3) and $\frac{dx}{dt}$ using eqn (4.5) into eqn (4.6),

$$i = -\mu_n W C_{ox} \left[v_{GS} - V_{TH} - v(x) \right] \frac{dv}{dx} \tag{4.7}$$

- Note that although the current is evaluated at a particular point x in the channel, it must be constant throughout the channel due to current continuity. Also, the direction of this current, i, is defined to be in the +x direction.

- We are interested in the drain-to-source current (in short, the drain current), i_D, In the figure on slide 11, i_D would be flowing in the –x direction. Hence we have

$$i_D = -i = \mu_n W C_{ox} \left[v_{GS} - V_{TH} - v(x) \right] \frac{dv}{dx} \tag{4.8}$$

or, by re-arranging terms,

$$i_D \, dx = -i = \mu_n W C_{ox} \left[v_{GS} - V_{TH} - v(x) \right] dv \tag{4.9}$$

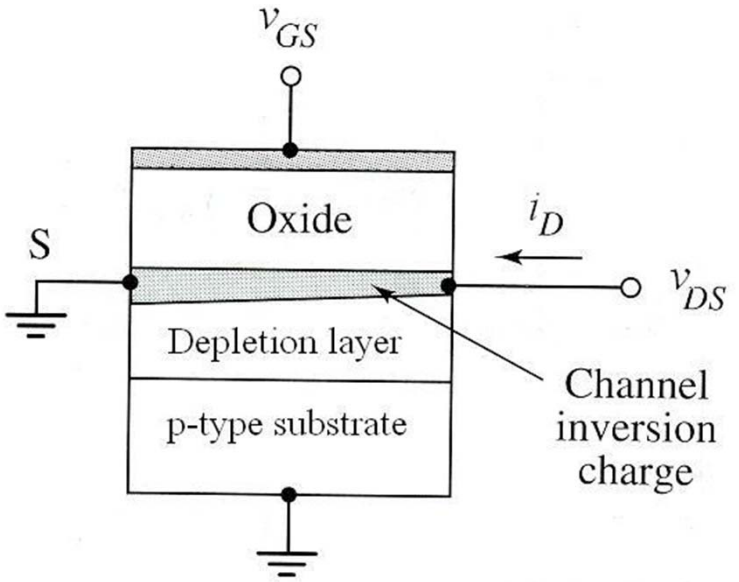
- By integrating both sides of eqn (4.9), from $x = 0$ to $x = L$, and correspondingly, from $v(0) = 0$ to $v(L) = v_{DS}$,

$$i_D \int_0^L dx = \mu_n C_{ox} W \int_0^{v_{DS}} \left[v_{GS} - V_{TH} - v(x) \right] dv \qquad (4.10)$$

we get an expression for the drain current of the MOSFET

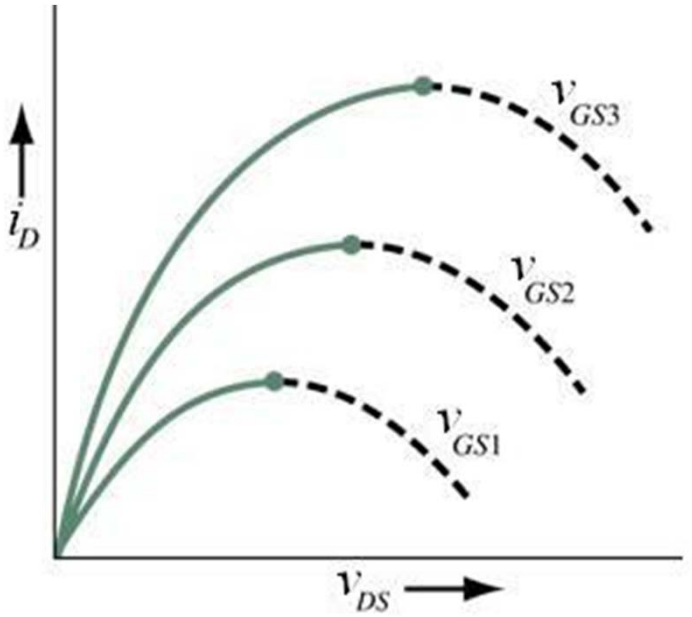
$$i_D = \mu_n C_{ox} \frac{W}{L} \left[\left(v_{GS} - V_{TH} \right) v_{DS} - \frac{1}{2} v_{DS}^2 \right] \qquad (4.11)$$

- Equation (4.11) is valid when the channel extends from the source end to the drain end of the MOSFET, as shown in the figure on the right. Note that the channel at the drain end is narrower because the voltage between the gate and the drain ($v_{GS} - v_{DS}$) is less than that between the gate and the source (v_{GS}), and hence the channel depth at the drain end is less than that at the source end of the channel.

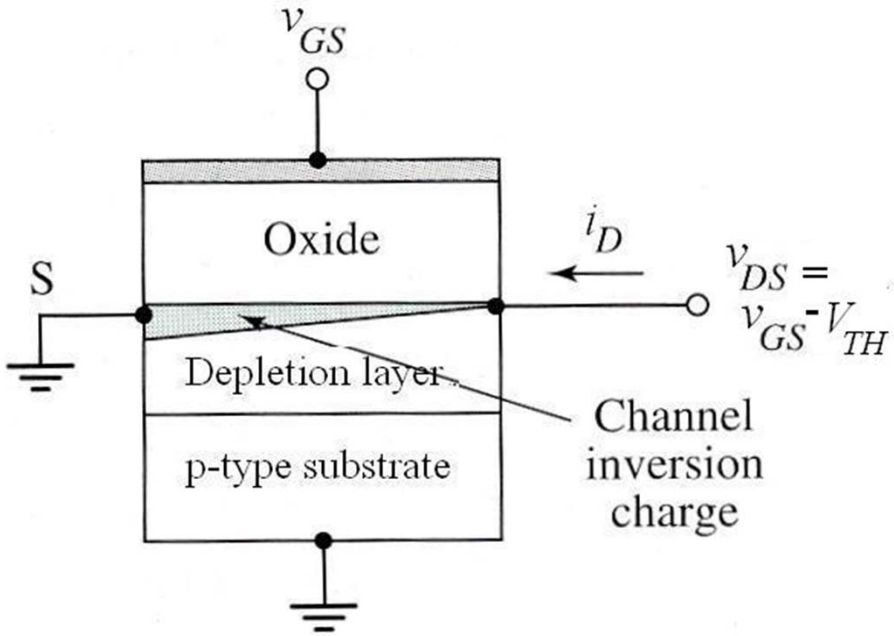


- The $i_D - v_{DS}$ curves based on eqn (4.11) are shown in the figure, for 3 different values of v_{GS}, ➔
- The $i_D - v_{DS}$ curves consist of a series of parabolas having their maxima at $v_{DS} = v_{GS} - V_{TH}$

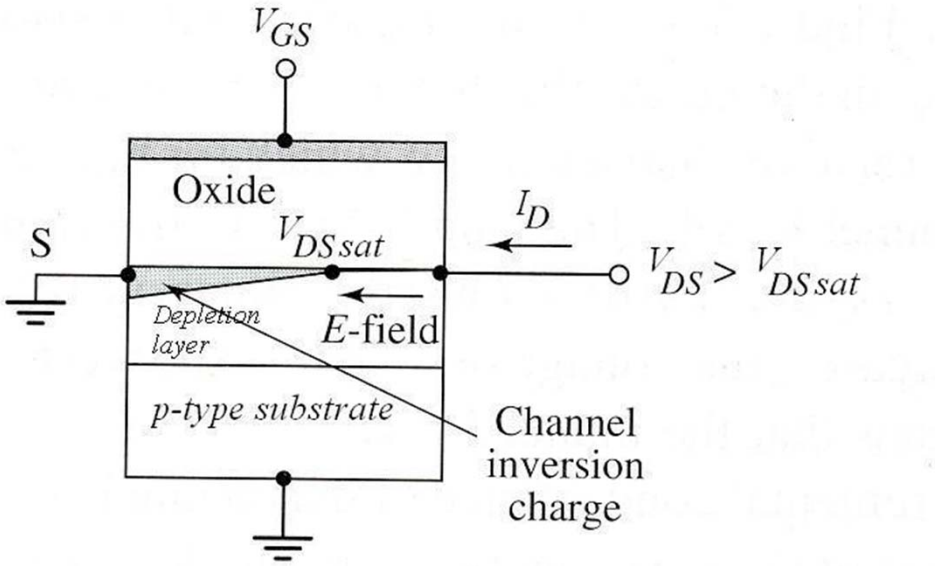
  for the respective values of v_{GS}.



- For $v_{DS} > (v_{GS} - V_{TH})$, i_D decreases with increasing V_{DS} which is physically unreasonable.
- Equation (4.11) is not applicable in this region of the MOSFET operation. The analysis we have carried out, which assumes that the channel extends throughout from the source to the drain, is no longer valid.

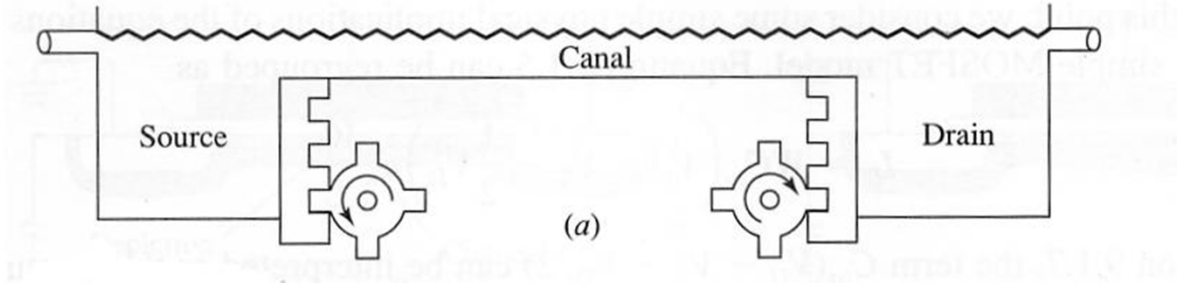


- When $v_{DS} = (v_{GS} - V_{TH})$, the voltage between the gate and the drain end of the channel
  $= v_{GS} - (v_{GS} - V_{TH}) = V_{TH}$.
- Recall that an inversion layer forms under the gate only when $v_{GS} > V_{TH}$.
- Therefore, When $v_{DS} = (v_{GS} - V_{TH})$, the channel depth at the drain end has reduced to zero. The channel is said to be pinched off at the drain end.

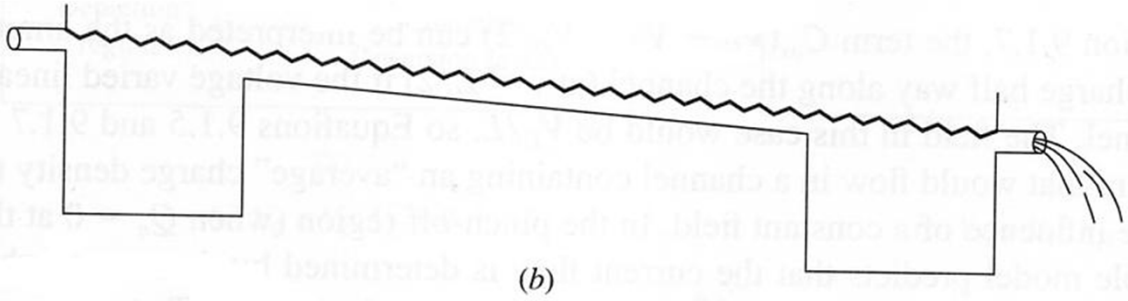


- When $v_{DS} > (v_{GS} - V_{TH})$, the pinch-off point moves towards the source terminal. A high electric field then exists in the depletion layer near the drain end of the device.
- We assume that the MOSFET has a long channel. This means that the shortening of the channel as the pinch-off point moves is insignificant compared to the length of the channel.
- The electrons, after drifting through the channel to the pinch-off point, are then swept by the electric field near the drain into the drain terminal.
- The channel length and channel charge density, for a given v_{GS}, is therefore not changed significantly. The drain current i_D, which is due to the drift of the electrons through the channel, is then approximately, constant when $v_{DS} > (v_{GS} - V_{TH})$.
- The drain current is then said to be saturated, and the voltage $(v_{GS} - V_{TH})$. at which this occurs is called the saturation drain voltage, V_{DSsat}, where $V_{DSsat} = (v_{GS} - V_{TH})$.

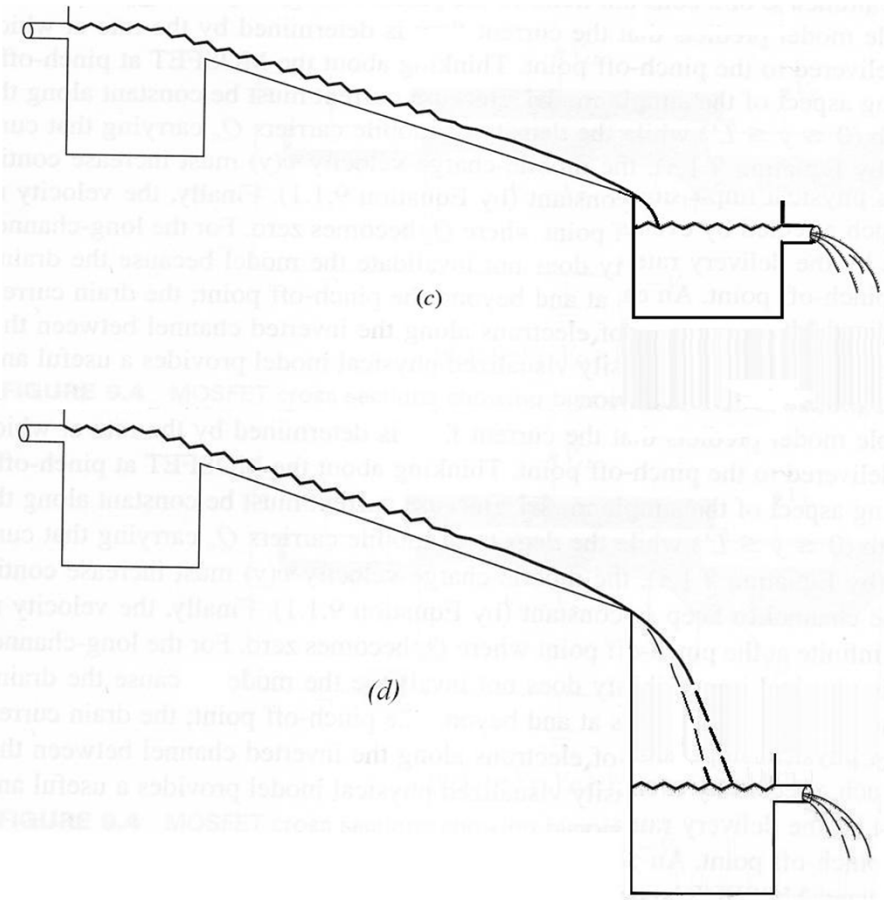
The phenomenon of the saturation of the drain current can be likened, albeit imperfectly. to a water analogy, as shown below.



(a) The water depth in the channel can be varied by the gear and track (v_{GS}). When the source and drain are level (v_{DS} = 0) there is no flow.



(b) When the drain is lower than the source ($v_{DSsat} > v_{DS} > 0$), and a water channel exists between them due to the "bias" by the gear and track ($v_{GS} > V_{TH}$), water flows along the channel. This corresponds to the linear region of operation of the MOSFET.



(c) The flow is limited by the channel capacity. When the drain has been lowered to the point where the limit is reached, the rate of water flow cannot be increased further. This corresponds to $v_{DS} = v_{DSsat}$.

(d) Lowering the drain further (increasing v_{DS} beyond v_{DSsat}) only increases the height of the waterfall at its edge, but does not increase the rate of flow of water in the channel.

- For a given v_{GS}, the drain current i_D reaches the constant (saturation) value, called i_{Dsat}, when

$$v_{DS} = v_{DSsat} = v_{GS} - V_{TH} \tag{4.12}$$

- Substituting eqn (4.12) into eqn (4.11) , we get

$$i_D = i_{Dsat} = \frac{1}{2}\mu_n \frac{W}{L} C_{ox}(v_{GS} - V_{TH})^2 \tag{4.13}$$

for $v_{DS} \geq v_{DSsat}$.

- The conductance parameter K_n is defined as

$$K_n = \frac{1}{2}\mu_n \frac{W}{L} C_{ox}. \tag{4.14}$$

- Hence, eqn (4.13) can also be expressed as

$$i_D = i_{Dsat} = K_n(v_{GS} - V_{TH})^2 \tag{4.15}$$

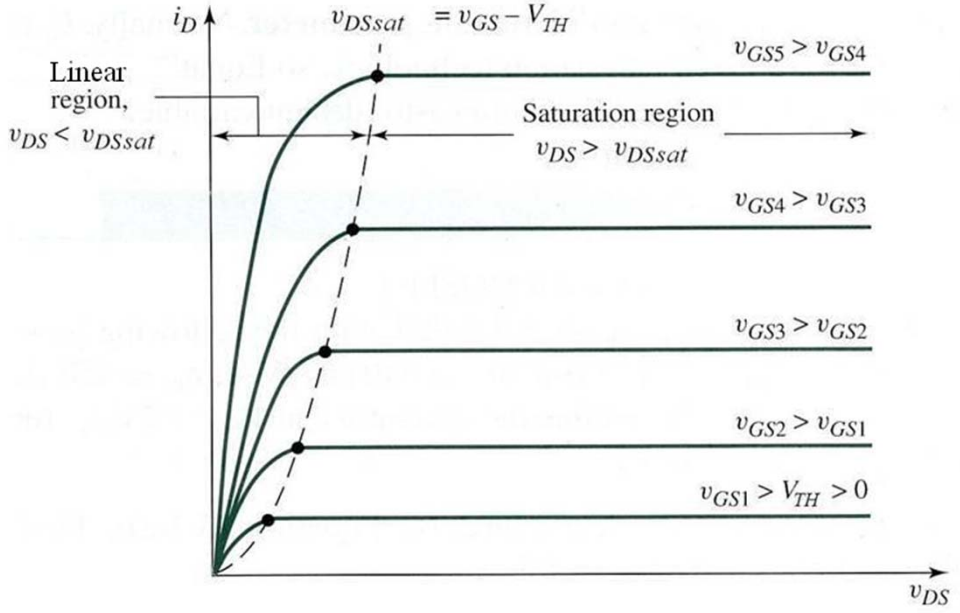
- In summary, the i_D - v_{DS} characteristics of an n-channel MOSFET are given by the following equations :

$$i_D = \mu_n \frac{W}{L} C_{ox}\left[(v_{GS} - V_{TH})\, v_{DS} - \frac{1}{2} v_{DS}^2\right] \qquad \text{in the linear region,} \quad v_{DS} < v_{GS} - V_{TH} \qquad (4.16)$$

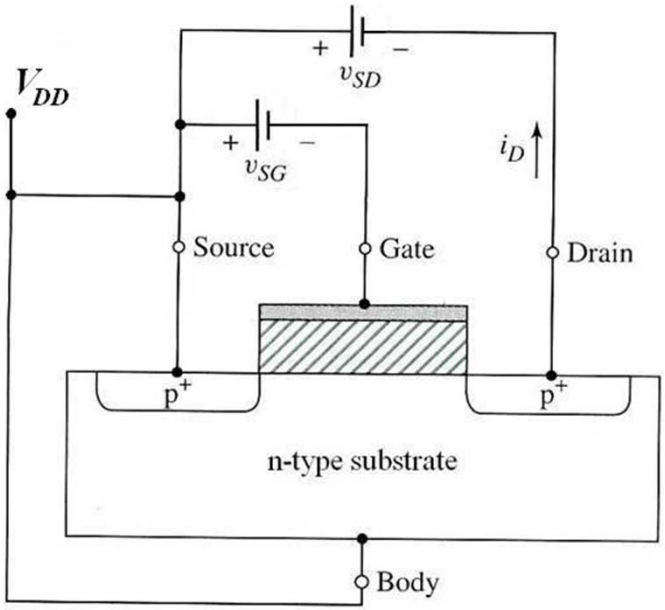
$$i_D = i_{Dsat} = \frac{1}{2} \mu_n \frac{W}{L} C_{ox} (v_{GS} - V_{TH})^2 = K_n (v_{GS} - V_{TH})^2 \qquad (4.17)$$

in the saturation region, $v_{DS} \geq v_{GS} - V_{TH}$

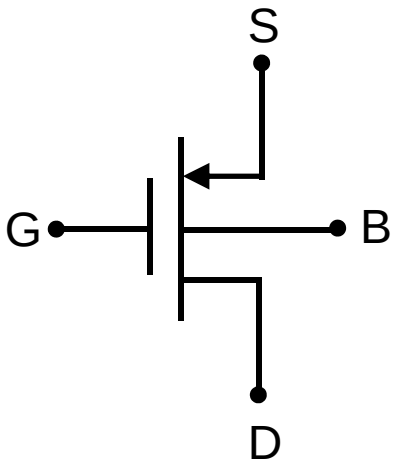
where $K_n = \frac{1}{2} \mu_n \frac{W}{L} C_{ox}$ (4.18)



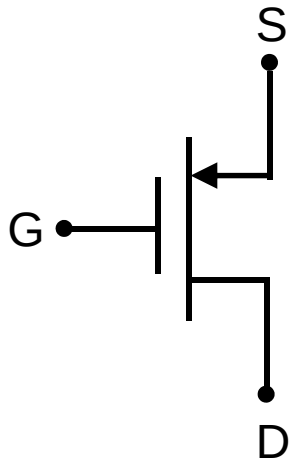
p-channel MOSFET (pMOS)



Cross-sectional view of a p-channel enhancement-mode MOSFET.



Circuit symbols for a p-channel MOSFET



Simplified symbol of the p-channel MOSFET when the substrate is connected to V_{DD}.

- In a p-channel MOSFET, also called a PMOS transistor, heavily doped p^+ regions make up the source and drain regions. The substrate is n-type.

- When a negative voltage whose magnitude is greater than the threshold voltage (which is also negative) is applied to gate, an inversion layer of holes is formed. Holes flow from the source to the drain when a voltage v_{DS}, which is negative, is applied.
- In a p-channel MOSFET, v_{DS}, v_{GS} and V_{TH} are all negative.
- Holes are the majority carriers. They flow from the source to the drain.
- To maintain the same notation and sign as n-channel MOSFET, we shall express the i_D - v_{DS} equations for the p-channel MOSFET in terms of absolute values.

$$|i_D| = \mu_p \frac{W}{L} C_{ox}\left[(|v_{GS}| - |V_{TH}|)\,|v_{DS}| - \frac{1}{2}|v_{DS}|^2\right] \quad \text{in the linear region,} \quad |v_{DS}| < |v_{GS}| - |V_{TH}| \qquad (4.19)$$

$$|i_D| = |i_{Dsat}| = \frac{1}{2}\mu_p \frac{W}{L} C_{ox}(|v_{GS}| - |V_{TH}|)^2 = K_p(|v_{GS}| - |V_{TH}|)^2 \qquad (4.20)$$

in the saturation region, $|v_{DS}| \geq |v_{GS}| - |V_{TH}|$

where $$K_p = \frac{1}{2}\mu_p \frac{W}{L} C_{ox} \qquad (4.21)$$

3. Comparison between MOS and Bipolar transistors

An MOS transistor is a four terminal device while a bipolar transistor is a three terminal device. Both of them can be used as logic switches or as amplifiers. The comparison table below sets out some of the differences.

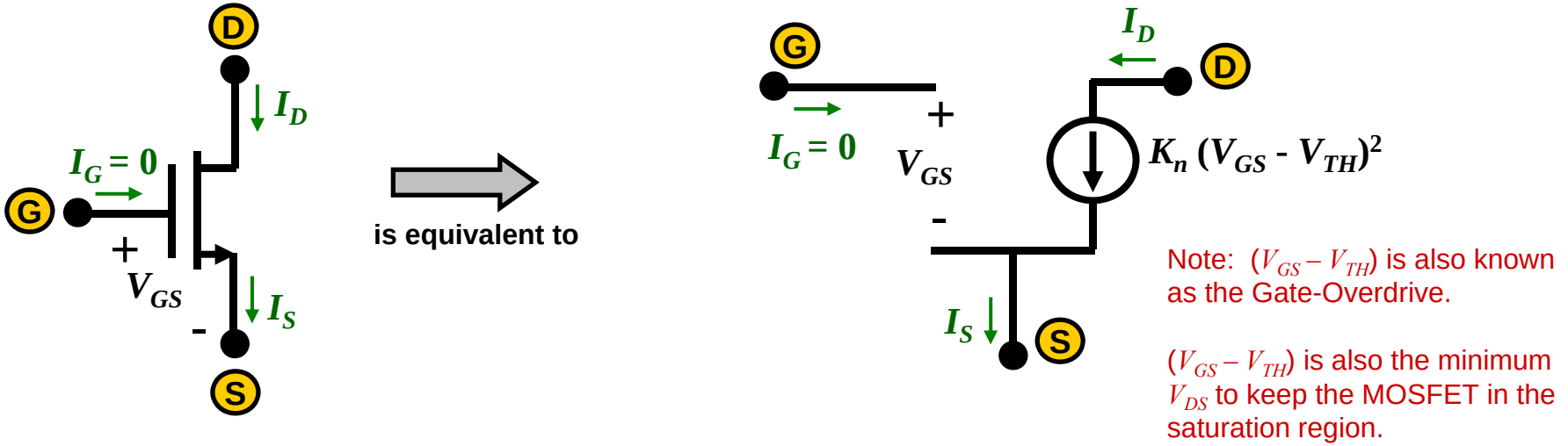
Feature	Bipolar Transistor	MOS Transistor
Terminals	Emitter Base Collector	Source Drain Gate Substrate
Charge carriers	Bipolar (both electrons and holes are involved in operation)	Unipolar (only either electrons or holes are involved in operation)
Current flow	Diffusion dominated (in the base)	Drift dominated (in the channel)
Conduction	Bulk phenomenon	Surface phenomenon
Main Applications	High frequency, high speed, high power circuits	Logic, memory, mixed signal circuits, low power and VLSI circuits

4. Large Signal Model of the MOSFET (Saturation)

4.1 N-Channel MOSFET

In the Saturation region ($V_{GS} > V_{TH}$ and $V_{DS} \geq V_{GS} - V_{TH}$),

from eqn (4.17), we have, under d.c. condition, $I_{Dsat} = K_n (V_{GS} - V_{TH})^2$



Note: $(V_{GS} - V_{TH})$ is also known as the Gate-Overdrive.

$(V_{GS} - V_{TH})$ is also the minimum V_{DS} to keep the MOSFET in the saturation region.

Large Signal Model of the MOSFET (Linear)

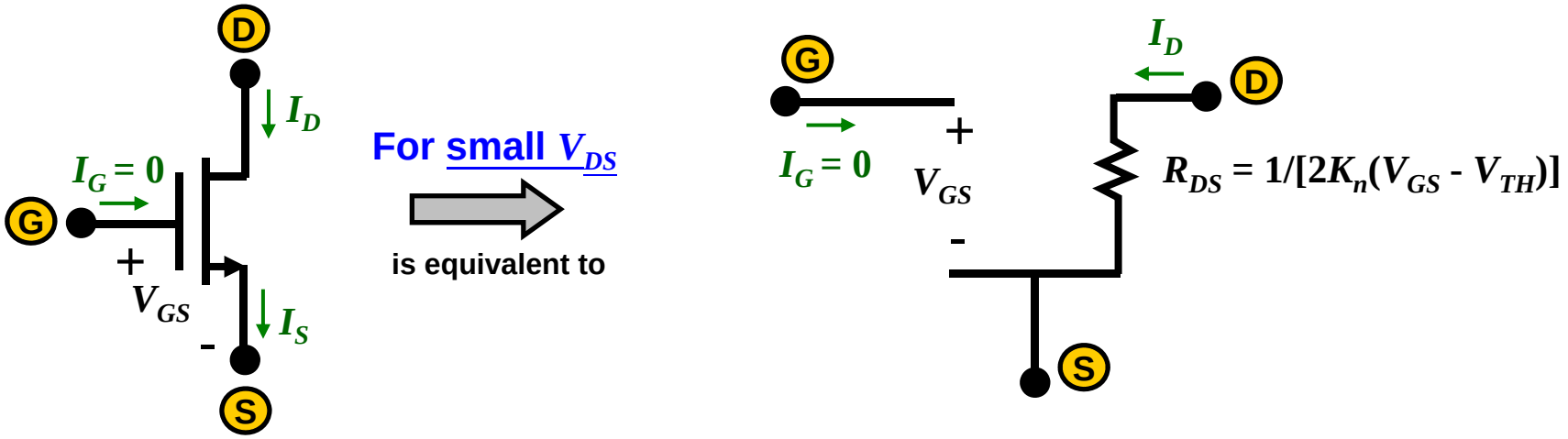
In the Linear region ($V_{GS} > V_{TH}$ and $V_{DS} < V_{GS} - V_{TH}$), from eqn (4.16), under d.c. condition,

$$I_D = \mu_n C_{ox} \frac{W}{L}\left[(V_{GS} - V_{TH})V_{DS} - \frac{V_{DS}^2}{2}\right]$$

For small V_{DS}, we neglect $V_{DS}^2/2$, $\quad I_D \approx \mu_n C_{ox} \frac{W}{L}(V_{GS} - V_{TH})V_{DS} = 2K_n(V_{GS} - V_{TH})V_{DS}$

The drain-to-source resistance for small V_{DS} is

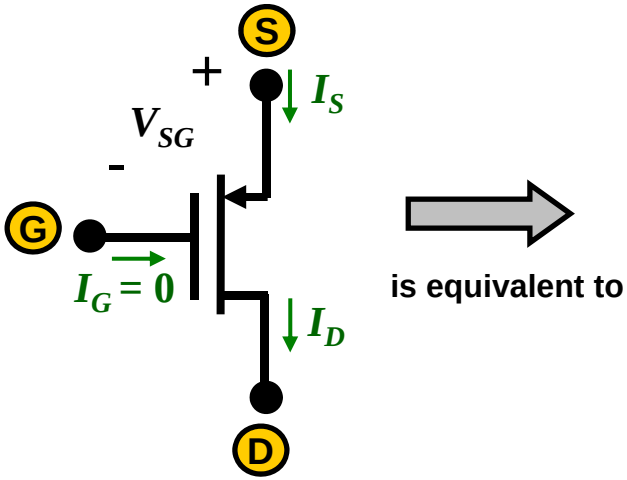
$$R_{DS} = \left.\frac{V_{DS}}{I_D}\right|_{\substack{\text{Small} \\ V_{DS}}} = \frac{1}{2K_n(V_{GS} - V_{TH})}$$



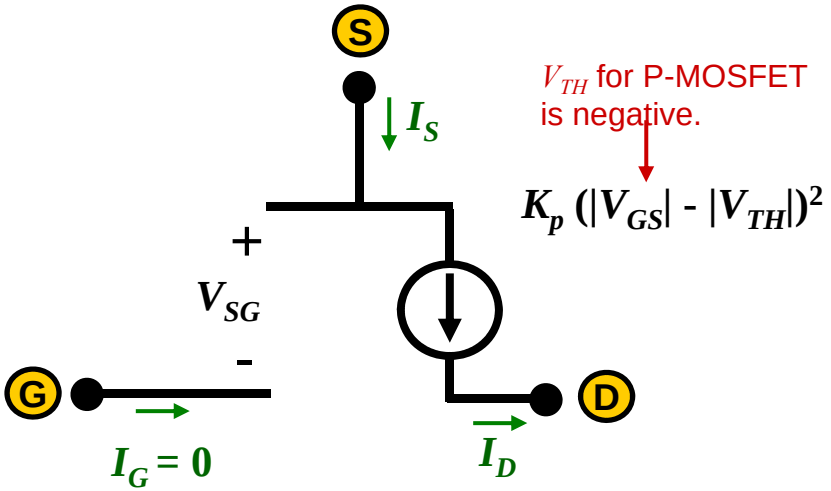
Large Signal Model of the MOSFET

4.2 p-channel MOSFET

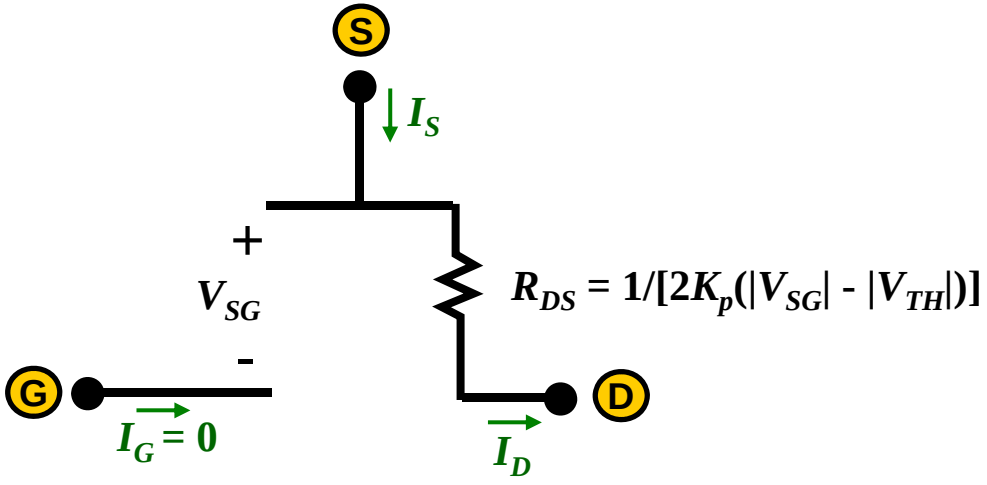
In the Saturation region ($|V_{GS}| > |V_{TH}|$ and $|V_{DS}| \geq |V_{GS}| - |V_{TH}|$), and under d.c. condition,



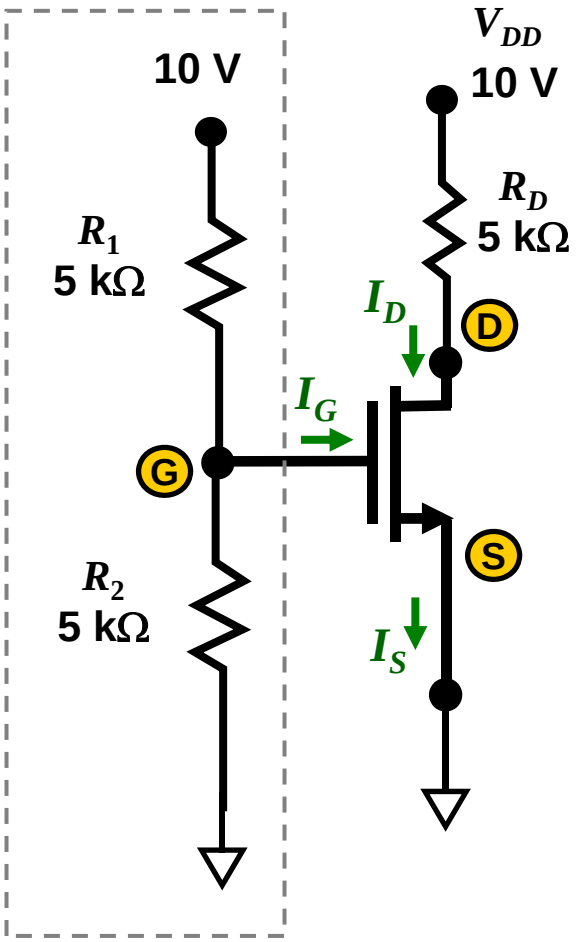
is equivalent to



In the Linear region ($|V_{GS}| > |V_{TH}|$ and $|V_{DS}| < |V_{GS}| - |V_{TH}|$), and under d.c. condition,



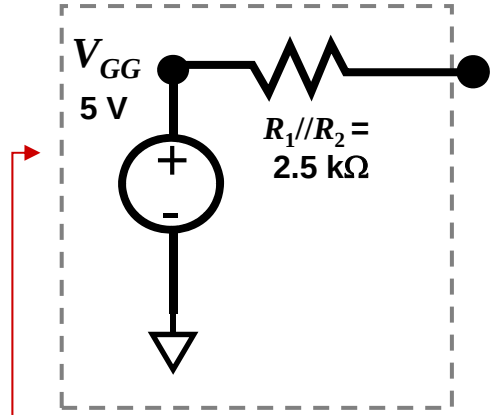
5. Bias Point for a MOSFET



Example 1.

Find the current I_D and the voltage V_D. Assume that $\mu_n C_{ox}$ = 2.0×10^{-5} A/V^2, W/L = 5, and V_{TH} = 1 V.

- First, we obtain the Thevenin's Equivalent Circuit of the Gate-biasing circuit shown in the dashed box (gray):

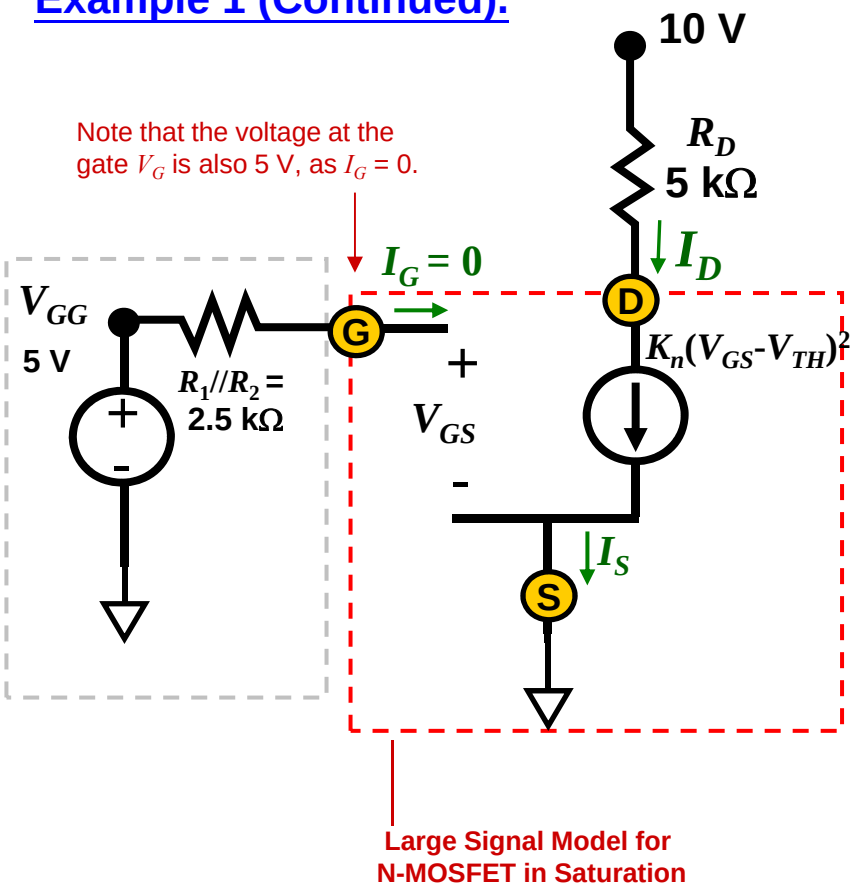


5kΩ / (5kΩ+5kΩ) x 10V

Note that the voltage divider method can also be used to find the voltage at node G as the gate current I_G = 0.

Bias Point for a MOSFET

Example 1 (Continued).



- Next, we assume the MOSFET is in saturation (needs to be checked later) and replace it with the corresponding large signal model.
- See that $V_{GS} = V_{GG} = 5$ V
- Substitute V_{GS} and other given parameters into the equation for I_{Dsat}:

$$I_D = I_{Dsat} = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS} - V_{TH})^2$$

$$I_{Dsat} = (0.5)(2.0\times10^{-5}\ \text{A/V}^2)(5)(5 - 1\text{V})^2$$
$$= 0.8\ \text{mA}$$

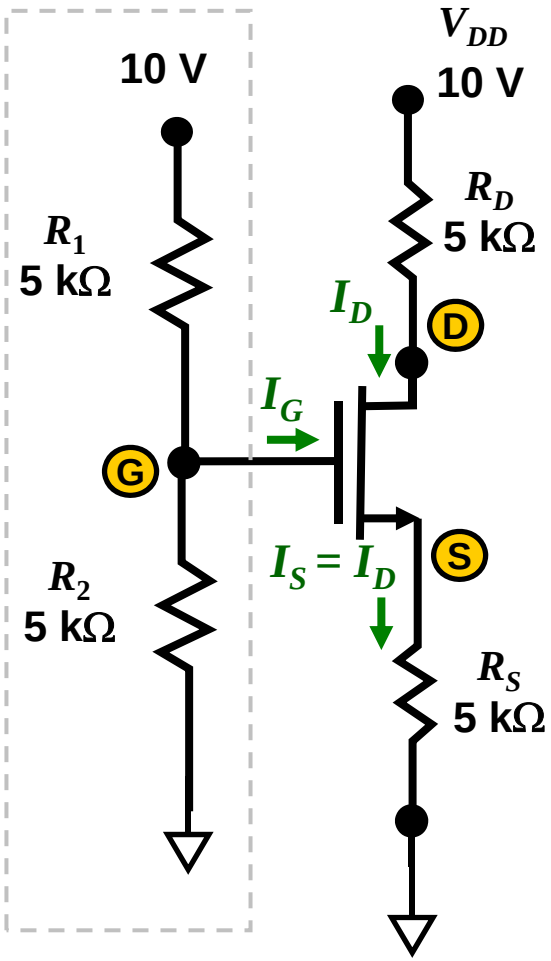
Hence, $V_D = 10\text{ V} - I_D R_D = 6$ V.

Check if MOSFET is indeed in Saturation:

$V_{DS} = 6$ V $> V_{GS} - V_{TH} = 4$ V

Yes.

Bias Point for a MOSFET



Example 2.

A 5 kΩ resistance is connected between the N-MOSFET source and ground of the circuit of Example 1. Determine the values of I_D and V_D.

We see that V_G = 5 V.

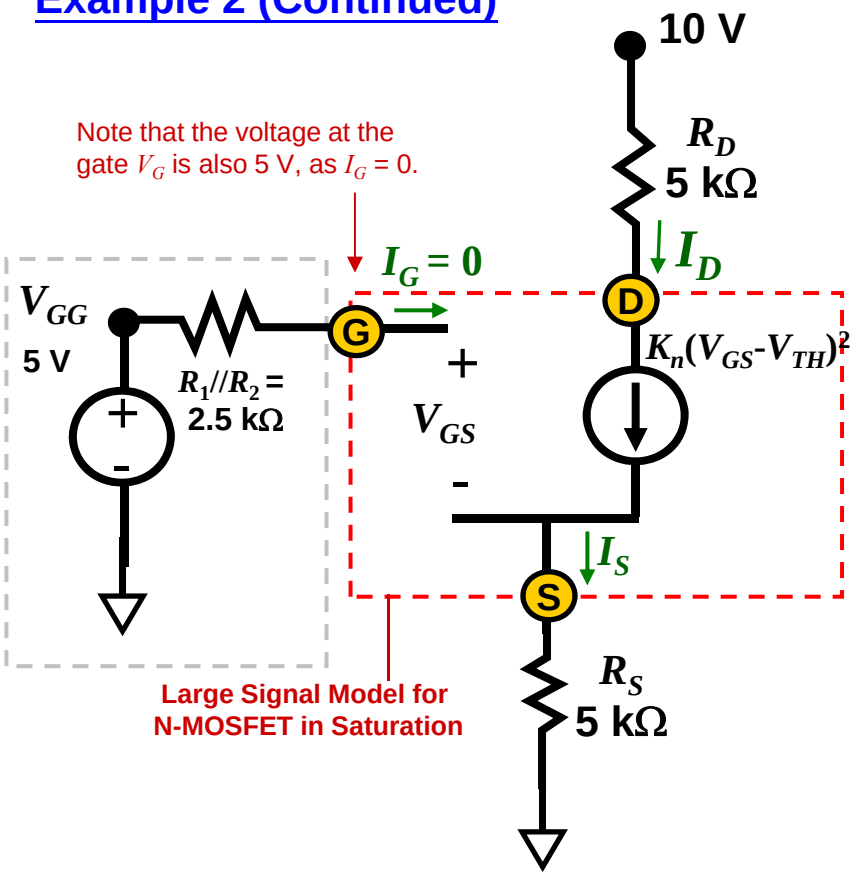
$V_{GS} = V_G - V_S$.

How about V_S?

$V_S = I_D R_S$ which depends on the solution for I_D.

Bias Point for a MOSFET

Example 2 (Continued)



- We assume the MOSFET is in saturation (needs to be checked later) and replace it with the corresponding large signal model.
- Examine the equation for I_{Dsat}:

$$I_D = I_{Dsat} = \tfrac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS} - V_{TH})^2$$

$$I_{Dsat} = (0.5)(2.0\times10^{-2}\ \text{mA/V}^2)(5)(V_G - V_S - 1\text{V})^2$$

I_{Dsat} ↑ In units of mA

R_S [in kΩ] ↓

$$I_{Dsat} = 0.05[5 - 5I_{Dsat} - 1]^2$$

- Solving the above quadratic equation, we obtain

$$I_{Dsat} = 2.09\ \text{mA or } 0.31\ \text{mA}.$$

- We recognize that $I_{Dsat} = 2.09$ mA cannot be a solution as this leads to $V_S > 10$ V.
- Therefore, $I_{Dsat} = 0.31$ mA is a solution.

- In this case, $V_D = 8.45$ V, $V_S = 1.55$ V, $V_{DS} = 6.9$ V, $V_{GS} = 3.45$ V.

- Check that the assumption that MOSFET is in saturation is valid.

6. Small Signal Model of the MOSFET

- It is shown in eqns (4.17) and (4.18) that for an n-channel MOSFET, the drain current i_D is a function of the gate-source voltage v_{GS} and drain source-voltage v_{DS}.
- The corresponding equations for the p-channel MOSFET are eqns (4.19) and (4.20).
- In general, we can write $i_D = f(v_{GS}, v_{DS})$. We note that the function relationship is non-linear.

- We can express the total instantaneous currents and voltages in terms of the d.c. (operating point) and a.c. (signal) currents and voltages, that is

$$i_D = I_D + i_d, \quad v_{DS} = V_{DS} + v_{ds}, \quad v_{GS} = V_{GS} + v_{gs}.$$

- Hence, we can write

$$i_D = I_D + i_d = f(V_{GS} + v_{gs}, V_{DS} + v_{ds}) \tag{4.22}$$

- Expanding eqn (4.22) as a Taylor series, and neglecting higher order terms for small v_{ds} and v_{gs}, we have

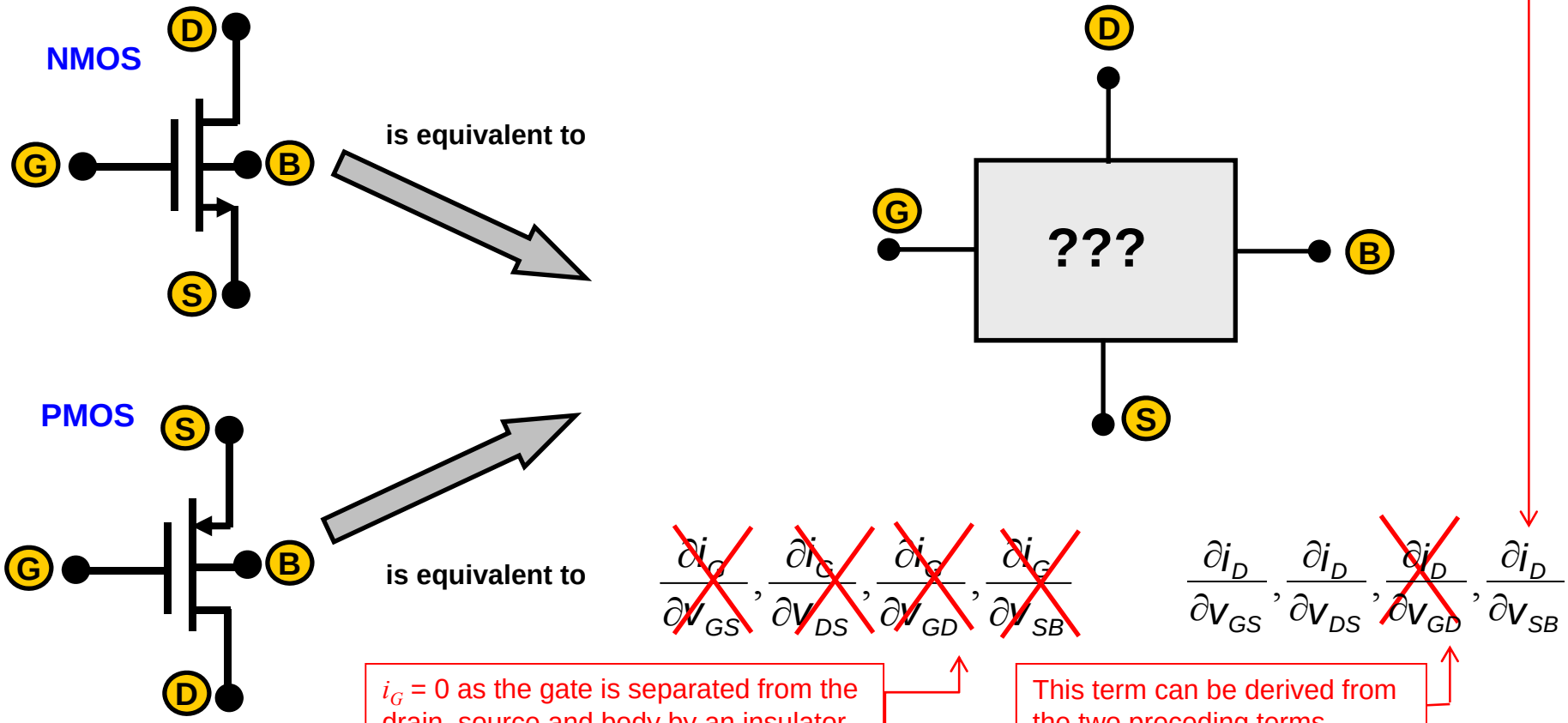
$$i_D = I_D + i_d = f(V_{GS} + v_{gs}, V_{DS} + v_{ds}) = f(V_{GS}, V_{DS}) + \left.\frac{\partial i_D}{\partial v_{GS}}\right|_{V_{GS}} \times v_{gs} + \left.\frac{\partial i_D}{\partial v_{DS}}\right|_{V_{DS}} \times v_{ds}$$

- Hence

$$i_d = \left.\frac{\partial i_D}{\partial v_{GS}}\right|_{V_{GS}} \times v_{gs} + \left.\frac{\partial i_D}{\partial v_{DS}}\right|_{V_{DS}} \times v_{ds} \tag{4.23}$$

Small Signal Model of the MOSFET

- In developing the small signal model of the MOSFET, we seek a set of linear relationships between the small signal components , namely, i_d, v_{gs} and v_{ds}.
- If the body (substrate) is not tied to the source, then a voltage applied to the body (w.r.t. to source) will affect the current in the MOSFET. This will be dealt with in Section 8.
- We are interested in small signal model under the **saturation region**.



Transconductance g_m

- Consider $i_D = K_n(v_{GS} - V_{TH})^2$ for a N-MOSFET. We take the derivative of i_D with respect to v_{GS} to examine how much i_D changes when v_{GS} changes:

This is the change in the Drain current. — lowercase '*d*'. — Uppercase '*D*'.

$$\lim_{v_{gs} \to 0} \frac{i_d}{v_{gs}} = \frac{di_D}{dv_{GS}} = 2K_n(v_{GS} - V_{TH})$$

This is the change in the Gate-Source voltage.

- Note that at the Bias Point, $i_D = I_D$ and $v_{GS} = V_{GS}$, so that $I_D = K_n(V_{GS} - V_{TH})^2$
- We evaluate di_D/dv_{GS} at the Bias Point for the N-MOSFET, also known as the transconductance g_m, to be:

$$g_m = \left.\frac{di_D}{dv_{GS}}\right|_{\substack{\text{Bias Point} \\ (V_{GS},\, I_D)}} = 2K_n(V_{GS} - V_{TH}) = 2\sqrt{K_n I_D} = \frac{2I_D}{(V_{GS} - V_{TH})}$$

Change in Drain current. Change in Gate-Source voltage.

$$i_d = g_m v_{gs}$$

The transconductance models the change in Drain current i_d caused by a change in the Gate-Source voltage v_{gs}. Note that (di_D/dv_{GS}) is the limit of (i_d/v_{gs}) when v_{gs} tends to zero.

- For P-MOSFET, we have $i_D = K_p(v_{SG} + V_{TH})^2$ and

$$g_m = \left.\frac{di_D}{dv_{SG}}\right|_{\substack{\text{Bias Point} \\ (V_{SG},\, I_D)}} = 2K_p(V_{SG} + V_{TH}) = 2K_p(|V_{GS}| - |V_{TH}|)$$

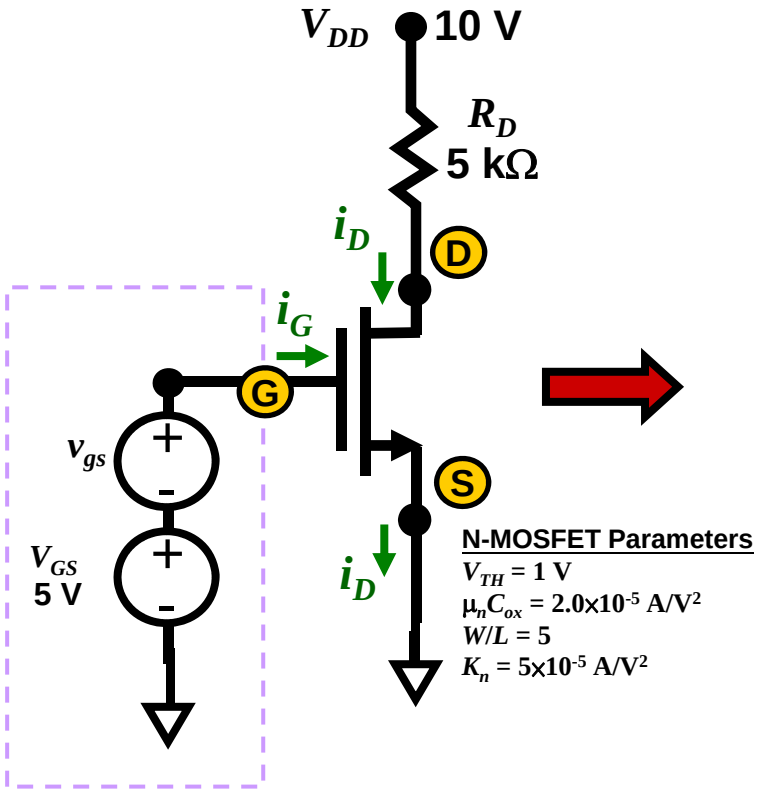
Change in Drain current. Change in Gate-Source voltage.

$$i_d = g_m v_{sg}$$

DC Bias Point of a MOSFET circuit

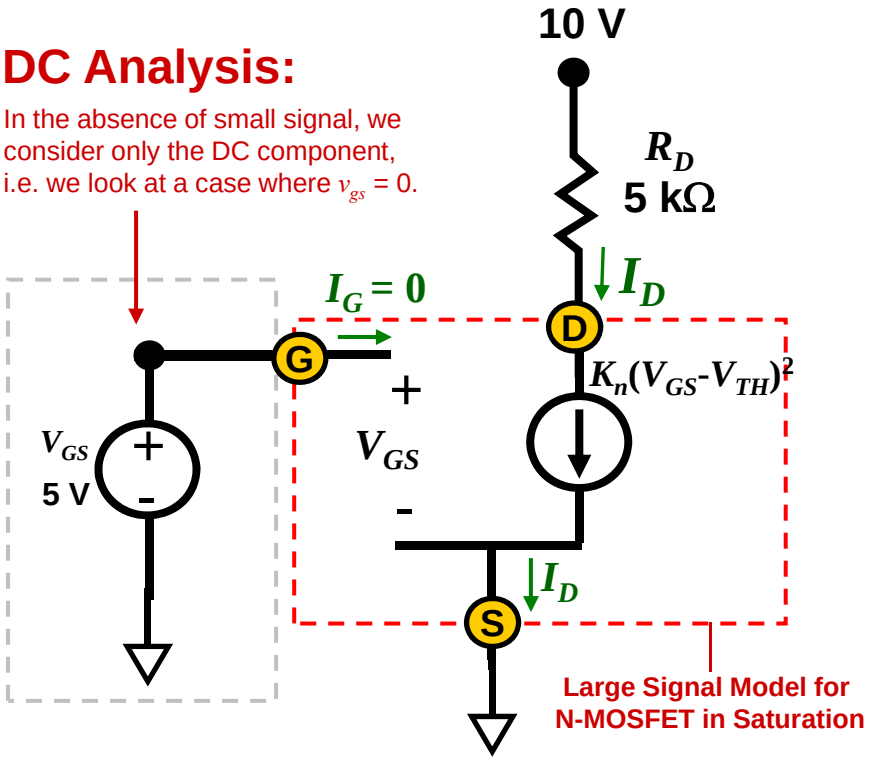
- Consider the circuit below (left). We need to determine the DC Bias Point for the MOSFET before analyzing what happens when there is a small signal (voltage signal v_{gs} which varies with time).

Conceptual Circuit used to study the Operation of MOSFET as a Small-Signal Amplifier



DC Analysis:

In the absence of small signal, we consider only the DC component, i.e. we look at a case where v_{gs} = 0.



- DC Analysis to Obtain Bias Point.

We see that V_{GS} = 5 V,

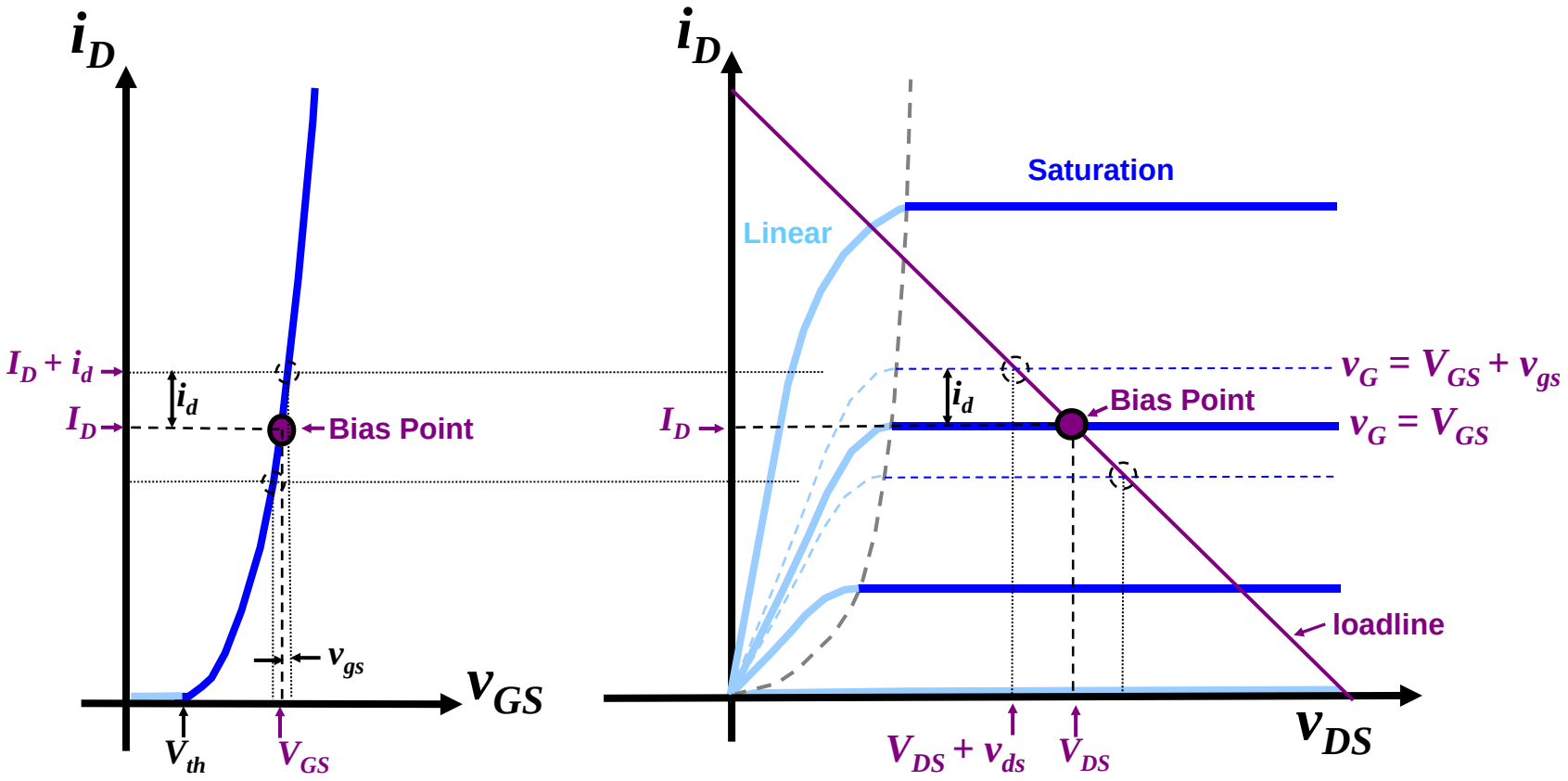
which can be substituted into the equation for I_D

$$I_D = K_n(V_{GS} - V_{TH})^2 = 0.8 \text{ mA}.$$

This gives $V_{DS} = 10 \text{ V} - I_D R_D = 6 \text{ V}$.

DC Bias Point of a MOSFET circuit (contd.)

- The Bias Point on the i_D-v_{GS} and i_D-v_{DS} curves are shown below.
- In the presence of a small signal v_{gs}, the solution for i_D, v_{GS}, and v_{DS} varies with time.

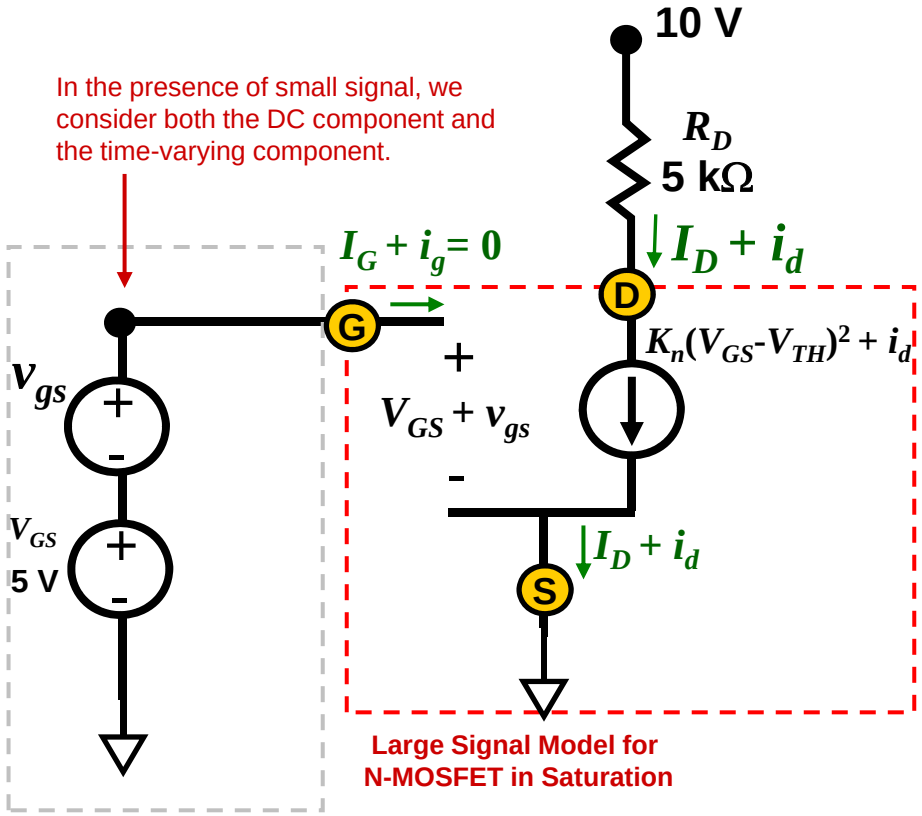


The small signal voltage v_{gs} varies with time. It contains information that is to be amplified.

We note that $i_D R_D + v_{DS} = V_{DD}$.
Rearranging, we have the loadline equation:
$i_D = (10\text{V} - v_{DS})/5\ \text{k}\Omega = 2\ \text{mA} - (v_{DS}/5\text{k}\Omega)$

Consider the Presence of Small Signal v_{gs}

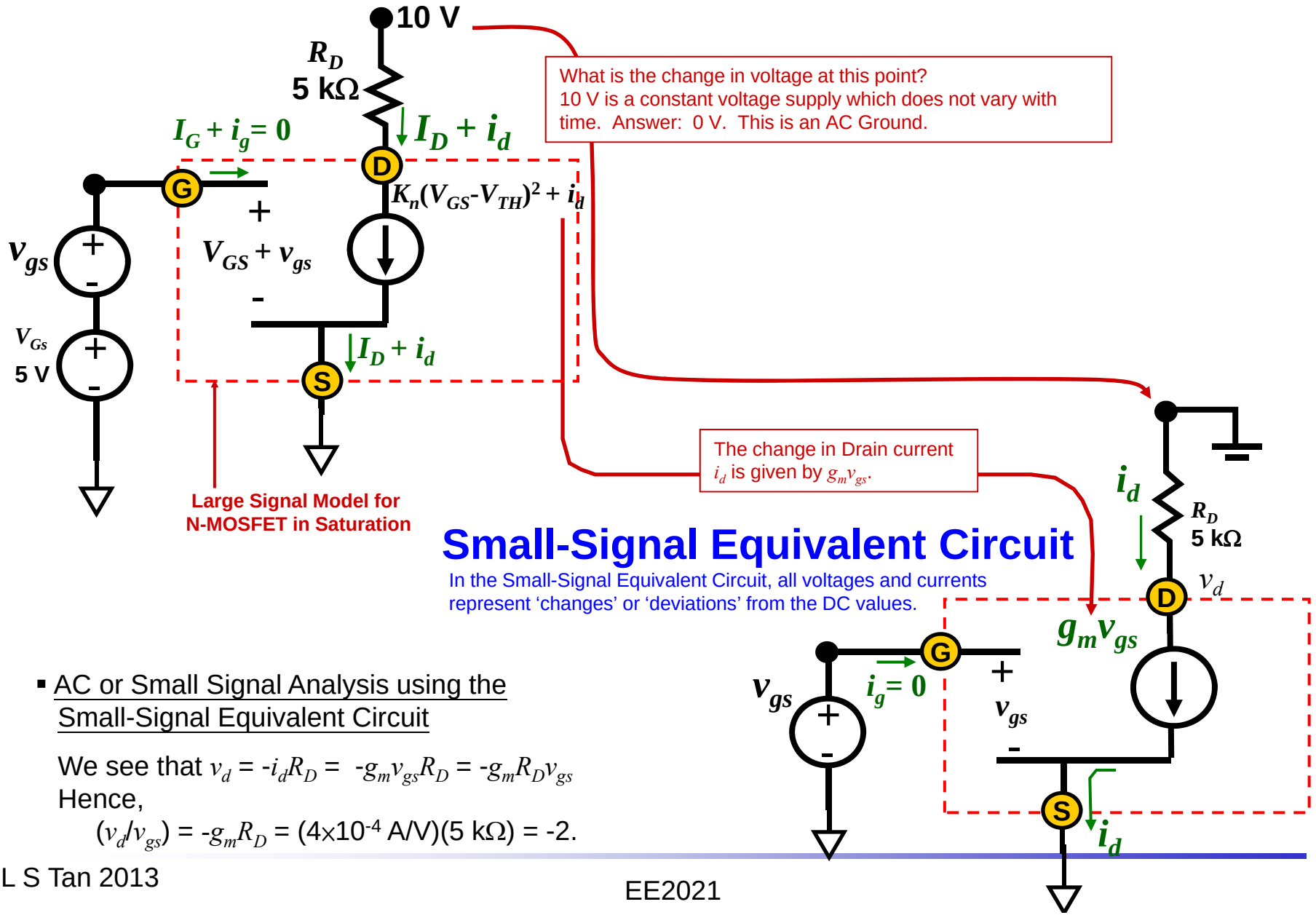
- We then consider the circuit where a small signal v_{gs} is present.
- Voltage and current quantities generally contain a DC component and a time-varying.
- Note that $i_G = I_G + i_g = 0$ since no current flows into the gate of the MOSFET, i.e. $I_G = 0$ and $i_g = 0$.



- We wish to examine the changes in currents or voltages. From Slide 35 , we know that $i_d = g_m v_{gs}$

  Substituting numerical values, we have $g_m = 2K_n(V_{GS} - V_{TH}) = 2\ (5\times10^{-5}\text{A/V}^2)(5\text{V} - 1\text{V}) = 4\times10^{-4}\ \text{A/V}.$

AC Analysis using Small-Signal Equivalent Circuit

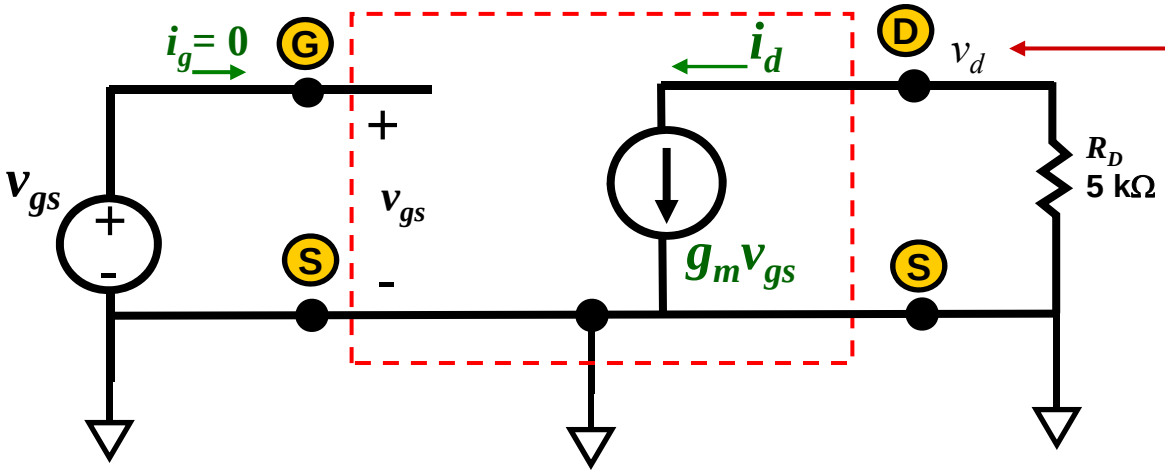


- AC or Small Signal Analysis using the Small-Signal Equivalent Circuit

  We see that $v_d = -i_d R_D = -g_m v_{gs} R_D = -g_m R_D v_{gs}$
  Hence,
  $(v_d/v_{gs}) = -g_m R_D = (4\times10^{-4}\ \text{A/V})(5\ \text{k}\Omega) = -2.$

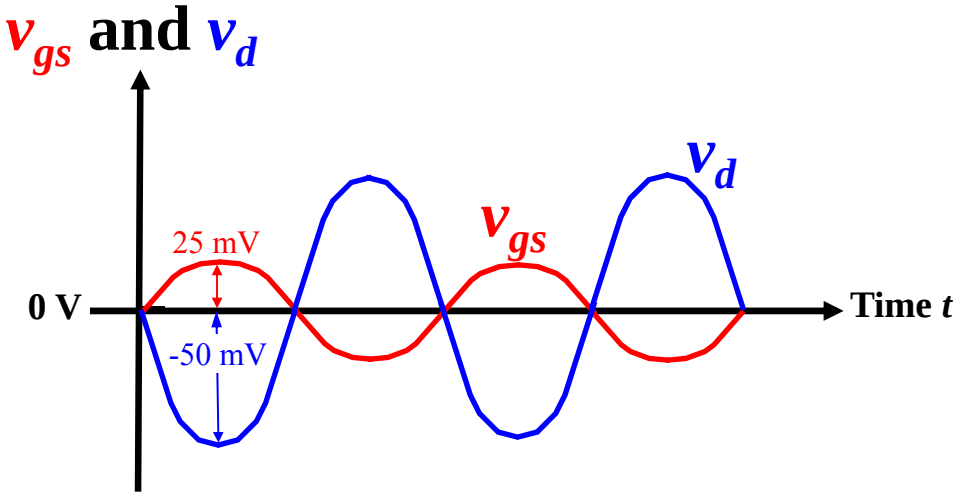
Interpretation of Results from Small-Signal Analysis

The Small-Signal Equivalent Circuit shown in the previous slide can be re-drawn as



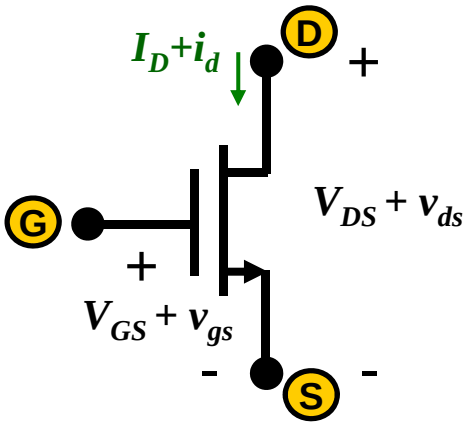
We found that $v_d = -(g_m R_D) v_{gs}$

For $v_d = -2v_{gs}$ it means that when the change in Gate-Source voltage is +25 mV, then the change in the Drain-Source voltage is -50 mV.



A Simple Hybrid-π Model for MOSFET

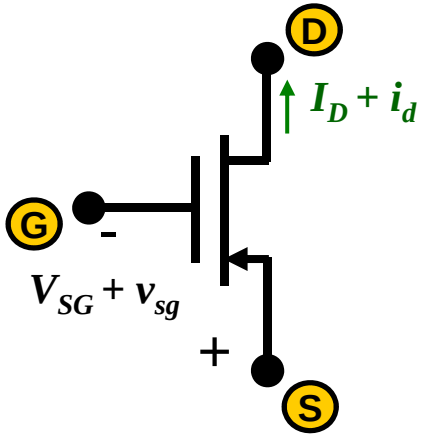
N-MOSFET



The change in drain current for the N-MOSFET is positive when there is an increase in the Drain current flowing into the drain

$$i_d = g_m v_{gs}$$

P-MOSFET

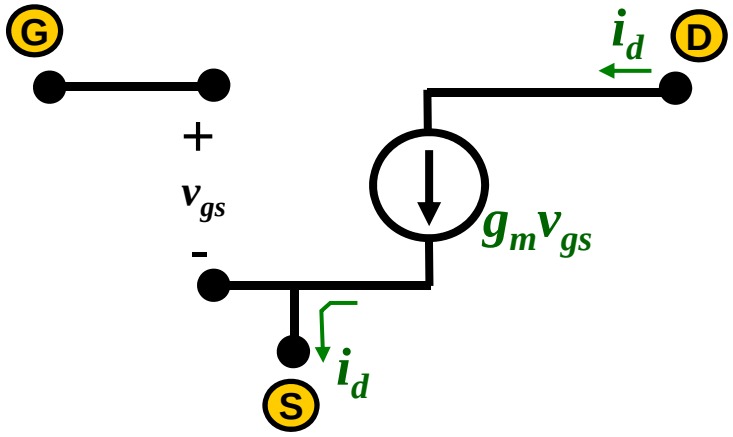


The Change in drain current for the P-MOSFET is positive when there is an increase in the Drain current flowing out of the drain

$$i_d = g_m v_{sg}$$

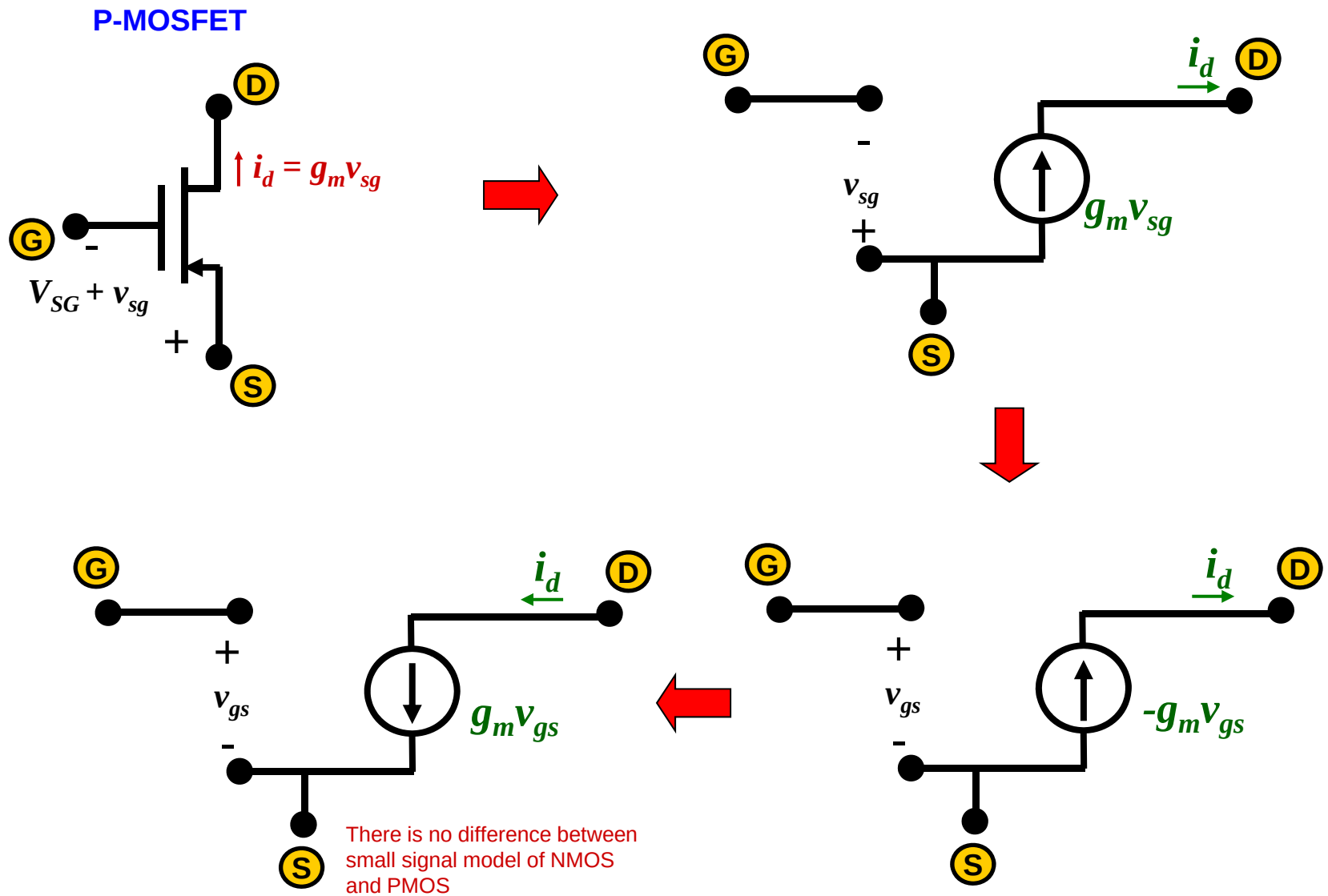
Replace the MOSFET by this Hybrid-π Model for Small-Signal Analysis

Hybrid-π Model for N-MOSFET or P-MOSFET (The dependence of i_D on v_{DS} is neglected)

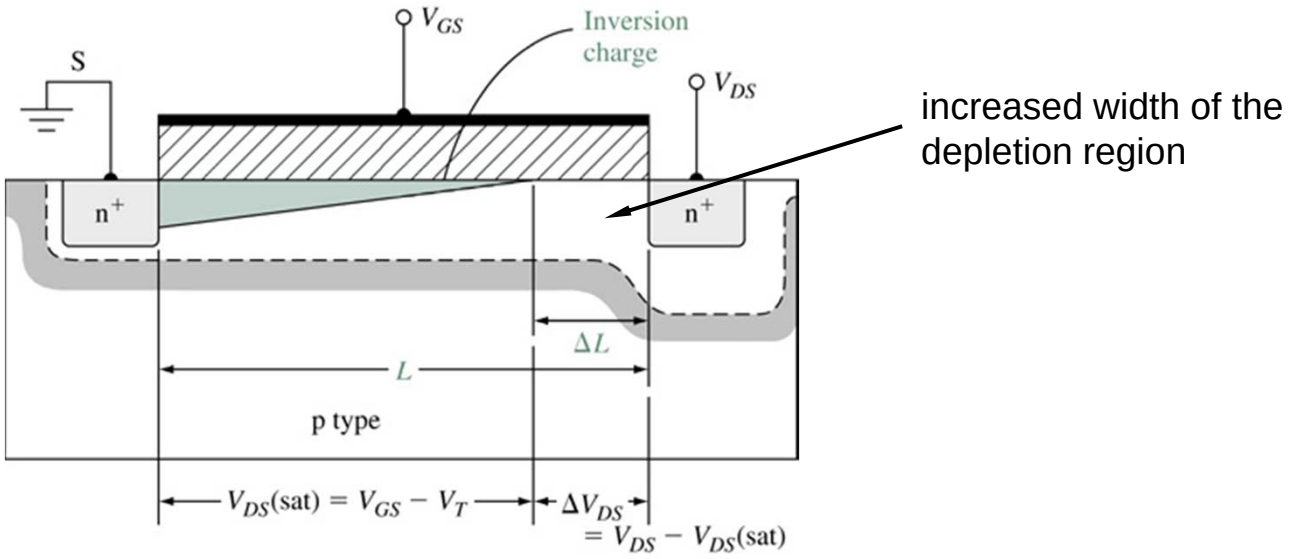


This Hybrid-π Model is in its simplest form here. We will use this simplest form by default.

A Simple Hybrid-π Model for MOSFET



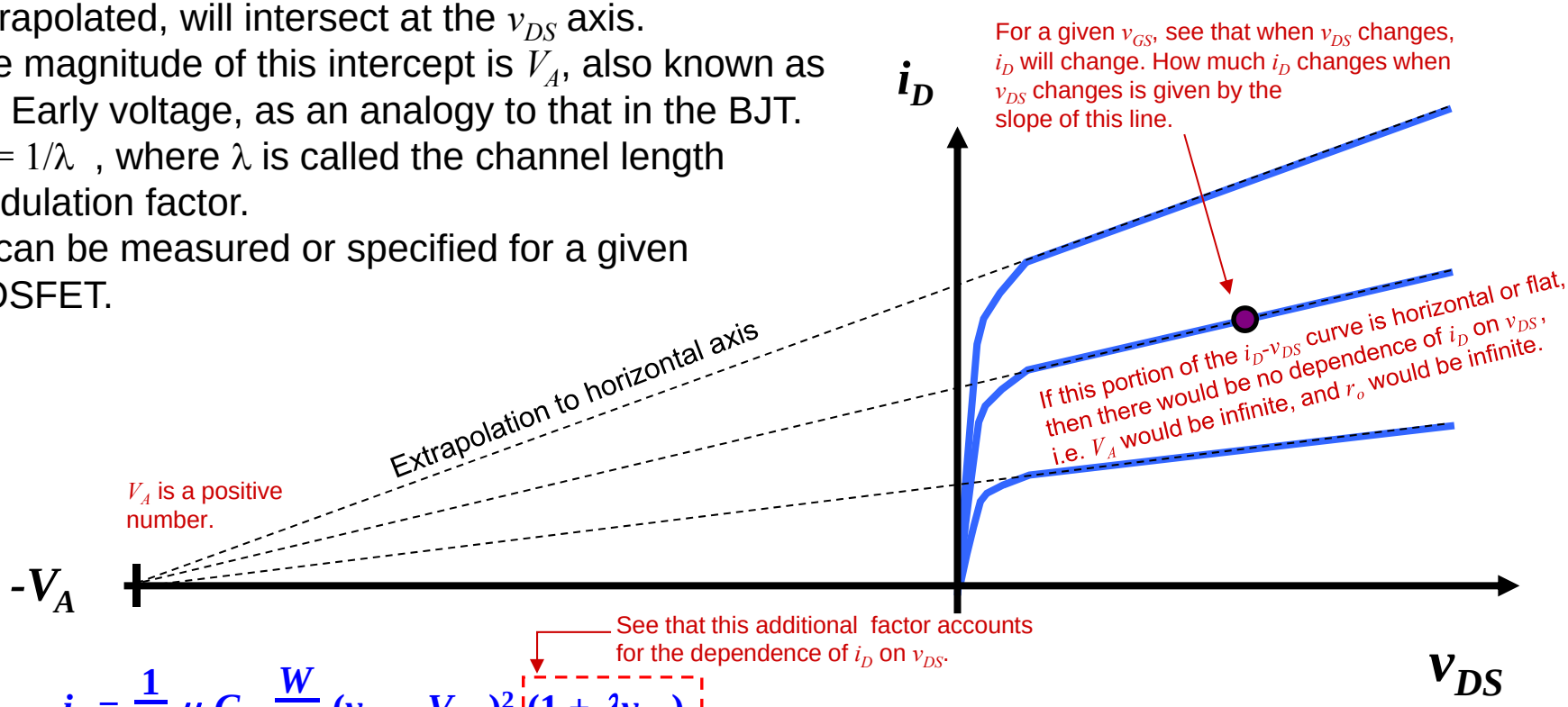
7. Channel Length Modulation



- In the derivation of the ideal I-V relationship of the MOSFET, we assumed that the channel length L was constant.
- However, when $v_{DS} > v_{DSsat}$, the depletion region at the drain junction extends laterally into the channel and the pinch-off point moves toward the source. Effectively, the channel length is reduced.
- If the channel is long, the reduction in the channel length is negligible, and L_{eff} is approximately equal to L. Otherwise, the effective channel length, L_{eff}, is less than L.
- L_{eff} is bias dependent and is modulated by v_{DS}. This is called "**channel length modulation**" . As the effective channel length is reduced, the conductance of the channel is therefore increased, which leads to a slight increase in the drain current i_D.

Output Resistance r_o

- Due to Channel-Length Modulation effects the i_D-v_{DS} characteristics in the saturation region, when extrapolated, will intersect at the v_{DS} axis.
- The magnitude of this intercept is V_A, also known as the Early voltage, as an analogy to that in the BJT.
- $V_A = 1/\lambda$, where λ is called the channel length modulation factor.
- V_A can be measured or specified for a given MOSFET.



See that this additional factor accounts for the dependence of i_D on v_{DS}.

$$i_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(v_{GS} - V_{TH})^2(1 + \lambda v_{DS})$$

$$i_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(v_{GS} - V_{TH})^2\left(1 + \frac{v_{DS}}{V_A}\right)$$

$$g_{ds} = \left.\frac{di_D}{dv_{DS}}\right|_{\text{Bias Point}} \approx \frac{I_D}{V_A} = \lambda I_D$$

$$r_o = \frac{1}{g_{ds}} \approx \frac{V_A}{I_D} = \frac{1}{\lambda I_D}$$

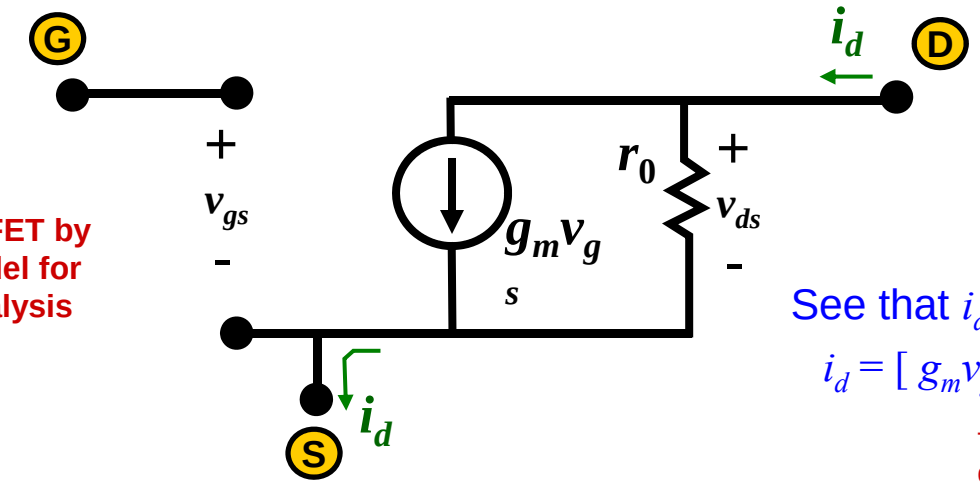
Hybrid-π Model with Output Resistance

- To model the increase in i_D with an increase in v_{DS}, a resistance r_o is included between nodes D and S in the Hybrid-π Model for the MOSFET:

$$\underbrace{\delta i_D(v_{GS},v_{DS})}_{i_d} = \underbrace{\frac{di_D}{dv_{GS}}}_{g_m}\underbrace{\delta v_{GS}}_{v_{gs}} + \underbrace{\frac{di_D}{dv_{DS}}}_{g_{ds}\ \text{or}\ 1/r_o}\underbrace{\delta v_{DS}}_{v_{ds}}$$

Hybrid-π Model with Output Resistance

(The dependence of i_D on v_{DS} is accounted for)



Replace the MOSFET by this Hybrid-π Model for Small-Signal Analysis

See that i_d is given by

$$i_d = [\, g_m v_{gs} + (v_{ds}/r_o)]$$

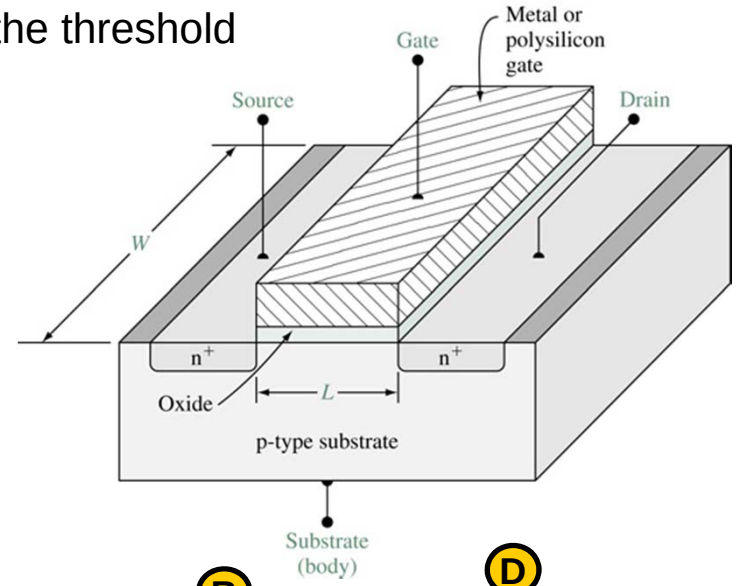
This term accounts for the dependence of i_d on v_{ds}.

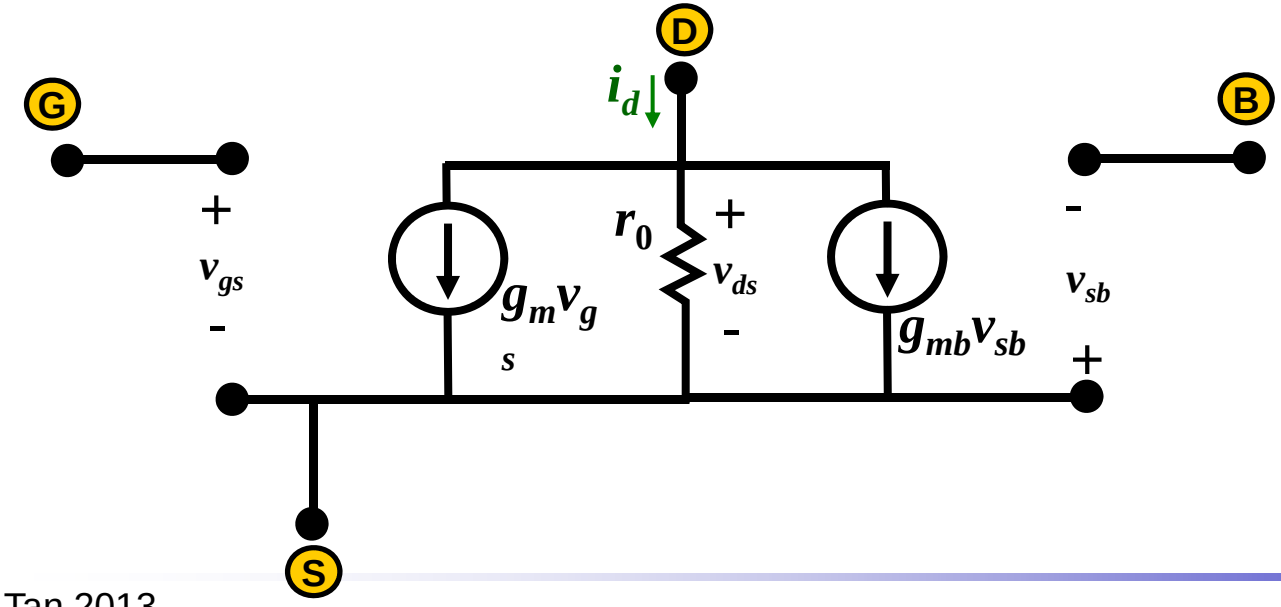
Note: In EE2021, you can assume that r_o is infinite by default. If V_A or λ is given, then r_o should be calculated and employed in the Small-Signal Analysis.

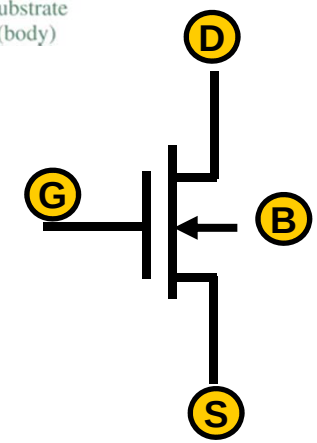
8. Bulk or Body Effect

- The Body Effect occurs when $v_{SB} \neq 0$ V, i.e. the source is not tied to the body.
- Consider a N-MOSFET, and suppose $v_{SB} = V_{SB} = 0$ V, but v_{SB} changes momentarily such that v_{sb} is positive. This increases the threshold voltage V_{TH}, and reduces i_D.
- The Body Effect can be modeled by considering

$$g_{mb} = \left.\frac{di_D}{dv_{SB}}\right|_{\substack{v_{GS}=\text{constant}\\ v_{DS}=\text{constant}}} < 0$$



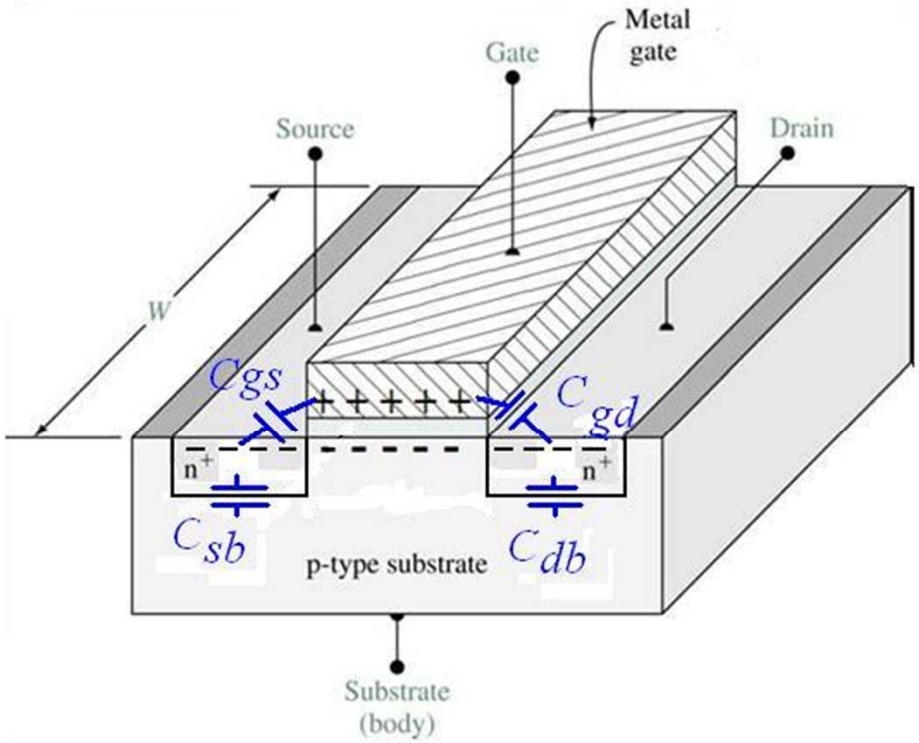




Body not tied to Source

9. MOSFET Capacitances

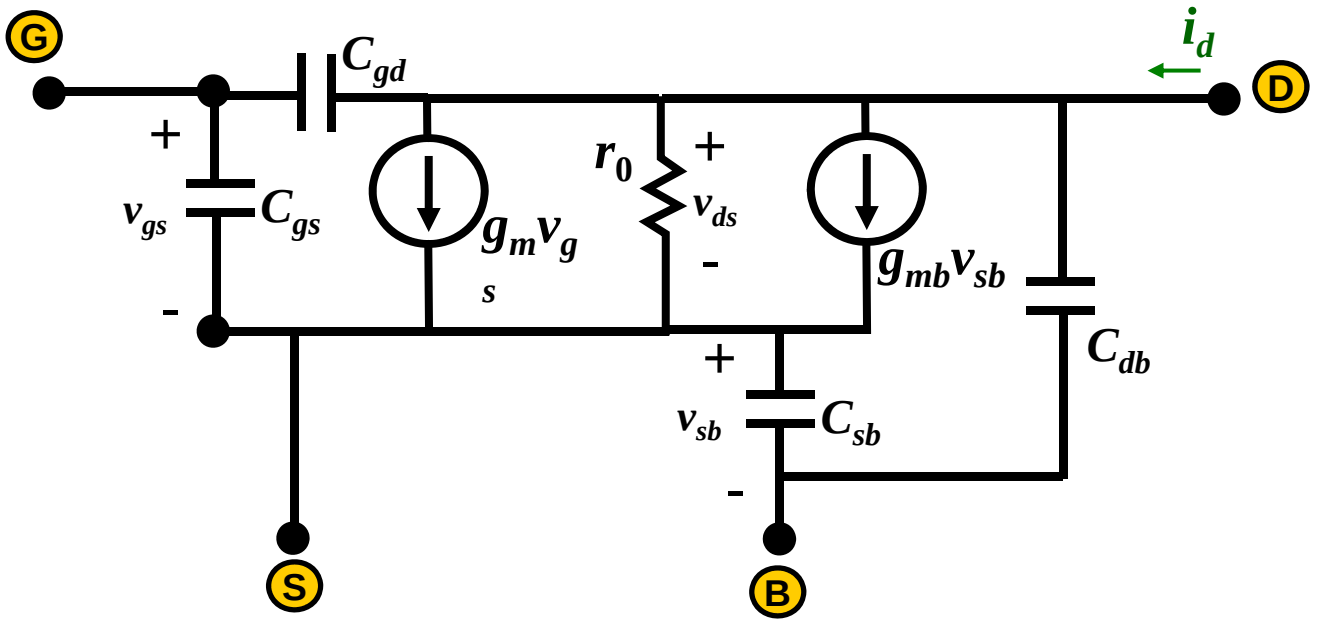
- There are charges stored in MOSFETs, and capacitances are associated with the charge storage mechanism.
- When terminal voltages change, the amount of charge stored changes.
- For studying frequency response, and for design of circuit operating at high frequencies, parasitic capacitances have to be included, e.g. C_{gs} and C_{gd}.



Full Hybrid-π Model at High Frequency

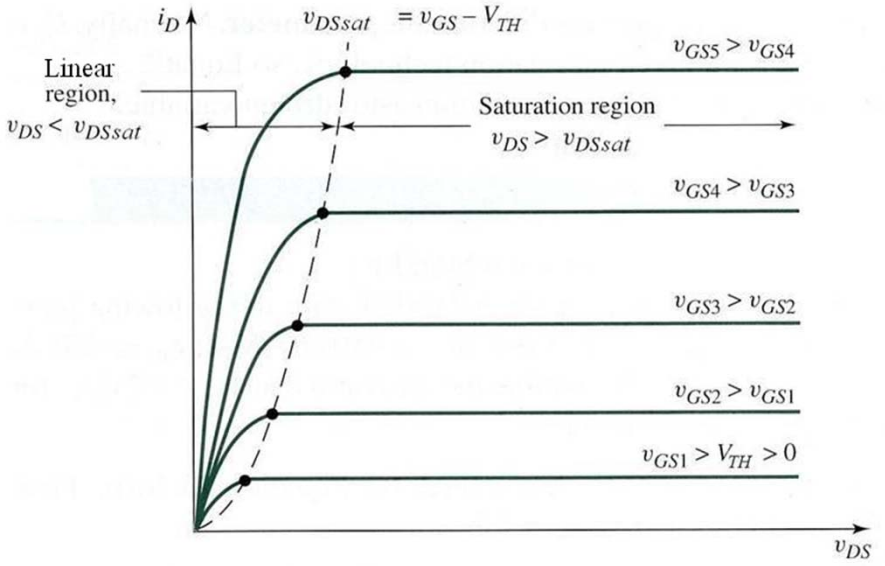
We introduce the existence of these capacitances here, and their inclusion in the Hybrid-π Model is necessary when frequency response is discussed. We will ignore these capacitances for low frequency signals.

High-Frequency Hybrid-π Model for MOSFET

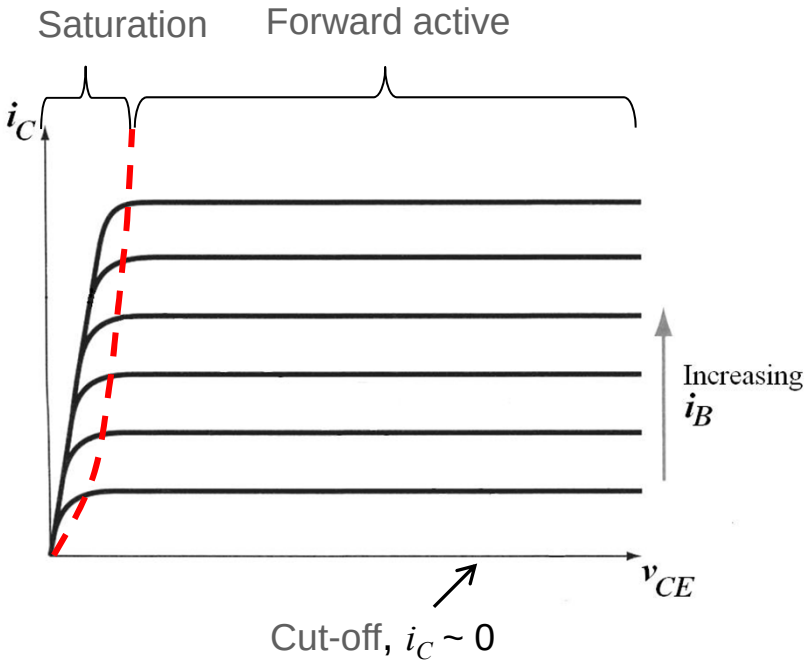


APPENDIX

Comparison of MOSFET and BJT i-v characteristics



MOSFET *i-v* characteristics



BJT i-v characteristics

Return