NATIONAL UNIVERSITY *of* SINGAPORE

Department of Electrical and Computer Engineering

EE2021 – Devices and Circuits

Tutorial 5

Q1.

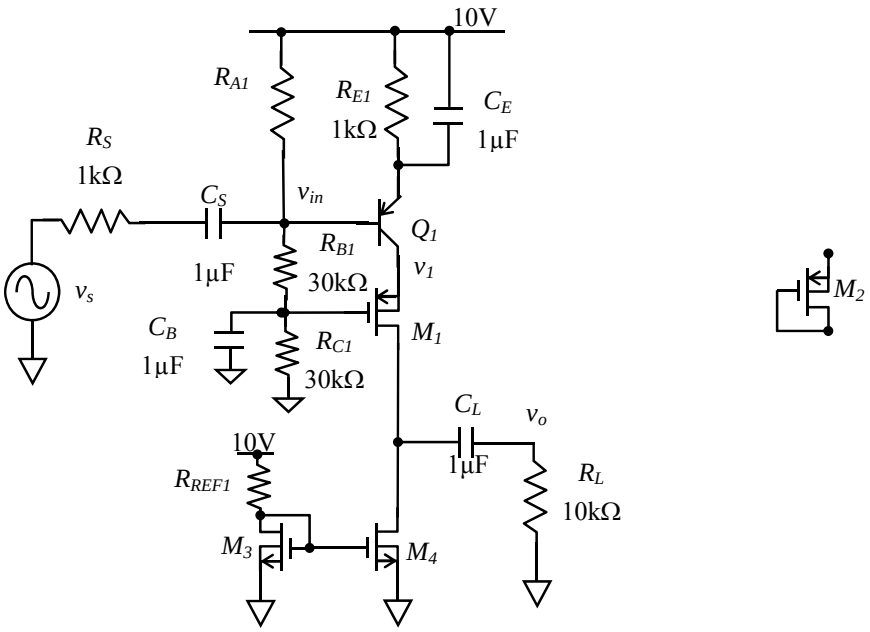

Fig. Q1

In the two-stage amplifier circuit shown in Fig. Q1, assume that the pnp BJT, the NMOS transistors and the PMOS transistors have the following device parameters:

- V_A = 100 V and β = 100 for the BJT, Q_1;
- K_n = 2m A/V^2, V_{THN} = 1 V, λ_n = 0.001V^{-1} and no body effect for the NMOS transistors, M_3 and M_4.
- K_p = 2m A/V^2, V_{THP} = -1 V, λ_p = 0.001V^{-1} and no body effect for the PMOS transistors, M_1 and M_2.

(a) Identify the configuration of each stage of the multi-stage amplifier.

(b) Design R_{REF1} such that M_1, M_3 and M_4 each has a drain current of 1 mA assuming these transistors are operating in the saturation region.

(c) Estimate the small signal parameters of M_1, i.e. $g_{m,M1}$, and $r_{o,M1}$ and the small signal parameters of Q_1, i.e., $g_{m,Q1}$, $r_{\pi,Q1}$, $r_{o,Q1}$, assuming the value of the drain current in part (b).

(d) Design R_{A1} to ensure that M_1, M_3 and M_4 each has a drain current of 1 mA assuming these transistors are operating in the saturation region.

(e) Estimate the overall gain, i.e., v_o/v_s.

(f) Diode connected transistor M_2 shown in the right of Fig. Q1 can be used to replace R_{E1}. Comment whether the overall gain will be affected and if the gain is affected, which component values need to be changed to restore the gain in part (e).

[Ans. 8.3 kΩ, 2.8 mA/V, 1 MΩ, 40 mA/V, 2.5 kΩ, 100 kΩ, 12.3 kΩ, 264]

Q2.

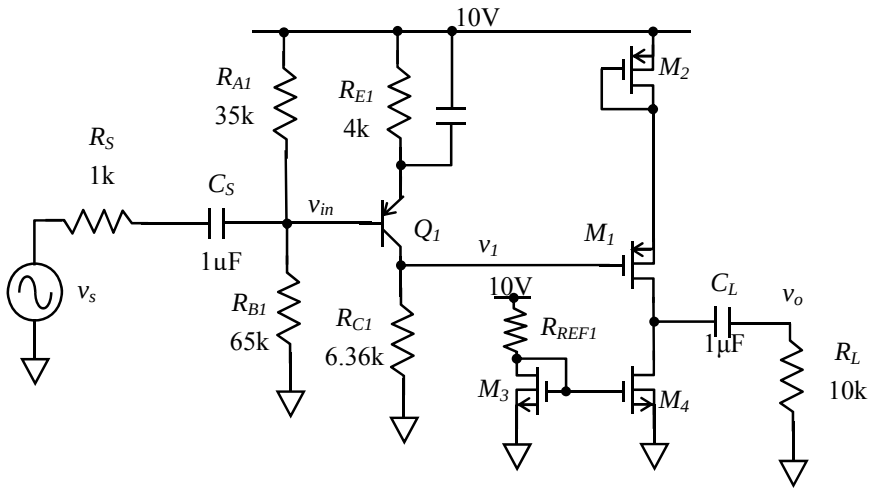

Fig. Q2

In the two-stage amplifier circuit shown in Fig. Q2, assume that the pnp BJT, the NMOS and the PMOS have the following device parameters:

- V_A = 100 V and β = 100 for the BJT, Q_1;
- K_n = 2m A/V^2, V_{THN} = 1 V, λ_n = 0.001 and no body effect for the MOSFETs, M_3 and M_4.
- K_p = 2m A/V^2, V_{THP} = -1 V, λ_p = 0.001 and no body effect for the MOSFETs, M_1 and M_2.

(a) Identify the configuration of each stage of the multi-stage amplifier.

(b) Estimate the collector current for Q_1 and its corresponding small signal parameter, i.e. g_{m_Q1}, r_{π_Q1}, r_{o_Q1}.

(c) Design R_{REF1} such that M_1, M_3, M_4 and M_2 each has a drain current of 3 mA.

(d) Estimate the small signal parameters of M_1, i.e. g_{m_M1}, and r_{o_M1} assuming the value of the drain current in (c).

(e) Estimate the overall gain, i.e., v_o/v_s.

(g) M_2 can be replaced with an NMOS transistor. Show part of the new circuit including only M_1, M_2 and V_{DD} but with M_2 replaced using NMOS transistor. Comment on the effect on the overall gain with reasoning.

[0.7 mA, 28 mA/V, 3.57 kΩ, 143 kΩ, 2.59 kΩ, 4.9 mA/V, 333 kΩ, 3175]

Q3. Analyze the following circuit. Write down the expressions for all the equivalent resistances (R_1-R_{10}, R_{in}, R_{out}). All expressions must be in terms of transistor small signal parameters. Neglect body effect.

(Hints: Some of the resistances are inter-dependent, so some resistances need to be worked out first before other resistances can be solved.)

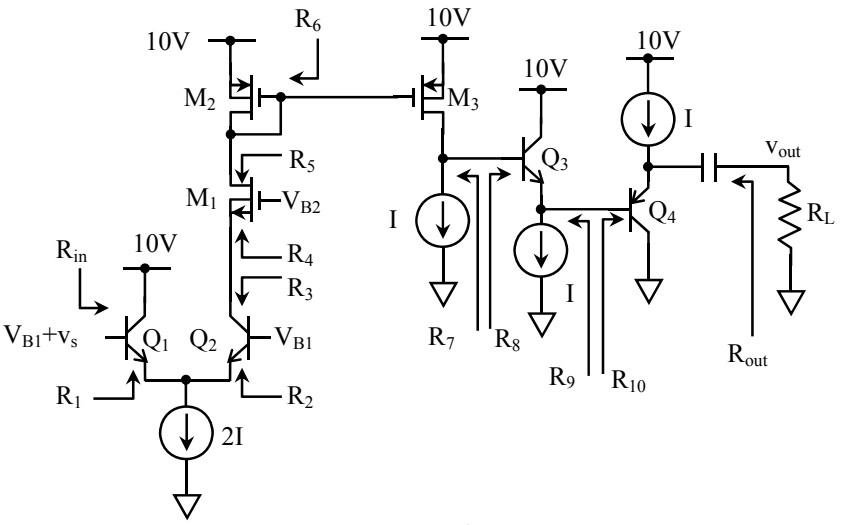

Fig. Q3

Q4. Show an opamp circuit that can generate the following transfer function in Fig. Q4:

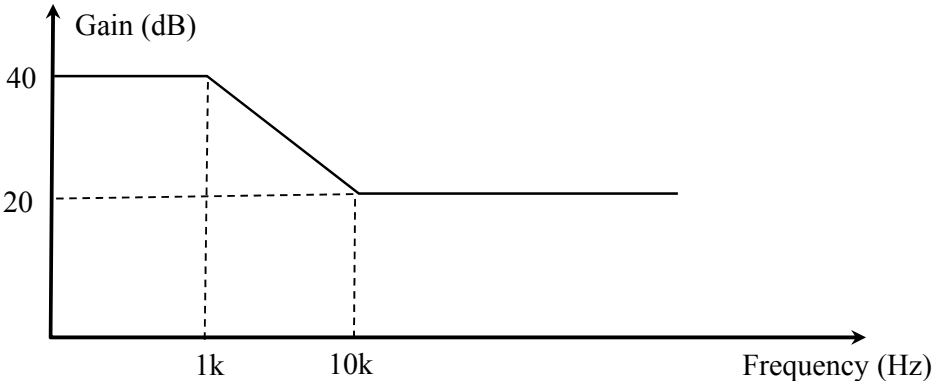

Fig. Q4

[Note : Gain(dB) =20×log$_{10}$(V_{out}/V_{in}). Hence, 40dB is equivalent to V_{out}/V_{in}=100, 20dB is equivalent to V_{out}/V_{in}=10]

Q5. (a) Derive R_x in the circuit shown in Fig. Q5a. (Note that v_1 is a voltage dependent voltage source and $R_x = v_x / i_x$.)

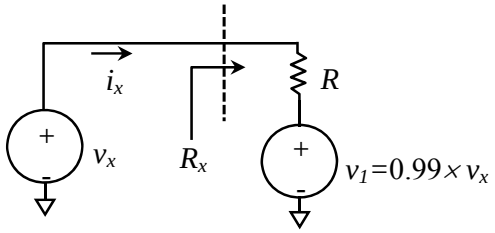

Fig. Q5a

(b) Derive the value k for the circuit shown in Fig. Q5b such that $v_1 = 0.99v_x$.

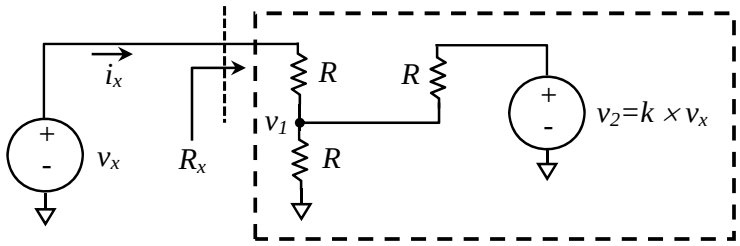

Fig. Q5b

(c) Design an opamp circuit that can realize circuit within the dash box in part (b). You can treat v_x as independent signal source.

(d) The circuit in part (c) is known as a resistance multiplier. It can realize huge resistance with relatively small resistor values. Suggest and show a simple filtering circuit that can make use of this technique.

Q6. You are given a task to build an arbitrary signal generator. You may assume that a square wave voltage source is readily available.

(a) Show an opamp circuit that can produce a triangular wave from a square wave input with 50% duty cycle, i.e. T_{POS}=T_{NEG}, as shown in Fig. Q6a.

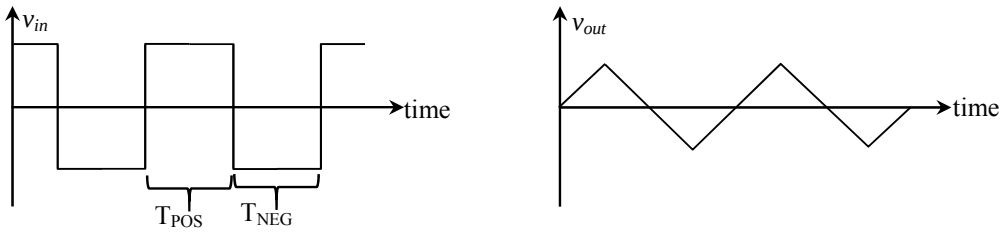

Fig. Q6a

(b) Consider the opamp circuit shown in Fig.Q6b. The switch will short circuit the capacitor whenever the input voltage is positive. Sketch the output waveform (v_{out}) when the input is a square wave with 50% duty cycle.

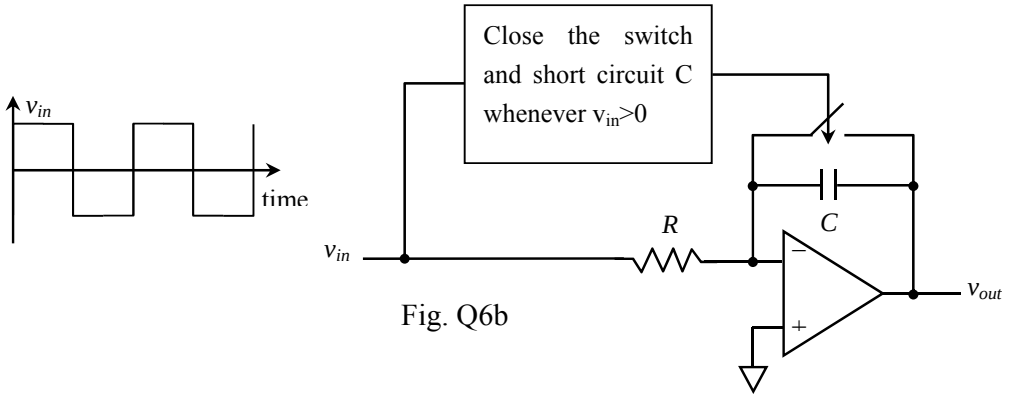

Fig. Q6b

(c) Show an opamp circuit that can produce a saw tooth wave from a square wave input with 50% duty cycle as shown in Fig. Q6c.

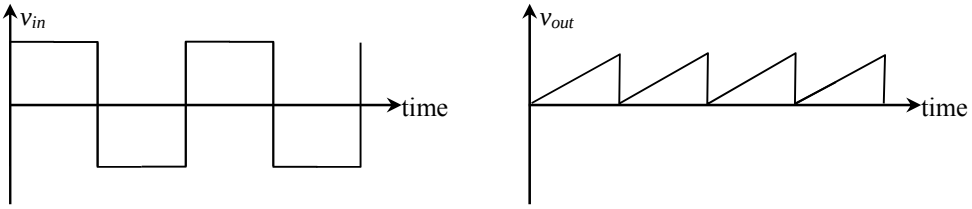

Fig. Q6c

Q7. (a) Draw an opamp circuit that can convert a square wave to a triangular wave.

(b) Consider the comparator circuit shown in Fig. Q7. Sketch the comparator output waveform for the given input waveform. Indicate clearly the timing and voltage information. You may assume that the maximum and minimum output voltages of the comparator are +5V and -5V, respectively.

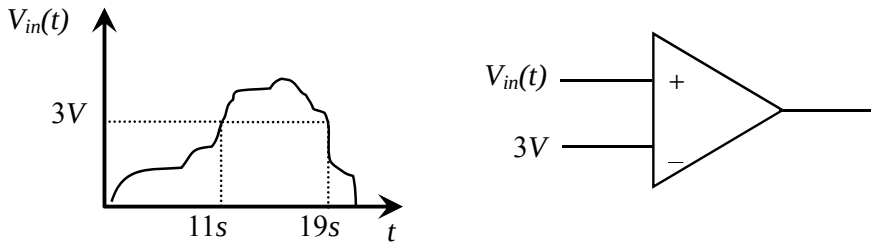

Fig. Q7

(c) Propose an opamp-based circuit that can produce a square wave with an arbitrary duty cycle. Duty cycle is defined as the ratio of the period that the waveform is high to the total clock period. For example, a 40% duty cycle means that the square wave is high for $0.4\times T_{period}$ and low for $0.6\times T_{period}$.