Strained Silicon Nanowire Transistors With Germanium Source and Drain Stressors

Tsung-Yang Liow, *Student Member, IEEE*, Kian-Ming Tan, Rinus Tek Po Lee, *Student Member, IEEE*, Ming Zhu, Ben Lian-Huat Tan, N. Balasubramanian, and Yee-Chia Yeo

***Abstract*—We report the first demonstration of pure germanium (Ge) source/drain (S/D) stressors on the ultranarrow or ultrathin Si S/D regions of nanowire FETs with gate lengths down to 5 nm. Ge S/D compressively strains the channel to provide up to $\sim$100% $I_{\rm Dsat}$ enhancement. We also introduce a novel Melt-Enhanced Dopant diffusion and activation technique to form fully embedded $Si_{0.15}Ge_{0.85}$ S/D stressors in nanowire FETs, further boosting the channel strain and achieving $\sim$125% $I_{\rm Dsat}$ enhancement.**

***Index Terms*—Germanium stressors, silicon–germanium stressors, strained silicon nanowires.**

I. Introduction

NANOWIRE transistors have great potential for extending the silicon CMOS roadmap. Silicon nanowires fabricated using top–down approaches are of particular importance due to their direct compatibility with conventional CMOS process flow [1]–[5]. It is also well known that strain engineering techniques improve the performance of transistors very significantly by enhancing the carrier mobility in the transistor channel. Although several reports have shown the effectiveness of strain techniques on nanoscale multiple-gate transistors [6]–[10], the direct applicability of such techniques on nanowire transistors has yet to be demonstrated. Furthermore, the thin and narrow active areas of nanowire transistors pose immense integration challenges for conventional strain engineering techniques. One method of integrating SiGe source/drain (S/D) stressors with nanowire transistors was presented in [11], but a drawback associated with their integration scheme is the relatively large size of the S/D mesa. It may also be difficult to selectively employ such SiGe S/D stressors for p-channel devices only.

In this paper, we demonstrate that pure germanium stressors can be selectively grown in the S/D regions of nanowire transistors for significant performance enhancement. We further show that the Ge S/D stressors can be embedded by a novel melting technique which simultaneously also redistributes and activates dopants uniformly in the Ge film.

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T.-Y. Liow is with the Department of Electrical and Computer Engineering, National University of Singapore, Singapore 119260, and also with the Institute of Microelectronics, Agency for Science, Technology and Research (A*STAR), Singapore 117685.

K.-M. Tan and R. T. P. Lee are with the Department of Electrical and Computer Engineering, National University of Singapore, Singapore 119260.

M. Zhu was with the Department of Electrical and Computer Engineering, National University of Singapore, Singapore 119260. He is now with the Technology Development Department, Chartered Semiconductor Manufacturing, Singapore 738406.

B. L.-H. Tan is with the Institute of Microelectronics, Agency for Science, Technology and Research (A*STAR), Singapore 117685.

N. Balasubramanian was with the Institute of Microelectronics, Agency for Science, Technology and Research (A*STAR), Singapore 117685. He is now with Silterra, Kulim 09000, Malaysia.

Y.-C. Yeo is with the Department of Electrical and Computer Engineering, National University of Singapore, Singapore 119260, and also with the Agency for Science, Technology and Research (A*STAR), Singapore 117685 (e-mail: yeo@ieee.org; eleyeoyc@nus.edu.sg).

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II. Device Fabrication

$\langle 110\rangle$-oriented Π-gate nanowire p-FETs were fabricated on silicon-on-insulator (SOI) wafers with (100) surface orientation using a CMOS-compatible top–down process. The SOI wafers are p-type and have low doping concentrations of less than 2×10^{-14} cm^{-3}. The SOI wafers were thinned down using thermal oxidation followed by HF wet etching of the thermal oxide. The final SOI thickness was $\sim$10 nm. A low-temperature 30-nm-thick silicon oxide hardmask was then deposited on the wafers using a plasma-enhanced chemical vapor deposition (PECVD) system. A lithography of 248 nm was used to pattern lines down to about 120 nm. An optimized photoresist-trimming plasma process was then performed to trim the photoresist lines down to 50 nm. These patterns were then transferred to the oxide hardmask using a reactive ion etch (RIE) process. These patterns were further trimmed down using HF wet chemical etching, which is isotropic in nature. The patterned lines were then transferred to the underlying SOI using a highly selective RIE Si etching process, forming rectangular nanowires of about 30 nm wide and 8 nm tall. Both the plasma and the wet chemical trimming steps improve the line edge roughness of the line patterns in the process of reducing the linewidths. This is of particular importance for ensuring that the final Si nanowires have low line edge roughness, since the line edge roughness of the oxide hardmask will be transferred to the underlying SOI during the Si etch step. This method of forming Si nanowires is completely compatible with conventional CMOS processes and enables easy scalability of the nanowire dimensions. Furthermore, the topography across the entire wafer is kept to a minimum. This is beneficial for the lithographic definition of the gate over the nanowire, since linewidth changes can occur at regions with sudden and large topographical changes.

For nanowire FETs with fully depleted channels, employing intrinsically doped channels suppresses random dopant fluctuation effects and reduces variation. These benefits are reaped without significantly sacrificing short channel control. In view of this, the nanowire channels were intentionally left undoped.

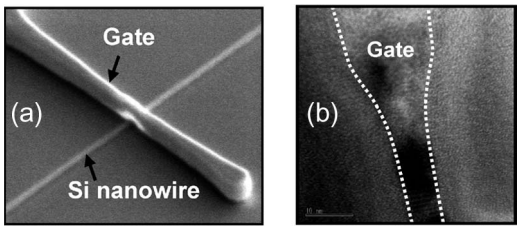

Fig. 1. (a) SEM image showing a nanowire device with a polysilicon gate running over it. The polysilicon gate is bottom tapered such that the gate is narrowest at the bottom. As the gate is extremely narrow at the bottom, it appears to be translucent. (b) Cross-sectional TEM image showing the bottom-tapered gate (dotted lines illustrate the gate/spacer boundary).

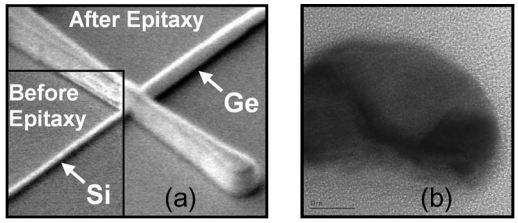

Fig. 2. (a) Composite SEM images depicting a nanowire FET before and after Ge epitaxy to form the raised Ge S/D regions. Excellent growth selectivity was achieved. Good surface morphology of the Ge film was also obtained. (b) Cross-sectional TEM image of a Si nanowire after epitaxially growing Ge. Defect density is lower than that obtained when growing Ge on wider Si structures.

A gate stack comprising thermally grown silicon oxide of 3- and 100-nm polysilicon was used. The polysilicon gate was implanted with boron, and rapid thermal anneal (RTA) was activated prior to gate definition. An oxide hardmask was also used for the gate. The gate definition step involved similar photoresist and hardmask trimming steps to those used in the fin definition process described earlier. The gate etching process was developed such that it produced bottom-tapered gates which were narrowest at the bottom, as shown in Fig. 1(a) and (b). This allows the physical gate length at the nanowire channel regions to be extremely small. Hence, the physical gate lengths are no longer limited by the linewidths of the hardmask lines, allowing the formation of gates down to 5 nm and below. However, as the processes are not optimized, an estimated gate length variation of around ± 5 nm is expected.

Source and drain extension implants of low dosages were performed after depositing a 10-nm-thick PECVD oxide liner, which has the benefit of reducing gate overlap. This improves the electrostatic control of the nanowire channel by the gate in the OFF-state [12]. Nitride spacers were then formed using a conventional spacer formation process. Due to the low S/D topography, a conservative spacer overetch was sufficient to remove the unwanted nitride spacers around the S/D regions while keeping the gate spacers intact.

Raised S/D regions comprising epitaxial Ge were grown on two device splits. Another device split without Ge S/D regions serves as the control. A low-temperature Ge epitaxy process in an ultrahigh vacuum chemical vapor deposition epitaxy reactor was used to selectively grow Ge films with good morphology in the S/D regions of the nanowire FETs. The growth process was carried out at a sufficiently low temperature of about 370 °C, which seems to exploit the properties of hydrogen as a surfactant [13]. This suppresses the Stranski–Krastanov growth mechanism [14], which would otherwise result in films with poor morphology. Fig. 2(a) shows a nanowire FET device before and after selective Ge epitaxial growth. There is a large lattice mismatch of 4.2% between Ge and Si. When Ge is epitaxially grown on Si, the large amount of lattice strain energy often results in the formation of defects at or near the interface [15]. However, it has been shown that the effect of substrate compliance in very thin films can reduce the relaxation of strain via the formation dislocations [16], [17]. An experimental study has also shown that it is possible to relax the strain in Ge nanostressors on very thin SOI films without the formation of any crystalline defects [18]. Fig. 2(b) shows the cross-sectional TEM image of a Si nanowire after epitaxially growing Ge. Due to the small dimensions of the nanowire, it is difficult to accurately extract the absolute defect density. Nevertheless, the defect density was observed to be lower than that obtained when growing Ge on wider structures in our experiments, which concurs with the observations in [16] and [17]. We have also experimentally demonstrated that Ge S/D stressors can be integrated with ultrathin body FETs for inducing beneficial compressive channel strain. The raised Ge S/D regions also have the added benefit of reducing the S/D series resistances [19]. The p-type dopant used for S/D formation was boron. For one of the device splits with Ge S/D regions, a BF_2^+ implant targeted at the surface of the S/D regions was performed. For the other device split with Ge S/D regions, the B^+ implant was targeted for uniform dopant distribution in the raised S/D regions. All devices were capped with a SiO_2 liner prior to the RTA activation of the dopants. Both the Si S/D control (*Si S/D*) and the Ge S/D split [*Ge S/D (not melted)*] which received the uniform B^+ implant were activated at 900 °C for 10 s. For the Ge S/D split [*Ge S/D (Melt-Enhanced Dopant, MeltED)*] which received the surface BF_2^+ implant, a 950-°C spike anneal was used to activate the dopants. During the spike anneal, the Ge S/D regions are melted, enabling the uniform distribution and activation of the dopants. This process will be further elaborated on in the next section. For the control devices with Si S/D regions, nickel silicidation was performed after S/D activation to reduce S/D series resistances. Germanidation of the devices with Ge S/D regions was not performed.

III. Results and Discussion

A. MeltED Diffusion and Activation

In the previous section, it was described that one of the device splits with Ge S/D regions underwent an RTA spike anneal at 950 °C. Since pure Ge has a melting point of 938 °C, the Ge S/D regions will melt as the temperature of the wafer ramps beyond its melting point. Upon cooling, the Ge S/D region rapidly recrystallizes, using the underlying or adjoining Si region as a seed for crystallization. In this section, the rationale behind this melting anneal is examined.

Ge films of two thicknesses were grown on SOI sheet resistance test structures. Low-energy BF_2^+ implants (5 keV, 2×10^{15} cm^{-2}) were performed, targeting the boron atoms at the surface of the Ge films. After capping with a SiO_2 liner, the wafers were RTA spike annealed at 950 °C. Fig. 3 shows the

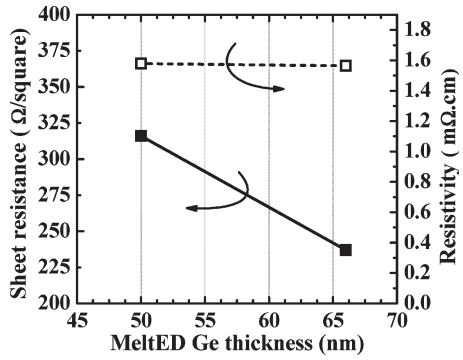

Fig. 3. Sheet resistance and resistivity values for two Ge films of different thicknesses annealed under the same conditions. Melting the Ge films causes the dopants to diffuse quickly and uniformly throughout the Ge films, resulting in nearly identical resistivity values.

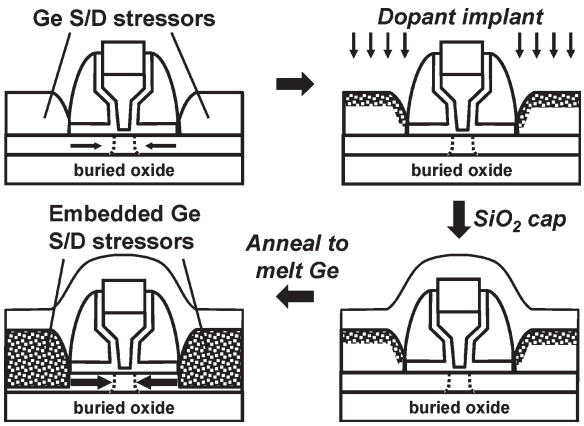

Fig. 4. Cross-sectional schematic showing the MeltED diffusion and activation technique applied to a transistor with Ge S/D regions. After shallow S/D implant and SiO_2 capping, a 950-°C spike anneal melts the Ge-rich S/D regions. This achieves these key objectives: Interface interdiffusion *embeds* the Ge stressor; dopants diffuse and redistribute uniformly and are substitutionally incorporated as Ge recrystallizes.

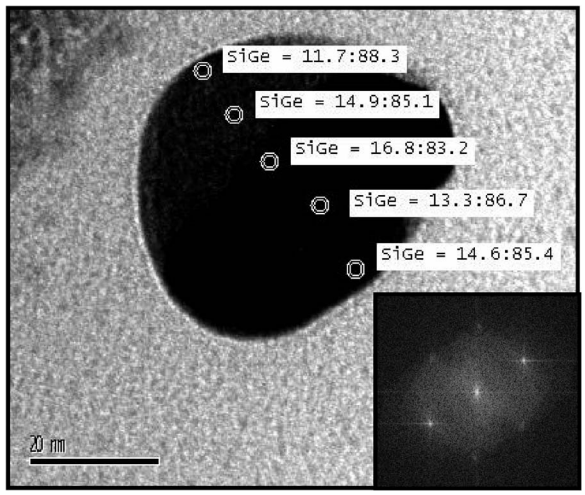

Fig. 5. Cross-sectional TEM of *MeltED* Ge nanowire S/D regions. The smoothening of the surface facets and the corresponding cross-sectional change in shape of the S/D region toward a more spherical shape are attributed to minute viscous flow of the encapsulating SiO_2 during the Ge-melting anneal process. EDS analysis shows uniform ∼85% Ge concentration from top to bottom. (Inset) The reciprocal space diffractogram shows single crystallinity.

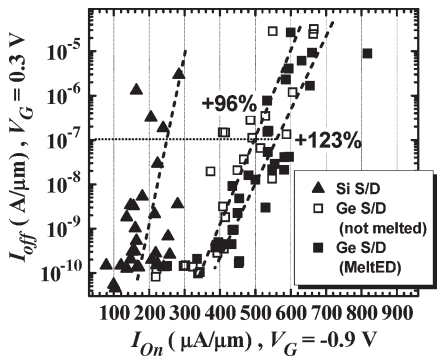

Fig. 6. At an $I_{\rm Off}$ of 1×10^{-7} A/μm, $I_{\rm On}$ enhancements of 96% and 123% are obtained for *Ge S/D (not melted)* and *Ge S/D (MeltED)*, respectively (the dashed lines serve as visual guides).

sheet resistance and resistivity values obtained. The resistivity values of the two relatively thick films were nearly identical, in spite of the thickness differences, and the dopants were only targeted at the surface of the films. These results indicate that the melting of the Ge films causes the uniform distribution and activation of boron throughout the films. This can be attributed to the much higher diffusivity of dopants in liquid-phase Ge compared with that in solid-phase Ge.

This gives us a viable method for doping structures (such as FinFETs or gate-all-around nanowire FETs) which may have S/D topographies that present doping challenges when conventional ion implantation and annealing are used. Fig. 4 shows the schematic representation of the Ge S/D doping and embedding scheme using the MeltED diffusion and activation technique. Fig. 5 shows the cross-sectional TEM of the Ge S/D regions of a nanowire transistor after the MeltED process. Energy dispersive X-ray spectrometry (EDS) indicates that the Ge concentration is almost uniform from the top to the bottom. It is evident that the MeltED process also causes intermixing of the Si and Ge at the heterointerface. The EDS results suggest that, in nanowire S/D regions, the small volume of Si completely dissolves in the large volume of molten Ge surrounding it during the anneal process. Si and Ge are completely miscible in all percentages. Upon cooling, the uniform SiGe alloy recrystallizes, taking the Si extension regions underneath the gate spacers as the seed for recrystallization. The single crystallinity of the recrystallized SiGe is confirmed by examining the reciprocal space diffractogram (inset of Fig. 5) of an HRTEM lattice image.

B. Electrical Characterization of Nanowire FETs

Fig. 6 shows the $I_{\rm Off}$–$I_{\rm On}$ plot of the three device splits (current values are normalized by the nanowire width of 30 nm). At a fixed $I_{\rm Off}$ of 1×10^{-7} A/μm, a very significant $I_{\rm On}$ enhancement of 96% is obtained by the incorporation of Ge S/D regions in the nanowire devices and conventional non-melting S/D activation annealing [*Ge S/D (not melted)*]. The combination of the Ge S/D regions and the MeltED technique for S/D activation annealing [*Ge S/D (MeltED)*] results in an $I_{\rm On}$ enhancement of 123%. The large enhancements in drive current performance are attributed partially to the reduction of the diffusion resistance component of the total S/D series resistances and to the beneficial compressive stress induced

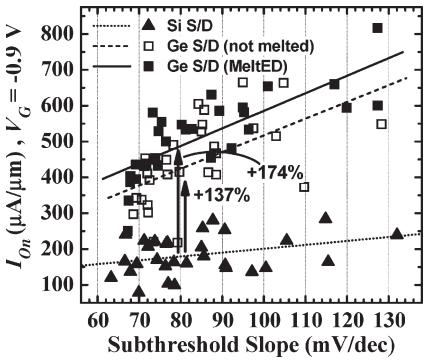

Fig. 7. At a fixed subthreshold slope of 80 mV/dec, $I_{\rm On}$ enhancements of 137% and 174% are obtained for *Ge S/D (not melted)* and *Ge S/D (MeltED)*, respectively. Linear fitting was performed on the data points to generate the trendlines. An increasing trend of $I_{\rm On}$ enhancement is observed for increasing values of subthreshold slope.

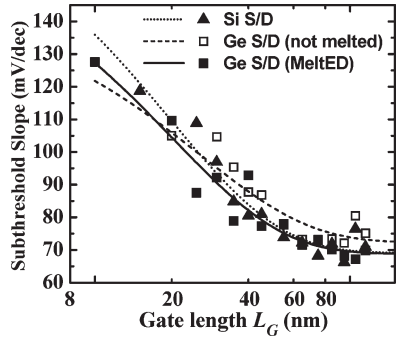

Fig. 8. Dependence of subthreshold slope on the physical gate length. Fitted trendlines show comparable subthreshold slope dependence for the three device splits. Data values of devices with 5-nm gate lengths were omitted due to the relatively large gate length variation compared with the absolute gate length.

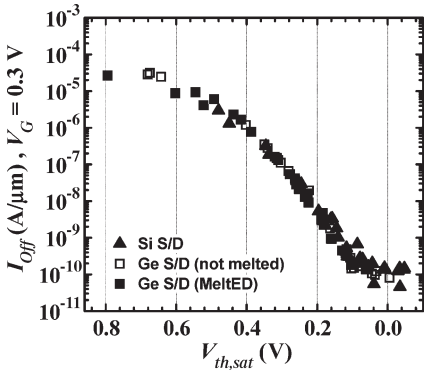

Fig. 9. Similar dependence of $I_{\rm Off}$ on $V_{\rm th,sat}$ illustrates the good matching of short channel control in all three device splits.

by the Ge S/D stressors. As the nanowire channels are oriented in the $\langle 110 \rangle$ direction, the induced uniaxial compressive stress has a pronounced enhancing effect on the hole mobility. A similar enhancement effect has also been reported in nanoscale multiple-gate transistors with embedded $Si_{0.8}Ge_{0.2}$ S/D stressors, albeit with a much lower enhancement percentage of 25% [8]. Uniaxial compressive stress reduces the conductivity hole effective mass. This is attributed to lifting of degeneracy in the valence band, as well as subband shape deformation and shifting [20], [21]. However, the Ge content in the S/D regions of our devices is much higher, which possibly induces much higher amounts of compressive lattice strain in the channel regions. For the *Ge S/D (MeltED)* devices, the Ge-rich S/D regions of the nanowire FETs are fully embedded as a result of the melting process. Previously, TCAD simulations have revealed enhanced channel stress effects due to SiGe stressor embedding in the S/D regions of FinFETs [10]. A similar stress enhancing effect is expected for these nanowire FETs by embedding the stressors.

Fig. 7 shows the dependence of $I_{\rm On}$ on the subthreshold slope. At a fixed subthreshold slope of 80 mV/dec, 137% and 174% $I_{\rm On}$ enhancements were obtained for the *Ge S/D (not melted)* and *Ge S/D (MeltED)* devices, respectively. The enhancement figures are larger than that obtained from the $I_{\rm Off}$–$I_{\rm On}$ plot due to threshold voltage shifts. Since subthreshold slope is an indication of short channel control, which is, in turn, a reflection of the effective channel length, Fig. 7 essentially shows the dependence of $I_{\rm On}$ on the effective channel length (and physical gate length). It was also observed that the $I_{\rm On}$ enhancement increases with increasing subthreshold slope values (physical gate length). This trend concurs with mechanical stress simulation results on the local nature of the S/D stressors from TCAD simulations. This is a simple concept to understand, since reducing the channel length of the device also reduces the interstressor spacing. The reduction in interstressor spacing causes an increase in the average channel stress and will become particularly pronounced when the influences of the source and the drain stressors overlap. This trend of increasing enhancement as gate lengths are scaled down is important for maintaining the high performance benefits in extremely scaled nanowire FETs.

The short channel matching of the devices is evaluated using Figs. 8 and 9. Fig. 8 shows the dependence of subthreshold slope on the physical gate length. The fitted lines serve as visual guides which indicate that the Ge S/D devices do not suffer from any significant degradation in short channel control. Even at physical gate lengths of 20 nm, subthreshold slope values of 105–110 mV/dec are obtained, which shows the highly effective electrostatic control of the fully depleted nanowire FETs in spite of the relative thick gate oxide (3 nm). Fig. 9 shows the dependence of $I_{\rm Off}$ on the saturation threshold voltage $V_{\rm th,sat}$. The data points for all device splits lie on a curve with good overlap, giving further evidence for the good short channel matching of the devices. Although the *Ge S/D (MeltED)* devices underwent a higher temperature S/D activation anneal at 950 °C, there was no degradation of the short channel effects. This can perhaps be attributed to the fact that the temperature of 950 °C during the activation anneal was still conservative. In devices utilizing the MeltED technique for S/D activation, higher temperatures are not necessary from the dopant activation point of view, since the Ge melts at 938 °C. However, the degree of embedding is likely to be dependent on the thermal budget of the annealing, since solid-state interdiffusion of Si and Ge is dependent on the thermal budget.

Fig. 10 shows the cumulative distributions of (a) the subthreshold slope values and (b) the linear region threshold voltage $V_{\rm th,lin}$. The data come from the same sets of devices used in the $I_{\rm Off}$–$I_{\rm On}$ (Fig. 6) and $I_{\rm On}$–SS (Fig. 7) statistical plots. The

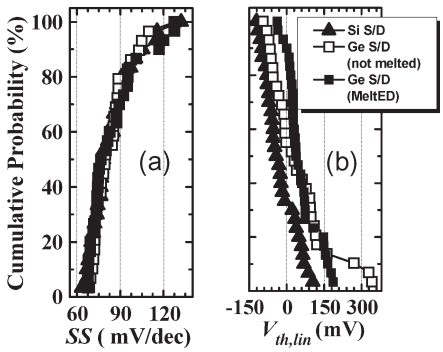

Fig. 10. Cumulative distributions of (a) subthreshold slope (SS) and (b) $V_{\rm th,lin}$. All three device splits have comparable subthreshold slope distributions. $V_{\rm th,lin}$ increases with the incorporation of Ge S/D regions. *Ge S/D (MeltED)* devices have better $V_{\rm th,lin}$ variability than *Ge S/D (not melted)* devices.

TABLE I
THRESHOLD VOLTAGE PROPERTIES

Device Split	Median (mV) $2^{\rm nd}$ & $3^{\rm rd}$ quartiles only	σ (mV) $2^{\rm nd}$ & $3^{\rm rd}$ quartiles only	σ (mV) All 4 quartiles
Si S/D	- 42	32	65
Ge S/D (not melted)	25	46	116
Ge S/D (MeltED)	38	20	62

subthreshold slope distributions show a range of values from ∼60 to ∼130 mV/dec as devices of a range of physical gate lengths were included. Nevertheless, the cumulative distributions clearly show that the subthreshold slopes of the devices are closely matched. For these same sets of devices, $V_{\rm th,lin}$ was extracted using the method involving maximum transconductance and tangential linear extrapolation from the I_D–V_G transfer curve. The $V_{\rm th,lin}$ distributions show that threshold voltage shifts positively with the incorporation of Ge S/D regions. The distribution for the Ge S/D (not melted) devices includes several outliers. For greater accuracy, we extracted median values of $V_{\rm th,lin}$ from data sets of each device split which only includes data points from the second and third quartiles (Table I). There is a median positive threshold voltage shift of about 67 and 80 mV in Ge S/D (not melted) and Ge S/D (MeltED) devices, respectively. This can possibly be explained by the bandgap narrowing effects of uniaxial compressive stress on the strained silicon channel [22]. It is noted that the threshold voltage variability of the *Ge S/D (MeltED)* devices is improved over that of the *Ge S/D (not melted)* devices, as can be qualitatively observed from the values of the standard deviation σ (note that emphasis should not be placed on the absolute accuracy of the values since the sample size is limited). This is a further benefit of the MeltED technique for S/D activation since it reduces the threshold voltage variability, and hence the device-to-device mismatch.

Next, the effects of the MeltED technique for S/D activation on the performance of the Ge S/D devices are evaluated in greater detail. The transfer characteristics of the *Ge S/D (MeltED)* and *Ge S/D (not melted)* devices ($L_G = 25$ nm) are shown in Fig. 11. The comparable subthreshold slope and DIBL of the devices indicate that they indeed have comparable effective channel lengths. Fig. 12 shows the I_D–V_D family of

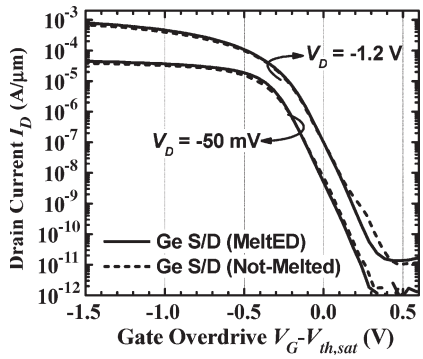

Fig. 11. Transfer characteristics of the *Ge S/D (MeltED)* and *Ge S/D (not melted)* devices. Comparable subthreshold slope and DIBL are observed.

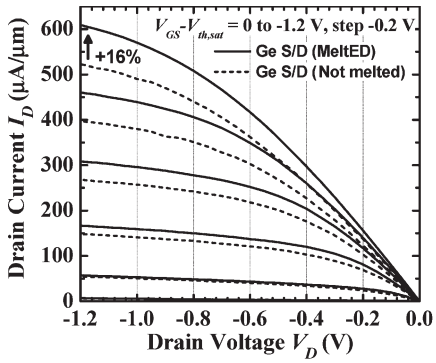

Fig. 12. I_D–V_D family of curves shows 16% $I_{\rm Dsat}$ enhancement for the *Ge S/D (MeltED)* device over the *Ge S/D (not melted)* device.

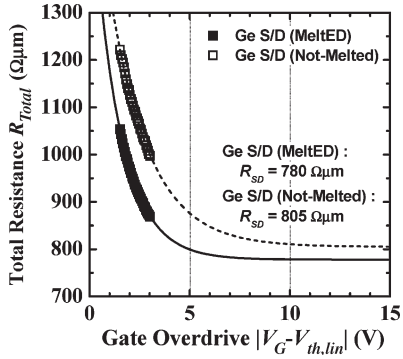

Fig. 13. Total resistance against gate overdrive voltage. S/D series resistance estimations using a first-order exponential curve fitting of the data points show that the series resistances are comparable.

curves for the same devices. A further $I_{\rm Dsat}$ enhancement of 16% is obtained for the *Ge S/D (MeltED)* device. The S/D series resistances $R_{\rm SD}$ were extracted using the total resistance and extrapolation method reported in [23] (Fig. 13). $R_{\rm SD}$ values of both the devices were estimated to be around 800 $\Omega \cdot \mu$m. Since the $R_{\rm SD}$ values are comparable, the additional $I_{\rm Dsat}$ enhancement is likely to have come from increased strain effects as a result of embedding the S/D stressors. Embedding the S/D stressors has the effect of bringing the stressors in closer proximity to the channel and extends the influence of the S/D stressors. For planar Si MOSFETs, this is typically accomplished by performing an S/D recess etch prior to SiGe epitaxy. A similar technique cannot be applied to nanowire transistors due to the limited S/D thickness, which makes it

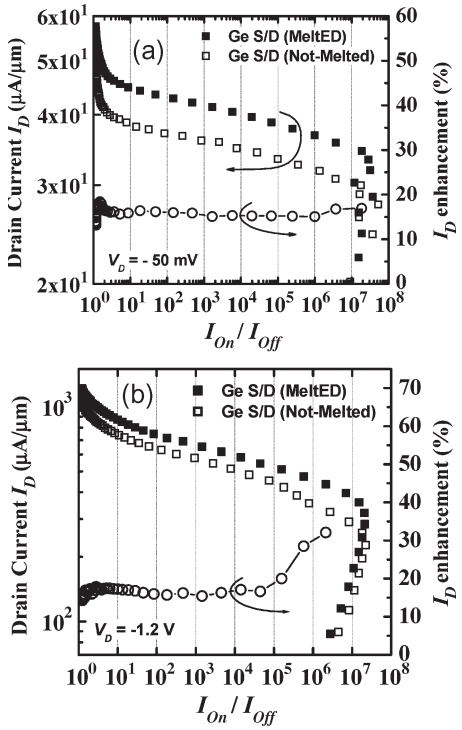

Fig. 14. By assuming control of the threshold voltage and sweeping through the I_D–V_G curves using a 1.2-V window, the $I_{\rm On}$ for a given $I_{\rm On}/I_{\rm Off}$ ratio was derived for (a) $V_D = -50$ mV and (b) $V_D = -1.2$ V. The right axis of each graph represents the $I_{\rm On}$ enhancement at each value of $I_{\rm On}/I_{\rm Off}$.

nearly impossible to perform the recess etch without completely etching the S/D regions away. Although embedded SiGe S/D stressors have been demonstrated in [11] with Si nanowire transistors, the structure that they employed comprises relatively large S/D mesa structures which have nanowires connecting the mesas. Such structures may not be utilized effectively in density-critical applications such as SRAM. It is important to differentiate that the MeltED technique offers a simple way of embedding stressors with very high Ge content for maximum lattice strain coupling, even for nanowire devices with very narrow and thin S/D regions.

High-performance transistors and low-operating power transistors have different requirements on the ON- and OFF-state drain currents. Fig. 14 shows a device drive current performance figure of merit which elucidates the benefits of the MeltED technique. By assuming control of the threshold voltage and sweeping through the I_D–V_G curves using a 1.2-V window, the $I_{\rm On}$ for a given $I_{\rm On}/I_{\rm Off}$ ratio was derived for both the linear and saturation regions. This is similar to the method of benchmarking proposed in [24], except that $I_{\rm On}$ instead of $C_G V_{\rm DD}/I_{\rm On}$ is plotted on the left axis. In [24], the benchmarking was performed for devices with altogether different device architectures. In this case, since the devices have the same dimensions, plotting $I_{\rm On}$ instead of $C_G V_{\rm DD}/I_{\rm On}$ is already sufficient as $C_G V_{\rm DD}$ for both devices are identical. The right axis of each graph represents the $I_{\rm On}$ enhancement at each value of $I_{\rm On}/I_{\rm Off}$. It is clear that the I_D enhancement can be obtained in both the linear and saturation regions and averages at about 16%. Furthermore, the I_D enhancement is maintained for a large range of $I_{\rm On}/I_{\rm Off}$ values. This means that the performance benefits are maintained, regardless of the threshold voltage that is selected for device operation.

IV. Conclusion

A novel Ge S/D stressor has been proposed and demonstrated for p-channel nanowire transistors. By activating the dopants using the MeltED technique, the S/D stressors can also be simultaneously embedded for further strain-induced enhancement. This technique also enables uniform doping of structures with topography and can be extended to other 3-D device structures. The experimental demonstration of the applicability of the Ge S/D technology to extremely scaled nanowire transistors illustrates its potential for extending the performance of future nanowire transistor circuits.

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Tsung-Yang Liow (S'06) received the B.Eng. degree in electrical and computer engineering from the National University of Singapore (NUS), Singapore, in 2003, where he is currently working toward the Ph.D. degree in electrical and computer engineering.

He is also currently with the Institute of Microelectronics, Agency for Science, Technology and Research, Singapore. His research interests include the design and fabrication of sub-10-nm multiple-gate FDSOI and nanowire transistors, as well as performance enhancement techniques such as channel strain engineering.

Mr. Liow was the recipient of the NUS Faculty of Engineering Innovation Award in 2003 and the 2004–2007 Agency for Science, Technology and Research Graduate Scholarship.

Kian-Ming Tan received the B.Eng. (with first class honors) and M.Eng. degrees in electrical engineering from the National University of Singapore, Singapore, where he is currently working toward the Ph.D. degree in electrical engineering in the Department of Electrical and Computer Engineering.

His research interests include plasma etching technologies, strained Si device, and fabrication of multiple-gate transistor.

Rinus Tek Po Lee (S'06) received the B.S. and M.S. degrees in electrical engineering and applied physics from the National University of Singapore, Singapore, where he is currently working toward the Ph.D. degree in electrical engineering in the Department of Electrical and Computer Engineering with Professor Yee-Chia Yeo, with a research focusing on parasitic resistance scaling in multiple-gate transistors.

He was with the Agency of Science Technology and Research, Institute of Materials Research and Engineering, Singapore, where he worked on the development of advanced process technologies for contact metallization. Since 2005, he has been with the Silicon Nano Device Laboratory, NUS. His current research interests include device physics and process technology integration for the multiple-gate transistor architecture.

Mr. Lee was the recipient of the Marubun Research Promotion Foundation Grant at the 2006 Solid State Devices and Materials Conference, Yokohama, and the Gold Award at the 2007 Taiwan Semiconductor Manufacturing Company Outstanding Student Research Award.

Ming Zhu received the B.S. degree in physics from Wuhan University, Wuhan, China, in 2000 and the Ph.D. degree in microelectronics from Shanghai Institute of Microsystem and Information Technology, Chinese Academy of Sciences, Shanghai, China, in 2005.

From 2005 to 2008, he was a Research Fellow with the Silicon Nano Device Laboratory, National University of Singapore, Singapore, where he worked on high mobility transistor fabrication. He is currently with the Technology Development Department, Chartered Semiconductor Manufacturing, Singapore.

Ben Lian-Huat Tan received the M.Sc. degree in material physics and nanotechnology from Linköping Institute of Technology, Linköping, Sweden, in 2005.

He is currently with the Institute of Microelectronics, Agency for Science, Technology and Research, Singapore, Singapore, where he is trained on both surface and structural failure analysis techniques. Currently, his main research interests include package failure analysis and characterization of semiconductor materials using TEM and FIB.

N. Balasubramanian received the Ph.D. degree in physics from the Indian Institute of Technology, Madras, India, in 1990.

He was an Engineering Section Manager for CMOS front-end technologies with Chartered Semiconductor Manufacturing Ltd., Singapore. In 1998, he joined the Institute of Microelectronics, Singapore, where he held various positions as Member of Technical Staff, Senior Technical Manager, and Lab Director for semiconductor process technology and as the Director for Bioelectronics and BioMEMS Program. Since April 2008, he has been a Fellow for technology development with Silterra, Kulim, Malaysia. He has more than 17 years of experience in the IC industry under different capacities in research and development, process module operations, technology development, and program management. He is the author or coauthor of more than 90 publications in peer-reviewed journals on research topics covering Si nanowire nanoelectronics and biosensor devices, CMOS devices, CMOS front-end technologies, and heterogeneous integration. He is also the holder of eight U.S. patents.

Yee-Chia Yeo received the B.Eng. (first class honors) and M.Eng. degrees in electrical engineering from the National University of Singapore (NUS), Singapore, Singapore, and the M.S. and Ph.D. degrees in electrical engineering and computer sciences from the University of California, Berkeley.

He had worked on optoelectronic devices with the British Telecommunications Laboratories, U.K., and on CMOS technology at Berkeley. From 2001 to 2003, he worked on exploratory transistor technologies with the Taiwan Semiconductor Manufacturing Company (TSMC). He is currently an Assistant Professor with the Department of Electrical and Computer Engineering, NUS, and a Research Program Manager with the Agency for Science, Technology and Research (A*STAR), Singapore. He leads research efforts in strained transistor technologies and sub-30-nm device work at NUS and manages a Nanoelectronics Research Program at A*STAR. He has authored or coauthored more than 270 journal and conference papers, and a book chapter. He is the holder of 72 U.S. patents.

Dr. Yeo served on the IEDM Sub-Committee on CMOS Devices from 2005 to 2006. He was the recipient of the 1995 IEE Prize from the Institution of Electrical Engineers, U.K., the 1996 Lee Kuan Yew Gold Medal, the 1996 Institution of Engineers Singapore Gold Medal, the 1997–2001 NUS Overseas Graduate Scholarship Award, the 2001 IEEE Electron Devices Society Graduate Student Fellowship Award, the 2002 IEEE Paul Rappaport Award, and 2003 TSMC Invention Awards. In 2006, he received the Singapore Young Scientist Award and the Singapore Youth Award in Science and Technology. In 2008, he received a National Research Foundation Fellowship and an NUS Young Researcher Award.