NATIONAL UNIVERSITY *of* SINGAPORE

Department of Electrical and Computer Engineering

EE2021 – Devices and Circuits

Tutorial 4 Solutions

<u>Homework 3:</u>

Homework 3 is <u>Question 2 and Question 6</u> of Tutorial 4. You have to submit the homework assignment in hardcopy in class on <u>Wednesday 1 April 2015</u>.

Unless otherwise stated, you may use the tables of the amplifier configurations and equivalent resistances in your lecture notes in your solutions to the questions.

Q1. Draw the pull down network (PDN) and pull up network (PUN) of the following logic function:

$$Y = \overline{\{[(A.B) + C].D\} + (E.F)}\ .$$

Determine also the best case propagation delay of the above PUN, $t_{pLH,best}$, in terms of that of an inverter, $t_{pLH,inv}$. All NMOS and PMOS transistors in the above logic networks and the inverter have sizing of $(W/L)_n = n$ and $(W/L)_p = p$, respectively.

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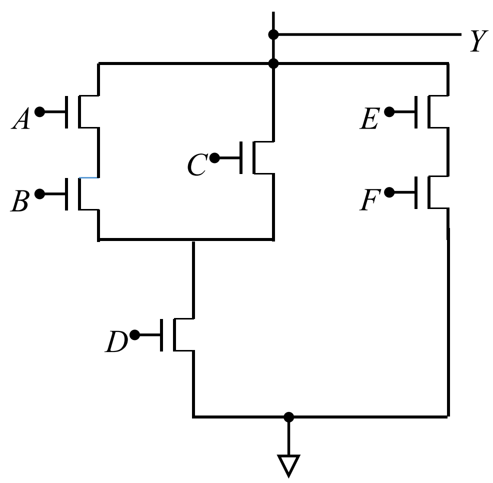
1. $Y = \overline{\{[(A.B) + C].D\} + (E.F)}$
$\bar{Y} = \{[(A.B) + C].D\} + (E.F)$

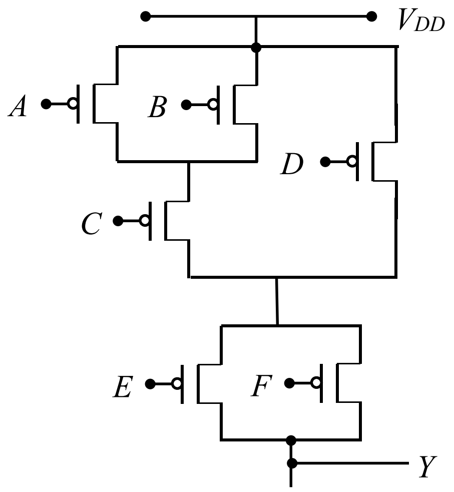
PDN



Based on PDN, construct PUN using duality, or

$$Y = \overline{\{[(A.B)+C].D\}+(E.F)} = \overline{\{[(A.B)+C].D\}}\,.\,\overline{(E.F)}$$
$$= \{\overline{[(A.B)+C]}+\bar{D}\}.(\bar{E}+\bar{F}) = \{[\overline{(A.B)}\,.\,\bar{C}]+\bar{D}\}.(\bar{E}+\bar{F})$$
$$= \{[(\bar{A}+\bar{B})\,.\bar{C}]+\bar{D}\}.(\bar{E}+\bar{F})$$

PUN



Best case equivalent sizing of PUN (i.e., with all PMOS transistors turned on)

$$(\tfrac{W}{L})_{eq,(\bar{A}+\bar{B})} = 2p$$
$$(\tfrac{W}{L})_{eq,[(\bar{A}+\bar{B})\,.\,\bar{C}]} = \left[\frac{1}{2p}+\frac{1}{p}\right]^{-1} = \frac{2}{3}p$$
$$(\tfrac{W}{L})_{eq,\{[(\bar{A}.+\bar{B})\,.\,\bar{C}]+\bar{D}\}} = \frac{2}{3}p+p = \frac{5}{3}p$$
$$(\tfrac{W}{L})_{eq,\{[(\bar{A}.+\bar{B})\,.\,\bar{C}]+\bar{D}\}\,.\,(\bar{F}+\bar{G})} = \left[\frac{1}{\frac{5}{3}p}+\frac{1}{2p}\right]^{-1} = \frac{10}{11}p$$
$$t_{pLH,best} = \frac{11}{10}t_{pLH,inv}$$

Q2. (i) Design the pull down network of the following logic function :

$$Y = \overline{(A+B)\cdot C\cdot(D+E)}.$$

[5 marks]

(ii) Assume that all the transistors have a sizing of $(W/L)_{min}$. Compare the worst case t_{pHL} of the logic circuit with the t_{pHL} of an inverter with the same transistor sizing.

[4 marks]

(iii) Suggest one way of sizing the transistors of the logic circuit such that its worst case t_{pHL} equals the t_{pHL} of an inverter with a sizing of $(W/L)_{min}$.

[3 marks]

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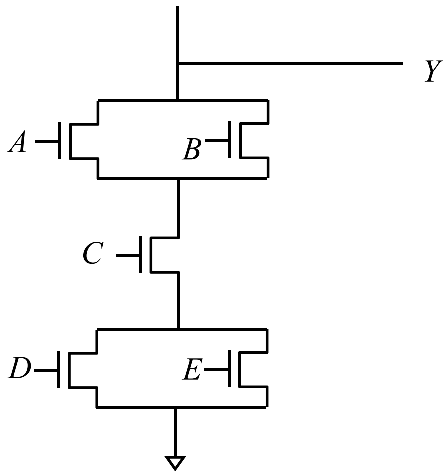
2. (i)



[5 marks]

(ii) $$\left(\frac{W}{L}\right)_{eq,logic} = \left[\left(\frac{W}{L}\right)_{min,A}^{-1} + \left(\frac{W}{L}\right)_{min,C}^{-1} + \left(\frac{W}{L}\right)_{min,D}^{-1}\right]^{-1} = \frac{1}{3}\left(\frac{W}{L}\right)_{min}$$ [2 marks]

$$\frac{t_{pHL,\log ic}}{t_{pHL,inverter}} = \frac{\left(\frac{W}{L}\right)_{\min}}{\frac{1}{3}\left(\frac{W}{L}\right)_{\min}} = 3$$ [2 marks]

(iii) Make the sizing of each of the transistors in the logic circuit equal to $3(W/L)_{min}$.

[3 marks]

Q3. Figure Q3 shows a pull-down network (PDN) for a logic function Y.

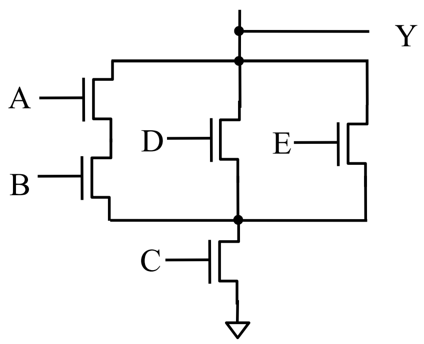


Fig. Q3

(i) Express Y in terms of A, B, C, D and E.

(ii) Draw the pull-up network (PUN) corresponding to the PDN in Fig. Q3.

(iii) All NMOS and PMOS transistors in the above logic circuit have a sizing of $(W/L)_{min}$. We shall compare the dynamic performance of the logic circuit with respect to a symmetric inverter where the sizing of NMOS transistor, $(W/L)_{NMOS} = (W/L)_{min}$, and the sizing of PMOS transistor, $(W/L)_{PMOS} = (\mu_n/\mu_p)(W/L)_{NMOS} = 2.5(W/L)_{min}$.

How many times is t_{PHL} of the above logic circuit compared to that of the symmetric inverter? Give the best and worst case values.

(iv) Repeat the calculations in part (iii) for t_{PLH} of the above logic circuit.

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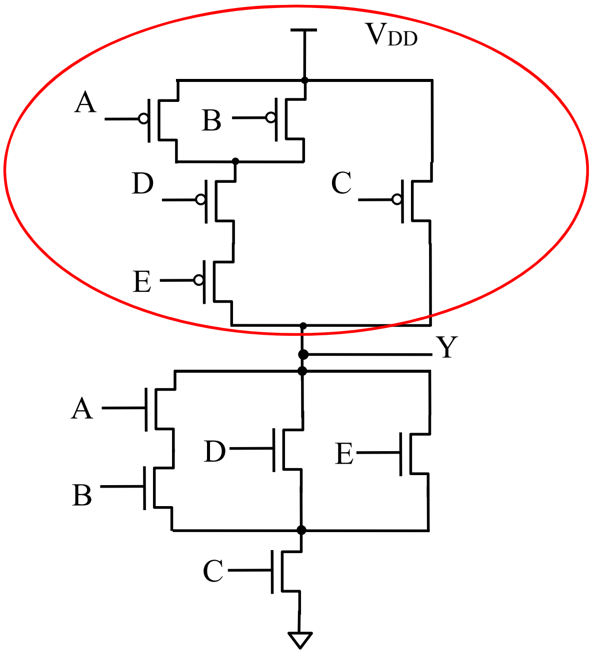
3. (i) $\overline{\mathrm{Y}} = [(\mathrm{A.B}) + \mathrm{D} + \mathrm{E}].\mathrm{C}$ or $\mathrm{Y} = \overline{[(\mathrm{A.B}) + \mathrm{D} + \mathrm{E}].\mathrm{C}}$

(ii) PUN



(iii) **Best case t_{PHL}, all NMOS transistors in PDN turn on -**

For (A.B): $\left(\frac{W}{L}\right)_{eq,AB} = \left[\left(\frac{W}{L}\right)_{min}^{-1} + \left(\frac{W}{L}\right)_{min}^{-1}\right]^{-1} = \frac{1}{2}\left(\frac{W}{L}\right)_{min}$

For [(A.B) + D + E]: $\left(\frac{W}{L}\right)_{eq,ABDE} = \left(\frac{W}{L}\right)_{eq,AB} + \left(\frac{W}{L}\right)_{min} + \left(\frac{W}{L}\right)_{min} = \frac{5}{2}\left(\frac{W}{L}\right)_{min}$

For [(A.B) + D + E].C: $\left(\frac{W}{L}\right)_{eq} = \left[\left(\frac{W}{L}\right)_{eq,ABDE}^{-1} + \left(\frac{W}{L}\right)_{min}^{-1}\right]^{-1} = \frac{5}{7}\left(\frac{W}{L}\right)_{min}$

$$\frac{t_{PHL,cct}}{t_{PHL,inv}} = \frac{\left(\frac{W}{L}\right)_{NMOS}}{\frac{5}{7}\left(\frac{W}{L}\right)_{min}} = \frac{\left(\frac{W}{L}\right)_{min}}{\frac{5}{7}\left(\frac{W}{L}\right)_{min}} = 1.4$$

Worst case t_{PHL}, only A, B and C NMOS transistors in PDN turn on –

$$\left(\frac{W}{L}\right)_{eq} = \left[\left(\frac{W}{L}\right)_{min}^{-1} + \left(\frac{W}{L}\right)_{min}^{-1} + \left(\frac{W}{L}\right)_{min}^{-1}\right]^{-1} = \frac{1}{3}\left(\frac{W}{L}\right)_{min}$$

$$\frac{t_{PHL,cct}}{t_{PHL,inv}} = \frac{\left(\frac{W}{L}\right)_{NMOS}}{\frac{1}{3}\left(\frac{W}{L}\right)_{min}} = \frac{\left(\frac{W}{L}\right)_{min}}{\frac{1}{3}\left(\frac{W}{L}\right)_{min}} = 3$$

(iv) **Best case t_{PLH}, all PMOS transistors in PUN turn on** -

For (A+B): $\left(\frac{W}{L}\right)_{eq,AB} = \left(\frac{W}{L}\right)_{min} + \left(\frac{W}{L}\right)_{min} = 2\left(\frac{W}{L}\right)_{min}$

For [(A+B).D.E]: $\left(\frac{W}{L}\right)_{eq,ABDE} = \left[\left(\frac{W}{L}\right)_{eq,AB}^{-1} + \left(\frac{W}{L}\right)_{min}^{-1} + \left(\frac{W}{L}\right)_{min}^{-1}\right]^{-1} = \frac{2}{5}\left(\frac{W}{L}\right)_{min}$

For [(A+B).D.E]+C: $\left(\frac{W}{L}\right)_{eq} = \left(\frac{W}{L}\right)_{eq,ABDE} + \left(\frac{W}{L}\right)_{min} = \frac{7}{5}\left(\frac{W}{L}\right)_{min}$

$$\frac{t_{PLH,cct}}{t_{PLH,inv}} = \frac{\left(\frac{W}{L}\right)_{PMOS}}{\frac{7}{5}\left(\frac{W}{L}\right)_{min}} = \frac{2.5\left(\frac{W}{L}\right)_{min}}{\frac{7}{5}\left(\frac{W}{L}\right)_{min}} = 1.79$$

Worst case t_{PLH}, only A (or B), D and E PMOS transistors in PUN turn on –

$$\left(\frac{W}{L}\right)_{eq} = \left[\left(\frac{W}{L}\right)_{min}^{-1} + \left(\frac{W}{L}\right)_{min}^{-1} + \left(\frac{W}{L}\right)_{min}^{-1}\right]^{-1} = \frac{1}{3}\left(\frac{W}{L}\right)_{min}$$

$$\frac{t_{PHL,cct}}{t_{PHL,inv}} = \frac{\left(\frac{W}{L}\right)_{PMOS}}{\frac{1}{3}\left(\frac{W}{L}\right)_{min}} = \frac{2.5\left(\frac{W}{L}\right)_{min}}{\frac{1}{3}\left(\frac{W}{L}\right)_{min}} = 7.5$$

Q4. Assume that the AC small signal parameters of the BJTs are $g_{m,Qi}$, $r_{\pi,Qi}$, $r_{o,Qi}$, and the AC small signal parameters of the MOSFETs are $g_{m,Mj}$, $g_{mb,Mj}$, $r_{i,Mj}$, $r_{o,Mj}$, where i (i = 1, 2) and j (j = 1, 2, 3) are the corresponding device indices. Using the equivalent resistance tables in your lecture notes, write down the expressions for the small signal AC equivalent resistances, R_{x1}, R_{x2} and R_{x3} in the circuit in Fig. Q4.

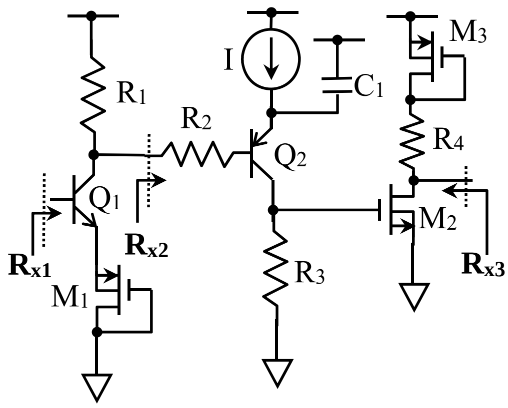


Fig. Q4

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4. $R_{x1} = r_{\pi,Q1}\left(1 + g_{m,Q1}\frac{1}{g_{m,M1}}\right)$;

$R_{x2} = R_2 + r_{\pi,Q2}$;

$R_{x3} = r_{o,M2}//\left(R_4 + \frac{1}{g_{m,M3}}\right)$.

Q5. Design a voltage amplifier that provides 0.25 W of signal output power to a 100 Ω load resistor. The signal source provides a 25 mV root-mean-square (RMS) voltage signal and has a source resistance of 0.5 MΩ.

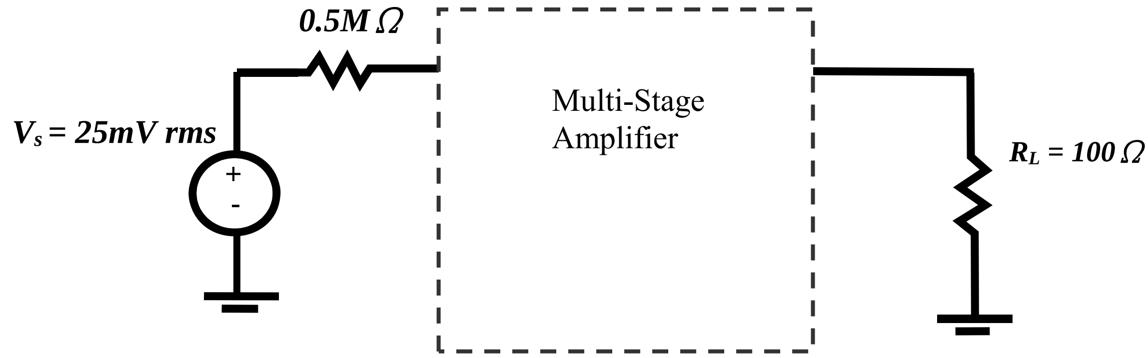
(i) Using the specifications given above, calculate the required voltage gain v_o/v_s. [Hint: You need to calculate the signal voltage v_o (RMS value) across the load, and compare it with the source voltage signal v_s (RMS value)]. [Ans: 200]

(ii) Design a multi-stage amplifier to meet the required voltage gain using chips given below. You may use a chip more than once. Please keep the number of stages in the multi-stage amplifier to a maximum of 3. The voltage gain of the multi-stage amplifier you design can be slightly higher (e.g. up to 20% higher) than the required voltage gain.

Three voltage amplifier chips are available:

Chip 1: Input resistance r_{i1} = 1 MΩ; Gain a_{v1} = 10; Output resistance r_{o1} = 10 kΩ.
Chip 2: Input resistance r_{i2} = 10 kΩ; Gain a_{v2} = 75; Output resistance r_{o2} = 1 kΩ.
Chip 3: Input resistance r_{i3} = 10 kΩ; Gain a_{v3} = 1; Output resistance r_{o3} = 10 Ω.

5.



(i) Required power, $P_L = 0.25$ W

$$= \frac{v_o^2}{100}$$

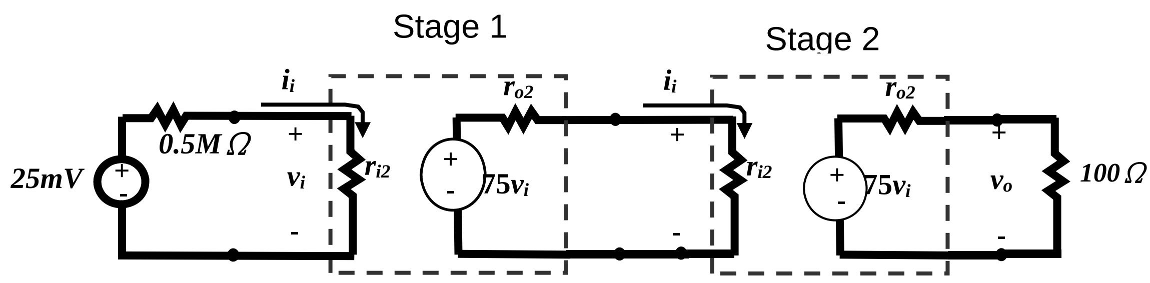
$v_o = 5$ V r.m.s.

Therefore required overall voltage gain $= \dfrac{5}{0.025}$

$= 200$

(b) First Try: chip 2 + chip 2

Since chip2 has a high gain of 75, let us try to cascade 2 stages, each stage using chip2.



The overall voltage gain is

$$v_o = \underbrace{\left(\frac{10k}{10k+500k}\cdot v_s \cdot 75\right)}_{Stage\ 1}\cdot\underbrace{\left(\frac{10k}{10k+1k}\cdot 75\right)}_{Stage\ 2}\cdot\left(\frac{0.100k}{0.100k+1k}\right)$$

Rearrange =>

$$\left[\frac{v_o}{v_s}\right]=\left(\frac{10k}{10k+500k}\cdot 75\right)\cdot\left(\frac{10k}{10k+1k}\cdot 75\right)\cdot\left(\frac{0.100k}{0.100k+1k}\right)$$

$= (1.47).(68.18).(0.09)$
$= 9.11$ V/V **too small, why ?**

The overall voltage gain is not high because of the factor $\frac{0.1k}{0.1k+1k}$ is too small. Therefore, the input resistance of the 1st stage amplifier should not be small compared to the source resistance.

Second Try: chip 2 + chip 2 + chip 2

Similarly,

$$\left[\frac{v_o}{v_s}\right]=\left(\frac{10k}{10k+500k}\cdot 75\right)\cdot\left(\frac{10k}{10k+1k}\cdot 75\right)\cdot\left(\frac{10k}{10k+1k}\cdot 75\right)\cdot\left(\frac{0.100k}{0.100k+1k}\right)$$

$= (1.47).(68.18).(68.18).(0.09)$

$= 615.00$ V/V **too large!**

Third Try: chip 1 + chip 2 + chip 3

Similarly,

$$\frac{v_o}{v_s}=\left(\frac{1000k}{1000k+500k}\cdot 10\right)\cdot\left(\frac{10k}{10k+10k}\cdot 75\right)\cdot\left(\frac{10k}{10k+1k}\cdot 1\right)\cdot\left(\frac{0.1k}{0.1k+0.01k}\right)$$

$= (6.67)\cdot(37.5)\cdot(0.909)\cdot(0.909)$
$= 206.71$ V/V **OK.**

Q6. Figure Q6 below shows a single stage amplifier with current mirror biasing.

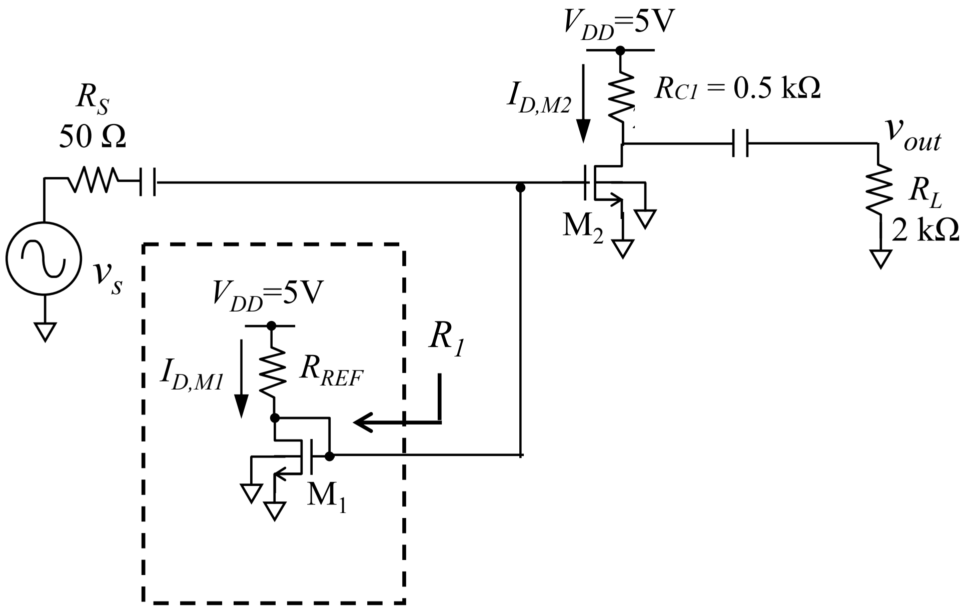


Fig. Q6

For the two n-channel MOSFETs, $V_{THN1} = V_{THN2} = 1$ V, $\lambda_{M1} = \lambda_{M2} = 0$, $K_{n,M1} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_{M1} =$ 2 mA V^{-2}, $K_{n,M2} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_{M2}$ = 4 mA V^{-2}, where $\left(\frac{W}{L}\right)_{M2} = 2\left(\frac{W}{L}\right)_{M1}$.

(i) Design R_{REF} such that $I_{D,M1}$ = 2 mA.

[5 marks]

(ii) What is the value of $I_{D,M2}$?

[2 marks]

(iii) Calculate the small signal parameters of the two MOSFETs, i.e., $g_{m,M1}$, $r_{o,M1}$, $g_{m,M2}$, $r_{o,M2}$.

[4 marks]

(iv) Calculate the value of the a.c. equivalent resistance, R_1, of the circuit enclosed in the dashed box in Fig. Q6.

[3 marks]

(v) Identify the configuration of the single stage amplifier.

[1 mark]

(vi) Determine the parameters, G_m, R_{in} and R_{out} of the two-port network of the amplifier.

[3 marks]

6. (i) $I_{D,M1} = K_{n,M1}\left(V_{GS,M1} - V_{THN1}\right)^2$

$$\left(V_{GS,M1} - V_{THN1}\right) = \sqrt{\frac{I_{D,M1}}{K_{n,M1}}} = \sqrt{\frac{2\text{ mA}}{2\text{ mA V}^{-2}}} = \pm 1\text{ V} \qquad \text{(1 mark)}$$

$V_{GS,M1} = 2$ V as $V_{GS,M1} = 0$ V is not applicable (MOSFET is off). (2 marks)

$$R_{REF} = \frac{V_{DD} - V_{GS,M1}}{I_{D,M1}} = \frac{(5-2)\text{ V}}{2\text{ mA}} = 1.5\text{ k}\Omega\,. \qquad \text{(2 marks)}$$

(ii) Since $V_{THN2} = V_{THN1}$ and $V_{GS2} = V_{GS1}$, but $K_{n,M2} = 2 \times K_{n,M1}$, therefore

$I_{D,M2} = 2 \times I_{D,M1} = 4$ mA. (2 marks)

(iii) $g_{m,M1} = 2\times\sqrt{K_{n,M1}\times I_{D,M1}} = 2\times\sqrt{2\,mA\,V^{-2}\times 2\,mA} = 4\,mA\,V^{-1}$.

$$r_{o,M1} = \frac{1}{\lambda_{M1}\times I_{D,M1}} = \infty$$

$$g_{m,M2} = 2\times\sqrt{K_{n,M2}\times I_{D,M2}} = 2\times\sqrt{4\,mA\,V^{-2}\times 4\,mA} = 8\,mA\,V^{-1}.$$

$$r_{o,M2} = \frac{1}{\lambda_{M2}\times I_{D,M2}} = \infty \qquad \text{(1 mark for each answer)}$$

(iv) The a.c. equivalent circuit of M_1 is a diode-connected transistor, with resistance equal to $1/g_{m,M1}$. Hence, after setting V_{DD} to a.c. ground,

$$R_1 = R_{REF} // \left(\frac{1}{g_{m,M1}}\right) = 214.3\ \Omega. \qquad \text{(3 marks)}$$

(v) Common source amplifier. (1 mark)

(vi) By using the table of equivalent resistances for amplifier configurations,

$G_m = g_{m,M2} = 8$ mA V^{-1}.

$R_{in} = R_1 // \infty = 214.3\ \Omega$.

$R_{out} = R_{C1} // \infty = 0.5$ k Ω. (1 mark for each answer)

Q7. [This question will not be discussed during tutorial class.]

This is a new amplifier circuit that we have not analyzed in the lectures. It is not among the amplifier configurations listed in the tables in the lecture notes. Hence, the two-port network parameters of this amplifier has to be derived from first principles.

For the amplifier circuit shown in Fig. Q7, the transistor Q_1 has the following parameter values: $I_S = 10^{-15}$ A, $\beta = 100$, $V_A = 100$ V.

(i) What are the values of the small signal parameters, $g_{m,Q1}$, $r_{\pi,Q1}$ and $r_{o,Q1}$ of Q_1?

[Ans. 20 mA/V, 5 k, 200 k]

(ii) Transform the circuit for AC analysis and replace the transistor with its small signal equivalent.

(iii) Assuming that the amplifier can be transformed into a 2-port transconductance amplifier, find the three parameters (G_m, R_{in}, R_{out}) of the 2-port network.

[Ans. 18 mA/V, 45 Ω, 268 Ω]

(iv) Derive the overall gain $A_V = v_{out}/v_S$.

[-2.6]

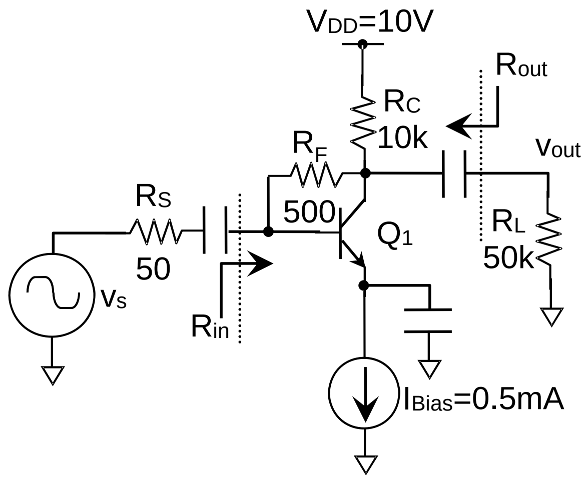


Fig. Q7

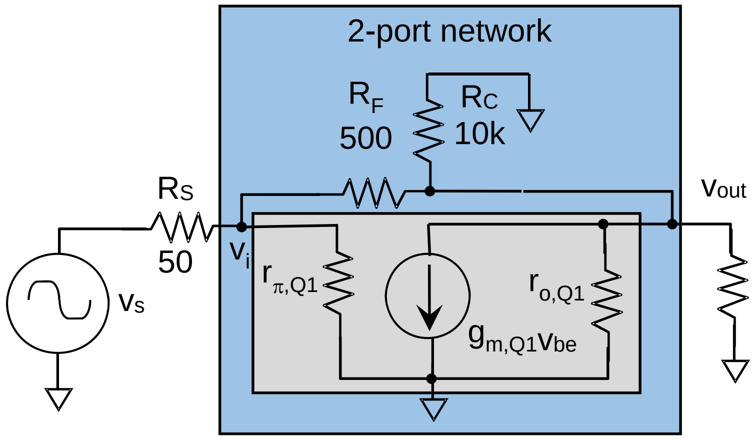
7. (i) $I_C \approx I_E = I_{BIAS} = 0.5$ mA.

$$g_{m,Q1} = \frac{I_C}{V_T} = \frac{0.5\text{ mA}}{0.025\text{ V}} = 20\text{ mA/V}.$$

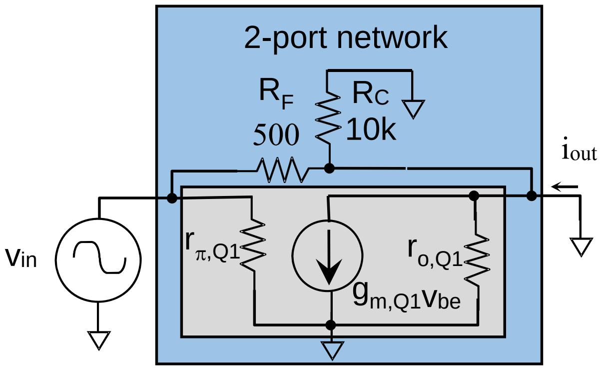
$$r_{\pi,Q1} = \frac{\beta}{g_m} = \frac{100}{20\times10^{-3}} = 5\text{ k}\Omega.$$

$$r_{o,Q1} = \frac{V_A}{I_C} = \frac{100}{0.5\times10^{-3}} = 200\text{ k}\Omega.$$

(ii)



(iii) <u>To find Gm</u> : we note that $v_{be} = v_{in}$.



$$i_{RC} = 0$$

$$i_{ro,Q1} \approx 0$$

$$i_{RF} = \frac{v_{in}}{R_F}$$

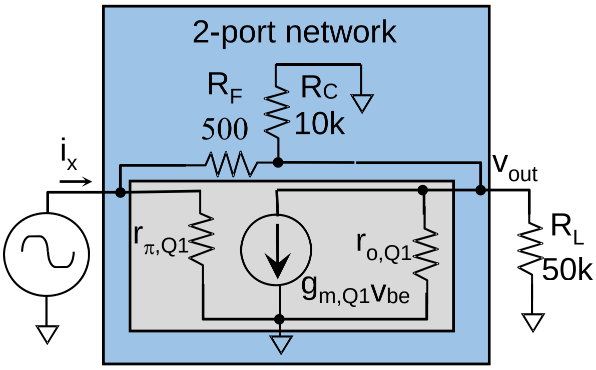
$$i_{out} = g_{m,Q1}v_{in} - i_{RF} = \left(g_{m,Q1} - \frac{1}{R_F}\right)v_{in}$$

$$G_m = g_{m,Q1} - \frac{1}{R_F} = 18\text{mAV}^{-1}$$

or

$$\approx g_{m,Q1} (= 20\text{mAV}^{-1})$$

To find R_{in} : We note that $v_{be} = v_x$.



$$i_{RF} = \frac{v_{out}}{R_C // R_L // r_{o,Q1}} + g_{m,Q1} v_x \cdots (1)$$

$$i_{r\pi,Q1} = \frac{v_x}{r_{\pi,Q1}} \cdots (2)$$

$$i_{RF} = \frac{v_x - v_{out}}{R_F} \cdots (3)$$

$$i_x = i_{r\pi,Q1} + i_{RF} \cdots (4)$$

$$(1),(3) v_{out}\left(\frac{1}{R_C // R_L // r_{o,Q1}} + \frac{1}{R_F}\right) = v_x\left(\frac{1}{R_F} - g_{m,Q1}\right)$$

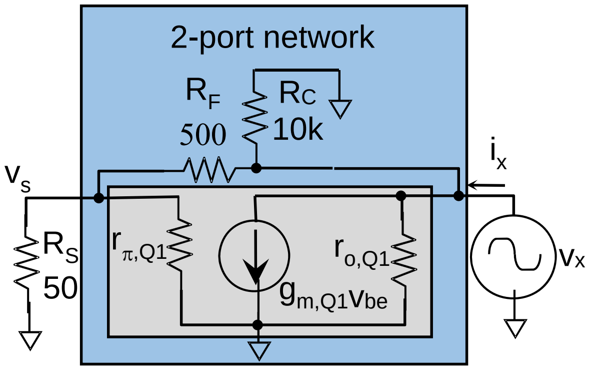
$$\because R_C, R_L, r_{o,Q1} >> R_F \quad and \quad g_{m,Q1} >> \frac{1}{R_F}$$

$$\Rightarrow v_{out} = -v_x g_{m,Q1} R_F$$

$$\Rightarrow i_x = \frac{v_x}{r_{\pi,Q1}} + \frac{v_x + v_x g_{m,Q1} R_F}{R_F}$$

$$R_{in} = \frac{v_x}{i_x} = \frac{1}{\dfrac{1}{r_{\pi,Q1}} + \dfrac{1 + g_{m,Q1} R_F}{R_F}} = 45\,\Omega \approx \frac{R_F}{1 + g_{m,Q1} R_F} \because R_F << r_{\pi,Q1}$$

To find R_{out} :



$$i_{RC} = \frac{v_x}{R_C} \qquad i_{RF} = \frac{v_x}{R_F + (R_S // r_{\pi,Q1})} \approx \frac{v_x}{R_F + R_S} \quad [R_S << r_{\pi,Q1}]$$

$$v_{be} = v_x \frac{(R_S // r_{\pi,Q1})}{R_F + (R_S // r_{\pi,Q1})} \approx v_x \frac{R_S}{R_F + R_S}$$

$$i_{ro,Q1} \approx 0$$

$$\Rightarrow i_x = i_{RC} + i_{RF} + g_{m,Q1} v_{be} = \frac{v_x}{R_C} + \frac{v_x}{R_F + R_S} + g_{m,Q1} v_x \frac{R_S}{R_F + R_S}$$

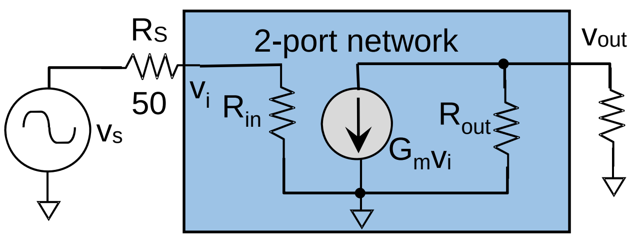
$$i_x = v_x \left(\frac{1}{R_C} + \frac{1}{R_F + R_S} + \frac{g_{m,Q1} R_S}{R_F + R_S} \right)$$

$$R_{out} = \frac{v_x}{i_x} = \left(\frac{1}{R_C} + \frac{1}{R_F + R_S} + \frac{g_{m,Q1} R_S}{R_F + R_S} \right) = 268\ \Omega$$

or

$$R_{out} \approx \frac{1}{R_F + R_S} + \frac{g_{m,Q1} R_S}{R_F + R_S} = 275\ \Omega \quad \text{since} \quad [R_F + R_S << R_C]$$

(iv)



$$R_{in} \approx \frac{R_F}{1 + g_{m,Q1} R_F} = 45 \qquad G_m \approx g_{m,Q1} = 20mA/V \qquad R_{out} \approx \frac{R_F + R_S}{2} = 275$$

$$v_i = \frac{R_{in}}{R_{in} + R_S} v_s$$

$$v_{out} = -G_m v_i (R_{out} // R_L) = -g_{m,Q1} \frac{R_{in}}{R_{in} + R_S} v_s \left(\frac{R_F + R_S}{2} // R_L \right)$$

$$A_V = \frac{v_{out}}{v_s} \approx -\frac{R_{in}}{R_{in} + R_S} g_{m,Q1} \left(\frac{R_F + R_S}{2} \right) = -2.6$$