NATIONAL UNIVERSITY OF SINGAPORE

EXAMINATION FOR

(Semester II : 2010/2011)

EE3304 - DIGITAL CONTROL SYSTEMS

April/May 2011 - Time Allowed: 2 Hours

INSTRUCTIONS TO CANDIDATES

(a) This examination paper contains **FOUR (4)** questions, and comprises **FIVE (5)** pages.

(b) All questions are compulsory. Answer **ALL** questions.

(c) This is a CLOSED book examination. Each student is allowed to bring **ONE** (1) sheet of A4 size paper.

Q1. Consider the computer control system shown in Figure 1, with $G(s) = e^{-Ts}\dfrac{1}{(s+3)}$, $D(z)=K$, and the sampling period T being such that $e^{-3T} = 0.4$.

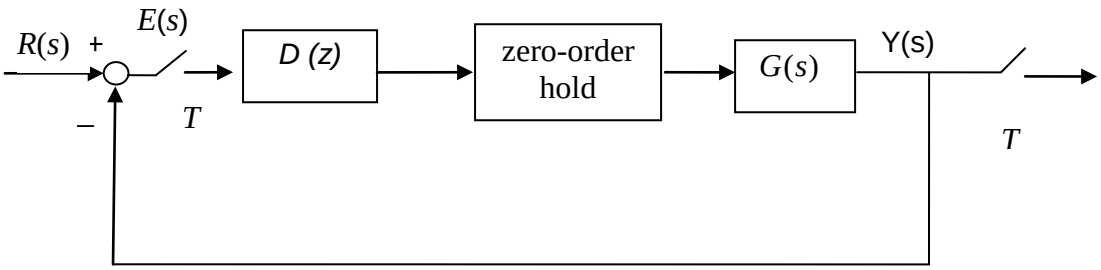

Figure 1

(a) Find the discrete-time closed-loop transfer function of the system, $\dfrac{Y(z)}{R(z)}$.

(10 marks)

(b) Check the closed-loop stability for K=1.

(7 marks)

(c) Obtain the output unit step response for K=0.15.

(8 marks)

Q2. (a) A continuous signal:

$$f(t) = \cos\ 2\pi t + \cos\ 20\pi t,$$

is sampled at the sampling rate of *10Hz*. Give the lowest 3 positive frequencies in the sampled signal and the magnitudes of the frequency response of the sampled signal at these three frequencies.

(15 marks)

(b) In the lectures, we have considered stability preservation issue for the forward rule via z=1+Ts which maps a continuous system G(s) to a discrete system G(z). Now address the inverse problem: will a stable discrete system G(z) always be mapped to a stable continuous system via this forward rule? And prove your answer.

(10 marks)

Q3. A process model is given by

$$\frac{z-b}{z(z-1)},$$

where b is a real number, $b \neq 1$.

(a) Assuming that the closed-loop system is stabilized by a controller $C(z) = l_p$, where l_p is the proportional control gain. Calculate the steady state error with respect to a unit ramp reference. Assuming that b and the sampling period T are given, find the minimum value of l_p such that the absolute value of the steady state error is less than a specified value ε.

(8 marks)

(b) Assume that $b = 0$. Choose an appropriate controller and apply the basic pole placement scheme to place both closed-loop poles at z_p, where z_p is a real number and $|z_p| < 1$.

(8 marks)

(c) Assume that $b = -0.81$, and a proportional controller $C(z) = 1$ is applied. When the desired settling time is 10 seconds or less, find the maximum admissible sampling period.

(9 marks)

Q4 (a) Discuss the applicability of phase lead and phase lag compensators to a double integrator system.

(8 marks)

(b) A plant is given as

$$\frac{e^{-0.1s}}{s}.$$

The second Ziegler-Nichols auto-tuning method is applied for PID auto-tuning. Find the critical gain that yields a sustained oscillation.

(7 marks)

(c) A process model is

$$G(z)=\frac{z-b}{z(z-1)}$$

whereas the nominal model is

$$G_0(z)=\frac{1}{z-1}.$$

i) Find the multiplicative modeling error $G_\Delta(z)$.

ii) Assume that the controller is $C(z)=1$. Show that the closed-loop system is robust stable for any frequencies if $|b|<1$.

(10 marks)

END OF PAPER