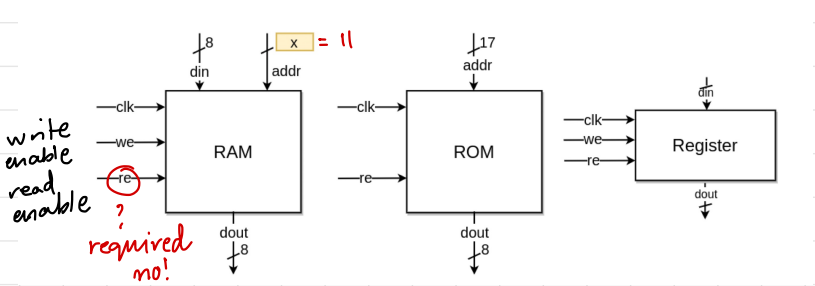
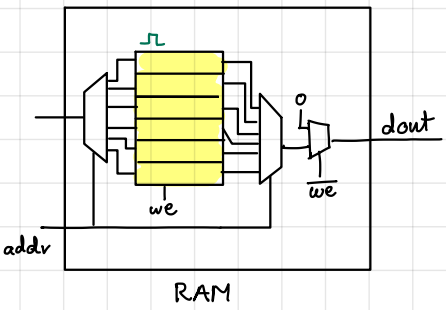
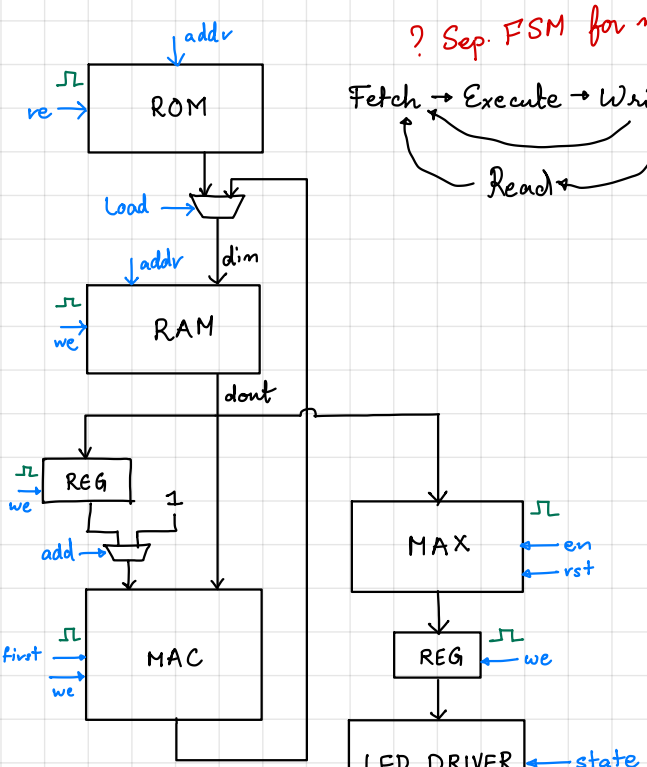


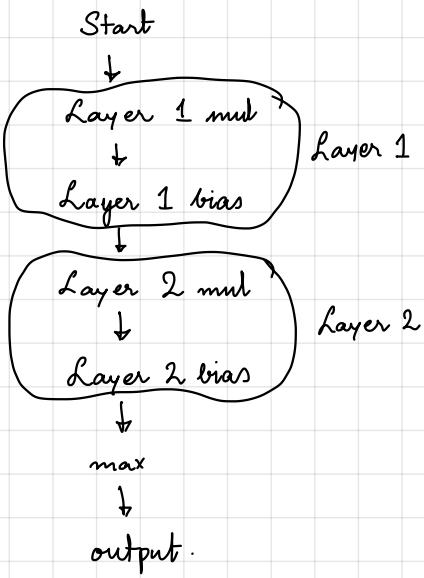
RAM: 2048 (> 784+784+128)





? Sep. FSM for mem. cntrlr ??

NO, need a HFSM (Hierarchy!!)



Network → Layers → Ops → FEW

LAYER:

- alloc in_vec, out_vec, cols
- if layer 1, read in img to in_vec (ROM→RAM)
- while curr_col < cols, do
  - load col from ROM→RAM
  - i ← 0
  - while i < rows do
    - accumulate curr_col[i] × in_vec[i]
  - out_vec[curr_col] ← MAC output
- i ← 0
- load biases from ROM to RAM (location same as mat_vector)
- while i < cols do
  - add biases[i] & out_vec[i] in MAC
  - out_vec[i] ← MAC output

procedure LAYER (rows, cols,
in_vec_ram_loc,
out_vec_ram_loc,
mat_rom_loc,
mat_col_ram_loc,
bias_rom_loc)
returns out_vec at out_vec_ram_loc