COL216 Assignment 2

Stage 7 report

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2020CS10869

Summary

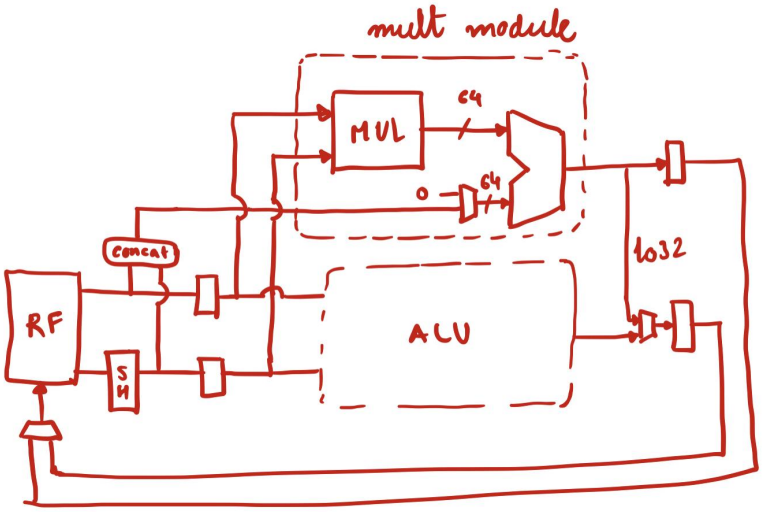
A full rewrite of the controller, datapath and several components was done in this stage. New datatypes for ALU opcodes as well as condition codes and other opcodes were added to make instruction decoding and debugging easier, and the modules were rewritten to work with these new datatypes. The controller was rewritten from a signal-oriented perspective rather than a state-oriented one: signals are now directly passed on to the components in the datapath depending on the state rather than passing bit-wide multiplexer controller signals to the datapath. The control logic is also all assignment-based rather than process based to:

a) avoid having to specify the value for each signal in each state, and
b) prevent the compiler from interpreting latches when a value is not specified in any state

In addition, we moved the registers from the datapath to the controller, and all the glue logic that was facilitated from the multiplexers was moved into the controller. A program gen_datapath.py was created to create the CPU datapath from the associated components, to reduce bugs and effort while doing so manually.

Backward compatibility with all previous assignment iterations holds: Since the CPU interface is compatible, no change was needed to the testing logic, and the previously written tests could simply be run directly.

Finally, the multiplier module was added: this module is purely combinatorial, and sits beside the ALU. The loading/storing of multiple registers is done in multiple cycles, and this lies outside the multiplier and in the datapath. New multiplier-specific states were added to implement these instructions and new registers as well to store the 64-bit values. The schematic working of the multiplier and how it fits into the datapath is shown below:



File Structure

```
2020CS10869.zip
├── Makefile
├── alu.vhdl
├── commons.vhdl
├── cpu.vhdl
├── cpu_datapath.vhdl
├── cpu_multicycle.vhdl
├── fsm.png
├── gen_datapath.py
├── instr_decoder.vhdl
├── logs
│   ├── cpu_synth_log.txt
│   └── multiplier_synth_log.txt
├── mem.vhdl
├── mul_tb.vhdl
├── multiplier.vhdl
├── mytypes.vhdl
├── pmconnect.vhdl
├── predicator.vhdl
├── regfile.vhdl
├── report.pdf
├── run.do
├── shifter.vhdl
├── test_progs
│   ├── gentest
│   ├── gentest.c
│   └── mult_test.s
├── wave_imgs
│   ├── mult_test_1.png
│   └── mult_test_2.png
└── waves
    └── mul_tb.ghw
```

Program Details

- `multiplier.vhdl` - implementation of the multiplier module. This module incorporates a multiplier as well as a 64-bit accumulator.
- `mul_tb.vhdl` - multiplication testbench to check all 6 types of multiply instructions.
- `cpu_datapath.vhdl` and `cpu_controller.vhdl` - the rewritten controller and datapath, which were originally in `cpu_multicycle.vhdl`
- `instr_decoder.vhdl` - the instruction decoder. Used to facilitate easier and more readable instruction decoding
- `gen_datapath.py` - takes as input a list of files and creates a VHDL file which maps all the input signals to the relevant modules.

Other program details are the same as previous stages.

Testing

Multiplier testing

```
0 => X"E3A00003",
1 => X"E3A01002",
2 => X"E0020091",
3 => X"E0230192",

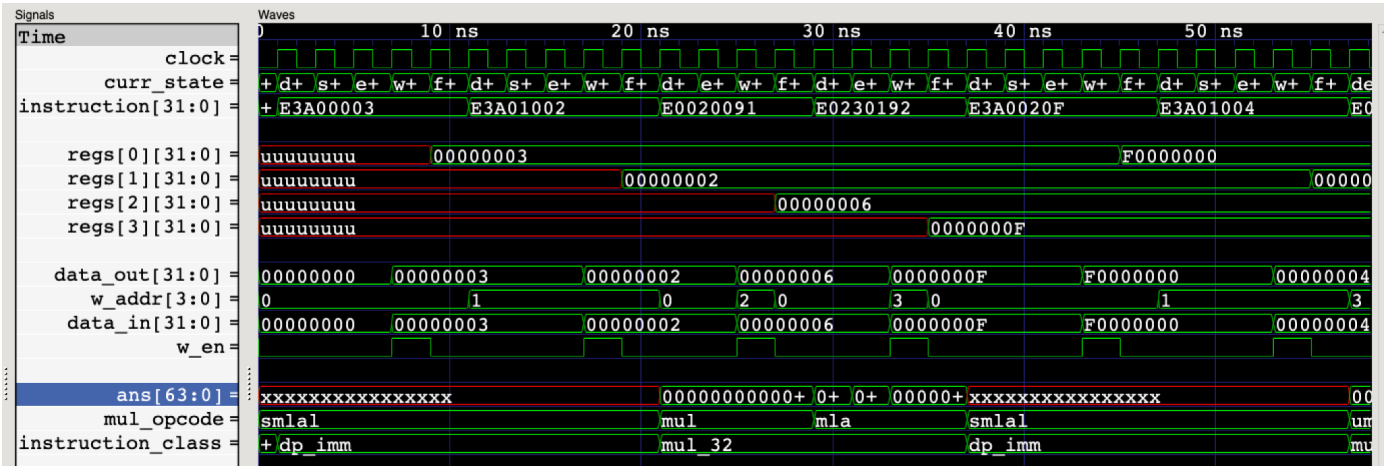
4 => X"E3A0020F",
5 => X"E3A01004",
6 => X"E0823091",
7 => X"E0A23091",

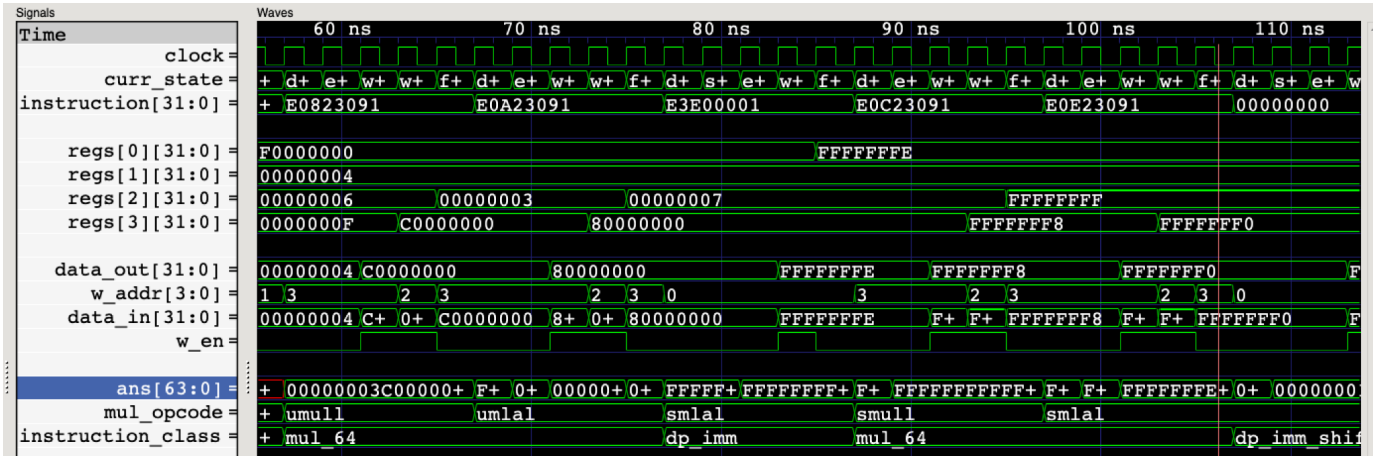
8 => X"E3E00001",
9 => X"E0C23091",
10 => X"E0E23091",
others => X"00000000"
```

```
@ mult_test.s
@ testing multiplier operations
@
    .text
    mov r0, #3
    mov r1, #2
    mul r2, r1, r0
    mla r3, r2, r1, r0 @ r3 = r2 * r1 + r0

    mov r0, #0xF0000000
    mov r1, #0x00000004
    umull r3, r2, r1, r0
    umlal r3, r2, r1, r0

    mov r0, #-2
    smull r3, r2, r1, r0 @ -8
    smlal r3, r2, r1, r0 @ -16
    .end
```





Synthesis

CPU

The CPU entity with the PMConnect module successfully synthesized using Mentor Precision on EDAPlayground. The logs are in cpu_synth_log.txt in logs. **Note that the CPU had only one IO pin, and that was synthesized. Mentor did not synthesize any of the other entities declared and port mapped inside the CPU (ALU, register file, program and data memory etc), although it did the syntax/synthesis checks for all the entities**

```
# Info: ************************************************************
# Info: Device Utilization for 7A100TCSG324
# Info: ************************************************************
# Info: Resource                          Used    Avail   Utilization
# Info: ------------------------------------------------------------
# Info: IOs                               1       210       0.48%
# Info: Global Buffers                    0       32        0.00%
# Info: LUTs                              0       63400     0.00%
# Info: CLB Slices                        0       15850     0.00%
# Info: Dffs or Latches                   0       126800    0.00%
# Info: Block RAMs                        0       135       0.00%
# Info: DSP48E1s                          0       240       0.00%
# Info: ------------------------------------------------------------
# Info: ****************************************************************
# Info: Library: work    Cell: cpu    View: cpu_multicycle_arch
# Info: ****************************************************************
# Info:  Number of ports :                            1
# Info:  Number of nets :                             0
# Info:  Number of instances :                        0
# Info:  Number of references to this view :          0
# Info: Total accumulated area :
# Info:  Number of gates :                            0
# Info:  Number of accumulated instances :            0
# Info: ****************************
# Info:  IO Register Mapping Report
# Info: ****************************
# Info: Design: work.cpu.cpu_multicycle_arch
# Info: +----------+-----------+----------+----------+----------+
# Info: | Port     | Direction |   INFF   |  OUTFF   |  TRIFF   |
# Info: +----------+-----------+----------+----------+----------+
# Info: | clock    | Input     |          |          |          |
# Info: +----------+-----------+----------+----------+----------+
# Info: Total registers mapped: 0
# Info: [12022]: Design has no timing constraint and no timing information.
```

Multiplier

The multiplier module was also separately designed, synthesized and tested.

```
# Info: ******************************************************************
# Info: Device Utilization for 7A100TCSG324
# Info: ******************************************************************
# Info: Resource                          Used    Avail   Utilization
# Info: ------------------------------------------------------------------
# Info: IOs                               206     210      98.10%
# Info: Global Buffers                    0       32        0.00%
# Info: LUTs                              129     63400     0.20%
# Info: CLB Slices                        33      15850     0.21%
# Info: Dffs or Latches                   0       126800    0.00%
# Info: Block RAMs                        0       135       0.00%
# Info: DSP48E1s                          8       240       3.33%
# Info: ------------------------------------------------------------------
# Info: ******************************************************************
# Info: Library: work    Cell: multiplier    View: multiplier_arc
# Info: ******************************************************************
# Info:  Number of ports :                          206
# Info:  Number of nets :                          1080
# Info:  Number of instances :                      467
# Info:  Number of references to this view :          0
# Info: Total accumulated area :
# Info:  Number of DSP48E1s :                         8
# Info:  Number of LUTs :                           129
# Info:  Number of Primitive LUTs :                 129
# Info:  Number of MUX CARRYs :                      63
# Info:  Number of accumulated instances :          467
# Info: ****************************
# Info:  IO Register Mapping Report
# Info: ****************************
# Info: Design: work.multiplier.multiplier_arc
# Info: +----------------------+-----------+----------+----------+----------+
# Info: | Port                 | Direction |   INFF   |  OUTFF   |  TRIFF   |
# Info: +----------------------+-----------+----------+----------+----------+
# Info: | op_m1(31)            | Input     |          |          |          |
# Info: +----------------------+-----------+----------+----------+----------+
# Info: | op_m1(30)            | Input     |          |          |          |
# Info: +----------------------+-----------+----------+----------+----------+
# Info: | op_m1(29)            | Input     |          |          |          |
# Info: +----------------------+-----------+----------+----------+----------+
# Info: | op_m1(28)            | Input     |          |          |          |
# Info: +----------------------+-----------+----------+----------+----------+
# Info: | op_m1(27)            | Input     |          |          |          |
# Info: +----------------------+-----------+----------+----------+----------+
# Info: | op_m1(26)            | Input     |          |          |          |
# Info: +----------------------+-----------+----------+----------+----------+
# Info: | op_m1(25)            | Input     |          |          |          |
# Info: +----------------------+-----------+----------+----------+----------+
# Info: | op_m1(24)            | Input     |          |          |          |
# Info: +----------------------+-----------+----------+----------+----------+
# Info: | op_m1(23)            | Input     |          |          |          |
# Info: +----------------------+-----------+----------+----------+----------+
# Info: | op_m1(22)            | Input     |          |          |          |
# Info: +----------------------+-----------+----------+----------+----------+
# Info: | op_m1(21)            | Input     |          |          |          |
# Info: +----------------------+-----------+----------+----------+----------+
# Info: | op_m1(20)            | Input     |          |          |          |
# Info: +----------------------+-----------+----------+----------+----------+
# Info: | op_m1(19)            | Input     |          |          |          |
# Info: +----------------------+-----------+----------+----------+----------+
# Info: | op_m1(18)            | Input     |          |          |          |
# Info: +----------------------+-----------+----------+----------+----------+
```

```
# Info: | op_m1(17)             | Input     |          |          |          |
# Info: +-----------------------+-----------+----------+----------+----------+
# Info: | op_m1(16)             | Input     |          |          |          |
# Info: +-----------------------+-----------+----------+----------+----------+
# Info: | op_m1(15)             | Input     |          |          |          |
# Info: +-----------------------+-----------+----------+----------+----------+
# Info: | op_m1(14)             | Input     |          |          |          |
# Info: +-----------------------+-----------+----------+----------+----------+
# Info: | op_m1(13)             | Input     |          |          |          |
# Info: +-----------------------+-----------+----------+----------+----------+
# Info: | op_m1(12)             | Input     |          |          |          |
# Info: +-----------------------+-----------+----------+----------+----------+
# Info: | op_m1(11)             | Input     |          |          |          |
# Info: +-----------------------+-----------+----------+----------+----------+
# Info: | op_m1(10)             | Input     |          |          |          |
# Info: +-----------------------+-----------+----------+----------+----------+
# Info: | op_m1(9)              | Input     |          |          |          |
# Info: +-----------------------+-----------+----------+----------+----------+
# Info: | op_m1(8)              | Input     |          |          |          |
# Info: +-----------------------+-----------+----------+----------+----------+
# Info: | op_m1(7)              | Input     |          |          |          |
# Info: +-----------------------+-----------+----------+----------+----------+
# Info: | op_m1(6)              | Input     |          |          |          |
# Info: +-----------------------+-----------+----------+----------+----------+
# Info: | op_m1(5)              | Input     |          |          |          |
# Info: +-----------------------+-----------+----------+----------+----------+
# Info: | op_m1(4)              | Input     |          |          |          |
# Info: +-----------------------+-----------+----------+----------+----------+
# Info: | op_m1(3)              | Input     |          |          |          |
# Info: +-----------------------+-----------+----------+----------+----------+
# Info: | op_m1(2)              | Input     |          |          |          |
# Info: +-----------------------+-----------+----------+----------+----------+
# Info: | op_m1(1)              | Input     |          |          |          |
# Info: +-----------------------+-----------+----------+----------+----------+
# Info: | op_m1(0)              | Input     |          |          |          |
# Info: +-----------------------+-----------+----------+----------+----------+
# Info: | op_m2(31)             | Input     |          |          |          |
# Info: +-----------------------+-----------+----------+----------+----------+
# Info: | op_m2(30)             | Input     |          |          |          |
# Info: +-----------------------+-----------+----------+----------+----------+
# Info: | op_m2(29)             | Input     |          |          |          |
# Info: +-----------------------+-----------+----------+----------+----------+
# Info: | op_m2(28)             | Input     |          |          |          |
# Info: +-----------------------+-----------+----------+----------+----------+
# Info: | op_m2(27)             | Input     |          |          |          |
# Info: +-----------------------+-----------+----------+----------+----------+
# Info: | op_m2(26)             | Input     |          |          |          |
# Info: +-----------------------+-----------+----------+----------+----------+
# Info: | op_m2(25)             | Input     |          |          |          |
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# Info: | op_m2(24)             | Input     |          |          |          |
# Info: +-----------------------+-----------+----------+----------+----------+
# Info: | op_m2(23)             | Input     |          |          |          |
# Info: +-----------------------+-----------+----------+----------+----------+
# Info: | op_m2(22)             | Input     |          |          |          |
# Info: +-----------------------+-----------+----------+----------+----------+
# Info: | op_m2(21)             | Input     |          |          |          |
# Info: +-----------------------+-----------+----------+----------+----------+
# Info: | op_m2(20)             | Input     |          |          |          |
# Info: +-----------------------+-----------+----------+----------+----------+
# Info: | op_m2(19)             | Input     |          |          |          |
# Info: +-----------------------+-----------+----------+----------+----------+
# Info: | op_m2(18)             | Input     |          |          |          |
# Info: +-----------------------+-----------+----------+----------+----------+
# Info: | op_m2(17)             | Input     |          |          |          |
# Info: +-----------------------+-----------+----------+----------+----------+
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```
# Info: | op_m2(16)             | Input     |          |          |          |
# Info: +-----------------------+-----------+----------+----------+----------+
# Info: | op_m2(15)             | Input     |          |          |          |
# Info: +-----------------------+-----------+----------+----------+----------+
# Info: | op_m2(14)             | Input     |          |          |          |
# Info: +-----------------------+-----------+----------+----------+----------+
# Info: | op_m2(13)             | Input     |          |          |          |
# Info: +-----------------------+-----------+----------+----------+----------+
# Info: | op_m2(12)             | Input     |          |          |          |
# Info: +-----------------------+-----------+----------+----------+----------+
# Info: | op_m2(11)             | Input     |          |          |          |
# Info: +-----------------------+-----------+----------+----------+----------+
# Info: | op_m2(10)             | Input     |          |          |          |
# Info: +-----------------------+-----------+----------+----------+----------+
# Info: | op_m2(9)              | Input     |          |          |          |
# Info: +-----------------------+-----------+----------+----------+----------+
# Info: | op_m2(8)              | Input     |          |          |          |
# Info: +-----------------------+-----------+----------+----------+----------+
# Info: | op_m2(7)              | Input     |          |          |          |
# Info: +-----------------------+-----------+----------+----------+----------+
# Info: | op_m2(6)              | Input     |          |          |          |
# Info: +-----------------------+-----------+----------+----------+----------+
# Info: | op_m2(5)              | Input     |          |          |          |
# Info: +-----------------------+-----------+----------+----------+----------+
# Info: | op_m2(4)              | Input     |          |          |          |
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# Info: | op_m2(3)              | Input     |          |          |          |
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# Info: | op_m2(2)              | Input     |          |          |          |
# Info: +-----------------------+-----------+----------+----------+----------+
# Info: | op_m2(1)              | Input     |          |          |          |
# Info: +-----------------------+-----------+----------+----------+----------+
# Info: | op_m2(0)              | Input     |          |          |          |
# Info: +-----------------------+-----------+----------+----------+----------+
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# Info: | op_a(62)              | Input     |          |          |          |
# Info: +-----------------------+-----------+----------+----------+----------+
# Info: | op_a(61)              | Input     |          |          |          |
# Info: +-----------------------+-----------+----------+----------+----------+
# Info: | op_a(60)              | Input     |          |          |          |
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# Info: | op_a(59)              | Input     |          |          |          |
# Info: +-----------------------+-----------+----------+----------+----------+
# Info: | op_a(58)              | Input     |          |          |          |
# Info: +-----------------------+-----------+----------+----------+----------+
# Info: | op_a(57)              | Input     |          |          |          |
# Info: +-----------------------+-----------+----------+----------+----------+
# Info: | op_a(56)              | Input     |          |          |          |
# Info: +-----------------------+-----------+----------+----------+----------+
# Info: | op_a(55)              | Input     |          |          |          |
# Info: +-----------------------+-----------+----------+----------+----------+
# Info: | op_a(54)              | Input     |          |          |          |
# Info: +-----------------------+-----------+----------+----------+----------+
# Info: | op_a(53)              | Input     |          |          |          |
# Info: +-----------------------+-----------+----------+----------+----------+
# Info: | op_a(52)              | Input     |          |          |          |
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# Info: | op_a(48)              | Input     |          |          |          |
# Info: +-----------------------+-----------+----------+----------+----------+
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# Info: | op_a(47)              | Input     |          |          |          |
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# Info: | op_a(45)              | Input     |          |          |          |
# Info: +-----------------------+-----------+----------+----------+----------+
# Info: | op_a(44)              | Input     |          |          |          |
# Info: +-----------------------+-----------+----------+----------+----------+
# Info: | op_a(43)              | Input     |          |          |          |
# Info: +-----------------------+-----------+----------+----------+----------+
# Info: | op_a(42)              | Input     |          |          |          |
# Info: +-----------------------+-----------+----------+----------+----------+
# Info: | op_a(41)              | Input     |          |          |          |
# Info: +-----------------------+-----------+----------+----------+----------+
# Info: | op_a(40)              | Input     |          |          |          |
# Info: +-----------------------+-----------+----------+----------+----------+
# Info: | op_a(39)              | Input     |          |          |          |
# Info: +-----------------------+-----------+----------+----------+----------+
# Info: | op_a(38)              | Input     |          |          |          |
# Info: +-----------------------+-----------+----------+----------+----------+
# Info: | op_a(37)              | Input     |          |          |          |
# Info: +-----------------------+-----------+----------+----------+----------+
# Info: | op_a(36)              | Input     |          |          |          |
# Info: +-----------------------+-----------+----------+----------+----------+
# Info: | op_a(35)              | Input     |          |          |          |
# Info: +-----------------------+-----------+----------+----------+----------+
# Info: | op_a(34)              | Input     |          |          |          |
# Info: +-----------------------+-----------+----------+----------+----------+
# Info: | op_a(33)              | Input     |          |          |          |
# Info: +-----------------------+-----------+----------+----------+----------+
# Info: | op_a(32)              | Input     |          |          |          |
# Info: +-----------------------+-----------+----------+----------+----------+
# Info: | op_a(31)              | Input     |          |          |          |
# Info: +-----------------------+-----------+----------+----------+----------+
# Info: | op_a(30)              | Input     |          |          |          |
# Info: +-----------------------+-----------+----------+----------+----------+
# Info: | op_a(29)              | Input     |          |          |          |
# Info: +-----------------------+-----------+----------+----------+----------+
# Info: | op_a(28)              | Input     |          |          |          |
# Info: +-----------------------+-----------+----------+----------+----------+
# Info: | op_a(27)              | Input     |          |          |          |
# Info: +-----------------------+-----------+----------+----------+----------+
# Info: | op_a(26)              | Input     |          |          |          |
# Info: +-----------------------+-----------+----------+----------+----------+
# Info: | op_a(25)              | Input     |          |          |          |
# Info: +-----------------------+-----------+----------+----------+----------+
# Info: | op_a(24)              | Input     |          |          |          |
# Info: +-----------------------+-----------+----------+----------+----------+
# Info: | op_a(23)              | Input     |          |          |          |
# Info: +-----------------------+-----------+----------+----------+----------+
# Info: | op_a(22)              | Input     |          |          |          |
# Info: +-----------------------+-----------+----------+----------+----------+
# Info: | op_a(21)              | Input     |          |          |          |
# Info: +-----------------------+-----------+----------+----------+----------+
# Info: | op_a(20)              | Input     |          |          |          |
# Info: +-----------------------+-----------+----------+----------+----------+
# Info: | op_a(19)              | Input     |          |          |          |
# Info: +-----------------------+-----------+----------+----------+----------+
# Info: | op_a(18)              | Input     |          |          |          |
# Info: +-----------------------+-----------+----------+----------+----------+
# Info: | op_a(17)              | Input     |          |          |          |
# Info: +-----------------------+-----------+----------+----------+----------+
# Info: | op_a(16)              | Input     |          |          |          |
# Info: +-----------------------+-----------+----------+----------+----------+
# Info: | op_a(15)              | Input     |          |          |          |
# Info: +-----------------------+-----------+----------+----------+----------+
```

```
# Info: | op_a(14)              | Input     |          |          |          |
# Info: +-----------------------+-----------+----------+----------+----------+
# Info: | op_a(13)              | Input     |          |          |          |
# Info: +-----------------------+-----------+----------+----------+----------+
# Info: | op_a(12)              | Input     |          |          |          |
# Info: +-----------------------+-----------+----------+----------+----------+
# Info: | op_a(11)              | Input     |          |          |          |
# Info: +-----------------------+-----------+----------+----------+----------+
# Info: | op_a(10)              | Input     |          |          |          |
# Info: +-----------------------+-----------+----------+----------+----------+
# Info: | op_a(9)               | Input     |          |          |          |
# Info: +-----------------------+-----------+----------+----------+----------+
# Info: | op_a(8)               | Input     |          |          |          |
# Info: +-----------------------+-----------+----------+----------+----------+
# Info: | op_a(7)               | Input     |          |          |          |
# Info: +-----------------------+-----------+----------+----------+----------+
# Info: | op_a(6)               | Input     |          |          |          |
# Info: +-----------------------+-----------+----------+----------+----------+
# Info: | op_a(5)               | Input     |          |          |          |
# Info: +-----------------------+-----------+----------+----------+----------+
# Info: | op_a(4)               | Input     |          |          |          |
# Info: +-----------------------+-----------+----------+----------+----------+
# Info: | op_a(3)               | Input     |          |          |          |
# Info: +-----------------------+-----------+----------+----------+----------+
# Info: | op_a(2)               | Input     |          |          |          |
# Info: +-----------------------+-----------+----------+----------+----------+
# Info: | op_a(1)               | Input     |          |          |          |
# Info: +-----------------------+-----------+----------+----------+----------+
# Info: | op_a(0)               | Input     |          |          |          |
# Info: +-----------------------+-----------+----------+----------+----------+
# Info: | opcode(5)             | Input     |          |          |          |
# Info: +-----------------------+-----------+----------+----------+----------+
# Info: | opcode(4)             | Input     |          |          |          |
# Info: +-----------------------+-----------+----------+----------+----------+
# Info: | opcode(3)             | Input     |          |          |          |
# Info: +-----------------------+-----------+----------+----------+----------+
# Info: | opcode(2)             | Input     |          |          |          |
# Info: +-----------------------+-----------+----------+----------+----------+
# Info: | opcode(1)             | Input     |          |          |          |
# Info: +-----------------------+-----------+----------+----------+----------+
# Info: | opcode(0)             | Input     |          |          |          |
# Info: +-----------------------+-----------+----------+----------+----------+
# Info: | flags_in_overflow     | Input     |          |          |          |
# Info: +-----------------------+-----------+----------+----------+----------+
# Info: | flags_in_carry        | Input     |          |          |          |
# Info: +-----------------------+-----------+----------+----------+----------+
# Info: | flags_in_zero         | Input     |          |          |          |
# Info: +-----------------------+-----------+----------+----------+----------+
# Info: | flags_in_negative     | Input     |          |          |          |
# Info: +-----------------------+-----------+----------+----------+----------+
# Info: | flags_out_overflow    | Output    |          |          |          |
# Info: +-----------------------+-----------+----------+----------+----------+
# Info: | flags_out_carry       | Output    |          |          |          |
# Info: +-----------------------+-----------+----------+----------+----------+
# Info: | flags_out_zero        | Output    |          |          |          |
# Info: +-----------------------+-----------+----------+----------+----------+
# Info: | flags_out_negative    | Output    |          |          |          |
# Info: +-----------------------+-----------+----------+----------+----------+
# Info: | ans(63)               | Output    |          |          |          |
# Info: +-----------------------+-----------+----------+----------+----------+
# Info: | ans(62)               | Output    |          |          |          |
# Info: +-----------------------+-----------+----------+----------+----------+
# Info: | ans(61)               | Output    |          |          |          |
# Info: +-----------------------+-----------+----------+----------+----------+
# Info: | ans(60)               | Output    |          |          |          |
# Info: +-----------------------+-----------+----------+----------+----------+
```

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# Info: | ans(59)                | Output    |          |          |          |
# Info: +------------------------+-----------+----------+----------+----------+
# Info: | ans(58)                | Output    |          |          |          |
# Info: +------------------------+-----------+----------+----------+----------+
# Info: | ans(57)                | Output    |          |          |          |
# Info: +------------------------+-----------+----------+----------+----------+
# Info: | ans(56)                | Output    |          |          |          |
# Info: +------------------------+-----------+----------+----------+----------+
# Info: | ans(55)                | Output    |          |          |          |
# Info: +------------------------+-----------+----------+----------+----------+
# Info: | ans(54)                | Output    |          |          |          |
# Info: +------------------------+-----------+----------+----------+----------+
# Info: | ans(53)                | Output    |          |          |          |
# Info: +------------------------+-----------+----------+----------+----------+
# Info: | ans(52)                | Output    |          |          |          |
# Info: +------------------------+-----------+----------+----------+----------+
# Info: | ans(51)                | Output    |          |          |          |
# Info: +------------------------+-----------+----------+----------+----------+
# Info: | ans(50)                | Output    |          |          |          |
# Info: +------------------------+-----------+----------+----------+----------+
# Info: | ans(49)                | Output    |          |          |          |
# Info: +------------------------+-----------+----------+----------+----------+
# Info: | ans(48)                | Output    |          |          |          |
# Info: +------------------------+-----------+----------+----------+----------+
# Info: | ans(47)                | Output    |          |          |          |
# Info: +------------------------+-----------+----------+----------+----------+
# Info: | ans(46)                | Output    |          |          |          |
# Info: +------------------------+-----------+----------+----------+----------+
# Info: | ans(45)                | Output    |          |          |          |
# Info: +------------------------+-----------+----------+----------+----------+
# Info: | ans(44)                | Output    |          |          |          |
# Info: +------------------------+-----------+----------+----------+----------+
# Info: | ans(43)                | Output    |          |          |          |
# Info: +------------------------+-----------+----------+----------+----------+
# Info: | ans(42)                | Output    |          |          |          |
# Info: +------------------------+-----------+----------+----------+----------+
# Info: | ans(41)                | Output    |          |          |          |
# Info: +------------------------+-----------+----------+----------+----------+
# Info: | ans(40)                | Output    |          |          |          |
# Info: +------------------------+-----------+----------+----------+----------+
# Info: | ans(39)                | Output    |          |          |          |
# Info: +------------------------+-----------+----------+----------+----------+
# Info: | ans(38)                | Output    |          |          |          |
# Info: +------------------------+-----------+----------+----------+----------+
# Info: | ans(37)                | Output    |          |          |          |
# Info: +------------------------+-----------+----------+----------+----------+
# Info: | ans(36)                | Output    |          |          |          |
# Info: +------------------------+-----------+----------+----------+----------+
# Info: | ans(35)                | Output    |          |          |          |
# Info: +------------------------+-----------+----------+----------+----------+
# Info: | ans(34)                | Output    |          |          |          |
# Info: +------------------------+-----------+----------+----------+----------+
# Info: | ans(33)                | Output    |          |          |          |
# Info: +------------------------+-----------+----------+----------+----------+
# Info: | ans(32)                | Output    |          |          |          |
# Info: +------------------------+-----------+----------+----------+----------+
# Info: | ans(31)                | Output    |          |          |          |
# Info: +------------------------+-----------+----------+----------+----------+
# Info: | ans(30)                | Output    |          |          |          |
# Info: +------------------------+-----------+----------+----------+----------+
# Info: | ans(29)                | Output    |          |          |          |
# Info: +------------------------+-----------+----------+----------+----------+
# Info: | ans(28)                | Output    |          |          |          |
# Info: +------------------------+-----------+----------+----------+----------+
# Info: | ans(27)                | Output    |          |          |          |
# Info: +------------------------+-----------+----------+----------+----------+
```

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# Info: | ans(26)                | Output    |          |          |          |
# Info: +------------------------+-----------+----------+----------+----------+
# Info: | ans(25)                | Output    |          |          |          |
# Info: +------------------------+-----------+----------+----------+----------+
# Info: | ans(24)                | Output    |          |          |          |
# Info: +------------------------+-----------+----------+----------+----------+
# Info: | ans(23)                | Output    |          |          |          |
# Info: +------------------------+-----------+----------+----------+----------+
# Info: | ans(22)                | Output    |          |          |          |
# Info: +------------------------+-----------+----------+----------+----------+
# Info: | ans(21)                | Output    |          |          |          |
# Info: +------------------------+-----------+----------+----------+----------+
# Info: | ans(20)                | Output    |          |          |          |
# Info: +------------------------+-----------+----------+----------+----------+
# Info: | ans(19)                | Output    |          |          |          |
# Info: +------------------------+-----------+----------+----------+----------+
# Info: | ans(18)                | Output    |          |          |          |
# Info: +------------------------+-----------+----------+----------+----------+
# Info: | ans(17)                | Output    |          |          |          |
# Info: +------------------------+-----------+----------+----------+----------+
# Info: | ans(16)                | Output    |          |          |          |
# Info: +------------------------+-----------+----------+----------+----------+
# Info: | ans(15)                | Output    |          |          |          |
# Info: +------------------------+-----------+----------+----------+----------+
# Info: | ans(14)                | Output    |          |          |          |
# Info: +------------------------+-----------+----------+----------+----------+
# Info: | ans(13)                | Output    |          |          |          |
# Info: +------------------------+-----------+----------+----------+----------+
# Info: | ans(12)                | Output    |          |          |          |
# Info: +------------------------+-----------+----------+----------+----------+
# Info: | ans(11)                | Output    |          |          |          |
# Info: +------------------------+-----------+----------+----------+----------+
# Info: | ans(10)                | Output    |          |          |          |
# Info: +------------------------+-----------+----------+----------+----------+
# Info: | ans(9)                 | Output    |          |          |          |
# Info: +------------------------+-----------+----------+----------+----------+
# Info: | ans(8)                 | Output    |          |          |          |
# Info: +------------------------+-----------+----------+----------+----------+
# Info: | ans(7)                 | Output    |          |          |          |
# Info: +------------------------+-----------+----------+----------+----------+
# Info: | ans(6)                 | Output    |          |          |          |
# Info: +------------------------+-----------+----------+----------+----------+
# Info: | ans(5)                 | Output    |          |          |          |
# Info: +------------------------+-----------+----------+----------+----------+
# Info: | ans(4)                 | Output    |          |          |          |
# Info: +------------------------+-----------+----------+----------+----------+
# Info: | ans(3)                 | Output    |          |          |          |
# Info: +------------------------+-----------+----------+----------+----------+
# Info: | ans(2)                 | Output    |          |          |          |
# Info: +------------------------+-----------+----------+----------+----------+
# Info: | ans(1)                 | Output    |          |          |          |
# Info: +------------------------+-----------+----------+----------+----------+
# Info: | ans(0)                 | Output    |          |          |          |
# Info: +------------------------+-----------+----------+----------+----------+
# Info: Total registers mapped: 0
# Info: [12022]: Design has no timing constraint and no timing information.
```

Design and Verification

Multiplication required the addition of four new states: `execute_mul, writeback_mul32, writeback_mul64_lo, writeback_mul64_hi`. The new writeback states are required to allow us to writeback both the high word and the low word result of a 64 bit multiplication instruction. `execute_mul` reads in both the accumulate register (or pair of registers) directly from the register file, as well as the multiplicand registers from registers A and B, which feed into the ALU.