COL216 Assignment 2

Stage 6 report

Aniruddha Deb
2020CS10869

Summary

This stage implemented the PMConnect module, which acts as a memory controller for reading/writing. We also implemented post-indexed addressing for memory, which required a slight modification of the datapath.

The concept of storing bytes rather than words brings into question endianness. The memory that we implemented is big endian, meaning that the least significant byte is stored in the most significant position, similar to the following structure:

```
|31  ...  00|31  ...  00|31  ...  00|31  ...  00|31  ...  00|31  ...  00| ->
|    W00    |    W01    |    W02    |    W03    |    W04    |    W05    | ->
```

The big endian choice for memory was made early in the design stage, as it allowed us to initialize memory as an array of words, and easily load words out of memory. The code in mem.vhdl reflects this.

This stage implemented and tested all the types of operators for data transfer instructions, as well as implementing the necessary logic in the control unit decoding the instructions for loading and storing signed bytes/words.

File Structure

```
2020CS10869.zip
├── Assignment.png
├── Makefile
├── alu.vhdl
├── commons.vhdl
├── cpu.vhdl
├── cpu_multicycle.vhdl
├── dt_tb.vhdl
├── idx_tb.vhdl
├── logs
│   ├── cpu_synth_log.txt
│   └── pmconnect_synth_log.txt
├── mem.vhdl
├── mytypes.vhdl
├── pmconnect.vhdl
├── predicator.vhdl
├── regfile.vhdl
├── report.pdf
├── run.do
├── shifter.vhdl
```

```
├── test_progs
│   ├── dt_test.s
│   ├── gentest
│   ├── gentest.c
│   └── idx_test.s
├── wave_imgs
│   ├── dt_test_1.png
│   ├── dt_test_2.png
│   ├── dt_test_3.png
│   └── idx_test.png
└── waves
    ├── dt_tb.ghw
    └── idx_tb.ghw
```

Program Details

- `pmconnect.vhdl` - implements the PMConnect module
- `dt_tb.vhdl` - testbench for data transfer instructions (instructions defined in `test_progs/dt_test.s`)
- `idx_tb.vhdl` - testbench for data transfer instructions (instructions defined in `test_progs/idx_test.s`)

Other program details are the same as previous stages.

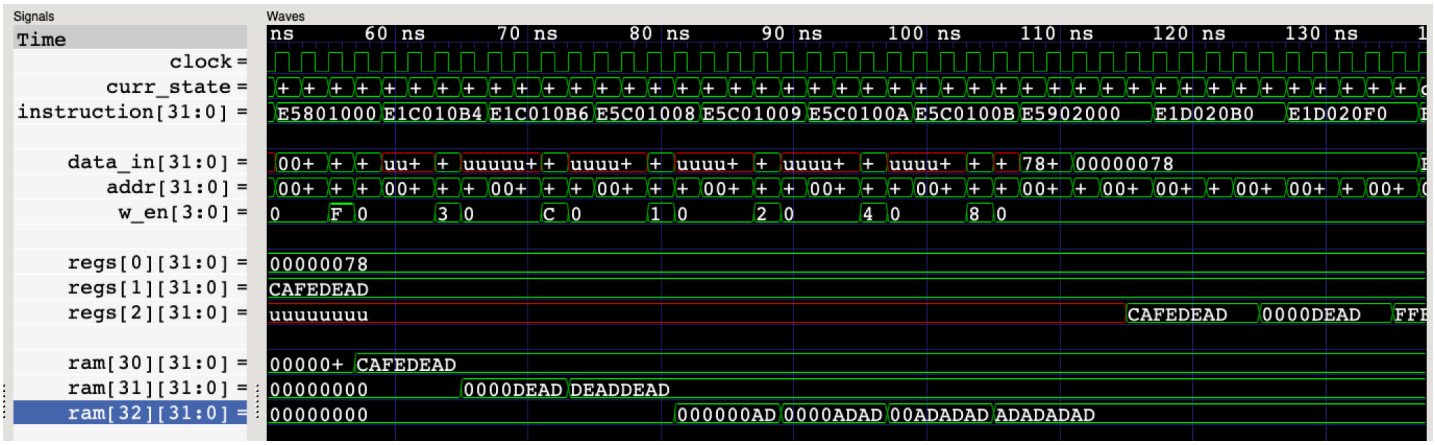
Testing

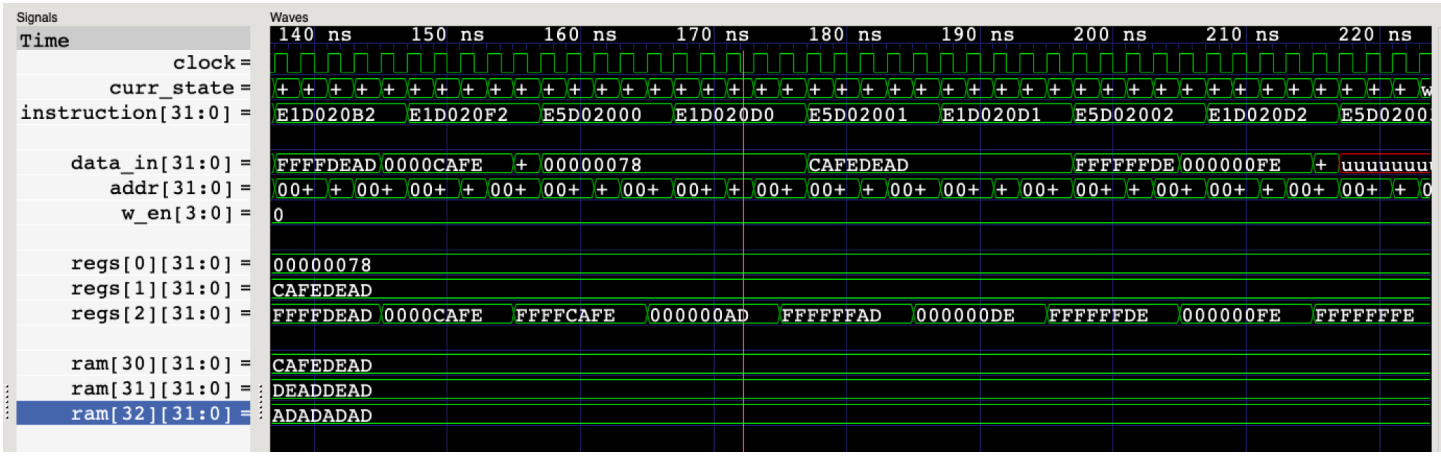
DT Testing

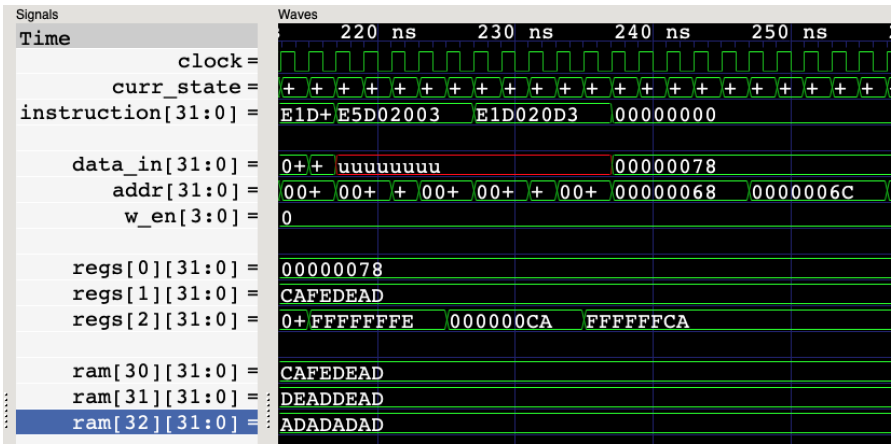
	`@ dt_test.s`
	`@ testing all types of DT instructions`
	`@`

	`.text`
`0 => X"E3A00078"`	`mov r0, #120 @ byte address 30`
`1 => X"E3A010AD"`	`mov r1, #0xAD`
`2 => X"E3811CDE"`	`orr r1, #0xDE00`
`3 => X"E38118FE"`	`orr r1, #0xFE0000`
`4 => X"E38114CA"`	`orr r1, #0xCA000000 @ r1 now stores 0xCAFEDEAD`
`5 => X"E5801000"`	`str r1, [r0]`
`6 => X"E1C010B4"`	`strh r1, [r0,#4]`
`7 => X"E1C010B6"`	`strh r1, [r0,#6]`
`8 => X"E5C01008"`	`strb r1, [r0,#8]`
`9 => X"E5C01009"`	`strb r1, [r0,#9]`
`10 => X"E5C0100A"`	`strb r1, [r0,#10]`
`11 => X"E5C0100B"`	`strb r1, [r0,#11]`
`12 => X"E5902000"`	`ldr r2, [r0]`
`13 => X"E1D020B0"`	`ldrh r2, [r0]`

```
    14 => X"E1D020F0"       ldrsh r2, [r0]
    15 => X"E1D020B2"       ldrh r2, [r0,#2]
    16 => X"E1D020F2"       ldrsh r2, [r0,#2]

    17 => X"E5D02000"       ldrb r2, [r0]
    18 => X"E1D020D0"       ldrsb r2, [r0]
    19 => X"E5D02001"       ldrb r2, [r0,#1]
    20 => X"E1D020D1"       ldrsb r2, [r0,#1]
    21 => X"E5D02002"       ldrb r2, [r0,#2]
    22 => X"E1D020D2"       ldrsb r2, [r0,#2]
    23 => X"E5D02003"       ldrb r2, [r0,#3]
    24 => X"E1D020D3"       ldrsb r2, [r0,#3]

                            .end
```

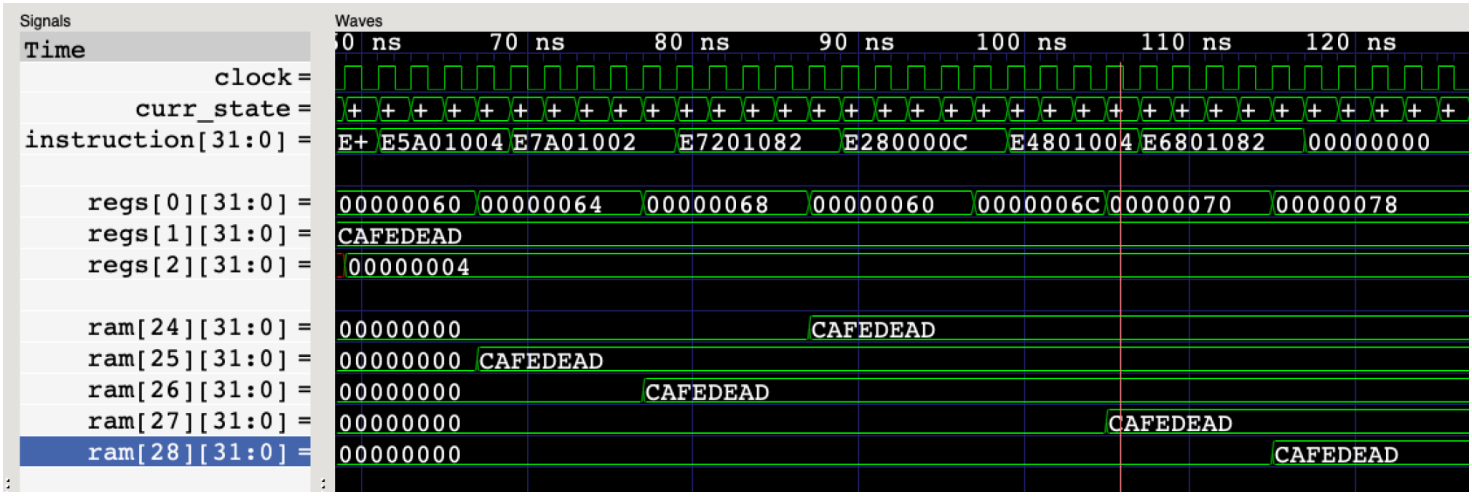






Index testing (post/pre addressing)

```
                                @ idx_test.s
                                @ tests preindexing, postindexing, and writeback
                                @ the following types of data transfer operators exist in ARM
                                @
                                @ 1. [<Rn>, #+/-<offset_12>]
                                @ 2. [<Rn>, +/-<Rm>]
                                @ 3. [<Rn>, +/-<Rm>, <shift> #<shift_imm>]
                                @ 4. [<Rn>, #+/-<offset_12>]!
                                @ 5. [<Rn>, +/-<Rm>]!
                                @ 6. [<Rn>, +/-<Rm>, <shift> #<shift_imm>]!
                                @ 7. [<Rn>], #+/-<offset_12>
                                @ 8. [<Rn>], +/-<Rm>
                                @ 9. [<Rn>], +/-<Rm>, <shift> #<shift_imm>
                                @ 1-3 were tested previously, here we test 4-9

                                    .text

    0 => X"E3A00060"            mov r0, #96 @ byte address 24
    1 => X"E3A010AD"            mov r1, #0xAD
    2 => X"E3811CDE"            orr r1, #0xDE00
    3 => X"E38118FE"            orr r1, #0xFE0000
    4 => X"E38114CA"            orr r1, #0xCA000000
    5 => X"E3A02004"            mov r2, #4

    6 => X"E5A01004"            str r1, [r0, #4]! @ store at 25, r0 = 100
    7 => X"E7A01002"            str r1, [r0, r2]! @ store at 26, r0 = 104
    8 => X"E7201082"            str r1, [r0, -r2, lsl #1]! @ store at 24, r0 = 96 again

    9 => X"E280000C"            add r0, #12
    10 => X"E4801004"           str r1, [r0], #4 @ store at 27, r0 = 108
    11 => X"E6801082"           str r1, [r0], r2, lsl #1 @ store at 28, r0 = 116

                                    .end
```



Synthesis

CPU

The CPU entity with the PMConnect module successfully synthesized using Mentor Precision on EDAPlayground. The logs are in cpu_synth_log.txt in logs. **Note that the CPU had only one IO pin, and that was synthesized. Mentor did not synthesize any of the other entities declared and port mapped inside the CPU (ALU, register file, program and data memory etc), although it did the syntax/synthesis checks for all the entities**

```
# Info: ************************************************************
# Info: Device Utilization for 7A100TCSG324
# Info: ************************************************************
# Info: Resource                          Used    Avail   Utilization
# Info: ------------------------------------------------------------
# Info: IOs                               1       210       0.48%
# Info: Global Buffers                    0       32        0.00%
# Info: LUTs                              0       63400     0.00%
# Info: CLB Slices                        0       15850     0.00%
# Info: Dffs or Latches                   0       126800    0.00%
# Info: Block RAMs                        0       135       0.00%
# Info: DSP48E1s                          0       240       0.00%
# Info: ------------------------------------------------------------
# Info: ******************************************************
# Info: Library: work    Cell: cpu    View: cpu_arch
# Info: ******************************************************
# Info:  Number of ports :                              1
# Info:  Number of nets :                               0
# Info:  Number of instances :                          0
# Info:  Number of references to this view :            0
# Info: Total accumulated area :
# Info:  Number of gates :                              0
# Info:  Number of accumulated instances :              0
# Info: ****************************
# Info:  IO Register Mapping Report
# Info: ****************************
# Info: Design: work.cpu.cpu_arch
# Info: +----------+-----------+----------+----------+----------+
# Info: | Port     | Direction |   INFF   |  OUTFF   |  TRIFF   |
# Info: +----------+-----------+----------+----------+----------+
# Info: | clock    | Input     |          |          |          |
# Info: +----------+-----------+----------+----------+----------+
# Info: Total registers mapped: 0
```

PMConnect

The PMConnect module was also separately designed, synthesized and tested.

```
# Info: ******************************************************************
# Info: Device Utilization for 7A100TCSG324
# Info: ******************************************************************
# Info: Resource                          Used    Avail   Utilization
# Info: ------------------------------------------------------------------
# Info: IOs                               143     210      68.10%
# Info: Global Buffers                    0       32        0.00%
# Info: LUTs                              71      63400     0.11%
# Info: CLB Slices                        8       15850     0.05%
# Info: Dffs or Latches                   0       126800    0.00%
# Info: Block RAMs                        0       135       0.00%
# Info: DSP48E1s                          0       240       0.00%
# Info: ------------------------------------------------------------------
# Info: ******************************************************************
# Info: Library: work    Cell: pmconnect    View: pmconnect_arc
# Info: ******************************************************************
# Info:  Number of ports :                            143
# Info:  Number of nets :                             301
# Info:  Number of instances :                        227
# Info:  Number of references to this view :            0
# Info: Total accumulated area :
# Info:  Number of LUTs :                              71
# Info:  Number of Primitive LUTs :                    85
# Info:  Number of LUTs with LUTNM/HLUTNM :            28
# Info:  Number of accumulated instances :            227
# Info: ******************************
# Info:  IO Register Mapping Report
# Info: ******************************
# Info: Design: work.pmconnect.pmconnect_arc
# Info: +-------------------+-----------+----------+----------+----------+
# Info: | Port              | Direction |   INFF   |  OUTFF   |  TRIFF   |
# Info: +-------------------+-----------+----------+----------+----------+
# Info: | Rout(31)          | Input     |          |          |          |
# Info: +-------------------+-----------+----------+----------+----------+
# Info: | Rout(30)          | Input     |          |          |          |
# Info: +-------------------+-----------+----------+----------+----------+
# Info: | Rout(29)          | Input     |          |          |          |
# Info: +-------------------+-----------+----------+----------+----------+
# Info: | Rout(28)          | Input     |          |          |          |
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# Info: | Rout(27)          | Input     |          |          |          |
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# Info: | Rout(26)          | Input     |          |          |          |
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# Info: | Rout(25)          | Input     |          |          |          |
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# Info: +-------------------+-----------+----------+----------+----------+
# Info: | Rout(18)          | Input     |          |          |          |
# Info: +-------------------+-----------+----------+----------+----------+
# Info: | Rout(17)          | Input     |          |          |          |
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# Info: +-------------------+-----------+----------+----------+----------+
# Info: | Rout(16)          | Input     |          |          |          |
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# Info: | Rout(15)          | Input     |          |          |          |
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# Info: | Rout(5)           | Input     |          |          |          |
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# Info: | Rout(4)           | Input     |          |          |          |
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# Info: | Rout(3)           | Input     |          |          |          |
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# Info: | Rout(2)           | Input     |          |          |          |
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# Info: | Rout(1)           | Input     |          |          |          |
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# Info: | Rout(0)           | Input     |          |          |          |
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# Info: | Min(3)            | Output    |          |          |          |
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# Info: | Min(2)            | Output    |          |          |          |
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# Info: | Min(1)            | Output    |          |          |          |
# Info: +-------------------+-----------+----------+----------+----------+
# Info: | Min(0)            | Output    |          |          |          |
# Info: +-------------------+-----------+----------+----------+----------+
# Info: | Mout(31)          | Input     |          |          |          |
# Info: +-------------------+-----------+----------+----------+----------+
# Info: | Mout(30)          | Input     |          |          |          |
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# Info: | Mout(29)          | Input     |          |          |          |
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# Info: | Mout(25)          | Input     |          |          |          |
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# Info: | Mout(24)          | Input     |          |          |          |
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# Info: | Mout(23)          | Input     |          |          |          |
# Info: +-------------------+-----------+----------+----------+----------+
# Info: | Mout(22)          | Input     |          |          |          |
# Info: +-------------------+-----------+----------+----------+----------+
# Info: | Mout(21)          | Input     |          |          |          |
# Info: +-------------------+-----------+----------+----------+----------+
# Info: | Mout(20)          | Input     |          |          |          |
# Info: +-------------------+-----------+----------+----------+----------+
# Info: | Mout(19)          | Input     |          |          |          |
# Info: +-------------------+-----------+----------+----------+----------+
# Info: | Mout(18)          | Input     |          |          |          |
# Info: +-------------------+-----------+----------+----------+----------+
# Info: | Mout(17)          | Input     |          |          |          |
# Info: +-------------------+-----------+----------+----------+----------+
# Info: | Mout(16)          | Input     |          |          |          |
# Info: +-------------------+-----------+----------+----------+----------+
# Info: | Mout(15)          | Input     |          |          |          |
# Info: +-------------------+-----------+----------+----------+----------+
# Info: | Mout(14)          | Input     |          |          |          |
# Info: +-------------------+-----------+----------+----------+----------+
# Info: | Mout(13)          | Input     |          |          |          |
# Info: +-------------------+-----------+----------+----------+----------+
# Info: | Mout(12)          | Input     |          |          |          |
# Info: +-------------------+-----------+----------+----------+----------+
# Info: | Mout(11)          | Input     |          |          |          |
# Info: +-------------------+-----------+----------+----------+----------+
# Info: | Mout(10)          | Input     |          |          |          |
# Info: +-------------------+-----------+----------+----------+----------+
# Info: | Mout(9)           | Input     |          |          |          |
# Info: +-------------------+-----------+----------+----------+----------+
# Info: | Mout(8)           | Input     |          |          |          |
# Info: +-------------------+-----------+----------+----------+----------+
# Info: | Mout(7)           | Input     |          |          |          |
# Info: +-------------------+-----------+----------+----------+----------+
# Info: | Mout(6)           | Input     |          |          |          |
# Info: +-------------------+-----------+----------+----------+----------+
# Info: | Mout(5)           | Input     |          |          |          |
# Info: +-------------------+-----------+----------+----------+----------+
# Info: | Mout(4)           | Input     |          |          |          |
# Info: +-------------------+-----------+----------+----------+----------+
# Info: | Mout(3)           | Input     |          |          |          |
# Info: +-------------------+-----------+----------+----------+----------+
# Info: | Mout(2)           | Input     |          |          |          |
# Info: +-------------------+-----------+----------+----------+----------+
# Info: | Mout(1)           | Input     |          |          |          |
# Info: +-------------------+-----------+----------+----------+----------+
# Info: | Mout(0)           | Input     |          |          |          |
# Info: +-------------------+-----------+----------+----------+----------+
# Info: | MW(3)             | Output    |          |          |          |
# Info: +-------------------+-----------+----------+----------+----------+
# Info: | MW(2)             | Output    |          |          |          |
# Info: +-------------------+-----------+----------+----------+----------+
# Info: | MW(1)             | Output    |          |          |          |
# Info: +-------------------+-----------+----------+----------+----------+
# Info: | MW(0)             | Output    |          |          |          |
# Info: +-------------------+-----------+----------+----------+----------+
# Info: Total registers mapped: 0
# Info: [12022]: Design has no timing constraint and no timing information.
```
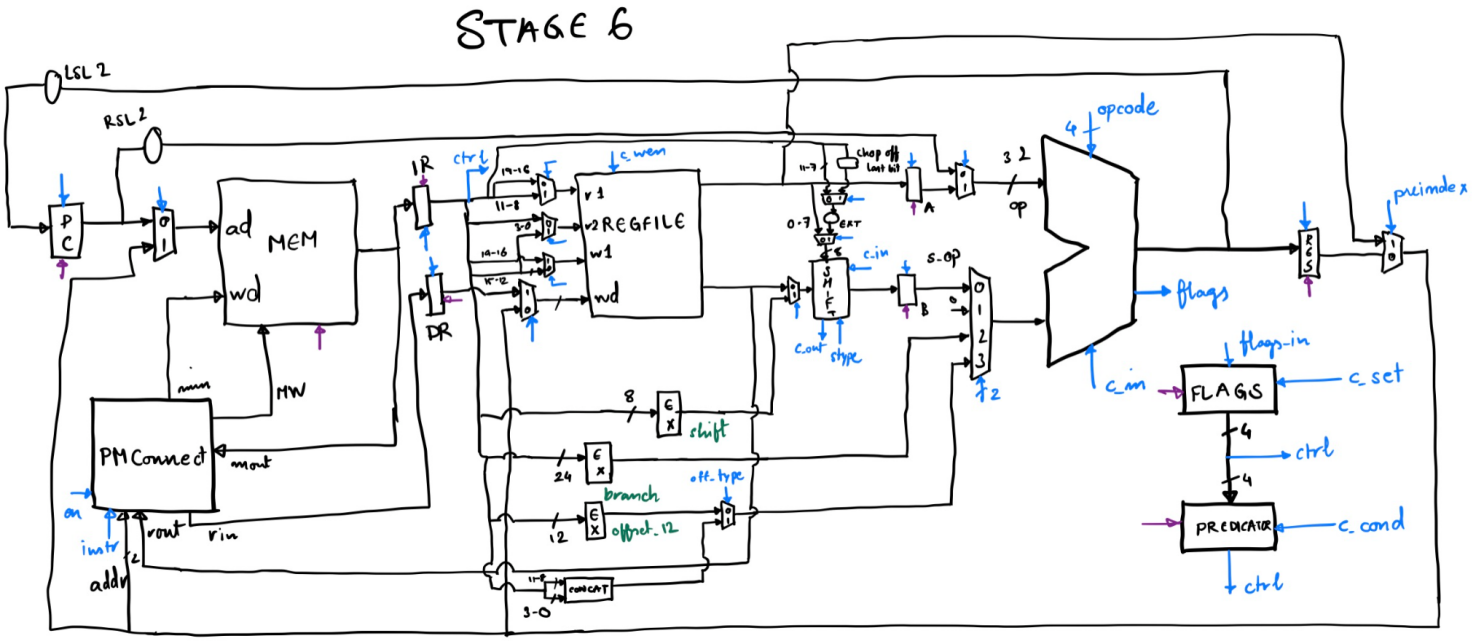

Design and Verification

The design to be implemented was as follows:



Note the addition of the extra multiplexer for the regfile write address, as we would be needed to write to Rn (19-16) in the case of an update. The design also allows for pre-indexed reading (directly taking the value for the memory write address from the register file), as well as post-indexed addressing. Finally, an extra mux/modifications are made to unify and supply the immediate offset for load/store half word instructions (the address is split between a high nibble and a low nibble)

The state diagram remains the same; for writeback during data transfer instructions, we write back to the register file in the writeback_dt_str state and the load_dt_ldr state (writeback_dt_ldr writes to the regfile, so we can't update Rn simultaneously), hence we need to introduce no new states for writing.