COL216 Assignment 2

Stage 1 report

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2020CS10869

Summary

This project implemented an ALU with 16 operations, the register file and the program/data memory files in VHDL. Testing was done partly in GHDL/GtkWave (easy to use on Mac, better waveform viewer) and on EDAPlayground (class-mandated, used for synthesis). The code uses the IEEE libraries `numeric_std` and `std_logic_1164`.

File Structure

```
2020CS10869.zip
├── alu.vhdl
├── alu_tb.vhdl
├── logs (stores synthesis report from EDAPlayground)
│   ├── alu_synth_log.txt
│   ├── data_mem_synth_log.txt
│   ├── prog_mem_synth_log.txt
│   └── regfile_synth_log.txt
├── mem.vhdl
├── mem_tb.vhdl
├── regfile.vhdl
├── regfile_tb.vhdl
├── report.pdf
├── run.do
├── wave_imgs (images of waveform tests)
│   ├── alu_test.png
│   ├── memfile_byte_test.png
│   ├── memfile_test.png
│   ├── regfile_altera_test.png
│   └── regfile_test.png
└── waves (GHDL waveforms, can be viewed through a wave viewer)
    ├── alu_tb.ghw
    ├── data_mem_tb.ghw
    ├── prog_mem_tb.ghw
    └── regfile_tb.ghw
```

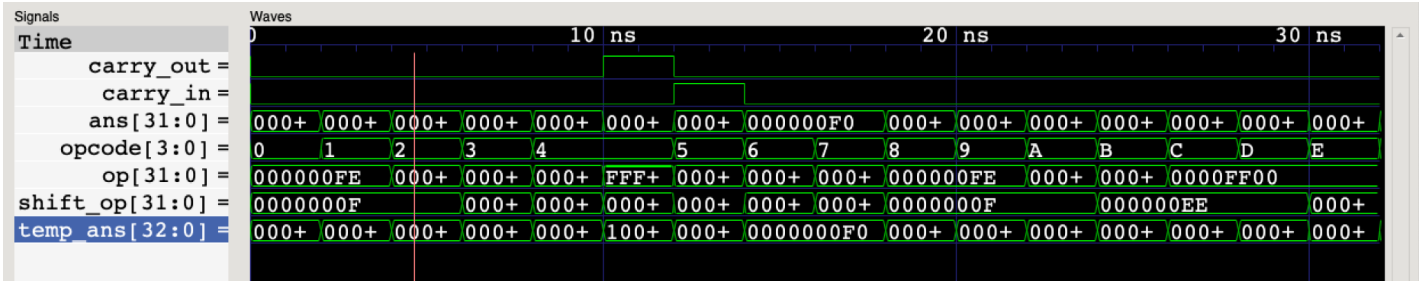
Program Details

- `alu.vhdl` - contains the ALU entity and it's behaviour.
- `mem.vhdl` - contains the Program and Data memories and their architectures. Program memory is Read only, and the read only encoding of the memory has to be done on initialization (I haven't initialized the memory, this is left to the programmer to do in his/her implementation)
- `regfile.vhdl` - contains the Register file entity and it's behaviour

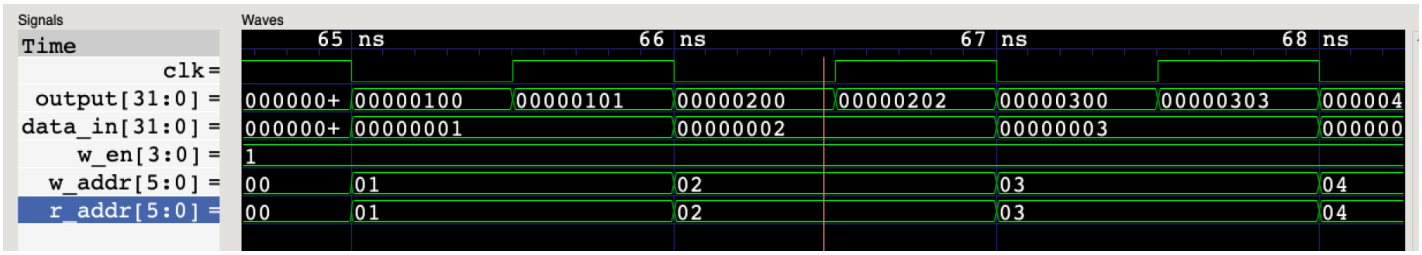
Testing

Associated testbenches are marked with `<filename>_tb.vhdl`. The testbenches have been made as extensive as possible, and the ALU testbench checks all 16 operations along with checking carry over functionality. Additional waveform snapshots have been attached here

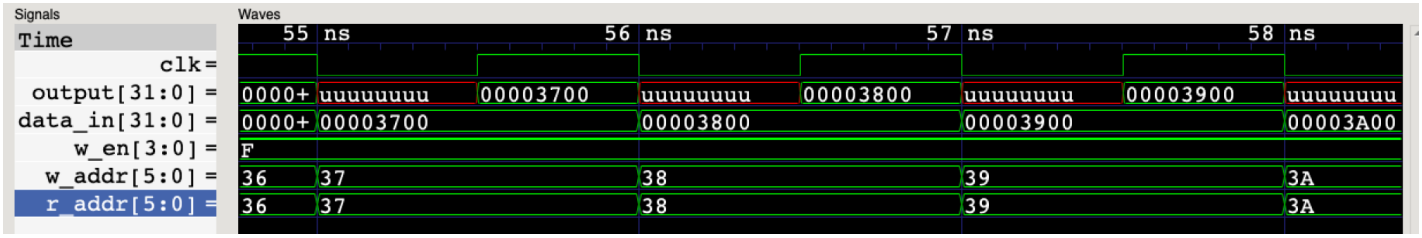
alu_test:



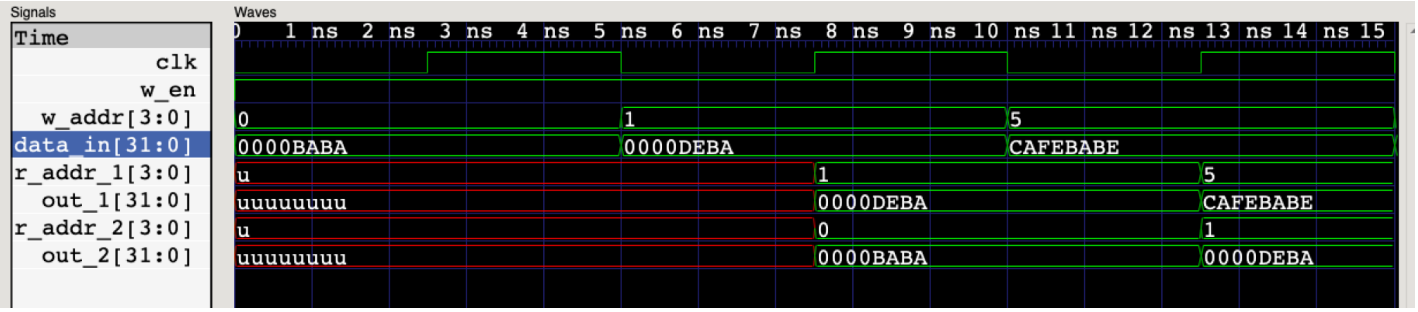
memfile_byte_test (writing bytes)



memfile_test (writing directly to memory file)



regfile_test (register file writing/reading)



Synthesis

Synthesis logs are placed in the `logs` folder. A small summary of the syntheses are shown here

ALU:

```
# Info: ************************************************************
# Info: Device Utilization for 7A100TCSG324
# Info: ************************************************************
# Info: Resource                          Used    Avail   Utilization
# Info: ------------------------------------------------------------
# Info: IOs                               102     210      48.57%
# Info: Global Buffers                    0       32        0.00%
# Info: LUTs                              133     63400     0.21%
# Info: CLB Slices                        33      15850     0.21%
# Info: Dffs or Latches                   0       126800    0.00%
# Info: Block RAMs                        0       135       0.00%
# Info: DSP48E1s                          0       240       0.00%
# Info: ------------------------------------------------------------
# Info: ****************************************************
# Info: Library: work    Cell: alu    View: alu_bvr
# Info: ****************************************************
# Info:  Number of ports :                          102
# Info:  Number of nets :                           435
# Info:  Number of instances :                      366
# Info:  Number of references to this view :          0
# Info: Total accumulated area :
# Info:  Number of LUTs :                           133
# Info:  Number of Primitive LUTs :                 134
# Info:  Number of LUTs with LUTNM/HLUTNM :           2
# Info:  Number of MUX CARRYs :                      64
# Info:  Number of accumulated instances :          366
```

Data Memory:

```
# Info: ***********************************************************
# Info: Device Utilization for 7A100TCSG324
# Info: ***********************************************************
# Info: Resource                          Used    Avail   Utilization
# Info: -----------------------------------------------------------
# Info: IOs                               81      210      38.57%
# Info: Global Buffers                    1       32        3.12%
# Info: LUTs                              64      63400     0.10%
# Info: CLB Slices                        16      15850     0.10%
# Info: Dffs or Latches                   0       126800    0.00%
# Info: Block RAMs                        0       135       0.00%
# Info: Distributed RAMs
# Info:    RAM64X1D                       32
# Info: DSP48E1s                          0       240       0.00%
# Info: -----------------------------------------------------------
# Info: ***********************************************************
# Info: Library: work    Cell: data_mem    View: data_mem_bvr
# Info: ***********************************************************
# Info:  Number of ports :                            81
# Info:  Number of nets :                            162
# Info:  Number of instances :                        82
# Info:  Number of references to this view :           0
# Info: Total accumulated area :
# Info:  Number of LUTs :                             64
# Info:  Number of Primitive LUTs :                   64
# Info:    Number of LUTs as Distributed RAM :        64
# Info:  Number of accumulated instances :           113
```

Program Memory:

```
# Info: ***********************************************************
# Info: Device Utilization for 7A100TCSG324
# Info: ***********************************************************
# Info: Resource                          Used    Avail   Utilization
# Info: -----------------------------------------------------------
# Info: IOs                               38      210      18.10%
# Info: Global Buffers                    0       32        0.00%
# Info: LUTs                              0       63400     0.00%
# Info: CLB Slices                        0       15850     0.00%
# Info: Dffs or Latches                   0       126800    0.00%
# Info: Block RAMs                        0       135       0.00%
# Info: DSP48E1s                          0       240       0.00%
# Info: -----------------------------------------------------------
# Info: ***********************************************************
# Info: Library: work    Cell: prog_mem    View: prog_mem_df
# Info: ***********************************************************
# Info:  Number of ports :                            38
# Info:  Number of nets :                             33
# Info:  Number of instances :                        33
# Info:  Number of references to this view :           0
# Info: Total accumulated area : unknown
```

Register File:

```
# Info: ******************************************************************
# Info: Device Utilization for 7A100TCSG324
# Info: ******************************************************************
# Info: Resource                          Used    Avail   Utilization
# Info: ------------------------------------------------------------------
# Info: IOs                               110     210      52.38%
# Info: Global Buffers                    1       32        3.12%
# Info: LUTs                              48      63400     0.08%
# Info: CLB Slices                        12      15850     0.08%
# Info: Dffs or Latches                   0       126800    0.00%
# Info: Block RAMs                        0       135       0.00%
# Info: Distributed RAMs
# Info:    RAM32M                         10
# Info:    RAM64M                         2
# Info: DSP48E1s                          0       240       0.00%
# Info: ------------------------------------------------------------------
# Info: ************************************************************
# Info: Library: work    Cell: regfile    View: regfile_bvr
# Info: ************************************************************
# Info:  Number of ports :                           110
# Info:  Number of nets :                            220
# Info:  Number of instances :                       111
# Info:  Number of references to this view :           0
# Info: Total accumulated area :
# Info:  Number of LUTs :                             48
# Info:  Number of Primitive LUTs :                   48
# Info:    Number of LUTs as Distributed RAM :        48
# Info:  Number of accumulated instances :           123
# Info: ****************************
```