Unit 2

Types of Materials

Insulators

- An insulator is a material that does not conduct electrical current under normal conditions.
- Rubber, plastics, glass, mica, and quartz.

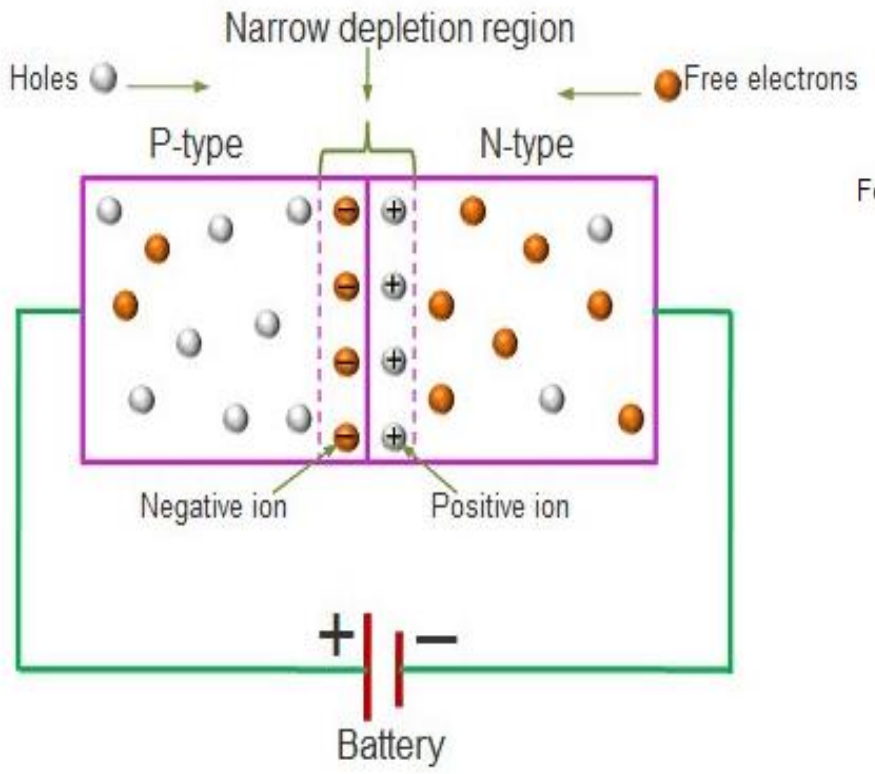
Conductors

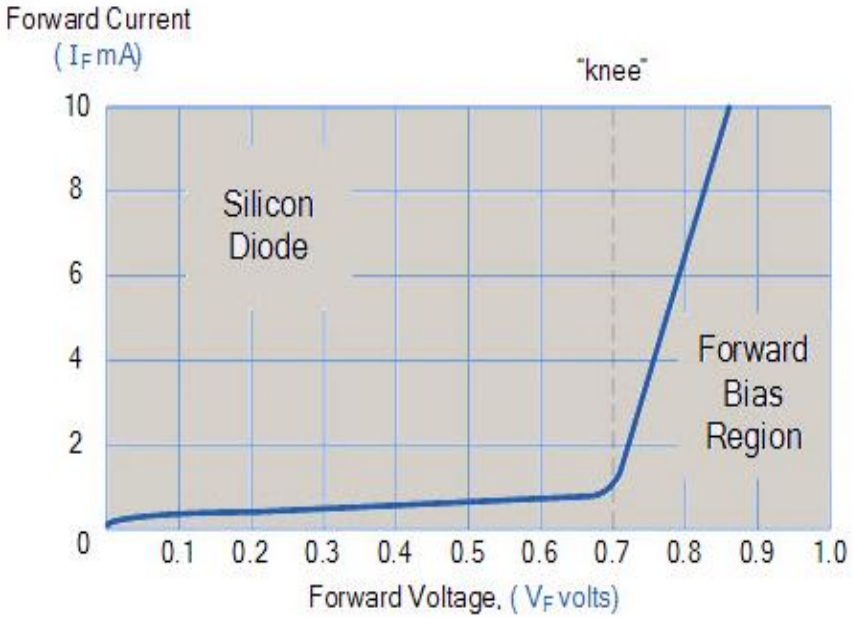
- A conductor is a material that easily conducts electrical current. Most metals are good conductors.
- Copper (Cu), silver (Ag), gold (Au), and aluminum (Al)

Semiconductors

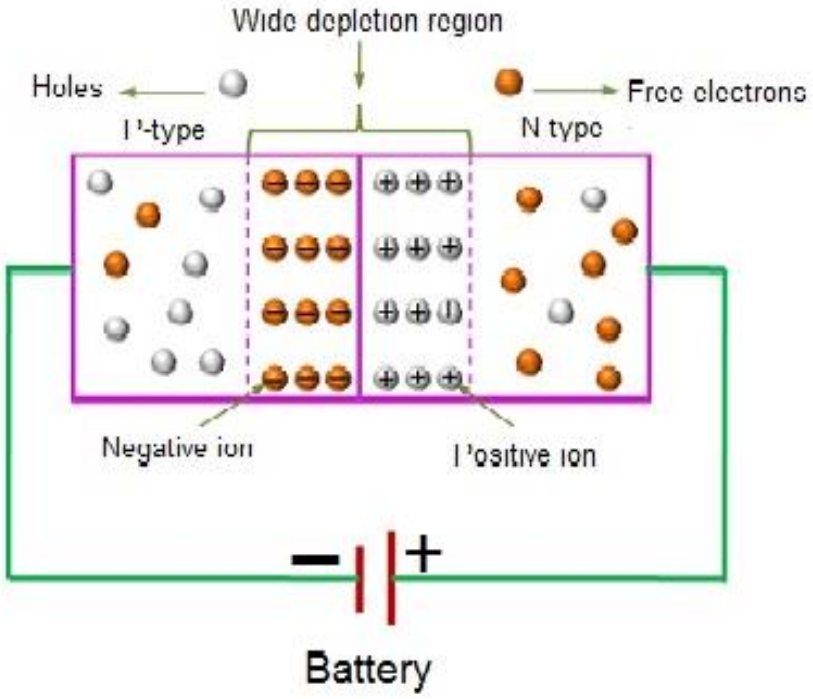
- A semiconductor is a material that is between conductors and insulators in its ability to conduct electrical current.
- Silicon (Si), and germanium (Ge)

PN Diode – Forward Bias

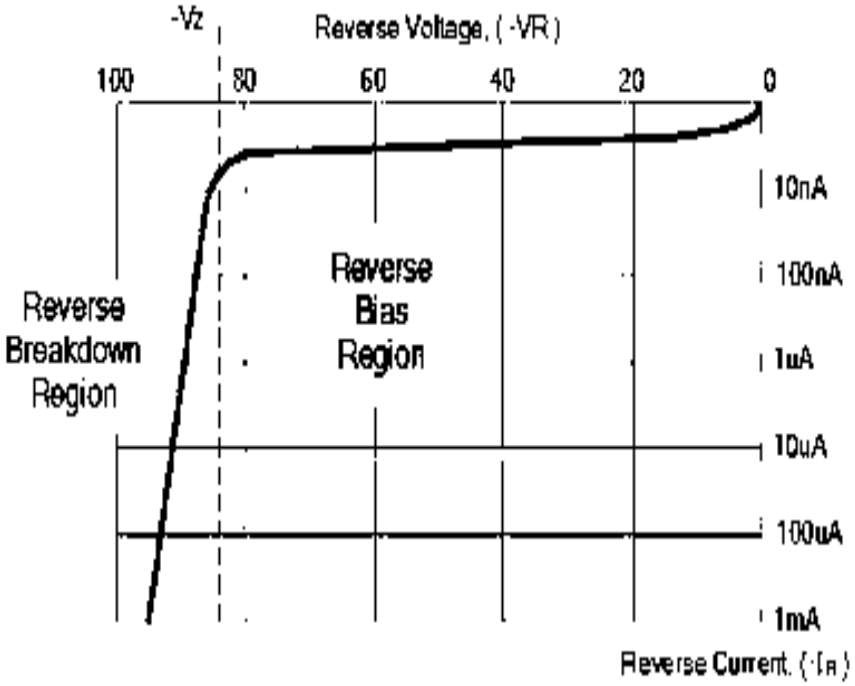




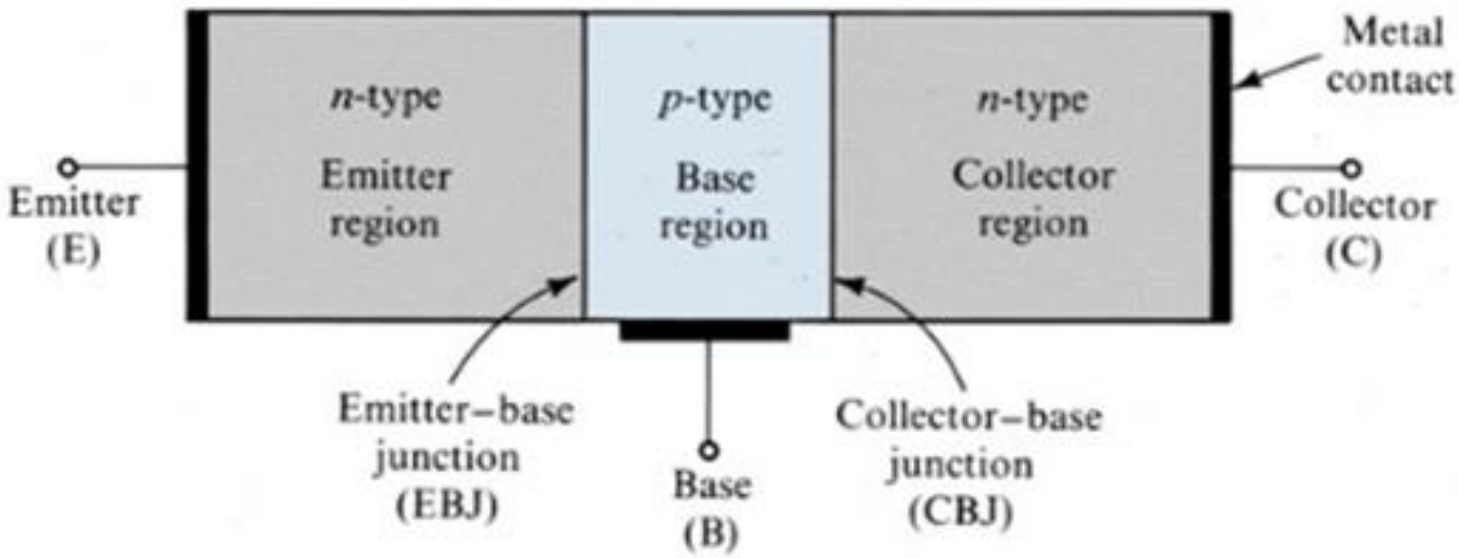
PN Diode – Reverse Bias



PN Junction Diode in Reverse Bias

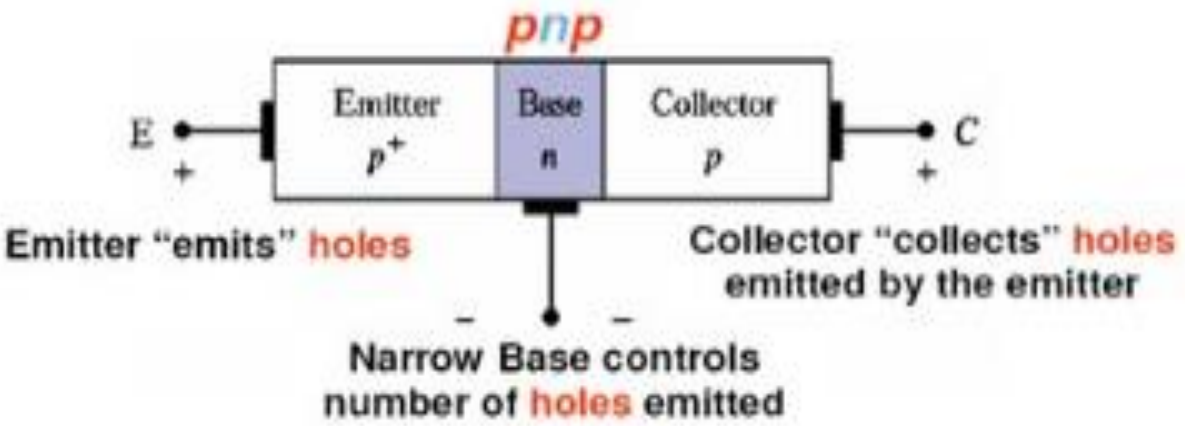


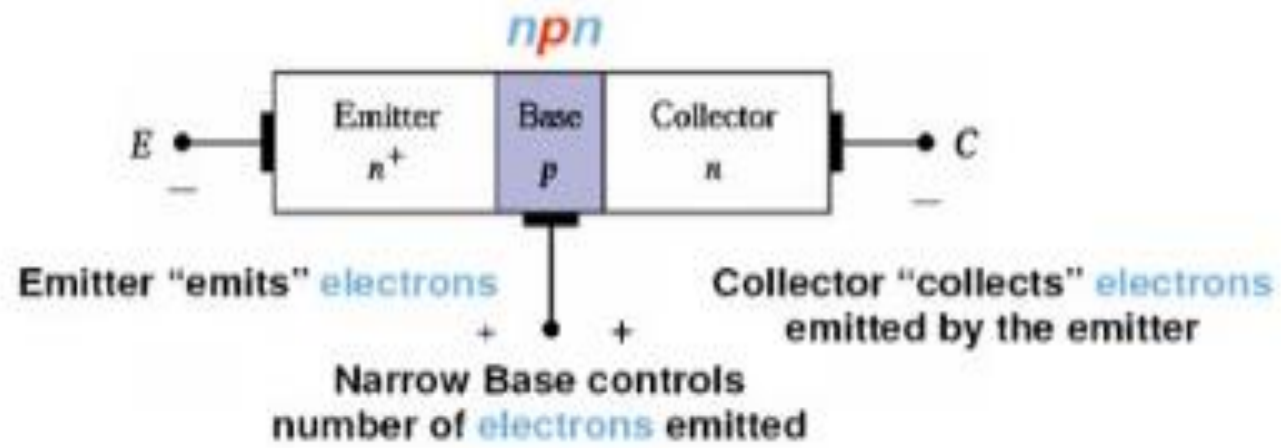
Bipolar Junction Transistor



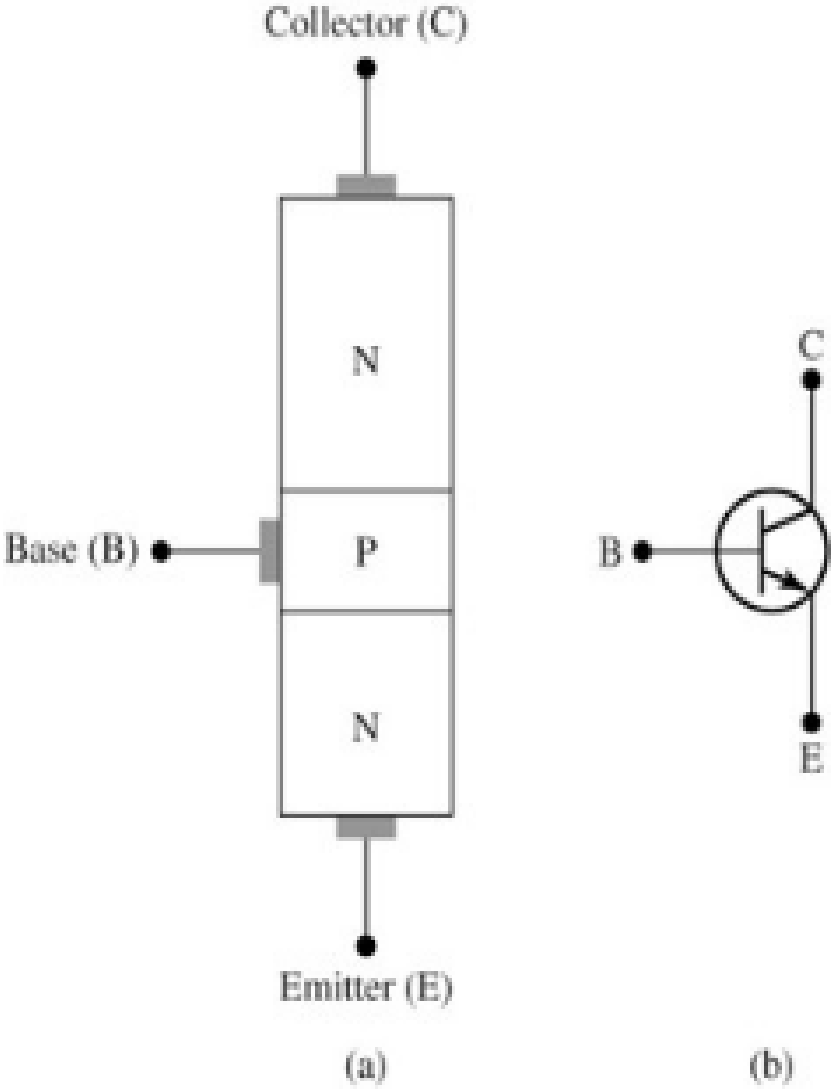
- **Bipolar** : both electrons and holes are involved in current flow.
- **Junction** : has two *p-n* junctions.
- **Transistor** : Transfer + Resistor.
- It can be either ***n-p-n*** type or ***p-n-p*** type.
- Has three regions with three terminals labeled as
  - i. Emitter (E)
  - ii. Base (B) and
  - iii. Collector (C)

- **Base** is made much narrow.
- **Emitter** is heavily doped (p^+, n^+).
- **Base** is lightly doped (p, n).
- **Collector** is lightly doped (p, n).

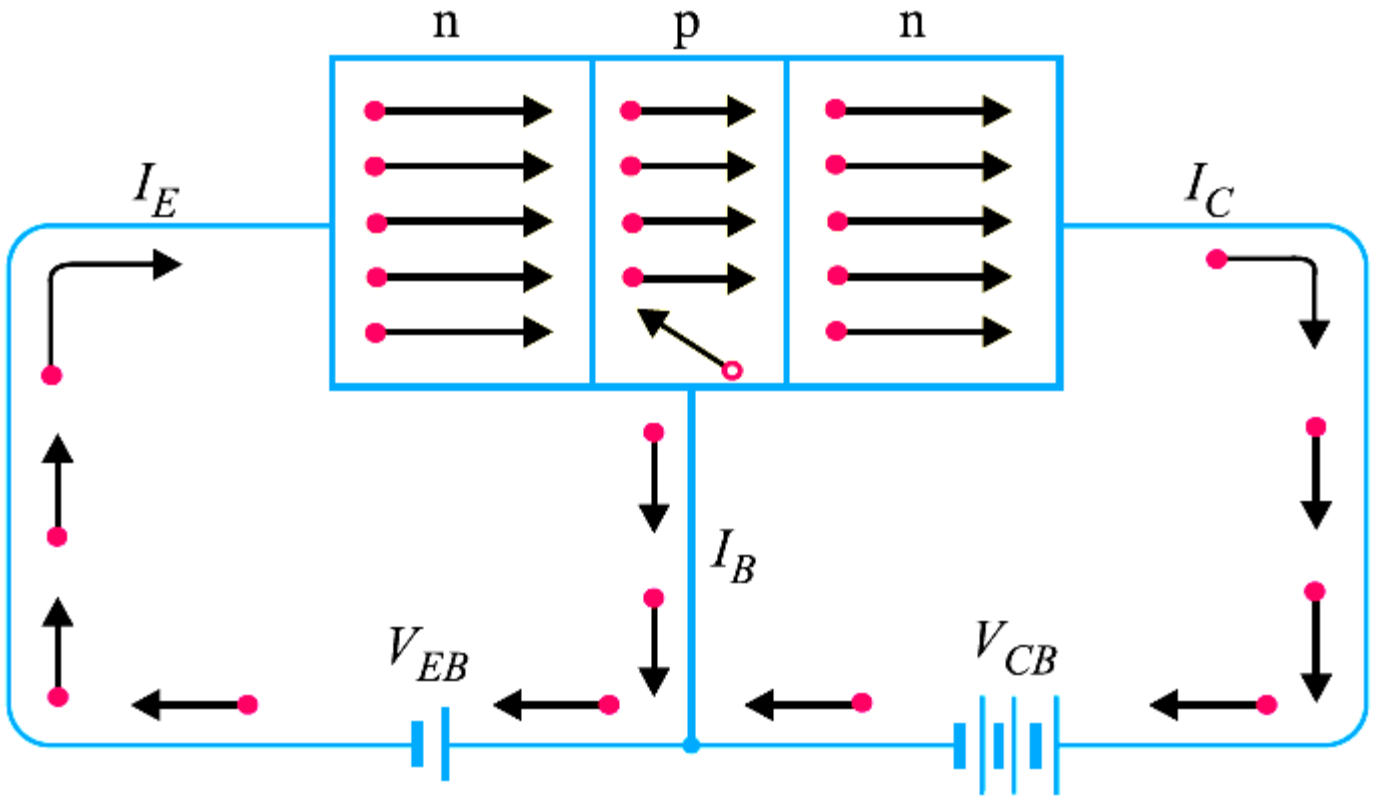




Layout and Circuit Symbol: n-p-n Transistor



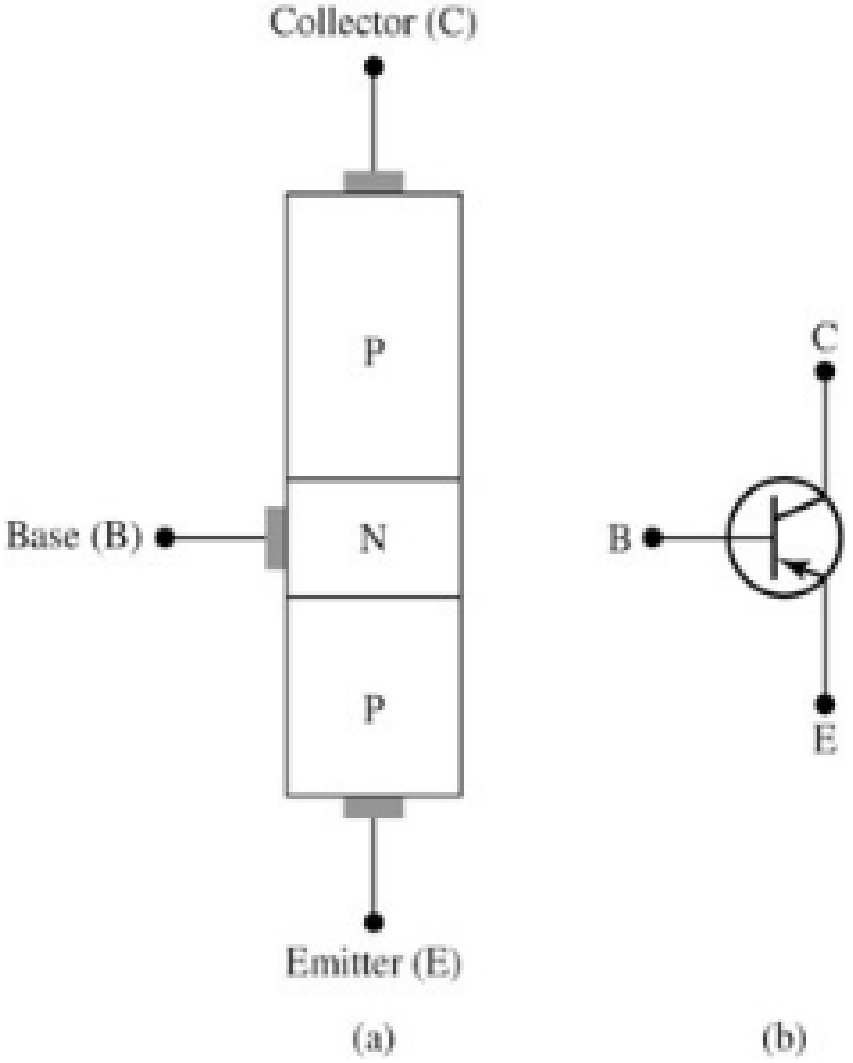
- The arrow indicates the direction of current flow.
- The current flows from collector to emitter in an n-p-n transistor.
- The arrow is drawn on the emitter.
- The arrow always points towards the n-type. So the emitter is n-type and the transistor is n-p-n type.



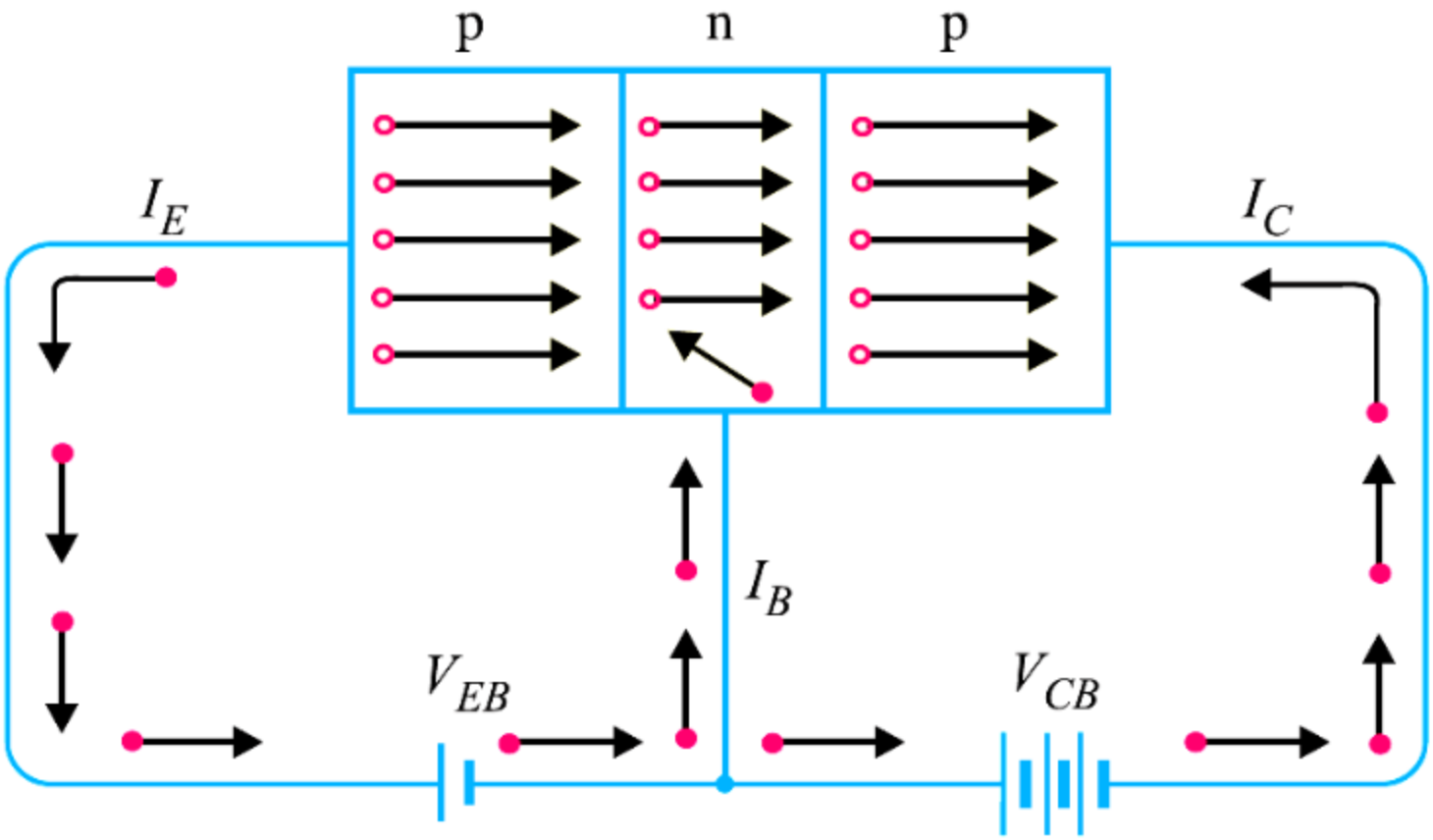
Basic connection of *npn* transistor

$$\mathbf{I_E = I_B + I_c}$$

Layout and Circuit Symbol: p-n-p Transistor



- The arrow indicates the direction of current flow.
- The current flows from emitter to collector in an p-n-p transistor.
- The arrow points towards the n-type.
- So the base is n-type and transistor is p-n-p type.



Basic connection of *pnp* transistor

$$\mathbf{I_E = I_B + I_c}$$

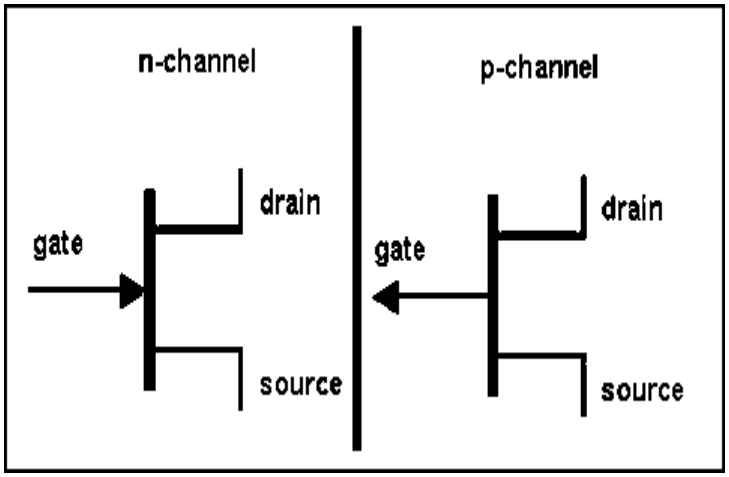
Uses of BJT

- The bipolar junction transistor (BJT) is used in logic circuits.
- The BJT is used as an oscillator.
- It is used as an amplifier.
- It is used as a multivibrator.
- For wave shaping, it is used in clipping circuits.
- Used as a detector or demodulator.
- It is also used as a modulator.
- Used in timer and time delay circuits.
- It is used in electronics switch.
- It is used in switching circuits.

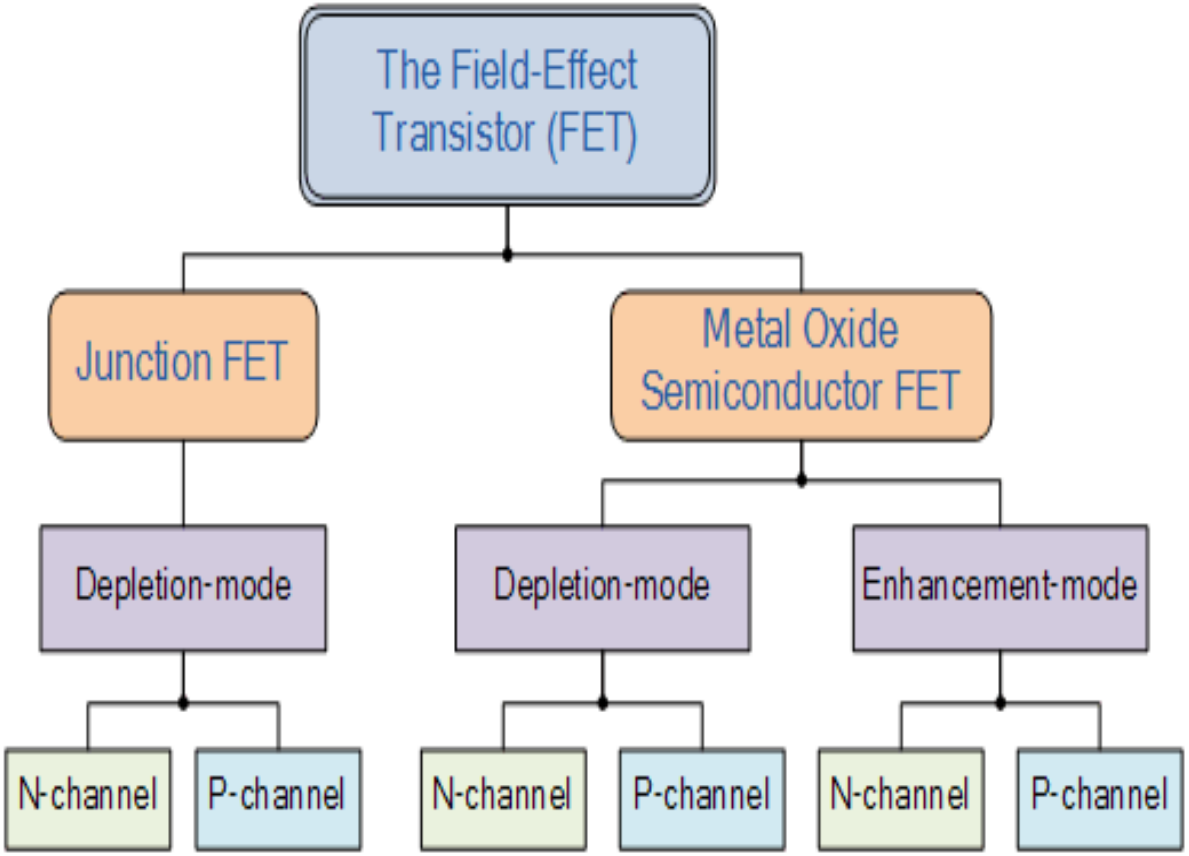
Field Effect Transistor (FET)

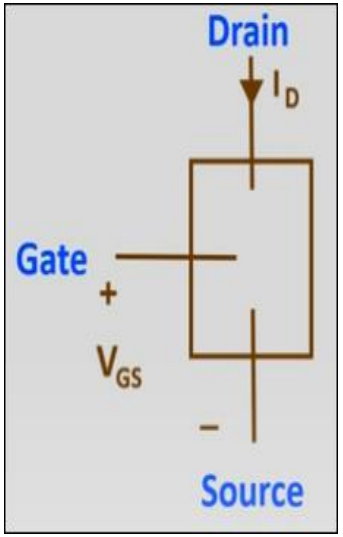
- Field effect transistors (FETs) are usually termed as unipolar transistors because these FETs operations are involved with single-carrier type.
- Electric field – to control current flow.
- It has 3 terminals.
  - Source (S)
  - Drain (D)
  - Gate (G)

Symbol

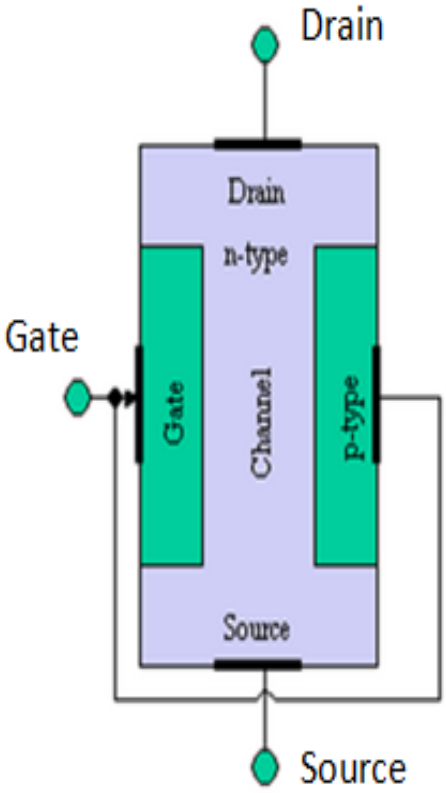


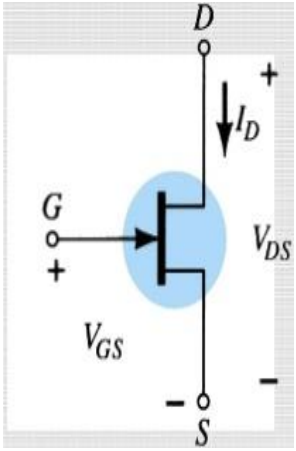
FET - Types


The Field-Effect Transistor (FET)
Junction FET
Metal Oxide Semiconductor FET
Depletion-mode
Depletion-mode
Enhancement-mode
N-channel
P-channel
N-channel
P-channel
N-channel
P-channel

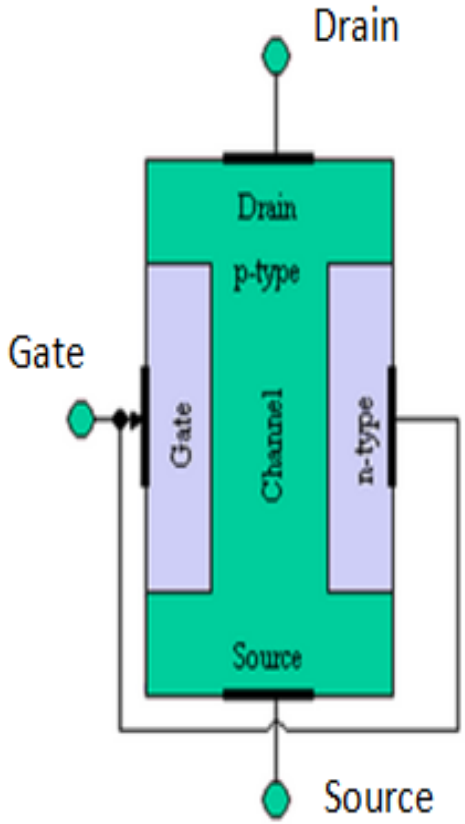

Drain
I_D
Gate
+
V_{GS}
–
Source

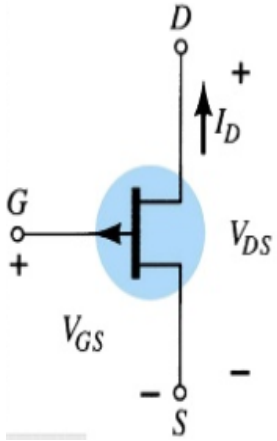
JFET Construction & Symbol





n-channel JFET





p-channel JFET

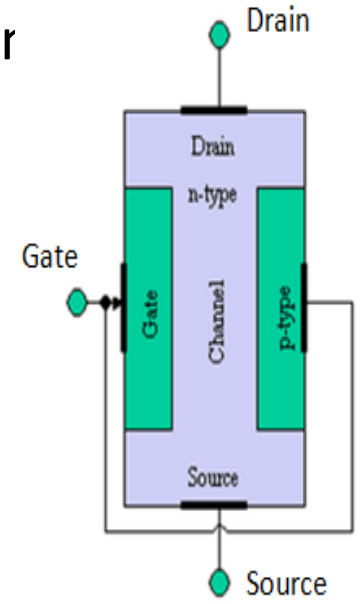
JFET Working

There are 3 basic operating conditions of JFET: (operates only in reverse bias)

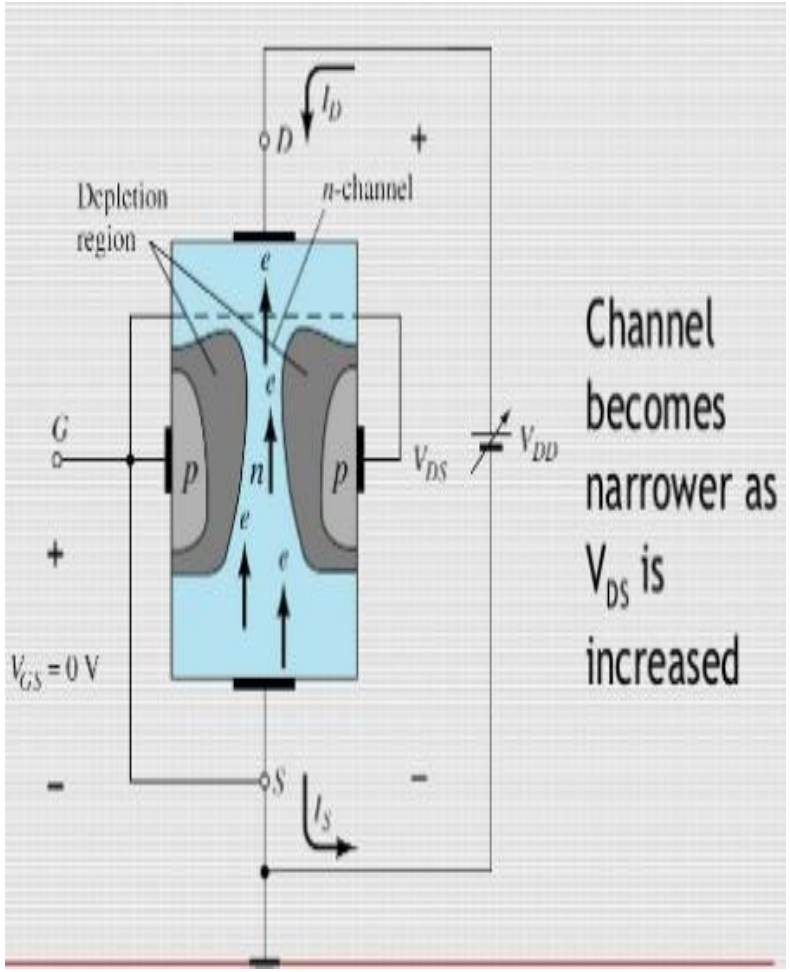
(i) Vgs = 0, Vds = +Ve (Vds increasing ir ich is less than pinch off voltage)

(ii) Vgs < 0, Vds = 0 (No operation)

(iii) Vgs < 0, Vds = +Ve

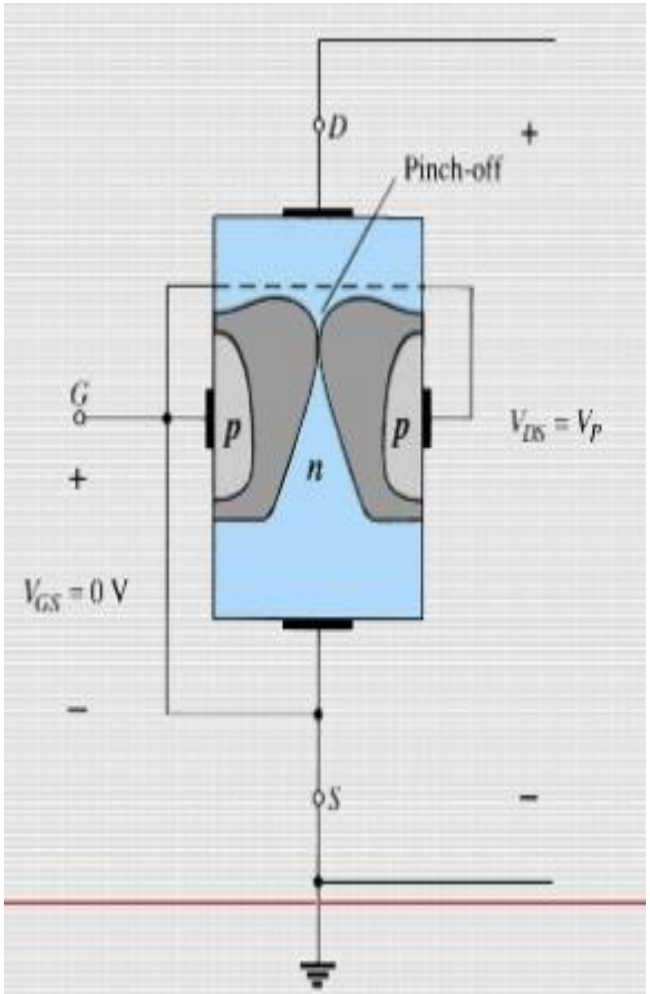


(i) When Vgs=0 , Vds = +Ve (Less than Vp)

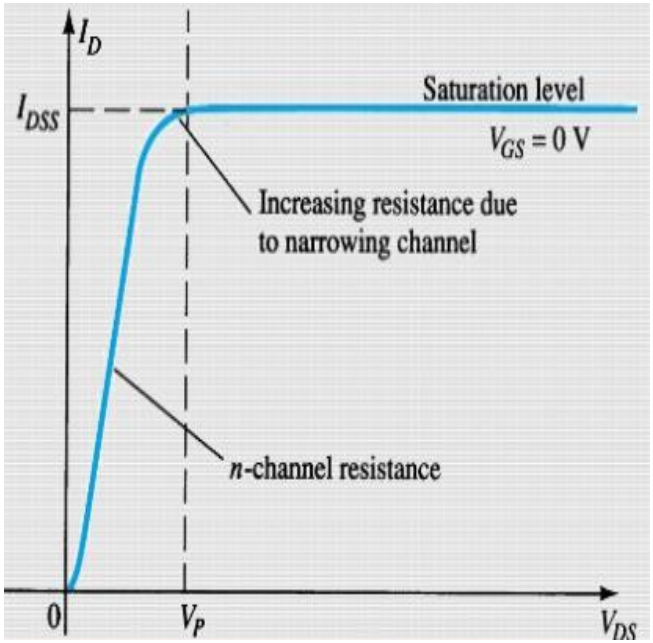


- When a voltage V_{DS} is applied between drain and source terminals and voltage on the gate is zero, the two pn junctions at the sides of the bar establish depletion layers.
- The electrons will flow from source to drain through a channel between the depletion layers.
- The size of the depletion layers determines the width of the channel and hence current conduction through the bar.

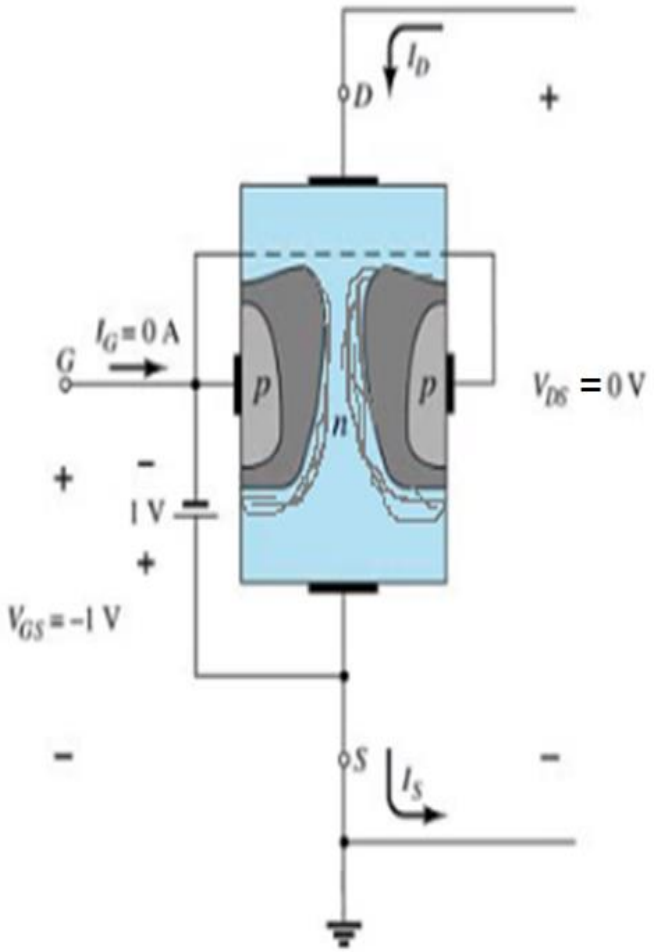
When Vds = Vp (at Vgs = 0)



- For larger value of Vds, the depletion layer becomes wider, causing the resistance of the channel increases.
- When **Vds = Vp, the Id current becomes constant.**
- It is maximum drain current, also called Idss.

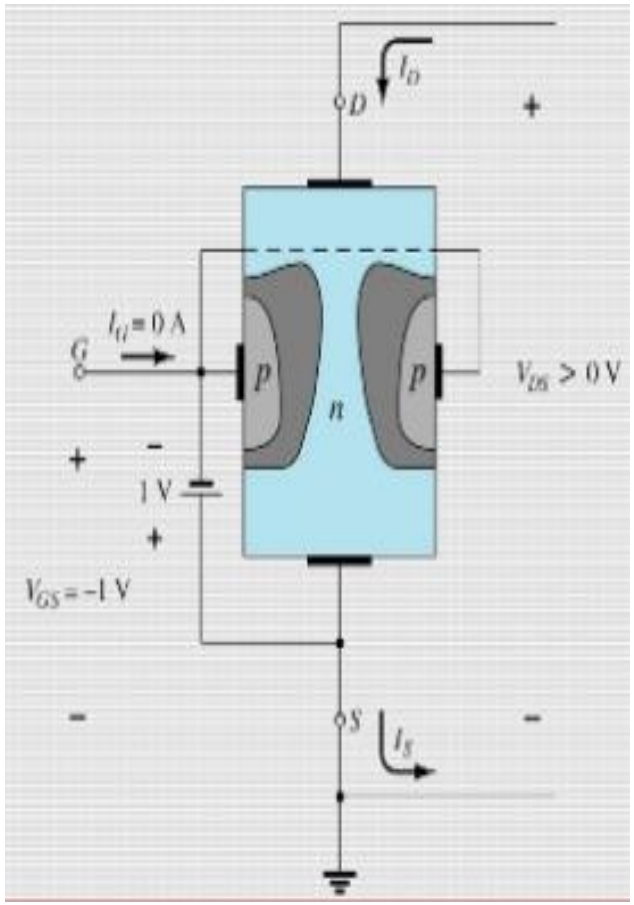


(ii) When Vgs<0, Vds=0

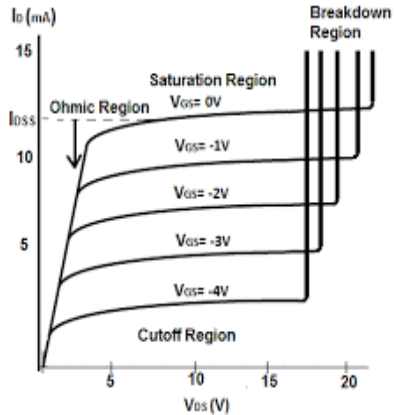


- When Vgs<0, Vds=0, it leads to reverse bias gate to channel.
- Width of the depletion layer increases, leads to reduce the drain current in the device.

(iii) When Vgs<0, Vds = +Ve



- For negative value of Vgs, the gate to channel junction is reverse biased even for Vds=0.
- Then the resistance of the channel is higher, leads to reduce the Id current value.
- When Vgs<0, Vds=+Ve, where Id current starts to reduce.
- When Vgs=Vp, the device reach cut-off region.
- Id constant – saturation region.
- Id depends on Vds – ohmic region

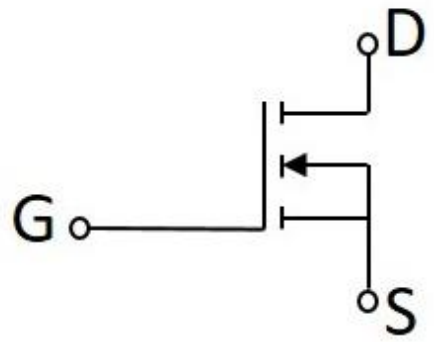


COMPARISON BETWEEN BJT AND JFET

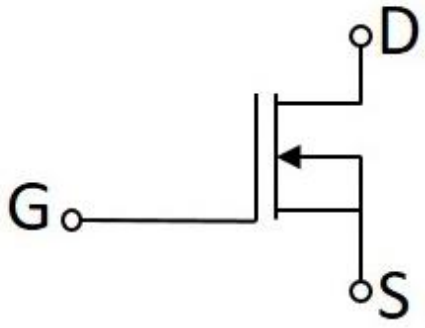
BJT	JFET
Bipolar device (current condition, by both types of carriers, i.e. majority and minority-electrons and hole).	Unipolar device (current conduction is only due to one type of majority carrier either electron or hole).
The operation depends on the injection of minority carries across a forward biased junction.	The operation depends on the control of a junction depletion width under reverse bias.
Current controlled device. The base current controls the output current.	Voltage controlled device. The gate voltage controls output current.
High noise level. (current conduction through junctions)	Low noise level. (current conduction is through n-channel or p-channel and no junction crossing)
Low input impedance (due to forward bias at input side).	High input impedance (due to reverse bias).
Gain is characterized by voltage gain.	Gain is characterised by transconductance.
Low thermal stability. (positive temperature coefficient at high current levels lead to thermal breakdown)	Better thermal stability.(NTC at high current levels prevent thermal breakdown)
Cheaper	Relatively costly

Types of MOSFETS

Symbols of N-Channel MOSFET

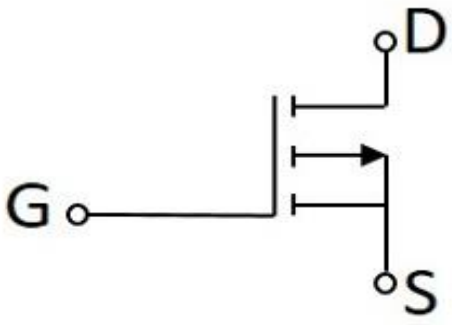


Enhancement Mode

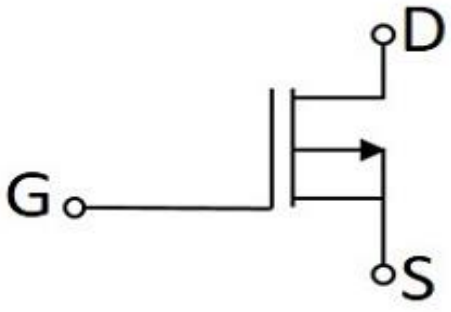


Depletion Mode

Symbols of P-Channel MOSFET

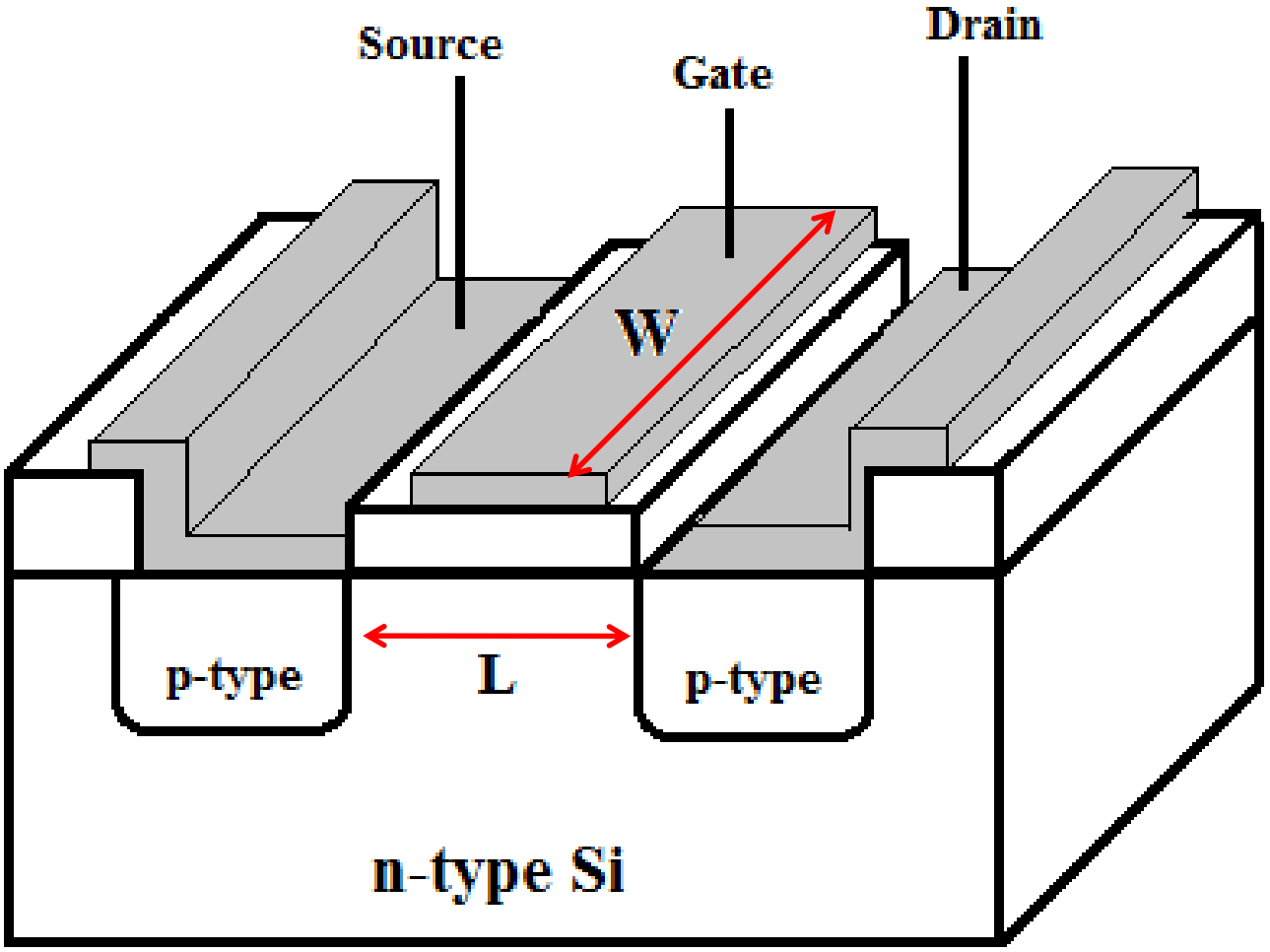


Enhancement Mode

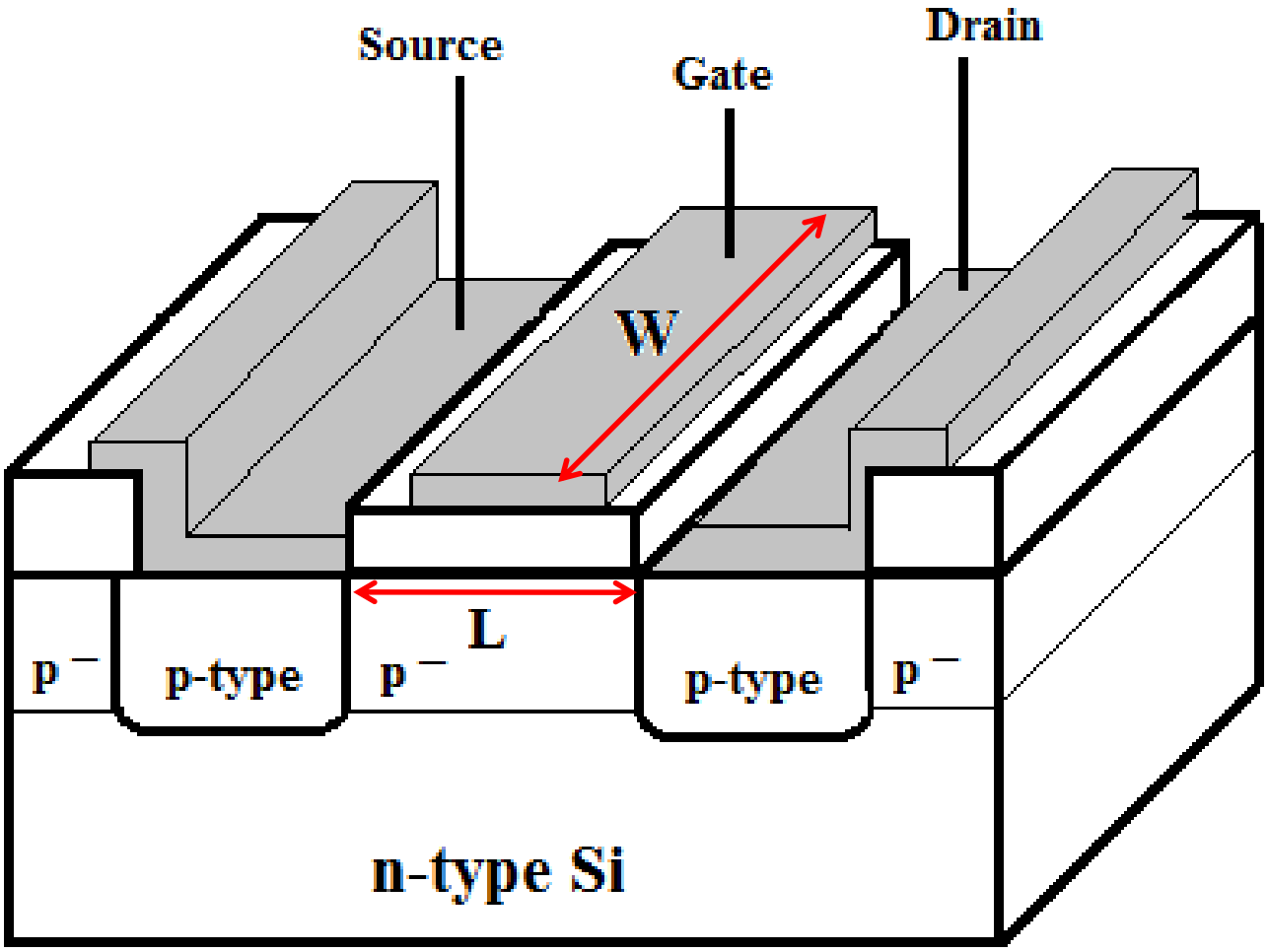


Depletion Mode

P-channel
Enhancement Mode Transistor



P-channel
Depletion Mode Transistor



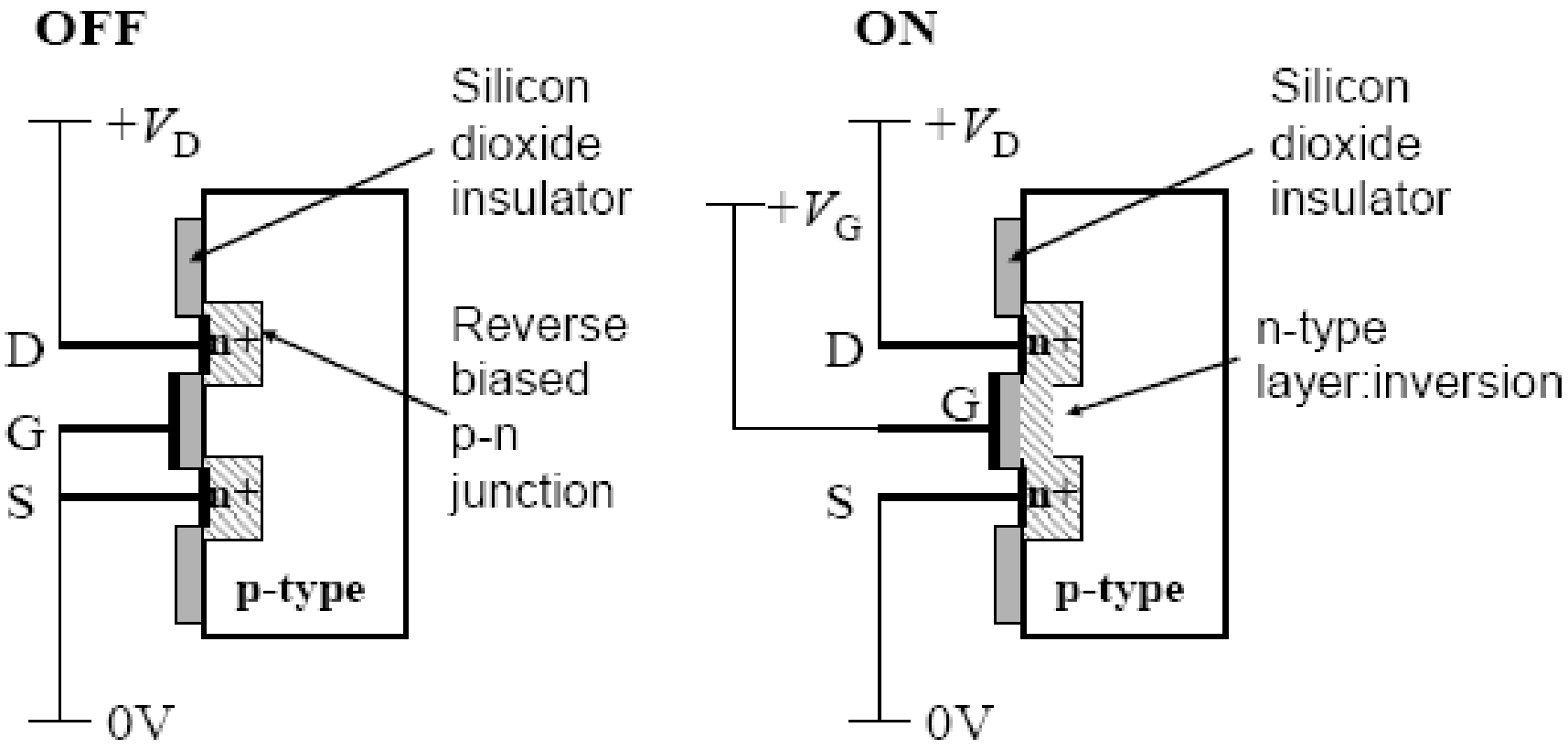
Enhancement MOSFET

- MOSFETs with enhancement modes can be switched on by powering the gate either higher than the source voltage for NMOS or lower than the source voltage for the PMOS.
- In most circuits, this means that pulling a MOSFET gate voltage into the leakage boost mode becomes ON.
- For N-type discharging devices, the threshold voltage could be about -3 V, so it could be stopped by dragging the 3 V negative gate (leakage by comparison is more positive than the NMOS source).
- In PMOS, polarities are reversed.
- The mode can be determined by the voltage threshold sign (gate voltage versus source voltage at the point where only a layer inversion is formed in the channel):
- For a N-type FET, modulation devices have positive and depleted thresholds – modulated devices have negative thresholds;
- For a P-type FET, positive mode to improve negative mode, depletion.

Depletion type MOSFET

- Junction-effect junction transistors are the depletion mode because the gate junction would transmit the bias if the gate was taken more than a bit from the source to the drain voltage.
- Such devices are used in gallium-arsenide and germanium chips, where it is difficult to make an oxide isolator.
- Figure describes the construction of MOSFET type of exhaustion. Also note the MOSFET circuit type N exhaust channel symbol.
- Due to its construction, it offers very high entry strength (approximately 1010 to 1015). Significant current flows for V_{DS} data at 0 volts V_{GS}.
- When the gate (ie, a capacitor plate) is made positive, the channel (i.e., the other capacitor plate) will have a positive charge induced therein.
- This will lead to the depletion of the major bearers (ie electrons) and therefore to the reduction in conductivity.

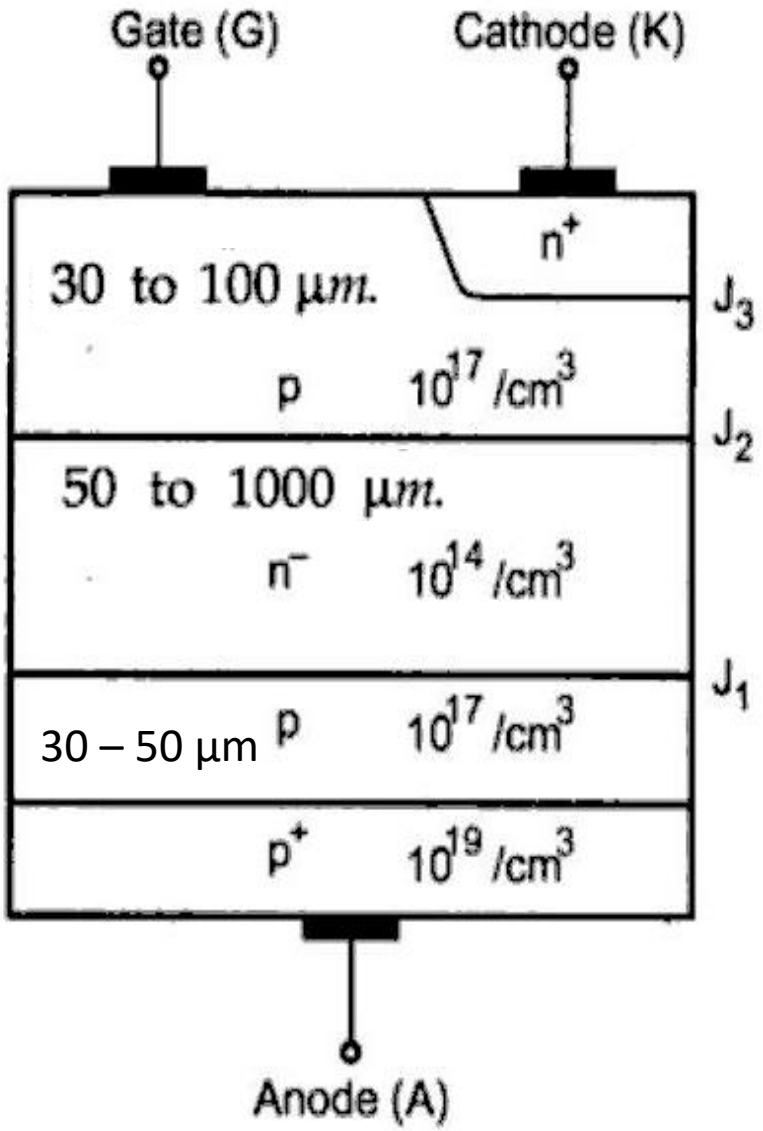
n-Channel MOSFET



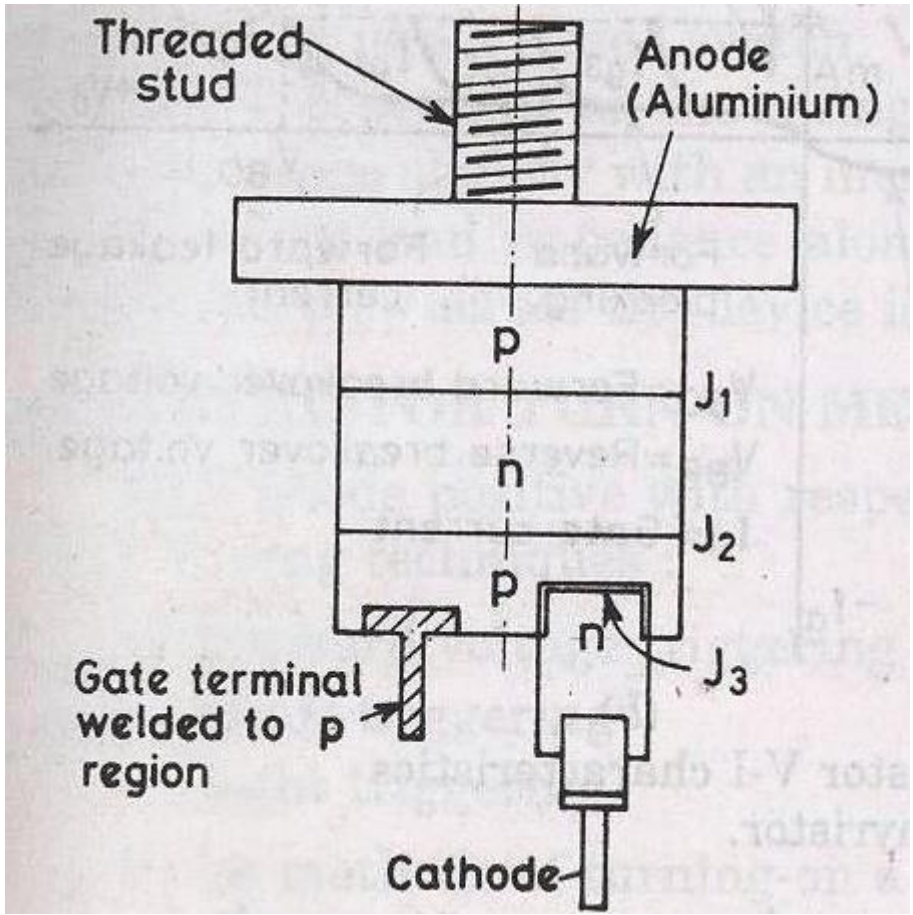
SCR (Silicon Controlled Rectifier)

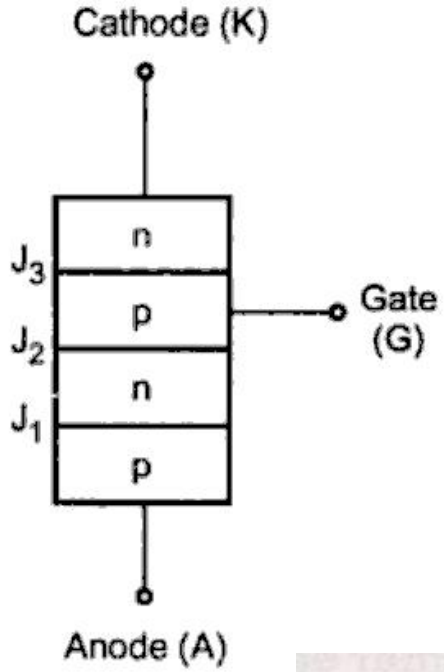
- Most commonly used device.
- Characteristics of SCR is similar as that of THYRATRON TUBE.
- Construction is similar to TRANSISTOR family.
- The name 'THYRISTOR' derived from THYRatron and transISTOR

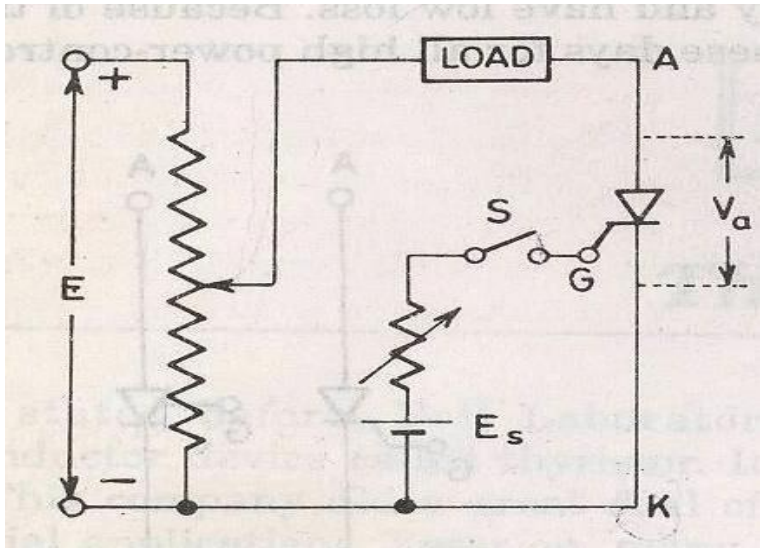
Structure of SCR

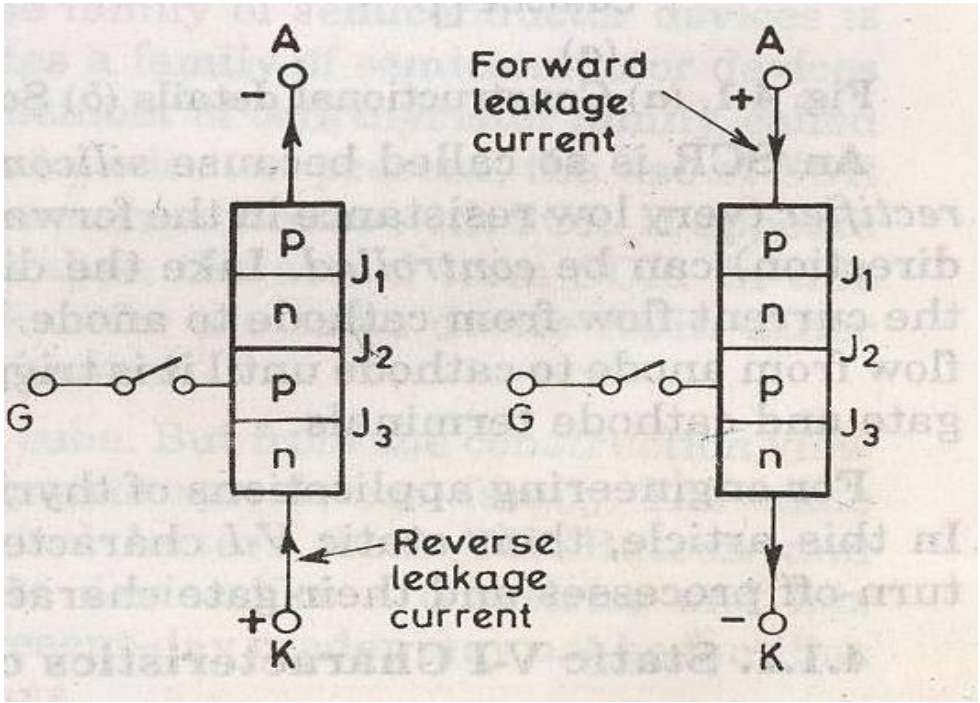


or



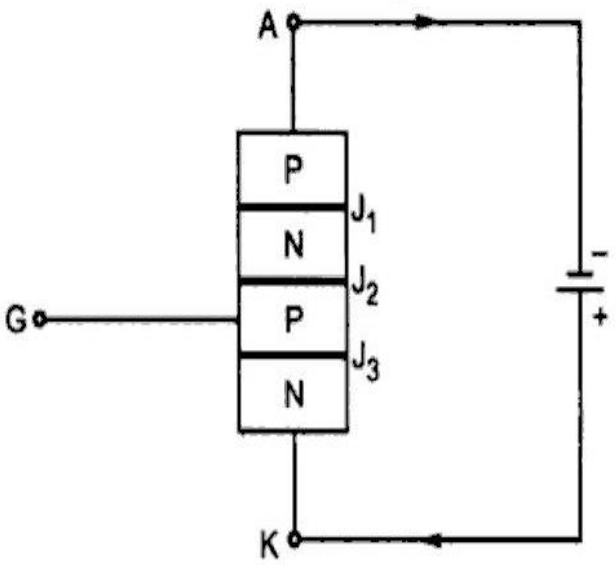

Cathode (K)
n
p
n
p
J_3
J_2
J_1
Gate
(G)
Anode (A)


LOAD
A
+
E
−
S
G
V_a
E_s
K

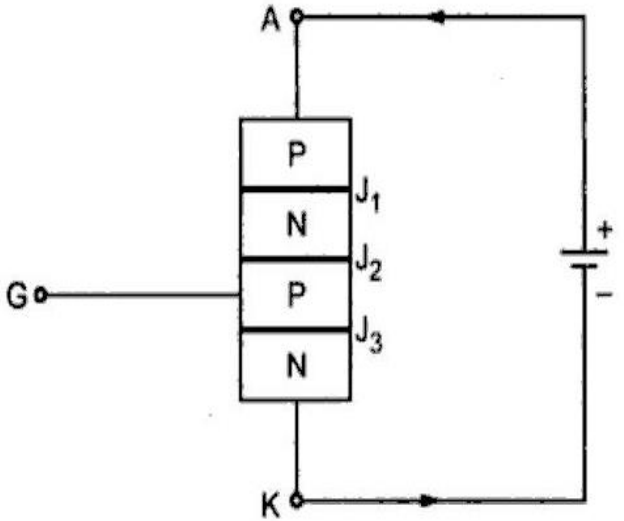

A
−
p
n
p
n
J_1
J_2
J_3
G
+
K
Reverse
leakage
current
A
+
Forward
leakage
current
p
n
p
n
J_1
J_2
J_3
G
−
K

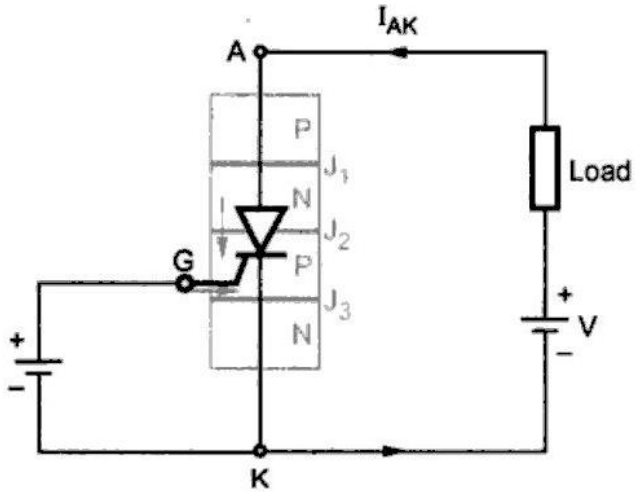
Modes of operation

Reverse Blocking Mode



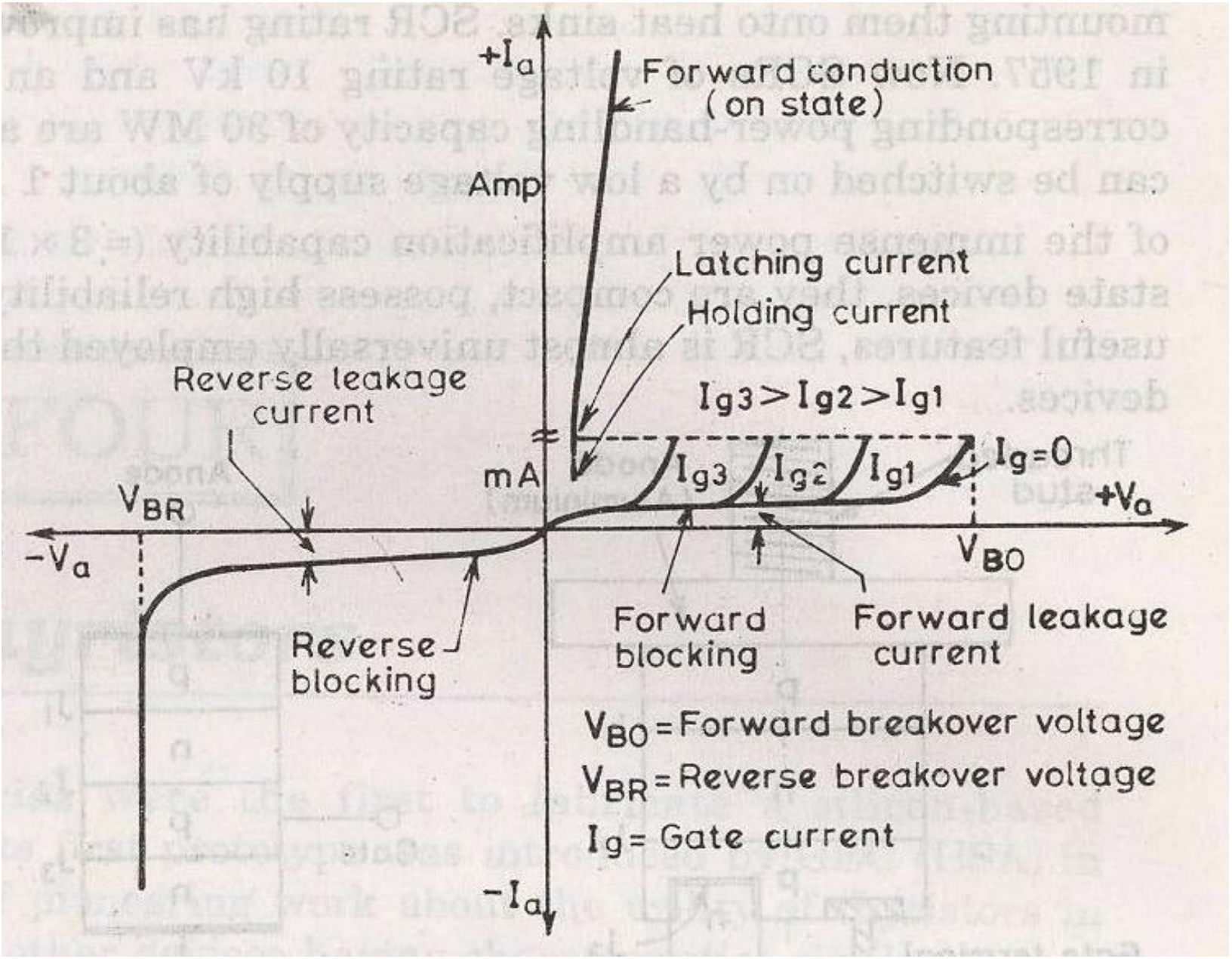
Forward Blocking Mode



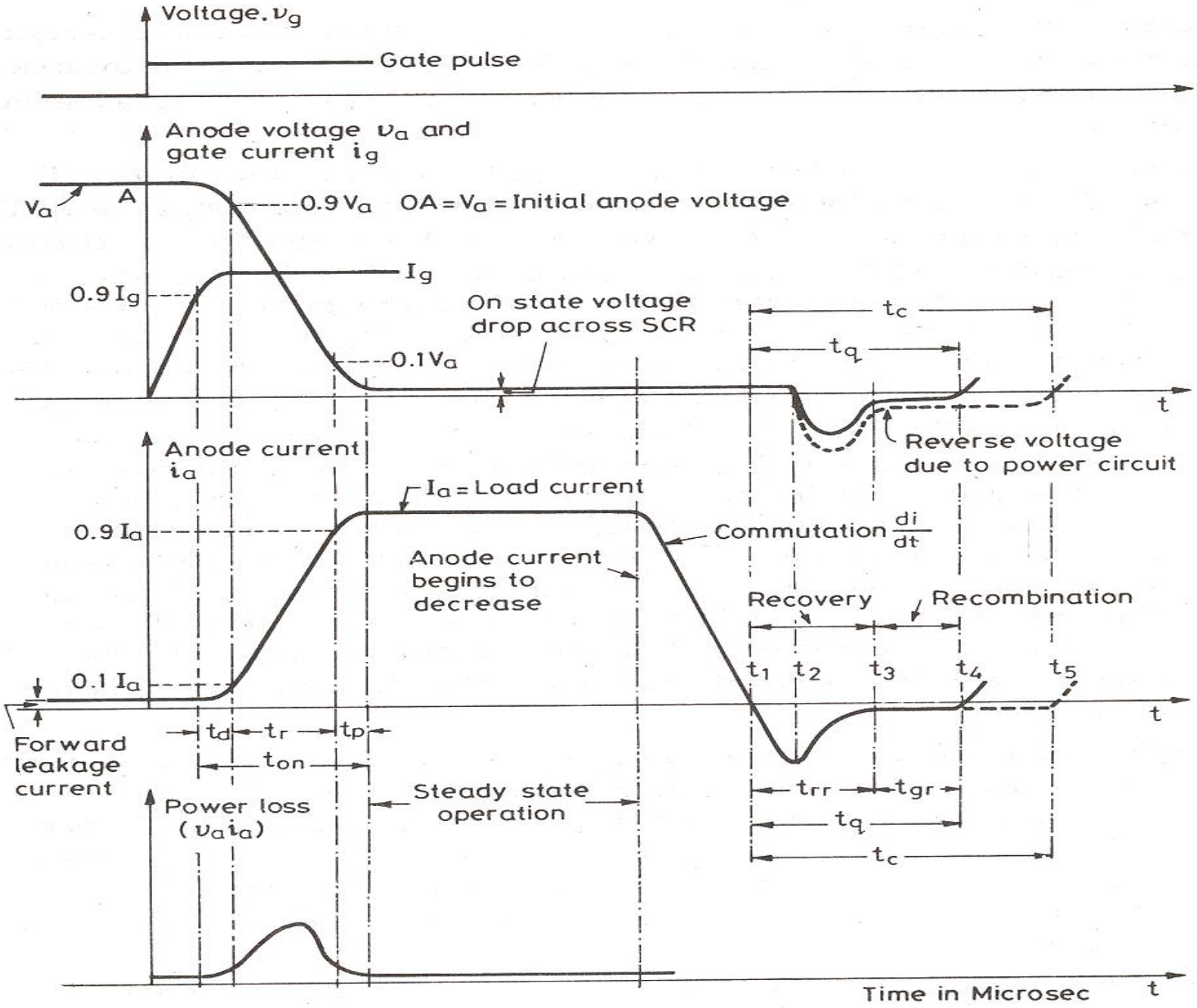


Forward Conduction Mode

Static Characteristics of SCR



Switching Characteristics of SCR



Insulated- gate bipolar transistor—IGBT

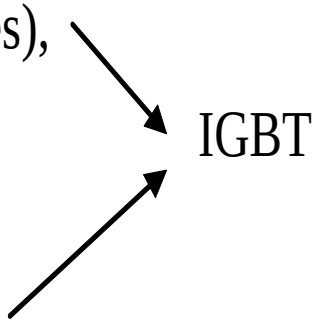
- Combination of MOSFET and GTR

GTR: low conduction losses (especially at larger blocking volta ges),

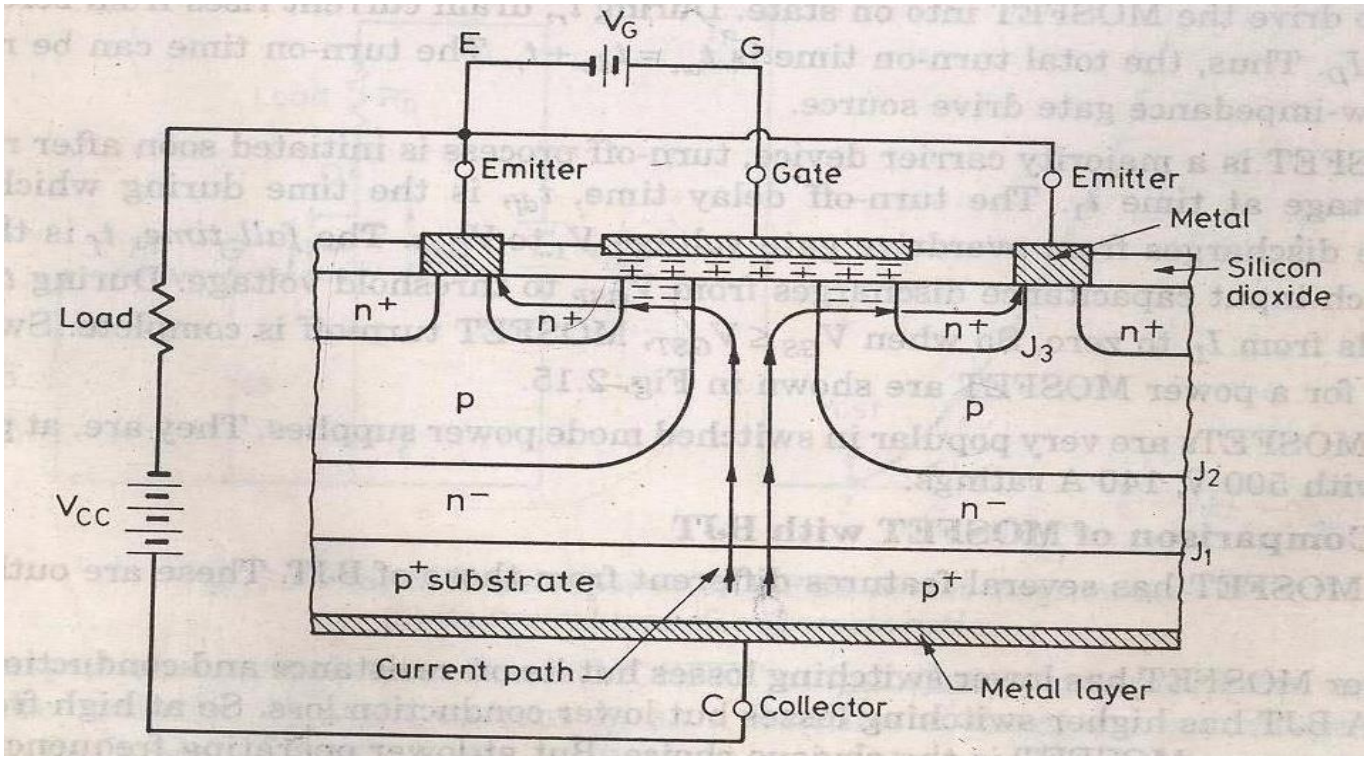
longer switching times, current- driven

MOSFET : faster switching speed, easy to drive (voltage- driven),

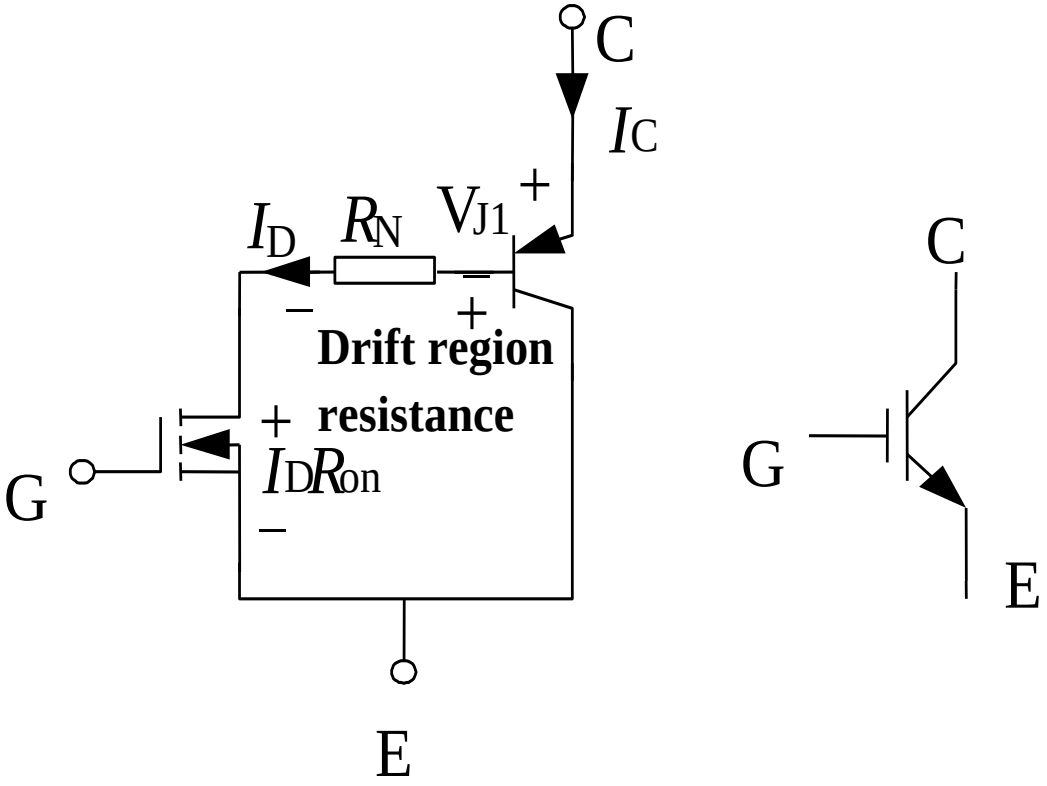
larger conduction losses (especially for higher blocking voltages)



- Features
- On- state losses are much smaller than those of a power MOSFET, and are comparable with those of a GTR
- Easy to drive —similar to power MOSFET Faster than GTR, but slower than power MOSFET
- **Structure and operation principle of IGBT**
- Also multiple cell structure Basic structure similar to power MOSFET, except extra p region
- On- state: minority carriers are injected into drift region, leading to conductivity modulation compared with power MOSFET: slower switching times, lower on- resistance, useful at higher voltages (up to 1700V)



- **Equivalent circuit and circuit symbol of IGBT**

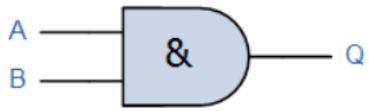


Types of Power Converters

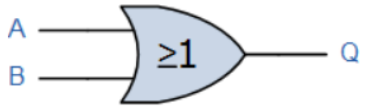
- Inverter (DC to AC)
- Rectifier (AC to DC)
- Chopper (DC to DC)
- Cycloconverters (AC to AC)

Basic Logic Gates

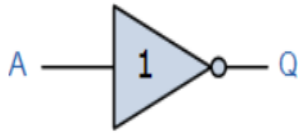
The Logic AND Gate

Symbol	Truth Table		
 2-input AND Gate	A	B	Q
	0	0	0
	0	1	0
	1	0	0
	1	1	1
Boolean Expression Q = A.B	Read as A AND B gives Q		

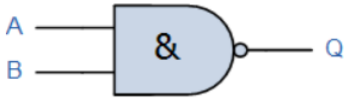
The Logic OR Gate

Symbol	Truth Table		
 2-input OR Gate	A	B	Q
	0	0	0
	0	1	1
	1	0	1
	1	1	1
Boolean Expression Q = A+B	Read as A OR B gives Q		

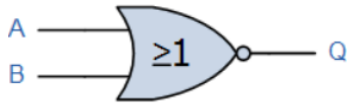
The Logic NOT Gate

Symbol	Truth Table	
 Inverter or NOT Gate	A	Q
	0	1
	1	0
Boolean Expression Q = NOT A or $\overline{A}$	Read as inversion of A gives Q	

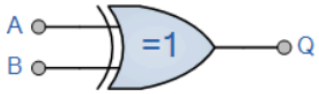
The Logic NAND Gate

Symbol	Truth Table		
 2-input NAND Gate	A	B	Q
	0	0	1
	0	1	1
	1	0	1
	1	1	0
Boolean Expression Q = $\overline{A.B}$	Read as A AND B gives NOT-Q		

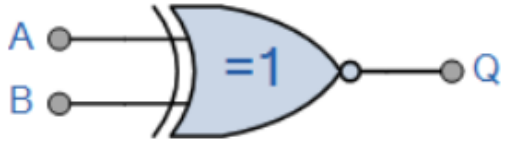
The Logic NOR Gate

Symbol	Truth Table		
 2-input NOR Gate	A	B	Q
	0	0	1
	0	1	0
	1	0	0
	1	1	0
Boolean Expression $Q = \overline{A+B}$	Read as A OR B gives NOT-Q		

The Logic EXOR Gate

Symbol	Truth Table		
	B	A	Q
	0	0	0
	0	1	1
	1	0	1
	1	1	0
Boolean Expression $Q = A \oplus B$	Read as A **OR** B but not **BOTH** gives Q (odd)		

The Logic EXNOR Gate

Symbol	Truth Table		
	B	A	Q
	0	0	1
	0	1	0
	1	0	0
	1	1	1
Boolean Expression $Q = \overline{A \oplus B}$	Read if A **AND** B the **SAME** gives Q (even)		

Consolidation of Logic Gates

Inputs		Truth Table Outputs For Each Gate					
A	B	AND	NAND	OR	NOR	EX-OR	EX-NOR
0	0	0	1	0	1	0	1
0	1	0	1	1	0	1	0
1	0	0	1	1	0	1	0
1	1	1	0	1	0	0	1

Logic Function	Boolean Notation
AND	$A.B$
OR	$A+B$
NOT	$\overline{A}$
NAND	$\overline{A.B}$
NOR	$\overline{A+B}$
EX-OR	$(A.\overline{B}) + (\overline{A}.B)$ or $A \oplus B$
EX-NOR	$(A.B) + (\overline{A}.\overline{B})$ or $\overline{A \oplus B}$

Boolean Rules and Laws

Name	AND form	OR form
Identity law	$1A = A$	$0 + A = A$
Null law	$0A = 0$	$1 + A = 1$
Idempotent law	$AA = A$	$A + A = A$
Inverse law	$A\overline{A} = 0$	$A + \overline{A} = 1$
Commutative law	$AB = BA$	$A + B = B + A$
Associative law	$(AB)C = A(BC)$	$(A + B) + C = A + (B + C)$
Distributive law	$A + BC = (A + B)(A + C)$	$A(B + C) = AB + AC$
Absorption law	$A(A + B) = A$	$A + AB = A$
De Morgan's law	$\overline{AB} = \overline{A} + \overline{B}$	$\overline{A + B} = \overline{A}\,\overline{B}$

Minterm and Maxterm

- A **minterm** is defined as the product term of n variables, in which each of the n variables will appear once either in its complemented or un-complemented form.
- A **maxterm** is defined as the sum term of n variables, in which each of the n variables will appear once either in its complemented or un-complemented form.

Variables			Min terms	Max terms
A	B	C	m_i	M_i
0	0	0	A' B' C' = m 0	A + B + C = M 0
0	0	1	A' B' C = m 1	A + B + C' = M 1
0	1	0	A' B C' = m 2	A + B' + C = M 2
0	1	1	A' B C = m 3	A + B' + C' = M 3
1	0	0	A B' C' = m 4	A' + B + C = M 4
1	0	1	A B' C = m 5	A' + B + C' = M 5
1	1	0	A B C' = m 6	A' + B' + C = M 6
1	1	1	A B C = m 7	A' + B' + C' = M 7

Sum of Product (SOP) Form

The Sum of Product form is a form of expression in Boolean algebra in which different product terms of inputs are being summed together.

Example:

A	B	C	F
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	0

$$F = \sum(m_1, m_2, m_3, m_5)$$

$$F = \bar{A}\bar{B}C + \bar{A}B\bar{C} + \bar{A}BC + A\bar{B}C$$

Canonical or Standard SOP form

Product of Sum (POS) Form

The Product of Sum form is a form in which products of different sum terms of inputs are taken.

Example:

A	B	C	F
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	0

$$F = \prod (M_0, M_4, M_6, M_7)$$

Canonical or Standard POS form

$$F = (A+B+C)(\bar{A}+B+C)(\bar{A}+\bar{B}+C)(\bar{A}+\bar{B}+\bar{C})$$

Conversion from Minimal SOP to Canonical SOP Form

Example:

$$F = \bar{A}B + \bar{B}C$$

The term $\bar{A}B$ is missing input C. So we will multiply $\bar{A}B$ with $(C+\bar{C})$ because $(C+\bar{C} = 1)$.
The term $\bar{B}C$ is missing input A, so it will be multiplied with $(A+\bar{A})$

Missing input variables need to be multiplied

$$F = \bar{A}B(C + \bar{C}) + \bar{B}C(A + \bar{A})$$

$$F = \bar{A}BC + \bar{A}B\bar{C} + A\bar{B}C + \bar{A}\bar{B}C$$

Conversion from Minimal POS to Canonical POS Form

Example:

$$F = (\bar{A}+\bar{B})\,(B+C)$$

$(\bar{A}+\bar{B})$ term is missing C input so we will add $(C\bar{C})$ with it.
$(B+C)$ term is missing A input so we will add $(A\bar{A})$ with it.

Missing input variables need to be added

$$F = (\bar{A}+\bar{B}+C\bar{C})\,(B+C+A\bar{A})$$

$$F = (\bar{A}+\bar{B}+C)(\bar{A}+\bar{B}+\bar{C})(A+B+C)(\bar{A}+B+C)$$

Conversion of SOP to POS

To convert the SOP form into POS form, first we should change the Σ to Π and then write the numeric indexes of missing variables of the given Boolean function.

Example:

$$\mathbf{F = \sum_{A, B, C} (0, 2, 3, 5, 7) = A' B' C' + A B' C' + A B' C + ABC' + ABC}$$

Note: writing the missing indexes of the terms i.e., 1 - 001, 4 - 100 and 6 - 110.

001 = (A + B + C'), 100 = (A' + B + C), 110 = (A' + B' + C)

Hence,

$$\mathbf{F = \Pi_{A, B, C} (1, 4, 6) = (A + B + C') * (A' + B + C) * (A' + B' + C)}$$

Conversion of POS to SOP

To convert the POS form into SOP form, first we should change the Π to Σ and then write the numeric indexes of missing variables of the given Boolean function.

Example:

$$F = \Pi_{A, B, C} (2, 3, 5) = (A+B'+C) * (A+B'+C') * (A'+B+C')$$

Note: writing the missing indexes of the terms, 0 - 000, 1 - 001, 4 - 100, 6 - 110, and 7 - 111.

000 = A' * B' * C', 001 = A' * B' * C, 100 = A * B' * C', 110 = A * B* C', 111 = A * B * C

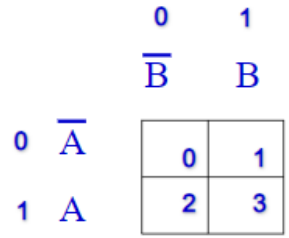
Hence,

$$F = \Sigma_{A, B, C} (0, 1, 4, 6, 7) = (A' * B' * C') + (A' * B' * C) + (A * B' * C') + (A * B* C') + (A * B * C)$$

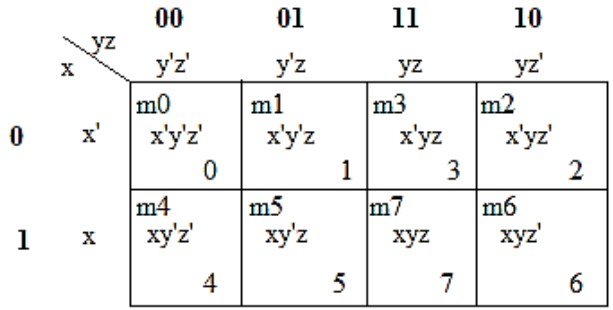
K-map

- K-Map is used to minimize the number of logic gates by minimizing the logical expression.
- The minimization will reduce cost, complexity and power consumption.
- An **n-variable K-map has 2^n cells** with each cell corresponding to an n-variable truth table value.
  - If 2 variable – 4 cells
  - If 3 variable – 8 cells
  - If 4 variable – 16 cells
  - If 5 variable – 32 cells
- K-map cells are arranged such that adjacent cells correspond to truth rows that differ in only one bit position.

2 variables K-Map



3 variables K-Map

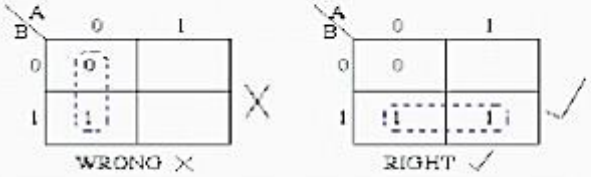


4 variables K-Map

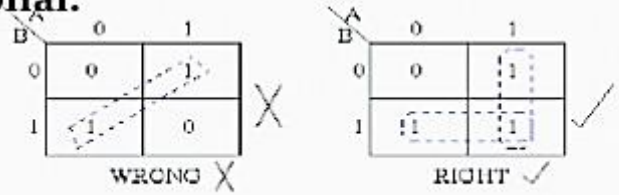
		0 0	0 1	1 1	1 0
		$\overline{C}\,\overline{D}$	$\overline{C}\,D$	$C\,D$	$C\,\overline{D}$
00	$\overline{A}\,\overline{B}$	0	1	3	2
01	$\overline{A}\,B$	4	5	7	6
11	$A\,B$	12	13	15	14
10	$A\,\overline{B}$	8	9	11	10

K-map Rules

1.Groups may not include any cell containing a zero.

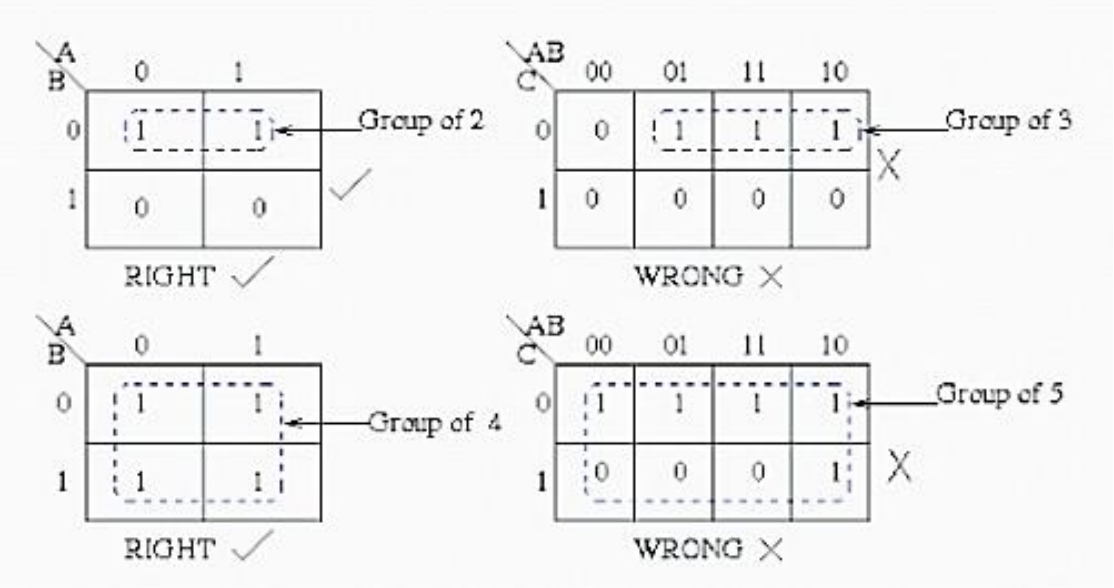


2.Groups may be horizontal or vertical, but not diagonal.



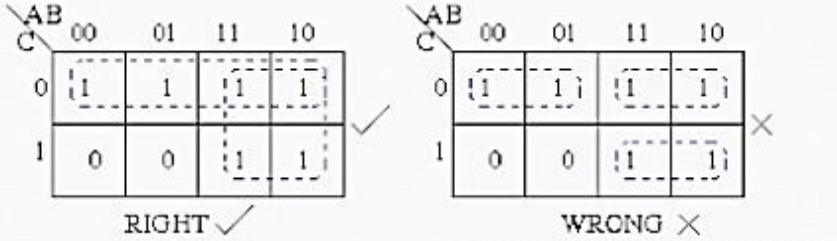
K-map Rules

3. Groups must contain 1, 2, 4, 8, or in general 2^n cells.



K-map Rules

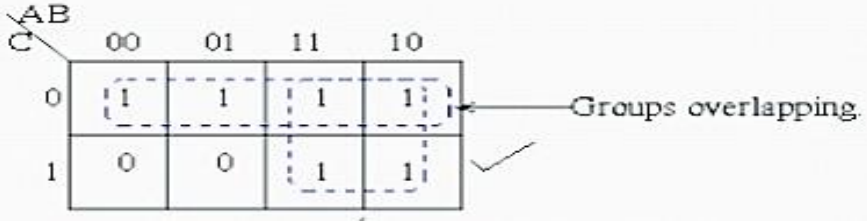
4. Each group should be as large as possible.



(Note that no Boolean laws broken, but not sufficiently minimal)

5.Each cell containing a one must be in at least one group.

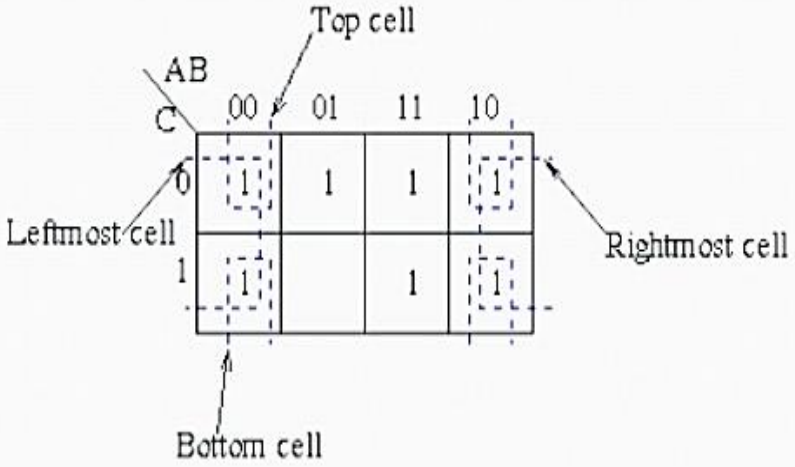
6.Groups may overlap.



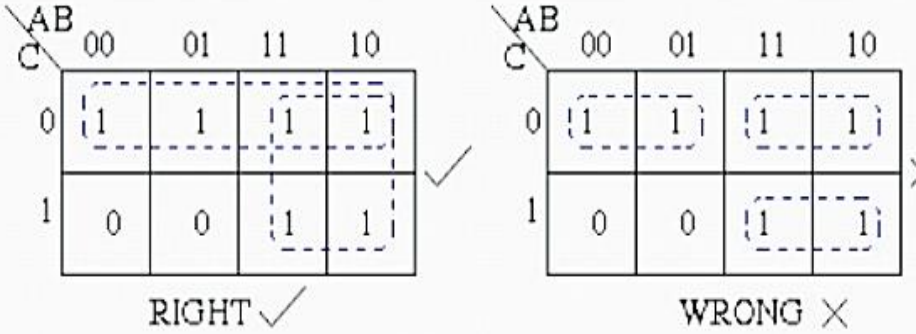
K-map Rules

7.Groups may wrap around the table.

The leftmost cell in a row may be grouped with the rightmost cell and the top cell in a column may be grouped with the bottom cell.



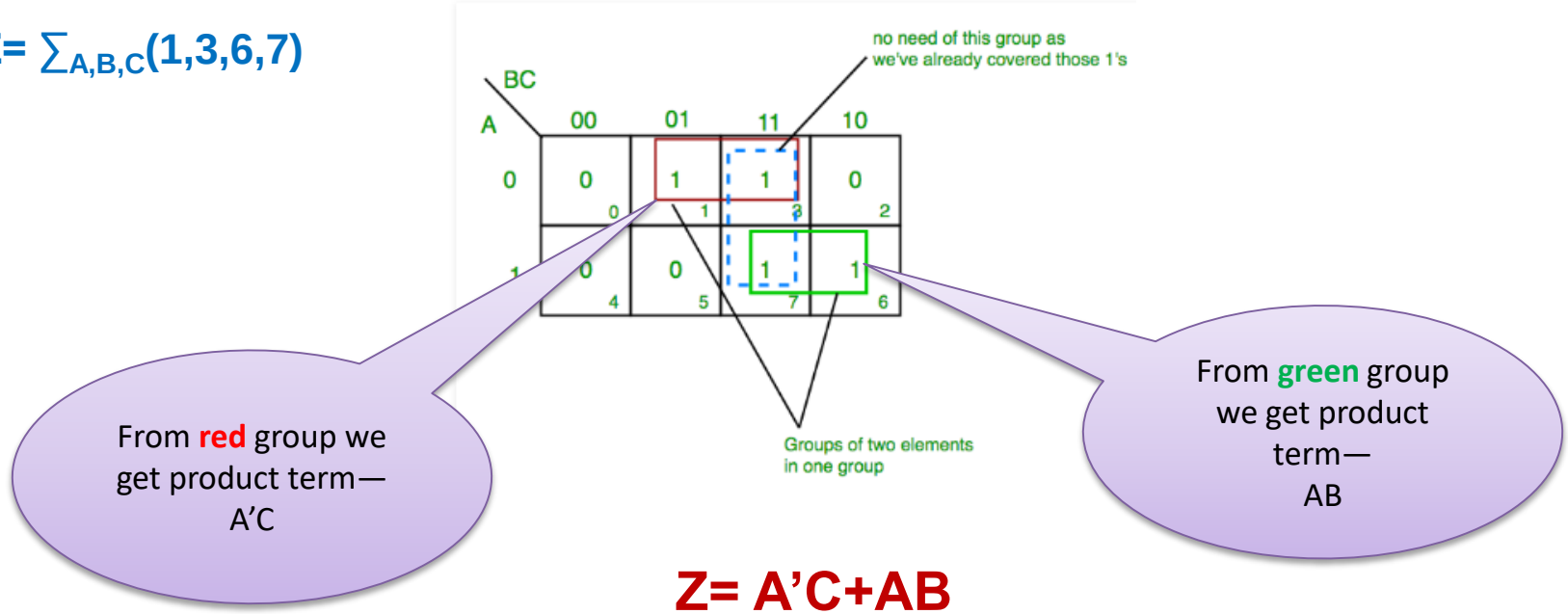
8. There should be as few groups as possible, as long as this does not contradict any of the previous rules.



Example 1

For the given minterms, find the reduced logical expression using K-Map

$Z = \sum_{A,B,C}(1,3,6,7)$

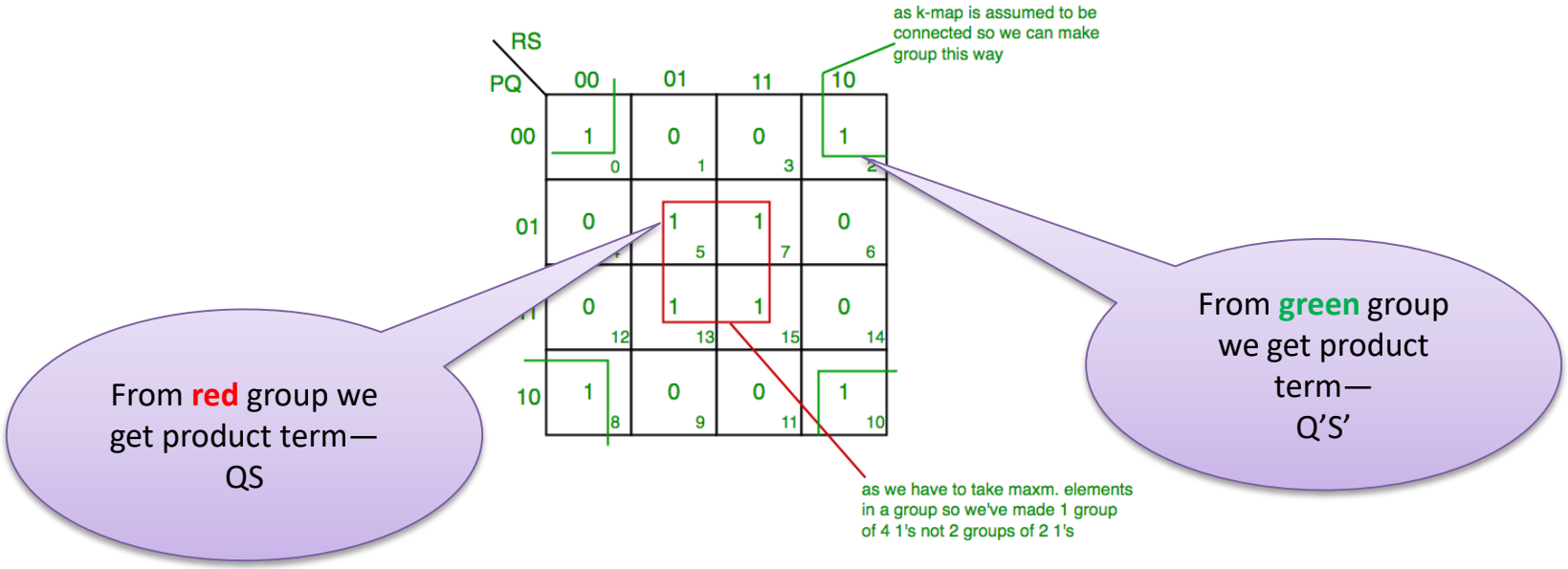


Z= A'C+AB

Example 2

For the given minterms, find the reduced logical expression using K-Map

F(P,Q,R,S)=∑(0,2,5,7,8,10,13,15)



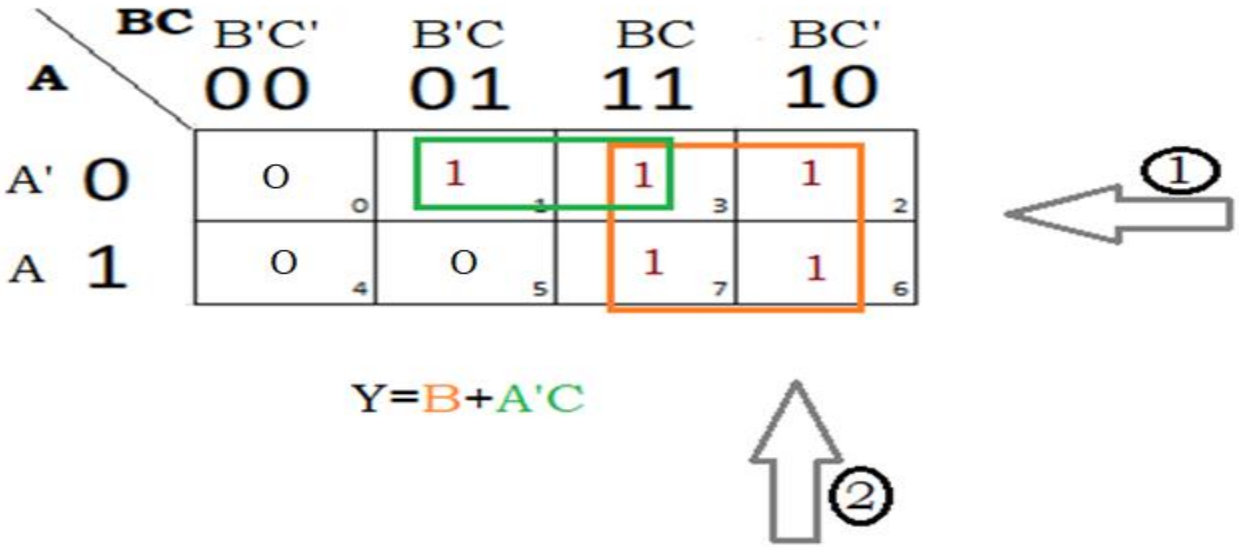
F = QS+Q'S'

1 Simply the following Boolean expression

$Y(A,B,C) = \sum m(1,2,3,6,7)$

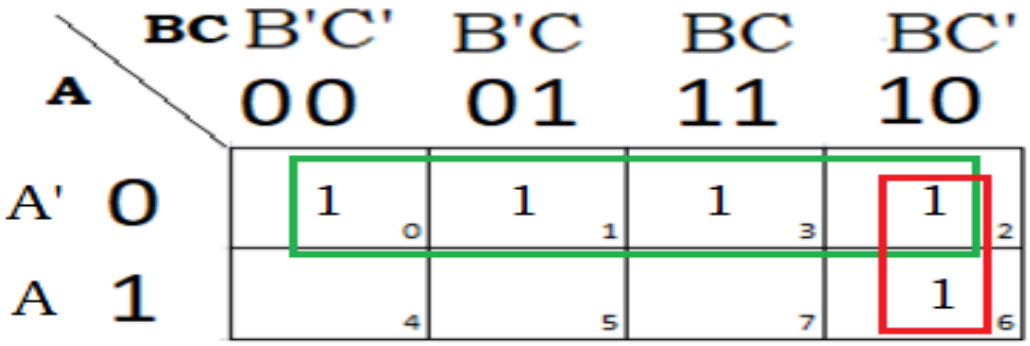
Method 2: K-MAP

Three variable (Inputs- A,B,C)



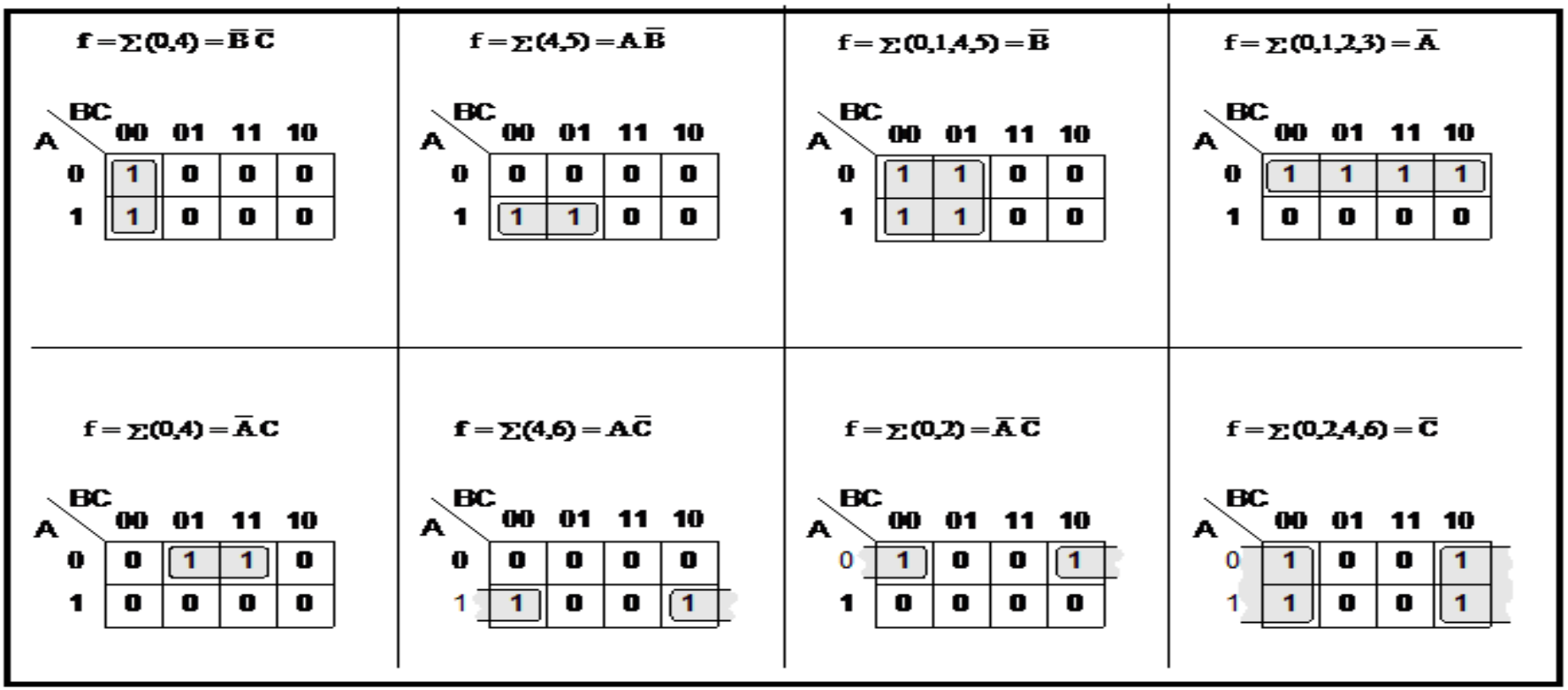
2 Simply the following Boolean expression

$Y(A,B,C) = \sum m(0,1,2,3,6)$



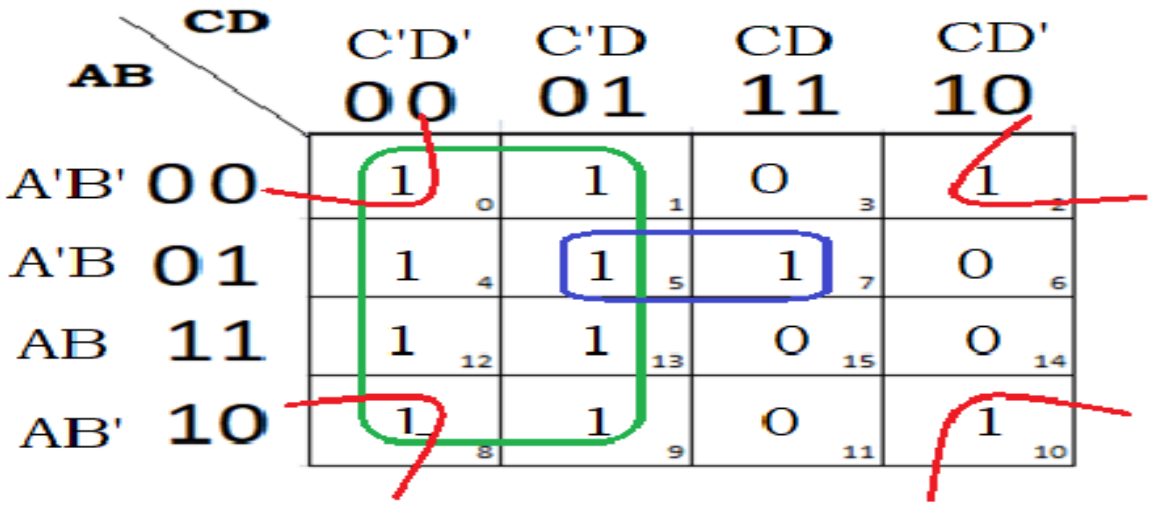
$Y = A' + BC'$

Three-Variable K-Map : Examples



3. Simply the following Boolean expression and implement it using logic gates

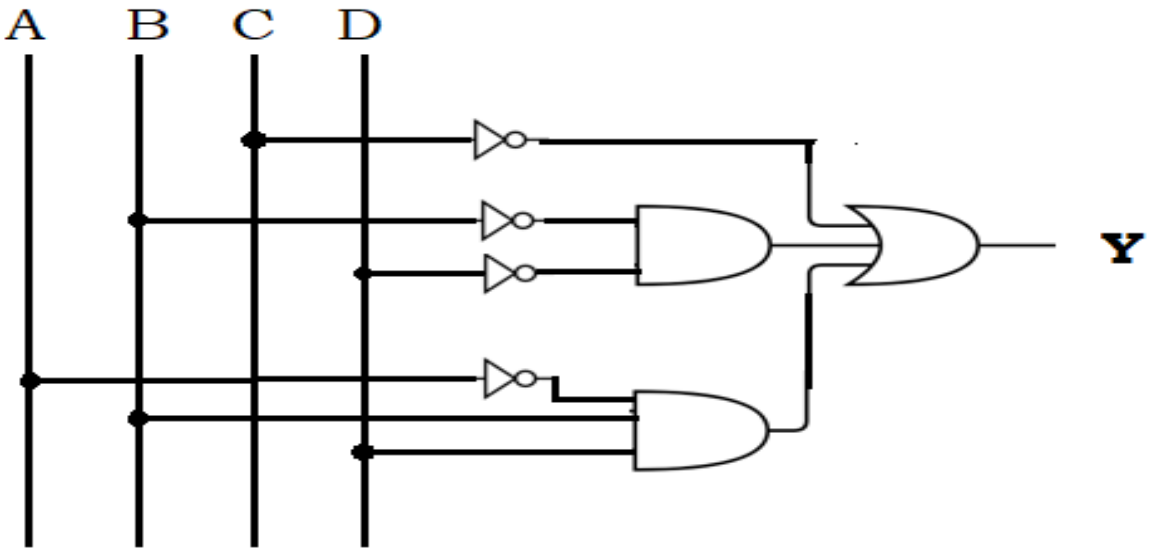
$Y(A,B,C,D) = \sum m(0,1,2,4,5,7,8,9,10,12,13)$



$Y = C' + B'D' + A'BD$

Implementation

Y=C'+B'D'+A'BD



Four-Variable K-Maps Examples

CD / AB	00	01	11	10
00	1	0	0	0
01	0	0	0	0
11	0	0	0	0
10	1	0	0	0

$f = \sum(0,8) = \overline{B} \bullet \overline{C} \bullet \overline{D}$

CD / AB	00	01	11	10
00	0	0	0	0
01	0	1	0	0
11	0	1	0	0
10	0	0	0	0

$f = \sum(5,13) = B \bullet \overline{C} \bullet D$

CD / AB	00	01	11	10
00	0	0	0	0
01	0	0	0	0
11	0	1	1	0
10	0	0	0	0

$f = \sum(13,15) = A \bullet B \bullet D$

CD / AB	00	01	11	10
00	0	0	0	0
01	1	0	0	1
11	0	0	0	0
10	0	0	0	0

$f = \sum(4,6) = \overline{A} \bullet B \bullet \overline{D}$

CD / AB	00	01	11	10
00	0	0	1	1
01	0	0	1	1
11	0	0	0	0
10	0	0	0	0

$f = \sum(2,3,6,7) = \overline{A} \bullet C$

CD / AB	00	01	11	10
00	0	0	0	0
01	1	0	0	1
11	1	0	0	1
10	0	0	0	0

$f = \sum(4,6,12,14) = B \bullet \overline{D}$

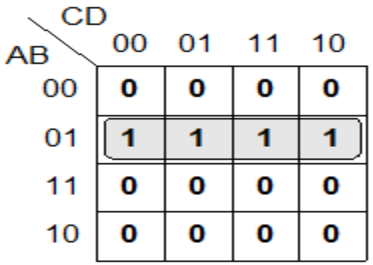
CD / AB	00	01	11	10
00	0	0	1	1
01	0	0	0	0
11	0	0	0	0
10	0	0	1	1

$f = \sum(2,3,10,11) = \overline{B} \bullet C$

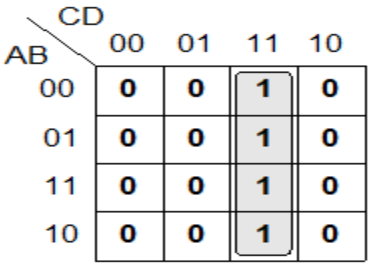
CD / AB	00	01	11	10
00	1	0	0	1
01	0	0	0	0
11	0	0	0	0
10	1	0	0	1

$f = \sum(0,2,8,10) = \overline{B} \bullet \overline{D}$

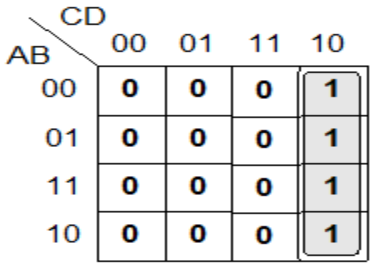
Four-Variable K-Maps Examples



$f = \sum(4,5,6,7) = \overline{A} \bullet B$

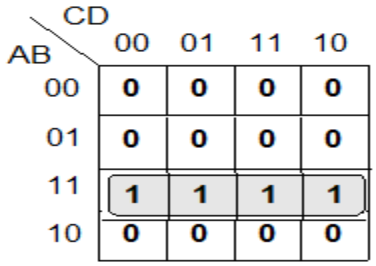


$f = \sum(3,7,11,15) = C \bullet D$

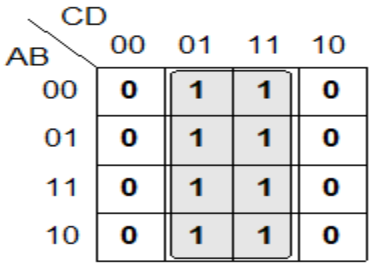


$f = \sum(2,6,10,14)$

$f = C\,\overline{D}$

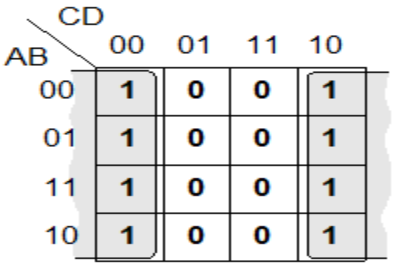


$f = \sum(12,13,14,15) = AB$



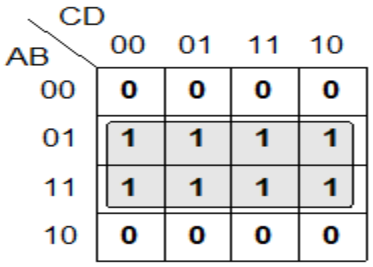
$f = \sum(1,3,5,7,9,11,13,15)$

$f = D$



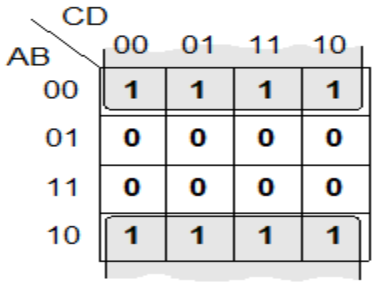
$f = \sum(0,2,4,6,8,10,12,14)$

$f = \overline{D}$



$f = \sum(4,5,6,7,12,13,14,15)$

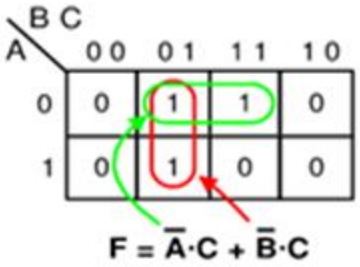
$f = B$

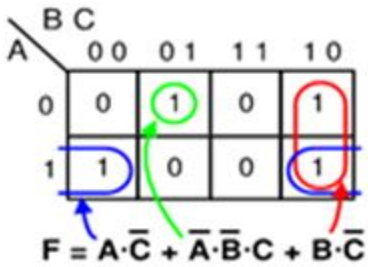


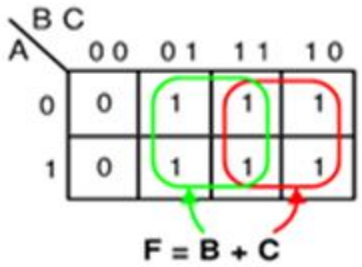
$f = \sum(0,1,2,3,8,9,10,11)$

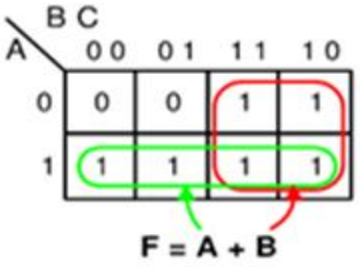
$f = \overline{B}$

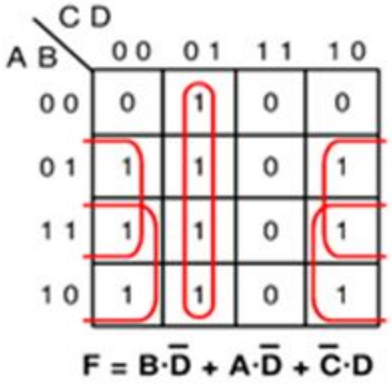
3,4-Variable K-Maps Examples

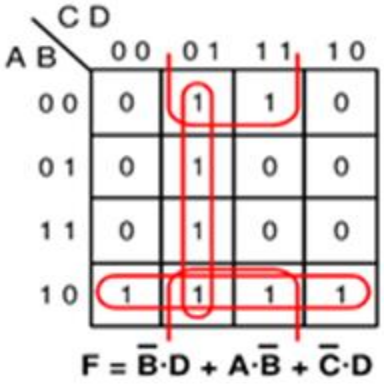


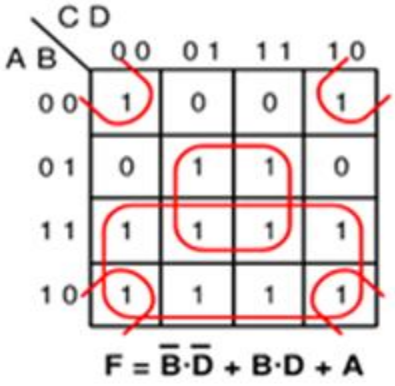


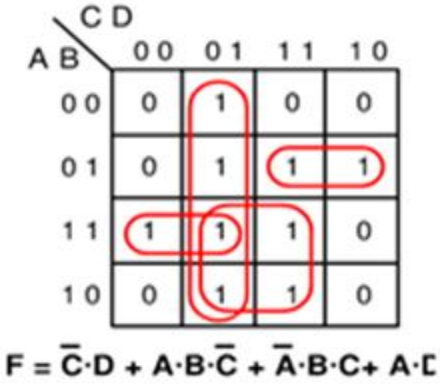








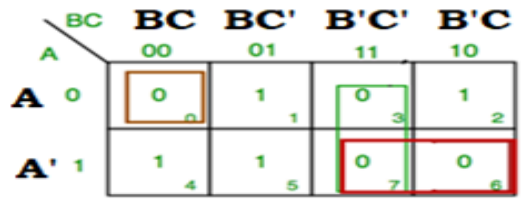




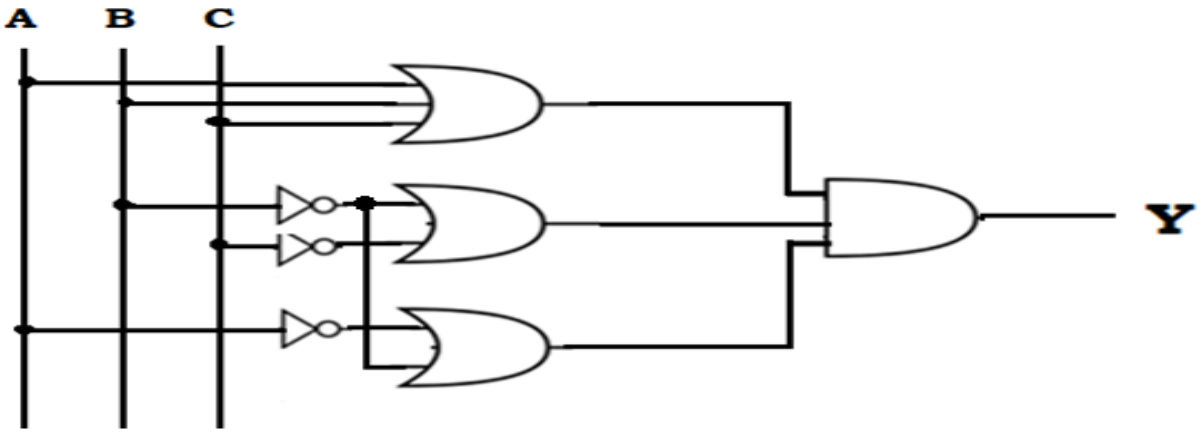
K-MAP-POS METHOD

1. Simply the following Boolean expression by POS method and implement it using logic gates

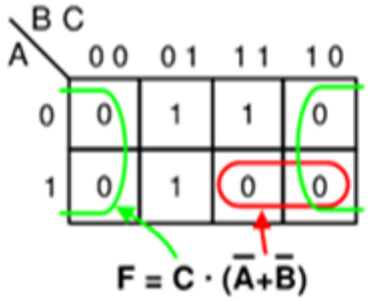
$Y(A,B,C) = \prod m(0,3,6,7)$



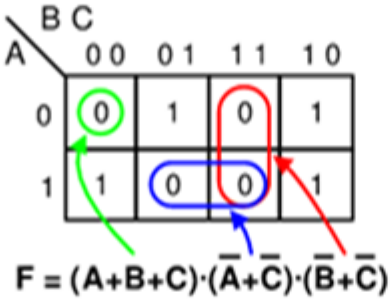
$Y = (A+B+C).(B'+C').(A'+B')$



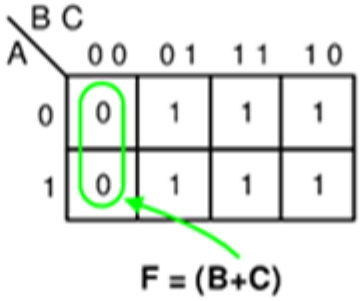
3,4-Variable K-Maps Examples [POS]



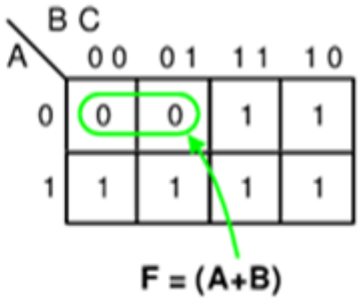
$F = C \cdot (\overline{A}+\overline{B})$



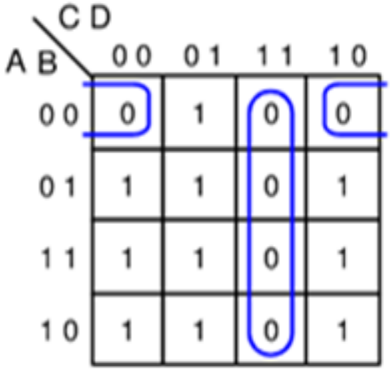
$F = (A+B+C)\cdot(\overline{A}+\overline{C})\cdot(\overline{B}+\overline{C})$



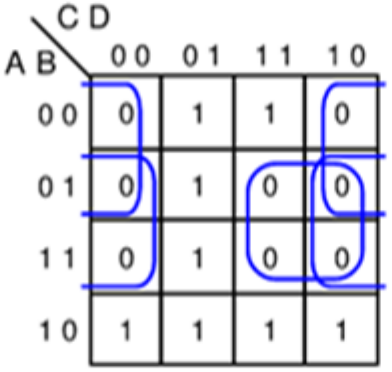
$F = (B+C)$



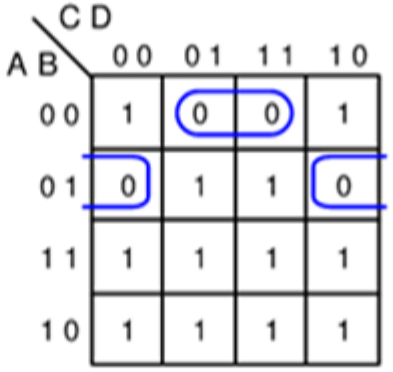
$F = (A+B)$



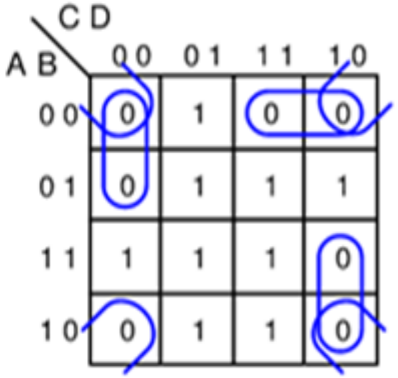
$F = (A+B+D)\cdot(\overline{C}+\overline{D})$



$F = (A+D)\cdot(\overline{B}+D)\cdot(\overline{B}+\overline{C})$



$F = (A+B+\overline{D})\cdot(A+\overline{B}+D)$

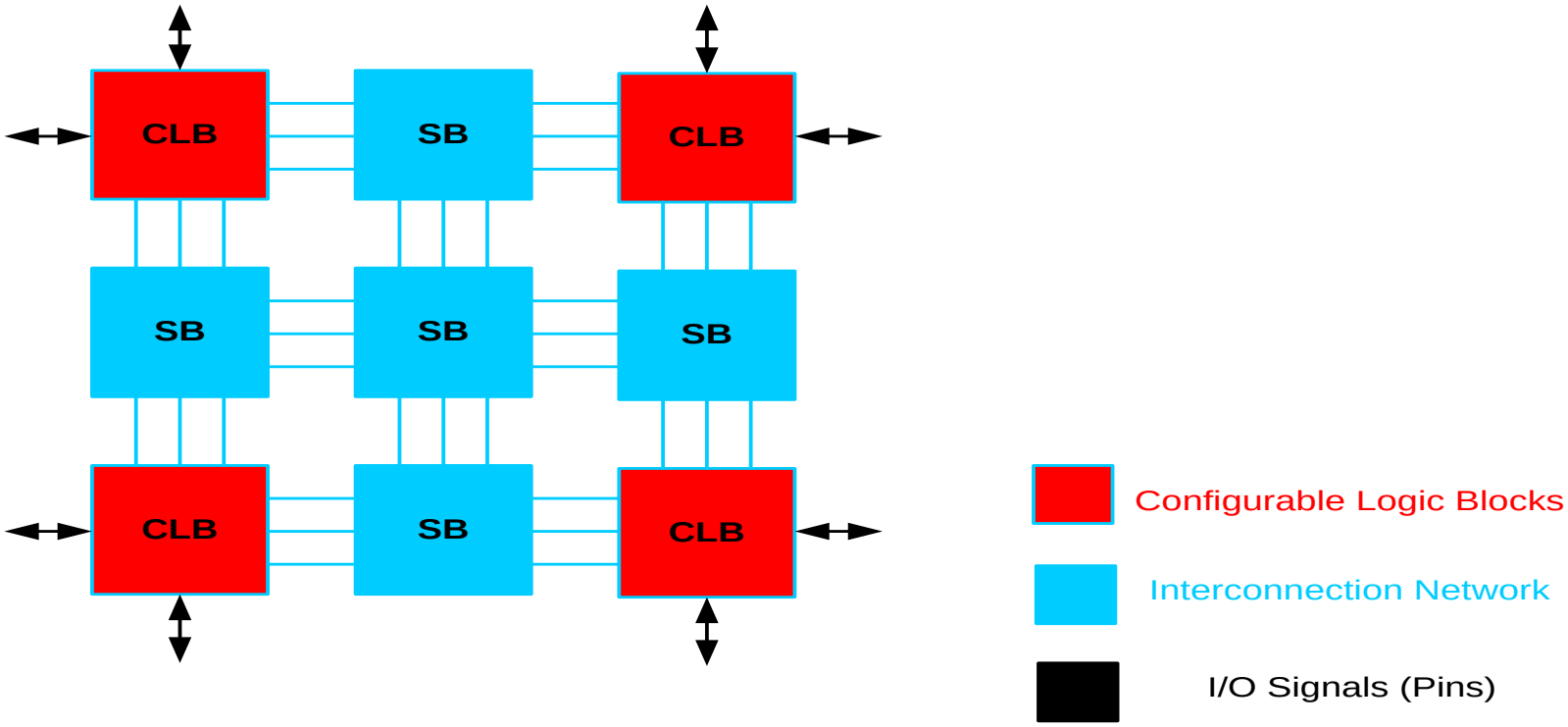


$F = (A+C+D)\cdot(A+B+\overline{C})\cdot(\overline{A}+\overline{C}+D)\cdot(B+D)$

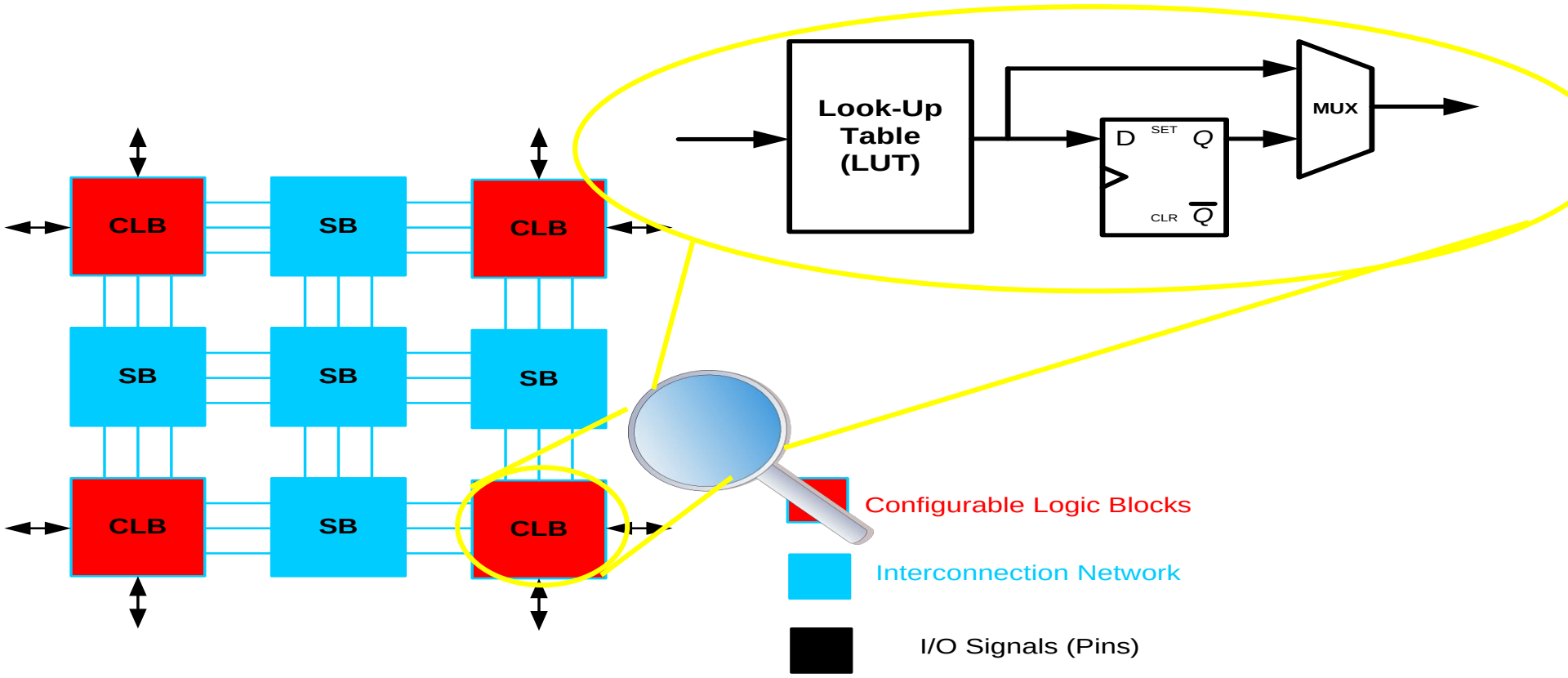
FPGA

- A Field-Programmable Gate Array (FPGA) is an integrated circuit that can be configured by the user to emulate any digital circuit as long as there are enough resources.
- The FPGA configuration is generally specified using a hardware description language (HDL)
- An FPGA can be seen as an array of Configurable Logic Blocks (CLBs) connected through programmable interconnect (Switch Boxes).

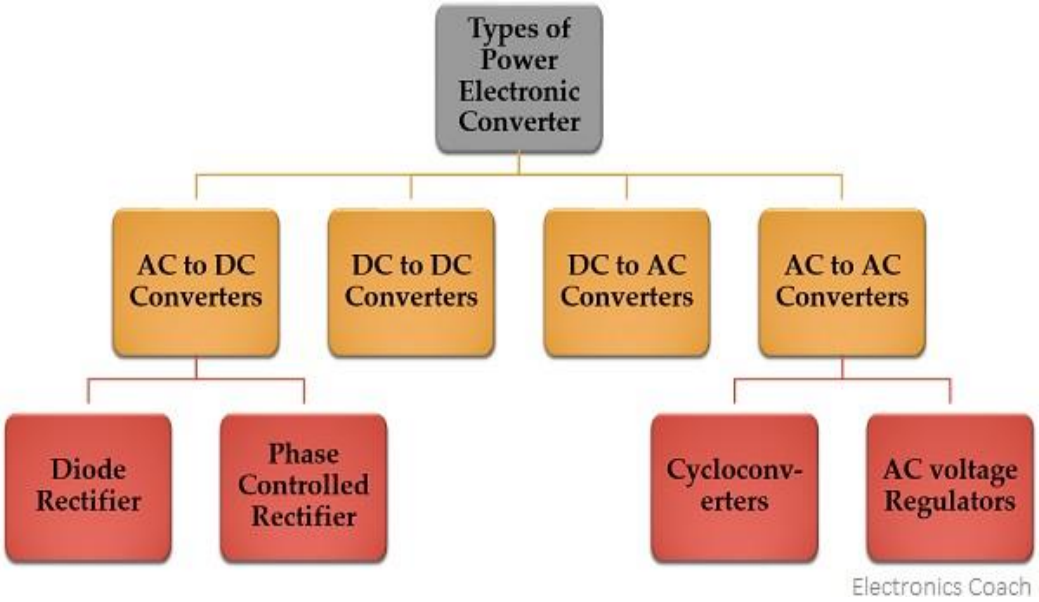
FPGA structure



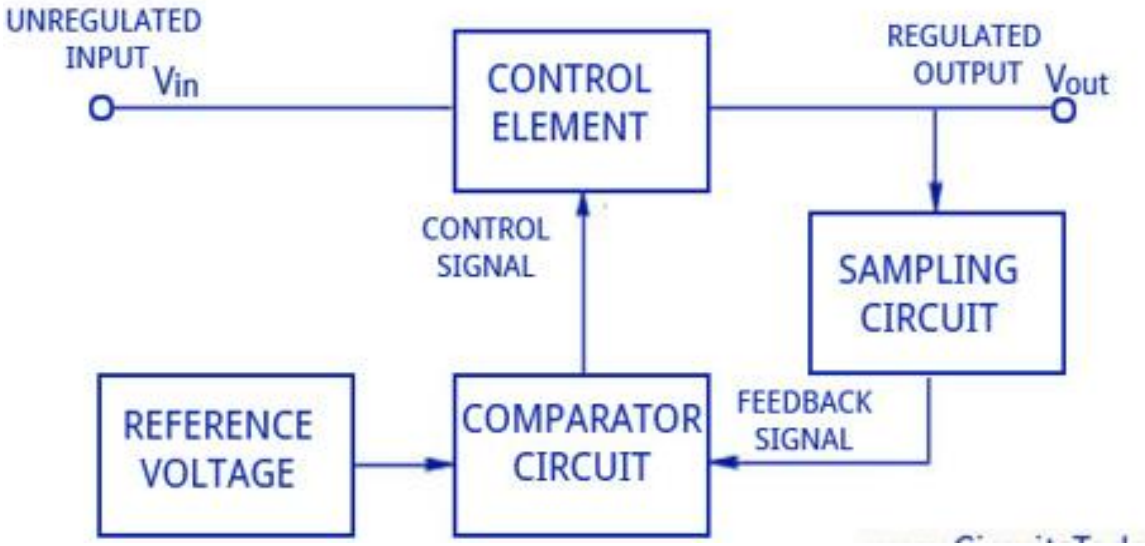
Simplified CLB Structure



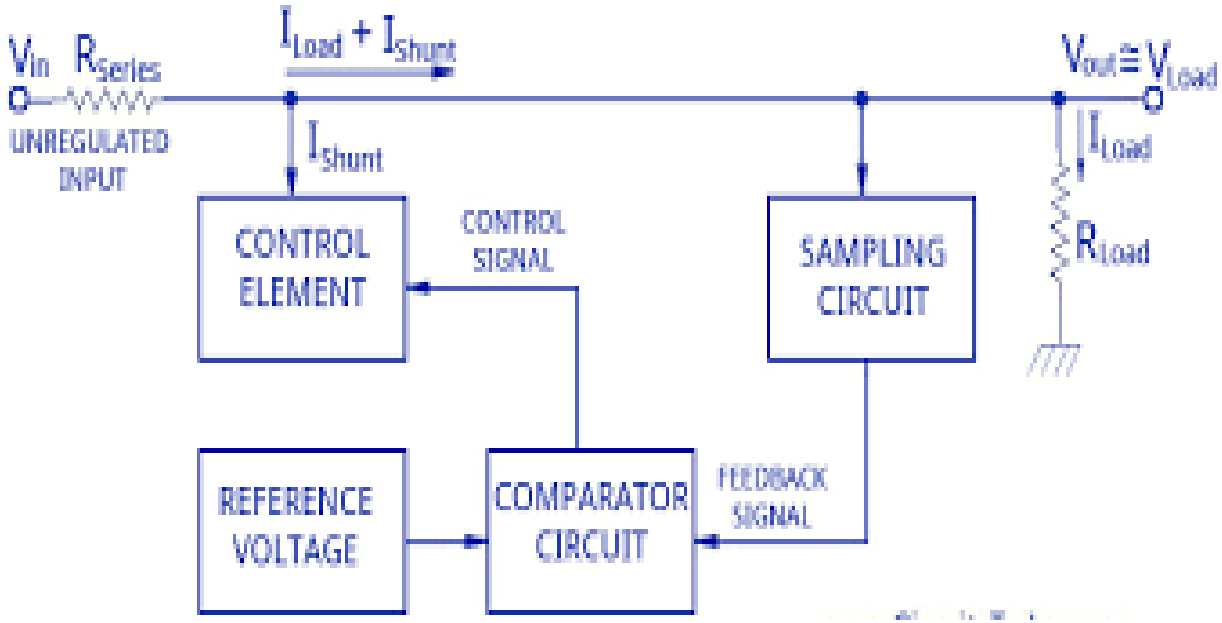
Power converter



SERIES VOLTAGE REGULATOR - BLOCK DIAGRAM

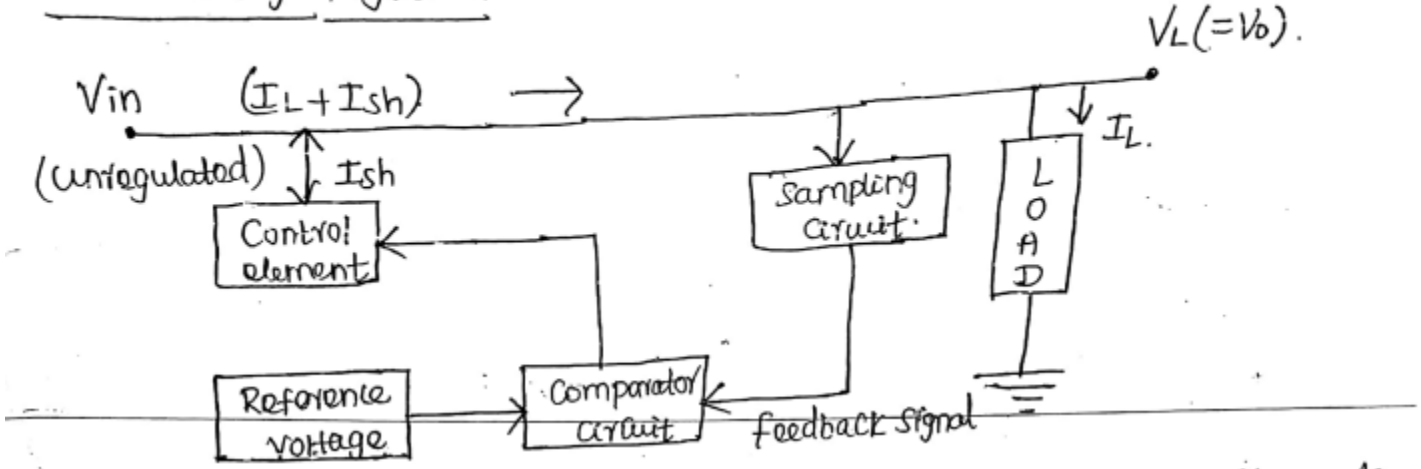


SHUNT VOLTAGE REGULATOR - BLOCK DIAGRAM



Voltage regulator

Shunt voltage regulator :-



→ The heart of any voltage regulator circuit is a control element. If such a control element is connected in shunt with the load, the regulated circuit is called shunt voltage regulator.

→ The unregulated I/p voltage Vin, tries to provide the load current, But part of the current is taken by control element, to maintain the constant voltage across the load.

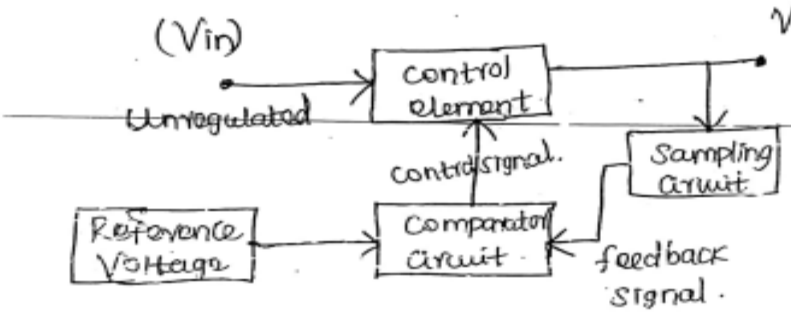
→ If there is any change in load voltage, the sampling circuit provides feedback signal to comparator ckt. which compares feedback signal with reference voltage & generates a control signal to keep the load voltage constant.

→ If Load voltage increases, the comparator changes the control signal [illegible] which increases Ish current. Due to this load

Current I_L decreases & load voltage decreases to its normal. The control element maintains the constant o/p voltage by shunting the current → voltage shunt regulator circuit.

→ efficiency depends on the load current I_L & hence shunt regulators are not prepared for varying Load conditions.

Series voltage Regulator:



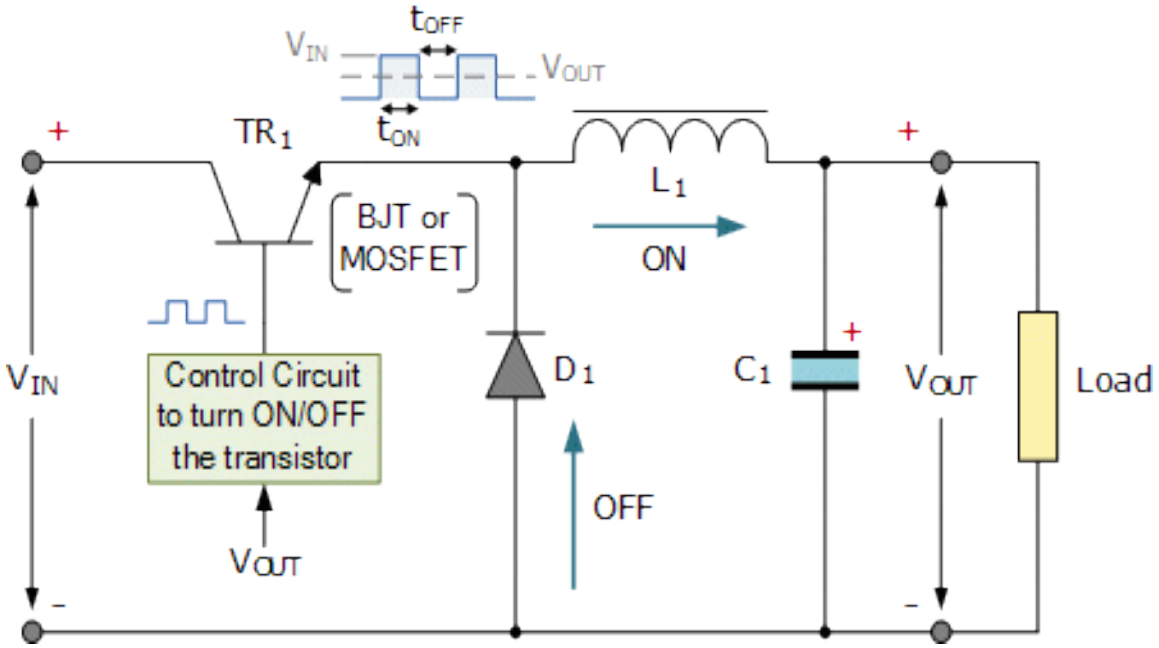
→ The control element is con
in series with load.

→ The unregulated dc voltage
input. The control element, contr
the amount of i/p voltage, that gets to the output. The sampli
circuit provides the necessary f/b signal. The comparator ckt com
the f/b with the reference voltage to generate the control signa

→ If load voltage tries to increase, the comparator generates a C
signal based on the f/b signal. This control signal causes the control
to decrease the amount of the o/p voltage.

→ Efficiency depends on the output voltage. It provides good regul
than shunt regulators. It can be used for fixed voltage and vari
conditions.

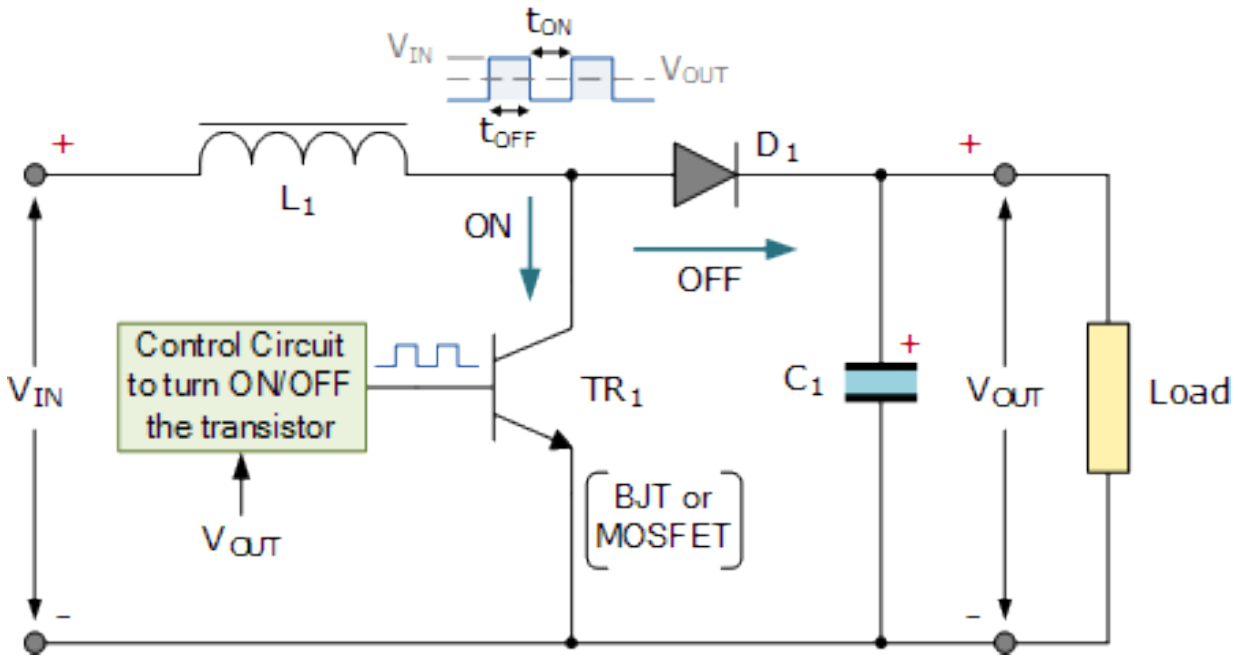
SMPS BUCK TYPES



- The basic circuit configuration for a buck converter is a series transistor switch, TR_1 with an associated drive circuit that keeps the output voltage as close to the desired level as possible, a diode, D_1, an inductor, L_1 and a smoothing capacitor, C_1. The buck converter has two operating modes, depending on if the switching transistor TR_1 is turned “ON” or “OFF”.
- When the transistor is biased “ON” (switch closed), diode D_1 becomes reverse biased and the input voltage, V_{IN} causes a current to flow through the inductor to the connected load at the output, charging up the capacitor, C_1.
- As a changing current flows through the inductor coil, it produces a back-emf which opposes the flow of current, according to Faraday’s law, until it reaches a steady state creating a magnetic field around the inductor, L_1. This situation continues indefinitely as long as TR_1 is closed. When transistor TR_1 is turned “OFF” (switch open) by the controlling circuitry, the input voltage is instantly disconnected from the emitter circuit causing the magnetic field around the inductor to collapse inducing a reverse voltage across the inductor. This reverse voltage causes the diode to become forward biased, so the stored energy in the inductors magnetic field forces current to continue to flow through the load in the same direction, and return back through diode.

- Then the inductor, L_1 returns its stored energy back to the load acting like a source and supplying current until all the inductor's energy is returned to the circuit or until the transistor switch closes again, whichever comes first. At the same time the capacitor also discharges supplying current to the load. The combination of the inductor and capacitor forms an LC filter smoothing out any ripple created by the switching action of the transistor. Therefore, when the transistor solid state switch is closed, current is supplied from the supply, and when the transistor switch is open, current is supplied by the inductor. Note that the current flowing through the inductor is always in the same direction, either directly from the supply or via the diode but obviously at different times within the switching cycle.
- As the transistor switch is being continuously closed and opened, the average output voltage value will therefore be related to the duty cycle, D which is defined as the conduction time of the transistor switch during one full switching cycle.

SMPS BOOST TYPES



In the *Boost Converter* circuit, when the transistor switch is fully-on, electrical energy from the supply, V_{IN} passes through the inductor and transistor switch and back to the supply. As a result, none of it passes to the output as the saturated transistor switch effectively creates a short-circuit to the output.

This increases the current flowing through the inductor as it has a shorter inner path to travel back to the supply. Meanwhile, diode D_1 becomes reverse biased as its anode is connected to ground via the transistor switch with the voltage level on the output remaining fairly constant as the capacitor starts to discharge through the load.

When the transistor is switched fully-off, the input supply is now connected to the output via the series connected inductor and diode. As the inductor field decreases the induced energy stored in the inductor is pushed to the output by V_{IN}, through the now forward biased diode. The result of all this is that the induced voltage across the inductor L_1 reverses and adds to the voltage of the input supply increasing the total output voltage as it now becomes, $V_{IN} + V_L$.

Current from the smoothing capacitor, C_1 which was used to supply the load when the transistor switch was closed, is now returned to the capacitor by the input supply via the diode. Then the current supplied to the capacitor is the diode current, which will always be "ON" or "OFF" as the diode is continually switched between its forward and reverse status by the switching action of transistor. Then the smoothing capacitor must be sufficiently large enough to produce a smooth steady output.

Power converter