An Overview of Compilation

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Compilation Overview: Outline

Introduction

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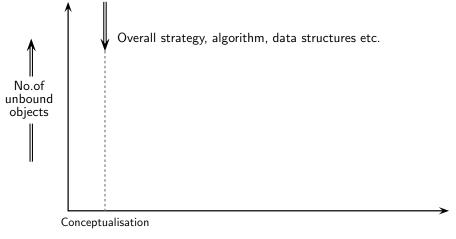
- compilation sequence
- compilation models

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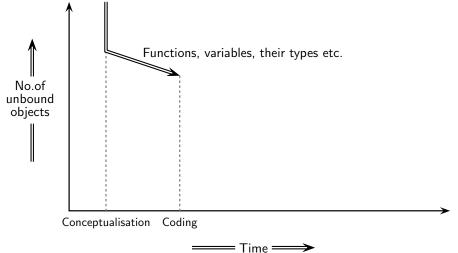
Part 1

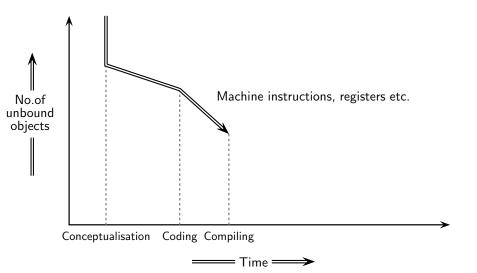
Introduction to Compilation

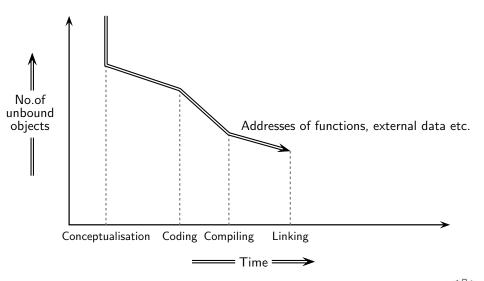
Binding



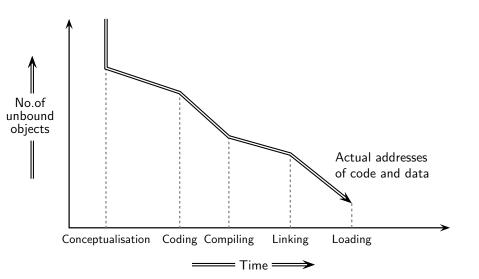
Time =

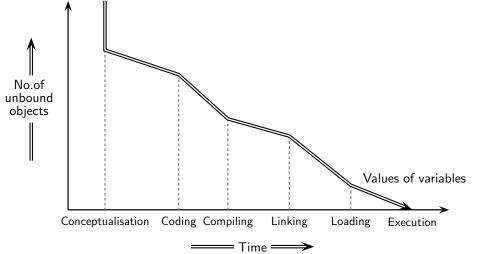




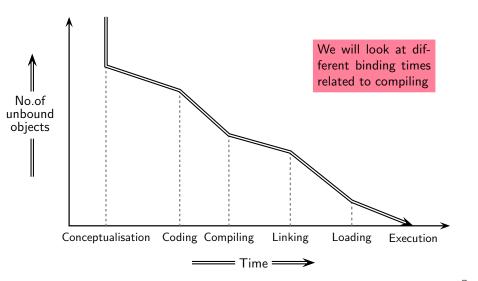


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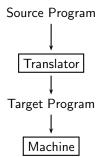




Binding

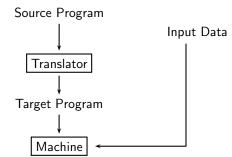


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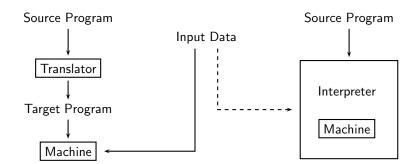
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Implementation Mechanisms





Implementation Mechanisms



Compilation Overview: Introduction to Compilation

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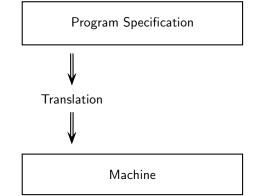
• "Gap" between the "levels" of program specification and execution

Program Specification

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Machine

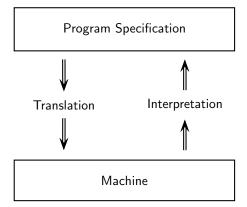
• "Gap" between the "levels" of program specification and execution



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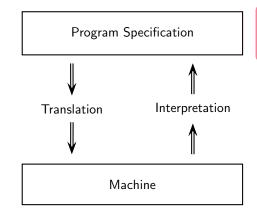
• "Gap" between the "levels" of program specification and execution



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Implementation Mechanisms as "Bridges"

• "Gap" between the "levels" of program specification and execution



State : Variables
Operations: Expressions,
Control Flow

State : Memory, Registers

Operations: Machine

Instructions

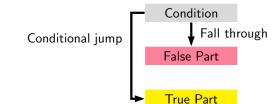
```
Input C statement
  a = b<10?b:c;
```

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Spim Assembly Equivalent

```
$t0, 4($fp); t0 <- b
                                     # Is b smaller
   slti $t0, $t0, 10; t0 <- t0 < 10 # than 10?
       $t0, $t0 ; t0 <- !t0
   not
   bgtz $t0, L0: ; if t0>0 goto L0
       $t0, 4($fp); t0 <- b
   lw
                                     # YES
   b
      L1:
                       goto L1
LO: lw $t0, 8($fp); LO: t0 <- c
                                     # NO
L1: sw 0(\$fp), \$t0; L1: a <- t0
```

High and Low Level Abstractions



Spim Assembly Equivalent

Input C statement a = b<10?b:c;

```
$t0, 4($fp) ; t0 <- b
                                      # Is b smaller
   slti $t0, $t0, 10; t0 <- t0 < 10 # than 10?
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   lw
                                      # YES
   b
       L1:
                       goto L1
LO: lw $t0, 8($fp) ;L0: t0 <- c
                                      # NO
L1: sw 0(\$fp), \$t0; L1: a <- t0
```

High and Low Level Abstractions

NOT Condition

True Part

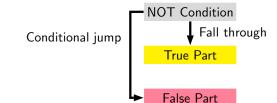
```
Input C statement
a = b<10?b:c;</pre>
```

False Part

Spim Assembly Equivalent

```
lw $t0, 4($fp); t0 <- b  # Is b smaller
slti $t0, $t0, 10; t0 <- t0 < 10  # than 10?
not $t0, $t0  ; t0 <- !t0
bgtz $t0, L0: ; if t0>0 goto L0
lw $t0, 4($fp); t0 <- b  # YES
b L1: ; goto L1
L0: lw $t0, 8($fp); L0: t0 <- c  # N0
L1: sw 0($fp), $t0; L1: a <- t0</pre>
```

High and Low Level Abstractions



Spim Assembly Equivalent

Input C statement
a = b<10?b:c;</pre>

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```

Compilation Overview: Introduction to Compilation

Implementation Mechanisms

 ${\sf Translation} \qquad = \quad {\sf Analysis} + {\sf Synthesis}$

 ${\sf Interpretation} \quad = \quad {\sf Analysis} \, + \, {\sf Execution}$

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Compilation Overview: Introduction to Compilation

• Translation = Analysis + Synthesis Interpretation = Analysis + Execution

• Translation Instructions \Longrightarrow Equivalent Instructions

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Translation

Interpretation

Compilation Overview: Introduction to Compilation

Translation Analysis + Synthesis Interpretation Analysis + Execution

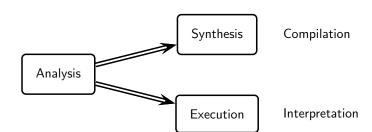
Instructions

Instructions

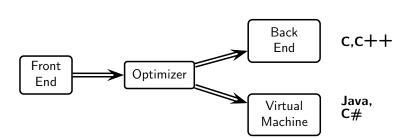
Actions Implied by Instructions

Equivalent

Instructions

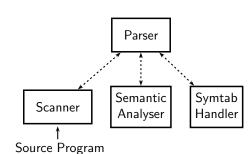


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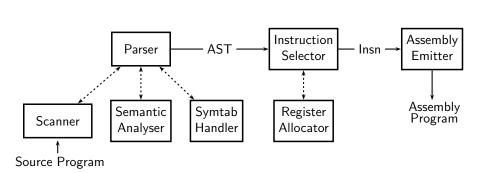
Part 2

An Overview of Compilation Phases

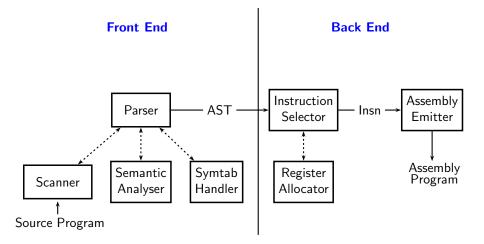


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The Structure of a Simple Compiler

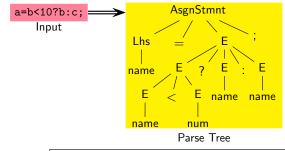


a=b<10?b:c;

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Input

Translation Sequence in Our Compiler: Parsing



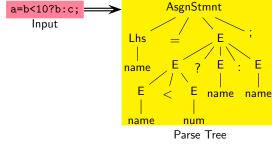
Issues:

- Grammar rules, terminals, non-terminals
- Order of application of grammar rules
 eg. is it (a = b<10?) followed by (b:c)?
- Values of terminal symbols

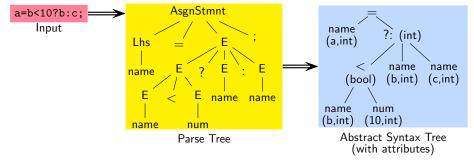
eg. string "10" vs. integer number 10.

Translation Sequence in Our Compiler: Semantic Analysis

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Translation Sequence in Our Compiler: Semantic Analysis



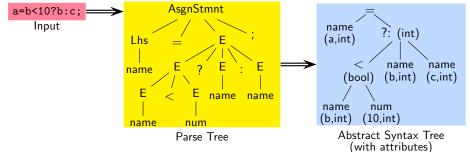
Issues:

- Symbol tables
 Have variables been declared? What are their types?
 - What is their scope?
- Type consistency of operators and operands
 The result of computing b<10? is bool and not int

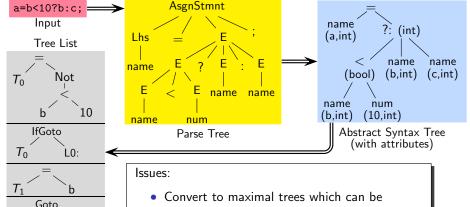
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Translation Sequence in Our Compiler: IR Generation



Translation Sequence in Our Compiler: IR Generation



- Convert to maximal trees which can be implemented without altering control flow
 Simplifies instruction selection and scheduling, register allocation etc.
- Linearise control flow by flattening nested control constructs

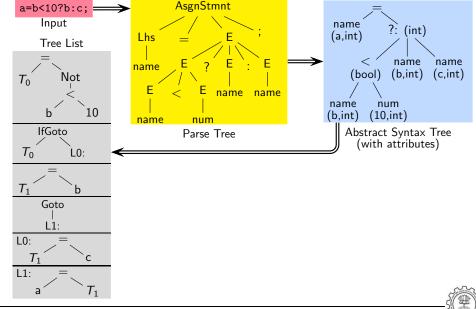
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L0:

L1:

L1:

Translation Sequence in Our Compiler: Instruction Selection

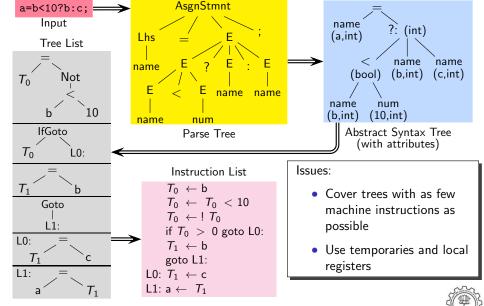


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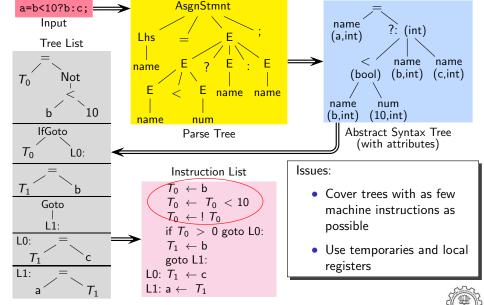
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Translation Sequence in Our Compiler: Instruction Selection



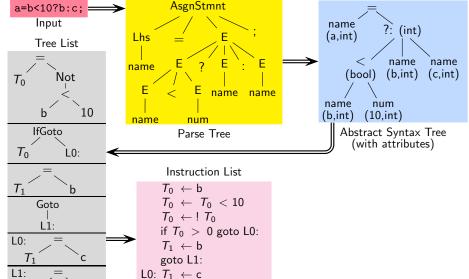
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Translation Sequence in Our Compiler: Instruction Selection



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Translation Sequence in Our Compiler: Emitting Instructions

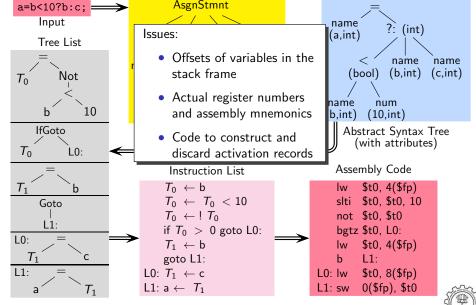


L1: a $\leftarrow T_1$

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Translation Sequence in Our Compiler: Emitting Instructions AsgnStmnt



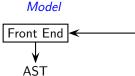
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Part 3

Compilation Models

Compilation Overview: Compilation Models

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Input Source Program

Compilation Overview: Compilation Models

Model

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Davidson Fraser

Model

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AST

Optimizer

Target Indep. IR

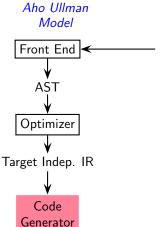
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Davidson Fraser

Model

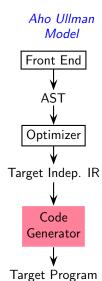
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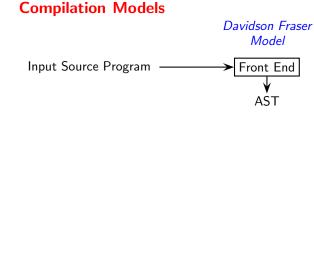
Input Source Program

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Target Program



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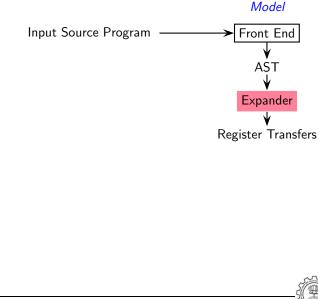
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Davidson Fraser

Davidson Fraser

Model

Front End

AST

Expander

Register Transfers

Optimizer

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Register Transfers



Model Front End **AST** Optimizer Target Indep. IR Code Generator

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Target Program

AST Optimizer Target Indep. IR Code Generator Target Program

Optimizer

Register Transfers

Recognizer

Target Program

AST

Expander

Register Transfers

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Model

Compilation Models

Aho Ullman Model

Front End AST Optimizer Target Indep. IR Code Generator Target Program

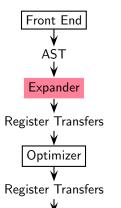
Aho Ullman: Instruction selection

- over optimized IR using
- cost based tree tiling matching

Davidson Fraser: Instruction selection

. . . .

- over AST using
- simple full tree matching based algorithms that generate
- naive code which is
 - target dependent, and is
 - target dependent, and itoptimized subsequently



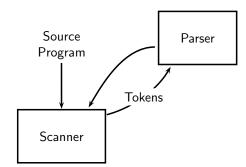
Target Program

Recognizer

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Parser

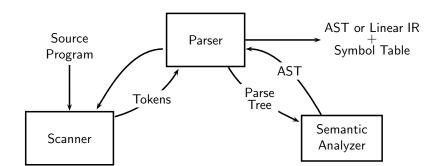
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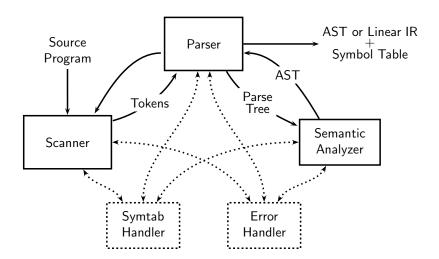


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Typical Front Ends

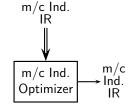


Typical Front Ends



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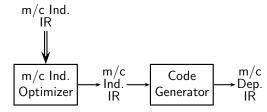
Typical Back Ends in Aho Ullman Model



- Compile time
- evaluations

 Eliminating redundant computations

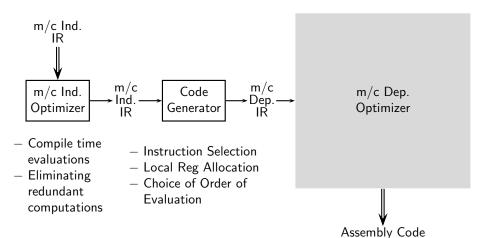
Typical Back Ends in Aho Ullman Model



- Compile time
 - evaluations
- Eliminating redundant computations
- Instruction SelectionLocal Reg Allocation
- Choice of Order of Evaluation

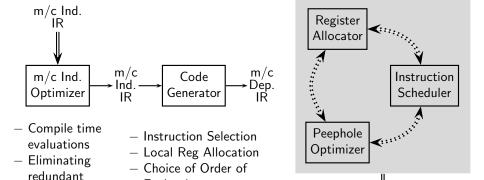
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Typical Back Ends in Aho Ullman Model



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Typical Back Ends in Aho Ullman Model



Evaluation

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computations

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Assembly Code

	Aho Ullman Model	Davidson Fraser Model
Instruction Selection	Machine instructions a	R is expressed in the form of trees re described in the form of trees overed" using the instruction trees
Optimization		

	Aho Ullman Model	Davidson Fraser Model
Instruction Selection	Machine independent IR is expressed in the form of trees Machine instructions are described in the form of trees Trees in the IR are "covered" using the instruction trees Cost based tree pattern matching	
Optimization		

	Aho Ullman Model	Davidson Fraser Model
Instruction Selection	 Machine independent IR is expressed in the form of trees Machine instructions are described in the form of trees Trees in the IR are "covered" using the instruction trees Cost based tree pattern matching 	
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	Aho Ullman Model	Davidson Fraser Model
Instruction Selection	Machine instructions a	R is expressed in the form of trees re described in the form of trees overed" using the instruction trees Structural tree pattern matching
Optimization	Machine independent	

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Instruction Selection	 Machine independent IR is expressed in the form of trees Machine instructions are described in the form of trees Trees in the IR are "covered" using the instruction trees Cost based tree pattern 	
	matching	Structural tree pattern matching
		Machine dependent
Optimization	Machine independent	

	Aho Ullman Model	Davidson Fraser Model
Instruction Selection	 Machine independent IR is expressed in the form of trees Machine instructions are described in the form of trees Trees in the IR are "covered" using the instruction trees 	
	Cost based tree pattern matching	Structural tree pattern matching
Optimization	Machine independent	Machine dependent
		Key Insight: Register transfers are target specific but their form is target independent

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